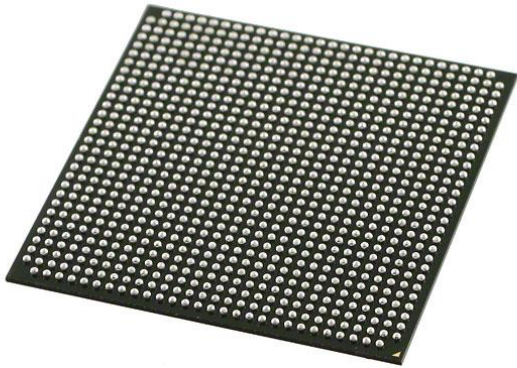


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5ASTMD3E3F31I3G Datasheet

| | |
|------------------------------|----------------------------------|
| DiGi Electronics Part Number | 5ASTMD3E3F31I3G-DG |
| Manufacturer | Intel |
| Manufacturer Product Number | 5ASTMD3E3F31I3G |
| Description | IC SOC CORTEX-A9 1.05GHZ 896FBGA |

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Detailed Description

Dual ARM® Cortex®-A9 MPCore™ with CoreSight™ System On Chip (SOC) IC Arria V ST FPGA - 350K Logic Elements

This model 5ASTMD3E3F31I3G is available at [DiGi Electronics](#) IC SOC CORTEX-A9 1.05GHZ 896-FBGA (31x31)

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Manufacturer Product Number:

5ASTMD3E3F31I3G

Series:

Arria V ST

Architecture:

MCU, FPGA

Flash Size:

-

Peripherals:

DMA, POR, WDT

Speed:

1.05GHz

Operating Temperature:

-40°C ~ 100°C (TJ)

Supplier Device Package:

896-FBGA (31x31)

Manufacturer:

Intel

Product Status:

Active

Core Processor:

Dual ARM® Cortex®-A9 MPCore™ with CoreSight™

RAM Size:

64KB

Connectivity:

EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG

Primary Attributes:

FPGA - 350K Logic Elements

Package / Case:

896-BBGA, FCBGA

Number of I/O:

MCU - 208, FPGA - 250

Moisture Sensitivity Level (MSL):

3 (168 Hours)

Environmental & Export classification

RoHS Status:

RoHS Compliant

REACH Status:

REACH Unaffected

Arria V Device Datasheet

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Arria V GX, GT, SX, and ST Device Datasheet

1

2016.06.20

AV-51002



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This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and I/O timing for Arria[®] V devices.

Arria V devices are offered in commercial and industrial grades. Commercial devices are offered in –C4 (fastest), –C5, and –C6 speed grades. Industrial grade devices are offered in the –I3 and –I5 speed grades.

Related Information

[Arria V Device Overview](#)

Provides more information about the densities and packages of devices in the Arria V family.

Electrical Characteristics

The following sections describe the operating conditions and power consumption of Arria V devices.

Operating Conditions

Arria V devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Arria V devices, you must consider the operating requirements described in this section.

Absolute Maximum Ratings

This section defines the maximum operating conditions for Arria V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms.

The functional operation of the device is not implied for these conditions.

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1-2 Absolute Maximum Ratings

Caution: Conditions outside the range listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 1-1: Absolute Maximum Ratings for Arria V Devices

| Symbol | Description | Minimum | Maximum | Unit |
|---------------------------|--|---------|---------|------|
| V _{CC} | Core voltage power supply | -0.50 | 1.43 | V |
| V _{CCP} | Periphery circuitry, PCIe [®] hardIP block, and transceiver physical coding sublayer (PCS) power supply | -0.50 | 1.43 | V |
| V _{CCPGM} | Configuration pins power supply | -0.50 | 3.90 | V |
| V _{CC_AUX} | Auxiliary supply | -0.50 | 3.25 | V |
| V _{CCBAT} | Battery back-up power supply for design security volatile key register | -0.50 | 3.90 | V |
| V _{CCPD} | I/O pre-driver power supply | -0.50 | 3.90 | V |
| V _{CCIO} | I/O power supply | -0.50 | 3.90 | V |
| V _{CCD_FPLL} | Phase-locked loop (PLL) digital power supply | -0.50 | 1.80 | V |
| V _{CCA_FPLL} | PLL analog power supply | -0.50 | 3.25 | V |
| V _{CCA_GXB} | Transceiver high voltage power | -0.50 | 3.25 | V |
| V _{CCH_GXB} | Transmitter output buffer power | -0.50 | 1.80 | V |
| V _{CCR_GXB} | Receiver power | -0.50 | 1.50 | V |
| V _{CCT_GXB} | Transmitter power | -0.50 | 1.50 | V |
| V _{CCL_GXB} | Transceiver clock network power | -0.50 | 1.50 | V |
| V _I | DC input voltage | -0.50 | 3.80 | V |
| V _{CC_HPS} | HPS core voltage and periphery circuitry power supply | -0.50 | 1.43 | V |
| V _{CCPD_HPS} | HPS I/O pre-driver power supply | -0.50 | 3.90 | V |
| V _{CCIO_HPS} | HPS I/O power supply | -0.50 | 3.90 | V |
| V _{CCRSTCLK_HPS} | HPS reset and clock input pins power supply | -0.50 | 3.90 | V |

| Symbol | Description | Minimum | Maximum | Unit |
|-----------------------|--------------------------------|---------|---------|------|
| V_{CCPLL_HPS} | HPS PLL analog power supply | -0.50 | 3.25 | V |
| $V_{CC_AUX_SHARED}$ | HPS auxiliary power supply | -0.50 | 3.25 | V |
| I_{OUT} | DC output current per pin | -25 | 40 | mA |
| T_J | Operating junction temperature | -55 | 125 | °C |
| T_{STG} | Storage temperature (no bias) | -65 | 150 | °C |

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in the following table and undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

For example, a signal that overshoots to 4.00 V can only be at 4.00 V for ~15% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 1.5 years.

1-4 Recommended Operating Conditions

Table 1-2: Maximum Allowed Overshoot During Transitions for Arria V Devices

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

| Symbol | Description | Condition (V) | Overshoot Duration as % of High Time | Unit |
|---------|------------------|---------------|--------------------------------------|------|
| Vi (AC) | AC input voltage | 3.8 | 100 | % |
| | | 3.85 | 68 | % |
| | | 3.9 | 45 | % |
| | | 3.95 | 28 | % |
| | | 4 | 15 | % |
| | | 4.05 | 13 | % |
| | | 4.1 | 11 | % |
| | | 4.15 | 9 | % |
| | | 4.2 | 8 | % |
| | | 4.25 | 7 | % |
| | | 4.3 | 5.4 | % |
| | | 4.35 | 3.2 | % |
| | | 4.4 | 1.9 | % |
| | | 4.45 | 1.1 | % |
| | | 4.5 | 0.6 | % |
| | | 4.55 | 0.4 | % |
| 4.6 | 0.2 | % | | |

Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Arria V devices.

Recommended Operating Conditions

Table 1-3: Recommended Operating Conditions for Arria V Devices

This table lists the steady-state voltage values expected from Arria V devices. Power supply ramps must all be strictly monotonic, without plateaus.

| Symbol | Description | Condition | Minimum ⁽¹⁾ | Typical | Maximum ⁽¹⁾ | Unit |
|-------------------|---|--------------------|------------------------|---------|------------------------|------|
| V_{CC} | Core voltage power supply | -C4, -I5, -C5, -C6 | 1.07 | 1.1 | 1.13 | V |
| | | -I3 | 1.12 | 1.15 | 1.18 | V |
| V_{CCP} | Periphery circuitry, PCIe hard IP block, and transceiver PCS power supply | -C4, -I5, -C5, -C6 | 1.07 | 1.1 | 1.13 | V |
| | | -I3 | 1.12 | 1.15 | 1.18 | V |
| V_{CCPGM} | Configuration pins power supply | 3.3 V | 3.135 | 3.3 | 3.465 | V |
| | | 3.0 V | 2.85 | 3.0 | 3.15 | V |
| | | 2.5 V | 2.375 | 2.5 | 2.625 | V |
| | | 1.8 V | 1.71 | 1.8 | 1.89 | V |
| V_{CC_AUX} | Auxiliary supply | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCBAT}^{(2)}$ | Battery back-up power supply (For design security volatile key register) | — | 1.2 | — | 3.0 | V |
| $V_{CCPD}^{(3)}$ | I/O pre-driver power supply | 3.3 V | 3.135 | 3.3 | 3.465 | V |
| | | 3.0 V | 2.85 | 3.0 | 3.15 | V |
| | | 2.5 V | 2.375 | 2.5 | 2.625 | V |

⁽¹⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽²⁾ If you do not use the design security feature in Arria V devices, connect V_{CCBAT} to a 1.5-V, 2.5-V, or 3.0-V power supply. Arria V power-on reset (POR) circuitry monitors V_{CCBAT} . Arria V devices do not exit POR if V_{CCBAT} is not powered up.

⁽³⁾ V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, 1.35, 1.25, or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V. V_{CCPD} must be 3.3 V when V_{CCIO} is 3.3 V.

1-6 Recommended Operating Conditions

| Symbol | Description | Condition | Minimum ⁽¹⁾ | Typical | Maximum ⁽¹⁾ | Unit |
|----------------------------------|--|--------------|------------------------|---------|------------------------|------|
| V _{CCIO} | I/O buffers power supply | 3.3 V | 3.135 | 3.3 | 3.465 | V |
| | | 3.0 V | 2.85 | 3.0 | 3.15 | V |
| | | 2.5 V | 2.375 | 2.5 | 2.625 | V |
| | | 1.8 V | 1.71 | 1.8 | 1.89 | V |
| | | 1.5 V | 1.425 | 1.5 | 1.575 | V |
| | | 1.35 V | 1.283 | 1.35 | 1.418 | V |
| | | 1.25 V | 1.19 | 1.25 | 1.31 | V |
| | | 1.2 V | 1.14 | 1.2 | 1.26 | V |
| V _{CCD_FPLL} | PLL digital voltage regulator power supply | — | 1.425 | 1.5 | 1.575 | V |
| V _{CCA_FPLL} | PLL analog voltage regulator power supply | — | 2.375 | 2.5 | 2.625 | V |
| V _I | DC input voltage | — | -0.5 | — | 3.6 | V |
| V _O | Output voltage | — | 0 | — | V _{CCIO} | V |
| T _J | Operating junction temperature | Commercial | 0 | — | 85 | °C |
| | | Industrial | -40 | — | 100 | °C |
| t _{RAMP} ⁽⁴⁾ | Power supply ramp time | Standard POR | 200 μs | — | 100 ms | — |
| | | Fast POR | 200 μs | — | 4 ms | — |

⁽¹⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽⁴⁾ This is also applicable to HPS power supply. For HPS power supply, refer to t_{RAMP} specifications for standard POR when HPS_PORSEL = 0 and t_{RAMP} specifications for fast POR when HPS_PORSEL = 1.

Transceiver Power Supply Operating Conditions

Table 1-4: Transceiver Power Supply Operating Conditions for Arria V Devices

| Symbol | Description | Minimum ⁽⁵⁾ | Typical | Maximum ⁽⁵⁾ | Unit |
|-----------------------|---|------------------------|-------------------------|------------------------|------|
| V _{CCA_GXBL} | Transceiver high voltage power (left side) | 2.375 | 2.500 | 2.625 | V |
| V _{CCA_GXBR} | Transceiver high voltage power (right side) | | | | |
| V _{CCR_GXBL} | GX and SX speed grades—receiver power (left side) | 1.08/1.12 | 1.1/1.15 ⁽⁶⁾ | 1.14/1.18 | V |
| V _{CCR_GXBR} | GX and SX speed grades—receiver power (right side) | | | | |
| V _{CCR_GXBL} | GT and ST speed grades—receiver power (left side) | 1.17 | 1.20 | 1.23 | V |
| V _{CCR_GXBR} | GT and ST speed grades—receiver power (right side) | | | | |
| V _{CCT_GXBL} | GX and SX speed grades—transmitter power (left side) | 1.08/1.12 | 1.1/1.15 ⁽⁶⁾ | 1.14/1.18 | V |
| V _{CCT_GXBR} | GX and SX speed grades—transmitter power (right side) | | | | |
| V _{CCT_GXBL} | GT and ST speed grades—transmitter power (left side) | 1.17 | 1.20 | 1.23 | V |
| V _{CCT_GXBR} | GT and ST speed grades—transmitter power (right side) | | | | |
| V _{CCH_GXBL} | Transmitter output buffer power (left side) | 1.425 | 1.500 | 1.575 | V |
| V _{CCH_GXBR} | Transmitter output buffer power (right side) | | | | |

⁽⁵⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽⁶⁾ For data rate ≤ 3.2 Gbps, connect V_{CCR_GXBL/R}, V_{CCT_GXBL/R}, or V_{CCL_GXBL/R} to either 1.1-V or 1.15-V power supply. For data rate > 3.2 Gbps, connect V_{CCR_GXBL/R}, V_{CCT_GXBL/R}, or V_{CCL_GXBL/R} to a 1.15-V power supply. For details, refer to the Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines.

1-8 HPS Power Supply Operating Conditions

| Symbol | Description | Minimum ⁽⁵⁾ | Typical | Maximum ⁽⁵⁾ | Unit |
|-----------------------|---|------------------------|-------------------------|------------------------|------|
| V _{CCL_GXBL} | GX and SX speed grades—clock network power (left side) | 1.08/1.12 | 1.1/1.15 ⁽⁶⁾ | 1.14/1.18 | V |
| V _{CCL_GXBR} | GX and SX speed grades—clock network power (right side) | | | | |
| V _{CCL_GXBL} | GT and ST speed grades—clock network power (left side) | 1.17 | 1.20 | 1.23 | V |
| V _{CCL_GXBR} | GT and ST speed grades—clock network power (right side) | | | | |

Related Information**[Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines](#)**

Provides more information about the power supply connection for different data rates.

HPS Power Supply Operating Conditions**Table 1-5: HPS Power Supply Operating Conditions for Arria V SX and ST Devices**

This table lists the steady-state voltage and current values expected from Arria V system-on-a-chip (SoC) devices with ARM®-based hard processor system (HPS). Power supply ramps must all be strictly monotonic, without plateaus. Refer to Recommended Operating Conditions for Arria V Devices table for the steady-state voltage values expected from the FPGA portion of the Arria V SoC devices.

| Symbol | Description | Condition | Minimum ⁽⁷⁾ | Typical | Maximum ⁽⁷⁾ | Unit |
|---------------------|---|--------------------|------------------------|---------|------------------------|------|
| V _{CC_HPS} | HPS core voltage and periphery circuitry power supply | -C4, -I5, -C5, -C6 | 1.07 | 1.1 | 1.13 | V |
| | | -I3 | 1.12 | 1.15 | 1.18 | V |

⁽⁵⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽⁷⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

| Symbol | Description | Condition | Minimum ⁽⁷⁾ | Typical | Maximum ⁽⁷⁾ | Unit |
|--------------------------------|---|-----------------------|------------------------|---------|------------------------|------|
| V_{CCPD_HPS} ⁽⁸⁾ | HPS I/O pre-driver power supply | 3.3 V | 3.135 | 3.3 | 3.465 | V |
| | | 3.0 V | 2.85 | 3.0 | 3.15 | V |
| | | 2.5 V | 2.375 | 2.5 | 2.625 | V |
| V_{CCIO_HPS} | HPS I/O buffers power supply | 3.3 V | 3.135 | 3.3 | 3.465 | V |
| | | 3.0 V | 2.85 | 3.0 | 3.15 | V |
| | | 2.5 V | 2.375 | 2.5 | 2.625 | V |
| | | 1.8 V | 1.71 | 1.8 | 1.89 | V |
| | | 1.5 V | 1.425 | 1.5 | 1.575 | V |
| | | 1.35 V ⁽⁹⁾ | 1.283 | 1.35 | 1.418 | V |
| $V_{CCRSTCLK_HPS}$ | HPS reset and clock input pins power supply | 3.3 V | 3.135 | 3.3 | 3.465 | V |
| | | 3.0 V | 2.85 | 3.0 | 3.15 | V |
| | | 2.5 V | 2.375 | 2.5 | 2.625 | V |
| | | 1.8 V | 1.71 | 1.8 | 1.89 | V |
| V_{CCPLL_HPS} | HPS PLL analog voltage regulator power supply | — | 2.375 | 2.5 | 2.625 | V |

⁽⁷⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽⁸⁾ V_{CCPD_HPS} must be 2.5 V when V_{CCIO_HPS} is 2.5, 1.8, 1.5, or 1.2 V. V_{CCPD_HPS} must be 3.0 V when V_{CCIO_HPS} is 3.0 V. V_{CCPD_HPS} must be 3.3 V when V_{CCIO_HPS} is 3.3 V.

⁽⁹⁾ V_{CCIO_HPS} 1.35 V is supported for HPS row I/O bank only.

1-10 DC Characteristics

| Symbol | Description | Condition | Minimum ⁽⁷⁾ | Typical | Maximum ⁽⁷⁾ | Unit |
|----------------------------|----------------------------|-----------|------------------------|---------|------------------------|------|
| V _{CC_AUX_SHARED} | HPS auxiliary power supply | — | 2.375 | 2.5 | 2.625 | V |

Related Information

[Recommended Operating Conditions](#) on page 1-5

Provides the steady-state voltage values for the FPGA portion of the device.

DC Characteristics**Supply Current and Power Consumption**

Altera offers two ways to estimate power for your design—the Excel-based Early Power Estimator (EPE) and the Quartus® Prime PowerPlay Power Analyzer feature.

Use the Excel-based EPE before you start your design to estimate the supply current for your design. The EPE provides a magnitude estimate of the device power because these currents vary greatly with the resources you use.

The Quartus Prime PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

Related Information

- [PowerPlay Early Power Estimator User Guide](#)
Provides more information about power estimation tools.
- [PowerPlay Power Analysis chapter, Quartus Prime Handbook](#)
Provides more information about power estimation tools.

⁽⁷⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

I/O Pin Leakage Current

Table 1-6: I/O Pin Leakage Current for Arria V Devices

| Symbol | Description | Condition | Min | Typ | Max | Unit |
|----------|--------------------|--|-----|-----|-----|---------------|
| I_I | Input pin | $V_I = 0\text{ V to }V_{CCIO\text{MAX}}$ | -30 | — | 30 | μA |
| I_{OZ} | Tri-stated I/O pin | $V_O = 0\text{ V to }V_{CCIO\text{MAX}}$ | -30 | — | 30 | μA |

Bus Hold Specifications

Table 1-7: Bus Hold Parameters for Arria V Devices

The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

| Parameter | Symbol | Condition | V_{CCIO} (V) | | | | | | | | | | | | Unit |
|------------------------------------|------------|----------------------------------|----------------|------|-----|------|-----|------|-----|------|-----|------|-----|------|---------------|
| | | | 1.2 | | 1.5 | | 1.8 | | 2.5 | | 3.0 | | 3.3 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Bus-hold, low, sustaining current | I_{SUSL} | $V_{IN} > V_{IL}$ (max) | 8 | — | 12 | — | 30 | — | 50 | — | 70 | — | 70 | — | μA |
| Bus-hold, high, sustaining current | I_{SUSH} | $V_{IN} < V_{IH}$ (min) | -8 | — | -12 | — | -30 | — | -50 | — | -70 | — | -70 | — | μA |
| Bus-hold, low, overdrive current | I_{ODL} | $0\text{ V} < V_{IN} < V_{CCIO}$ | — | 125 | — | 175 | — | 200 | — | 300 | — | 500 | — | 500 | μA |
| Bus-hold, high, overdrive current | I_{ODH} | $0\text{ V} < V_{IN} < V_{CCIO}$ | — | -125 | — | -175 | — | -200 | — | -300 | — | -500 | — | -500 | μA |

1-12 OCT Calibration Accuracy Specifications

| Parameter | Symbol | Condition | V_{CCIO} (V) | | | | | | | | | | | | Unit |
|---------------------|------------|-----------|----------------|-----|-------|-------|------|------|-----|-----|-----|-----|-----|-----|------|
| | | | 1.2 | | 1.5 | | 1.8 | | 2.5 | | 3.0 | | 3.3 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Bus-hold trip point | V_{TRIP} | — | 0.3 | 0.9 | 0.375 | 1.125 | 0.68 | 1.07 | 0.7 | 1.7 | 0.8 | 2 | 0.8 | 2 | V |

OCT Calibration Accuracy Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.

Table 1-8: OCT Calibration Accuracy Specifications for Arria V Devices

Calibration accuracy for the calibrated on-chip series termination (R_S OCT) and on-chip parallel termination (R_T OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

| Symbol | Description | Condition (V) | Calibration Accuracy | | | Unit |
|---|--|--------------------------------------|----------------------|------------|------------|------|
| | | | -I3, -C4 | -I5, -C5 | -C6 | |
| 25- Ω R_S | Internal series termination with calibration (25- Ω setting) | $V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2$ | ± 15 | ± 15 | ± 15 | % |
| 50- Ω R_S | Internal series termination with calibration (50- Ω setting) | $V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2$ | ± 15 | ± 15 | ± 15 | % |
| 34- Ω and 40- Ω R_S | Internal series termination with calibration (34- Ω and 40- Ω setting) | $V_{CCIO} = 1.5, 1.35, 1.25, 1.2$ | ± 15 | ± 15 | ± 15 | % |
| 48- Ω , 60- Ω , and 80- Ω R_S | Internal series termination with calibration (48- Ω , 60- Ω , and 80- Ω setting) | $V_{CCIO} = 1.2$ | ± 15 | ± 15 | ± 15 | % |
| 50- Ω R_T | Internal parallel termination with calibration (50- Ω setting) | $V_{CCIO} = 2.5, 1.8, 1.5, 1.2$ | -10 to +40 | -10 to +40 | -10 to +40 | % |
| 20- Ω , 30- Ω , 40- Ω , 60- Ω , and 120- Ω R_T | Internal parallel termination with calibration (20- Ω , 30- Ω , 40- Ω , 60- Ω , and 120- Ω setting) | $V_{CCIO} = 1.5, 1.35, 1.25$ | -10 to +40 | -10 to +40 | -10 to +40 | % |

| Symbol | Description | Condition (V) | Calibration Accuracy | | | Unit |
|---|--|---|----------------------|------------|------------|------|
| | | | -I3, -C4 | -I5, -C5 | -C6 | |
| 60- Ω and 120- Ω R _T | Internal parallel termination with calibration (60- Ω and 120- Ω setting) | V _{CCIO} = 1.2 | -10 to +40 | -10 to +40 | -10 to +40 | % |
| 25- Ω R _{S_left_shift} | Internal left shift series termination with calibration (25- Ω R _{S_left_shift} setting) | V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 | ±15 | ±15 | ±15 | % |

OCT Without Calibration Resistance Tolerance Specifications

Table 1-9: OCT Without Calibration Resistance Tolerance Specifications for Arria V Devices

This table lists the Arria V OCT without calibration resistance tolerance to PVT changes.

| Symbol | Description | Condition (V) | ResistanceTolerance | | | Unit |
|------------------------------|--|------------------------------|---------------------|----------|-----|------|
| | | | -I3, -C4 | -I5, -C5 | -C6 | |
| 25- Ω R _S | Internal series termination without calibration (25- Ω setting) | V _{CCIO} = 3.0, 2.5 | ±30 | ±40 | ±40 | % |
| 25- Ω R _S | Internal series termination without calibration (25- Ω setting) | V _{CCIO} = 1.8, 1.5 | ±30 | ±40 | ±40 | % |
| 25- Ω R _S | Internal series termination without calibration (25- Ω setting) | V _{CCIO} = 1.2 | ±35 | ±50 | ±50 | % |
| 50- Ω R _S | Internal series termination without calibration (50- Ω setting) | V _{CCIO} = 3.0, 2.5 | ±30 | ±40 | ±40 | % |
| 50- Ω R _S | Internal series termination without calibration (50- Ω setting) | V _{CCIO} = 1.8, 1.5 | ±30 | ±40 | ±40 | % |
| 50- Ω R _S | Internal series termination without calibration (50- Ω setting) | V _{CCIO} = 1.2 | ±35 | ±50 | ±50 | % |
| 100- Ω R _D | Internal differential termination (100- Ω setting) | V _{CCIO} = 2.5 | ±25 | ±40 | ±40 | % |

Figure 1-1: Equation for OCT Variation Without Recalibration

$$R_{OCT} = R_{SCAL} \left(1 + \left\langle \frac{dR}{dT} \times \Delta T \right\rangle \pm \left\langle \frac{dR}{dV} \times \Delta V \right\rangle \right)$$

The definitions for the equation are as follows:

- The R_{OCT} value calculated shows the range of OCT resistance with the variation of temperature and V_{CCIO} .
- R_{SCAL} is the OCT resistance value at power-up.
- ΔT is the variation of temperature with respect to the temperature at power up.
- ΔV is the variation of voltage with respect to the V_{CCIO} at power up.
- dR/dT is the percentage change of R_{SCAL} with temperature.
- dR/dV is the percentage change of R_{SCAL} with voltage.

OCT Variation after Power-Up Calibration

Table 1-10: OCT Variation after Power-Up Calibration for Arria V Devices

This table lists OCT variation with temperature and voltage after power-up calibration. The OCT variation is valid for a V_{CCIO} range of $\pm 5\%$ and a temperature range of 0°C to 85°C .

| Symbol | Description | V_{CCIO} (V) | Value | Unit |
|--------|--|----------------|-------|------|
| dR/dV | OCT variation with voltage without recalibration | 3.0 | 0.100 | %/mV |
| | | 2.5 | 0.100 | |
| | | 1.8 | 0.100 | |
| | | 1.5 | 0.100 | |
| | | 1.35 | 0.150 | |
| | | 1.25 | 0.150 | |
| | | 1.2 | 0.150 | |

| Symbol | Description | V _{CCIO} (V) | Value | Unit |
|--------|--|-----------------------|-------|-------------------|
| dR/dT | OCT variation with temperature without recalibration | 3.0 | 0.189 | %/ ^o C |
| | | 2.5 | 0.208 | |
| | | 1.8 | 0.266 | |
| | | 1.5 | 0.273 | |
| | | 1.35 | 0.200 | |
| | | 1.25 | 0.200 | |
| | | 1.2 | 0.317 | |

Pin Capacitance

Table 1-11: Pin Capacitance for Arria V Devices

| Symbol | Description | Maximum | Unit |
|---------------------|--|---------|------|
| C _{IOTB} | Input capacitance on top/bottom I/O pins | 6 | pF |
| C _{IOLR} | Input capacitance on left/right I/O pins | 6 | pF |
| C _{OUTFB} | Input capacitance on dual-purpose clock output/feedback pins | 6 | pF |
| C _{IOVREF} | Input capacitance on V _{REF} pins | 48 | pF |

Hot Socketing

Table 1-12: Hot Socketing Specifications for Arria V Devices

| Symbol | Description | Maximum | Unit |
|-------------------------|------------------------|-------------------|------|
| I _{IOPIN} (DC) | DC current per I/O pin | 300 | μA |
| I _{IOPIN} (AC) | AC current per I/O pin | 8 ⁽¹⁰⁾ | mA |

⁽¹⁰⁾ The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, |I_{IOPIN}| = C dv/dt, in which C is the I/O pin capacitance and dv/dt is the slew rate.

1-16 Internal Weak Pull-Up Resistor

| Symbol | Description | Maximum | Unit |
|--------------------|---|---------|------|
| $I_{XCVR-TX (DC)}$ | DC current per transceiver transmitter (TX) pin | 100 | mA |
| $I_{XCVR-RX (DC)}$ | DC current per transceiver receiver (RX) pin | 50 | mA |

Internal Weak Pull-Up Resistor

All I/O pins, except configuration, test, and JTAG pins, have an option to enable weak pull-up.

Table 1-13: Internal Weak Pull-Up Resistor Values for Arria V Devices

| Symbol | Description | Condition (V) ⁽¹¹⁾ | Value ⁽¹²⁾ | Unit |
|----------|---|-------------------------------|-----------------------|------------|
| R_{PU} | Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you have enabled the programmable pull-up resistor option. | $V_{CCIO} = 3.3 \pm 5\%$ | 25 | k Ω |
| | | $V_{CCIO} = 3.0 \pm 5\%$ | 25 | k Ω |
| | | $V_{CCIO} = 2.5 \pm 5\%$ | 25 | k Ω |
| | | $V_{CCIO} = 1.8 \pm 5\%$ | 25 | k Ω |
| | | $V_{CCIO} = 1.5 \pm 5\%$ | 25 | k Ω |
| | | $V_{CCIO} = 1.35 \pm 5\%$ | 25 | k Ω |
| | | $V_{CCIO} = 1.25 \pm 5\%$ | 25 | k Ω |
| | | $V_{CCIO} = 1.2 \pm 5\%$ | 25 | k Ω |

Related Information

[Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines](#)

Provides more information about the pins that support internal weak pull-up and internal weak pull-down features.

I/O Standard Specifications

Tables in this section list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Arria V devices.

⁽¹¹⁾ Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO} .

⁽¹²⁾ Valid with $\pm 10\%$ tolerances to cover changes over PVT.

You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.

Single-Ended I/O Standards

Table 1-14: Single-Ended I/O Standards for Arria V Devices

| I/O Standard | V_{CCIO} (V) | | | V_{IL} (V) | | V_{IH} (V) | | V_{OL} (V) | V_{OH} (V) | $I_{OL}^{(13)}$ (mA) | $I_{OH}^{(13)}$ (mA) |
|--------------|----------------|-----|-------|--------------|------------------------|------------------------|------------------|------------------------|------------------------|----------------------|----------------------|
| | Min | Typ | Max | Min | Max | Min | Max | Max | Min | | |
| 3.3-V LVTTL | 3.135 | 3.3 | 3.465 | -0.3 | 0.8 | 1.7 | 3.6 | 0.45 | 2.4 | 4 | -4 |
| 3.3-V LVCMOS | 3.135 | 3.3 | 3.465 | -0.3 | 0.8 | 1.7 | 3.6 | 0.2 | $V_{CCIO} - 0.2$ | 2 | -2 |
| 3.0-V LVTTL | 2.85 | 3 | 3.15 | -0.3 | 0.8 | 1.7 | 3.6 | 0.4 | 2.4 | 2 | -2 |
| 3.0-V LVCMOS | 2.85 | 3 | 3.15 | -0.3 | 0.8 | 1.7 | 3.6 | 0.2 | $V_{CCIO} - 0.2$ | 0.1 | -0.1 |
| 3.0-V PCI | 2.85 | 3 | 3.15 | — | $0.3 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $V_{CCIO} + 0.3$ | $0.1 \times V_{CCIO}$ | $0.9 \times V_{CCIO}$ | 1.5 | -0.5 |
| 3.0-V PCI-X | 2.85 | 3 | 3.15 | — | $0.35 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $V_{CCIO} + 0.3$ | $0.1 \times V_{CCIO}$ | $0.9 \times V_{CCIO}$ | 1.5 | -0.5 |
| 2.5 V | 2.375 | 2.5 | 2.625 | -0.3 | 0.7 | 1.7 | 3.6 | 0.4 | 2 | 1 | -1 |
| 1.8 V | 1.71 | 1.8 | 1.89 | -0.3 | $0.35 \times V_{CCIO}$ | $0.65 \times V_{CCIO}$ | $V_{CCIO} + 0.3$ | 0.45 | $V_{CCIO} - 0.45$ | 2 | -2 |
| 1.5 V | 1.425 | 1.5 | 1.575 | -0.3 | $0.35 \times V_{CCIO}$ | $0.65 \times V_{CCIO}$ | $V_{CCIO} + 0.3$ | $0.25 \times V_{CCIO}$ | $0.75 \times V_{CCIO}$ | 2 | -2 |
| 1.2 V | 1.14 | 1.2 | 1.26 | -0.3 | $0.35 \times V_{CCIO}$ | $0.65 \times V_{CCIO}$ | $V_{CCIO} + 0.3$ | $0.25 \times V_{CCIO}$ | $0.75 \times V_{CCIO}$ | 2 | -2 |

⁽¹³⁾ To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the 3.3-V LVTTL specification (4 mA), you should set the current strength settings to 4 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

1-18 Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

Table 1-15: Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Arria V Devices

| I/O Standard | V_{CCIO} (V) | | | V_{REF} (V) | | | V_{TT} (V) | | |
|-------------------------|----------------|------|-------|------------------------|-----------------------|------------------------|------------------------|-----------------------|------------------------|
| | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | $0.49 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.51 \times V_{CCIO}$ | $V_{REF} - 0.04$ | V_{REF} | $V_{REF} + 0.04$ |
| SSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 | $V_{REF} - 0.04$ | V_{REF} | $V_{REF} + 0.04$ |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | $0.49 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.51 \times V_{CCIO}$ | $0.49 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.51 \times V_{CCIO}$ |
| SSTL-135 Class I, II | 1.283 | 1.35 | 1.418 | $0.49 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.51 \times V_{CCIO}$ | $0.49 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.51 \times V_{CCIO}$ |
| SSTL-125 Class I, II | 1.19 | 1.25 | 1.26 | $0.49 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.51 \times V_{CCIO}$ | $0.49 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.51 \times V_{CCIO}$ |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.85 | 0.9 | 0.95 | — | $V_{CCIO}/2$ | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.68 | 0.75 | 0.9 | — | $V_{CCIO}/2$ | — |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | $0.47 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.53 \times V_{CCIO}$ | — | $V_{CCIO}/2$ | — |
| HSUL-12 | 1.14 | 1.2 | 1.3 | $0.49 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.51 \times V_{CCIO}$ | — | — | — |

Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications

Table 1-16: Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Arria V Devices

| I/O Standard | $V_{IL(DC)}$ (V) | | $V_{IH(DC)}$ (V) | | $V_{IL(AC)}$ (V) | $V_{IH(AC)}$ (V) | V_{OL} (V) | V_{OH} (V) | $I_{OL}^{(14)}$ (mA) | $I_{OH}^{(14)}$ (mA) |
|------------------|------------------|-------------------|-------------------|------------------|-------------------|-------------------|-----------------------|-----------------------|----------------------|----------------------|
| | Min | Max | Min | Max | Max | Min | Max | Min | | |
| SSTL-2 Class I | -0.3 | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | $V_{CCIO} + 0.3$ | $V_{REF} - 0.31$ | $V_{REF} + 0.31$ | $V_{TT} - 0.608$ | $V_{TT} + 0.608$ | 8.1 | -8.1 |
| SSTL-2 Class II | -0.3 | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | $V_{CCIO} + 0.3$ | $V_{REF} - 0.31$ | $V_{REF} + 0.31$ | $V_{TT} - 0.81$ | $V_{TT} + 0.81$ | 16.2 | -16.2 |
| SSTL-18 Class I | -0.3 | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | $V_{CCIO} + 0.3$ | $V_{REF} - 0.25$ | $V_{REF} + 0.25$ | $V_{TT} - 0.603$ | $V_{TT} + 0.603$ | 6.7 | -6.7 |
| SSTL-18 Class II | -0.3 | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | $V_{CCIO} + 0.3$ | $V_{REF} - 0.25$ | $V_{REF} + 0.25$ | 0.28 | $V_{CCIO} - 0.28$ | 13.4 | -13.4 |
| SSTL-15 Class I | — | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | — | $V_{REF} - 0.175$ | $V_{REF} + 0.175$ | $0.2 \times V_{CCIO}$ | $0.8 \times V_{CCIO}$ | 8 | -8 |
| SSTL-15 Class II | — | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | — | $V_{REF} - 0.175$ | $V_{REF} + 0.175$ | $0.2 \times V_{CCIO}$ | $0.8 \times V_{CCIO}$ | 16 | -16 |
| SSTL-135 | — | $V_{REF} - 0.09$ | $V_{REF} + 0.09$ | — | $V_{REF} - 0.16$ | $V_{REF} + 0.16$ | $0.2 \times V_{CCIO}$ | $0.8 \times V_{CCIO}$ | — | — |
| SSTL-125 | — | $V_{REF} - 0.85$ | $V_{REF} + 0.85$ | — | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | $0.2 \times V_{CCIO}$ | $0.8 \times V_{CCIO}$ | — | — |
| HSTL-18 Class I | — | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | — | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | 0.4 | $V_{CCIO} - 0.4$ | 8 | -8 |
| HSTL-18 Class II | — | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | — | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | 0.4 | $V_{CCIO} - 0.4$ | 16 | -16 |
| HSTL-15 Class I | — | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | — | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | 0.4 | $V_{CCIO} - 0.4$ | 8 | -8 |

⁽¹⁴⁾ To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

1-20 Differential SSTL I/O Standards

| I/O Standard | $V_{IL(DC)}$ (V) | | $V_{IH(DC)}$ (V) | | $V_{IL(AC)}$ (V) | $V_{IH(AC)}$ (V) | V_{OL} (V) | V_{OH} (V) | $I_{OL}^{(14)}$ (mA) | $I_{OH}^{(14)}$ (mA) |
|------------------|------------------|------------------|------------------|-------------------|------------------|------------------|------------------------|------------------------|----------------------|----------------------|
| | Min | Max | Min | Max | Max | Min | Max | Min | | |
| HSTL-15 Class II | — | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | — | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | 0.4 | $V_{CCIO} - 0.4$ | 16 | -16 |
| HSTL-12 Class I | -0.15 | $V_{REF} - 0.08$ | $V_{REF} + 0.08$ | $V_{CCIO} + 0.15$ | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | $0.25 \times V_{CCIO}$ | $0.75 \times V_{CCIO}$ | 8 | -8 |
| HSTL-12 Class II | -0.15 | $V_{REF} - 0.08$ | $V_{REF} + 0.08$ | $V_{CCIO} + 0.15$ | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | $0.25 \times V_{CCIO}$ | $0.75 \times V_{CCIO}$ | 16 | -16 |
| HSUL-12 | — | $V_{REF} - 0.13$ | $V_{REF} + 0.13$ | — | $V_{REF} - 0.22$ | $V_{REF} + 0.22$ | $0.1 \times V_{CCIO}$ | $0.9 \times V_{CCIO}$ | — | — |

Differential SSTL I/O Standards

Table 1-17: Differential SSTL I/O Standards for Arria V Devices

| I/O Standard | V_{CCIO} (V) | | | $V_{SWING(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{SWING(AC)}$ (V) | |
|---------------------|----------------|------|-------|---------------------|------------------|----------------------|--------------|----------------------|---------------------------|---------------------------|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 0.3 | $V_{CCIO} + 0.6$ | $V_{CCIO}/2 - 0.2$ | — | $V_{CCIO}/2 + 0.2$ | 0.62 | $V_{CCIO} + 0.6$ |
| SSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.25 | $V_{CCIO} + 0.6$ | $V_{CCIO}/2 - 0.175$ | — | $V_{CCIO}/2 + 0.175$ | 0.5 | $V_{CCIO} + 0.6$ |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | ⁽¹⁵⁾ | $V_{CCIO}/2 - 0.15$ | — | $V_{CCIO}/2 + 0.15$ | $2(V_{IH(AC)} - V_{REF})$ | $2(V_{IL(AC)} - V_{REF})$ |
| SSTL-135 | 1.283 | 1.35 | 1.45 | 0.18 | ⁽¹⁵⁾ | $V_{CCIO}/2 - 0.15$ | $V_{CCIO}/2$ | $V_{CCIO}/2 + 0.15$ | $2(V_{IH(AC)} - V_{REF})$ | $2(V_{IL(AC)} - V_{REF})$ |

⁽¹⁴⁾ To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the datasheet.

⁽¹⁵⁾ The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

| I/O Standard | V_{CCIO} (V) | | | $V_{SWING(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{SWING(AC)}$ (V) | |
|--------------|----------------|------|------|---------------------|------|---------------------|--------------|---------------------|---------------------------|---------------------------|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Max |
| SSTL-125 | 1.19 | 1.25 | 1.31 | 0.18 | (15) | $V_{CCIO}/2 - 0.15$ | $V_{CCIO}/2$ | $V_{CCIO}/2 + 0.15$ | $2(V_{IH(AC)} - V_{REF})$ | $2(V_{IL(AC)} - V_{REF})$ |

Differential HSTL and HSUL I/O Standards

Table 1-18: Differential HSTL and HSUL I/O Standards for Arria V Devices

| I/O Standard | V_{CCIO} (V) | | | $V_{DIF(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{CM(DC)}$ (V) | | | $V_{DIF(AC)}$ (V) | |
|------------------------|----------------|-----|-------|-------------------|------------------|------------------------------|-----------------------|------------------------------|-----------------------|-----------------------|-----------------------|-------------------|-------------------|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Typ | Max | Min | Max |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.2 | — | 0.78 | — | 1.12 | 0.78 | — | 1.12 | 0.4 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | — | 0.68 | — | 0.9 | 0.68 | — | 0.9 | 0.4 | — |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.16 | $V_{CCIO} + 0.3$ | — | $0.5 \times V_{CCIO}$ | — | $0.4 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.6 \times V_{CCIO}$ | 0.3 | $V_{CCIO} + 0.48$ |
| HSUL-12 | 1.14 | 1.2 | 1.3 | 0.26 | 0.26 | $0.5 \times V_{CCIO} - 0.12$ | $0.5 \times V_{CCIO}$ | $0.5 \times V_{CCIO} + 0.12$ | $0.4 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.6 \times V_{CCIO}$ | 0.44 | 0.44 |

Differential I/O Standard Specifications

Table 1-19: Differential I/O Standard Specifications for Arria V Devices

Differential inputs are powered by V_{CCPD} which requires 2.5 V.

| I/O Standard | V_{CCIO} (V) | | | V_{ID} (mV) ⁽¹⁶⁾ | | | $V_{ICM(DC)}$ (V) | | | V_{OD} (V) ⁽¹⁷⁾ | | | V_{OCM} (V) ⁽¹⁷⁾⁽¹⁸⁾ | | |
|---------------------------------|---|-----|-------|-------------------------------|-------------------|-----|-------------------|--------------------------|-------|------------------------------|-----|-----|-----------------------------------|------|-------|
| | Min | Typ | Max | Min | Condition | Max | Min | Condition | Max | Min | Typ | Max | Min | Typ | Max |
| PCML | Transmitter, receiver, and input reference clock pins of high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to Transceiver Specifications for Arria V GX and SX Devices and Transceiver Specifications for Arria V GT and ST Devices tables. | | | | | | | | | | | | | | |
| 2.5 V LVDS ⁽¹⁹⁾ | 2.375 | 2.5 | 2.625 | 100 | $V_{CM} = 1.25$ V | — | 0.05 | $D_{MAX} \leq 1.25$ Gbps | 1.80 | 0.247 | — | 0.6 | 1.125 | 1.25 | 1.375 |
| | | | | | | — | 1.05 | $D_{MAX} > 1.25$ Gbps | 1.55 | | | | | | |
| RSDS (HIO) ⁽²⁰⁾ | 2.375 | 2.5 | 2.625 | 100 | $V_{CM} = 1.25$ V | — | 0.25 | — | 1.45 | 0.1 | 0.2 | 0.6 | 0.5 | 1.2 | 1.4 |
| Mini-LVDS (HIO) ⁽²¹⁾ | 2.375 | 2.5 | 2.625 | 200 | — | 600 | 0.300 | — | 1.425 | 0.25 | — | 0.6 | 1 | 1.2 | 1.4 |
| LVPECL ⁽²²⁾ | — | — | — | 300 | — | — | 0.60 | $D_{MAX} \leq 700$ Mbps | 1.80 | — | — | — | — | — | — |
| | | | | | | | 1.00 | $D_{MAX} > 700$ Mbps | 1.60 | | | | | | |

⁽¹⁶⁾ The minimum V_{ID} value is applicable over the entire common mode range, V_{CM} .⁽¹⁷⁾ R_L range: $90 \leq R_L \leq 110 \Omega$.⁽¹⁸⁾ This applies to default pre-emphasis setting only.⁽¹⁹⁾ For optimized LVDS receiver performance, the receiver voltage input range must be within 1.0 V to 1.6 V for data rates above 1.25 Gbps and 0 V to 1.85 V for data rates below 1.25 Gbps.⁽²⁰⁾ For optimized RSDS receiver performance, the receiver voltage input range must be within 0.25 V to 1.45 V.⁽²¹⁾ For optimized Mini-LVDS receiver performance, the receiver voltage input range must be within 0.3 V to 1.425 V.⁽²²⁾ For optimized LVPECL receiver performance, the receiver voltage input range must be within 0.85 V to 1.75 V for data rates above 700 Mbps and 0.45 V to 1.95 V for data rates below 700 Mbps.

Related Information

- [Transceiver Specifications for Arria V GX and SX Devices](#) on page 1-23
Provides the specifications for transmitter, receiver, and reference clock I/O pin.
- [Transceiver Specifications for Arria V GT and ST Devices](#) on page 1-29
Provides the specifications for transmitter, receiver, and reference clock I/O pin.

Switching Characteristics

This section provides performance characteristics of Arria V core and periphery blocks.

Transceiver Performance Specifications

Transceiver Specifications for Arria V GX and SX Devices

Table 1-20: Reference Clock Specifications for Arria V GX and SX Devices

| Symbol/Description | Condition | Transceiver Speed Grade 4 | | | Transceiver Speed Grade 6 | | | Unit |
|---|--|---------------------------|-----|-----|---------------------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Supported I/O standards | 1.2 V PCML, 1.4 V PCML, 1.5 V PCML, 2.5 V PCML, Differential LVPECL ⁽²³⁾ , HCSL, and LVDS | | | | | | | |
| Input frequency from <small>REFCLK</small> input pins | — | 27 | — | 710 | 27 | — | 710 | MHz |
| Rise time | Measure at ± 60 mV of differential signal ⁽²⁴⁾ | — | — | 400 | — | — | 400 | ps |
| Fall time | Measure at ± 60 mV of differential signal ⁽²⁴⁾ | — | — | 400 | — | — | 400 | ps |
| Duty cycle | — | 45 | — | 55 | 45 | — | 55 | % |

⁽²³⁾ Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.

⁽²⁴⁾ REFCLK performance requires to meet transmitter REFCLK phase noise specification.

| Symbol/Description | Condition | Transceiver Speed Grade 4 | | | Transceiver Speed Grade 6 | | | Unit |
|--|--|---------------------------|--------------------------|-------------------------------|---------------------------|--------------------------|-------------------------------|--------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Peak-to-peak differential input voltage | — | 200 | — | 300 ⁽²⁵⁾ / 2000 | 200 | — | 300 ⁽²⁵⁾ / 2000 | mV |
| Spread-spectrum modulating clock frequency | PCI Express® (PCIe) | 30 | — | 33 | 30 | — | 33 | kHz |
| Spread-spectrum downspread | PCIe | — | 0 to -0.5% | — | — | 0 to -0.5% | — | — |
| On-chip termination resistors | — | — | 100 | — | — | 100 | — | Ω |
| V _{ICM} (AC coupled) | — | — | 1.1/1.15 ⁽²⁶⁾ | — | — | 1.1/1.15 ⁽²⁶⁾ | — | V |
| V _{ICM} (DC coupled) | HCSL I/O standard for the PCIe reference clock | 250 | — | 550 | 250 | — | 550 | mV |
| Transmitter REFCLK phase noise ⁽²⁷⁾ | 10 Hz | — | — | -50 | — | — | -50 | dBc/Hz |
| | 100 Hz | — | — | -80 | — | — | -80 | dBc/Hz |
| | 1 KHz | — | — | -110 | — | — | -110 | dBc/Hz |
| | 10 KHz | — | — | -120 | — | — | -120 | dBc/Hz |
| | 100 KHz | — | — | -120 | — | — | -120 | dBc/Hz |
| | ≥1 MHz | — | — | -130 | — | — | -130 | dBc/Hz |
| R _{REF} | — | — | 2000 ±1% | — | — | 2000 ±1% | — | Ω |

⁽²⁵⁾ The maximum peak-to-peak differential input voltage of 300 mV is allowed for DC coupled link.

⁽²⁶⁾ For data rate ≤3.2 Gbps, connect V_{CCR_GXBL/R} to either 1.1-V or 1.15-V power supply. For data rate >3.2 Gbps, connect V_{CCR_GXBL/R} to a 1.15-V power supply. For details, refer to the Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines.

⁽²⁷⁾ The transmitter REFCLK phase jitter is 30 ps p-p at bit error rate (BER) 10⁻¹².

Table 1-21: Transceiver Clocks Specifications for Arria V GX and SX Devices

| Symbol/Description | Condition | Transceiver Speed Grade 4 | | | Transceiver Speed Grade 6 | | | Unit |
|--|----------------------|---------------------------|-----|-----|---------------------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| fixedclk clock frequency | PCIe Receiver Detect | — | 125 | — | — | 125 | — | MHz |
| Transceiver Reconfiguration Controller IP (mgmt_clk_clk) clock frequency | — | 75 | — | 125 | 75 | — | 125 | MHz |

Table 1-22: Receiver Specifications for Arria V GX and SX Devices

| Symbol/Description | Condition | Transceiver Speed Grade 4 | | | Transceiver Speed Grade 6 | | | Unit |
|---|--|---------------------------|-----|--------|---------------------------|-----|------|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Supported I/O standards | 1.5 V PCML, 2.5 V PCML, LVPECL, and LVDS | | | | | | | |
| Data rate ⁽²⁸⁾ | — | 611 | — | 6553.6 | 611 | — | 3125 | Mbps |
| Absolute V_{MAX} for a receiver pin ⁽²⁹⁾ | — | — | — | 1.2 | — | — | 1.2 | V |
| Absolute V_{MIN} for a receiver pin | — | -0.4 | — | — | -0.4 | — | — | V |
| Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration | — | — | — | 1.6 | — | — | 1.6 | V |
| Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration | — | — | — | 2.2 | — | — | 2.2 | V |

⁽²⁸⁾ To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

⁽²⁹⁾ The device cannot tolerate prolonged operation at this absolute maximum.

| Symbol/Description | Condition | Transceiver Speed Grade 4 | | | Transceiver Speed Grade 6 | | | Unit |
|--|---------------------------|---|--------------------------|-----|---------------------------|--------------------------|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Minimum differential eye opening at the receiver serial input pins ⁽³⁰⁾ | — | 100 | — | — | 100 | — | — | mV |
| V _{ICM} (AC coupled) | — | — | 650 ⁽³¹⁾ /800 | — | — | 650 ⁽³¹⁾ /800 | — | mV |
| V _{ICM} (DC coupled) | ≤ 3.2Gbps ⁽³²⁾ | 670 | 700 | 730 | 670 | 700 | 730 | mV |
| Differential on-chip termination resistors | 85-Ω setting | — | 85 | — | — | 85 | — | Ω |
| | 100-Ω setting | — | 100 | — | — | 100 | — | Ω |
| | 120-Ω setting | — | 120 | — | — | 120 | — | Ω |
| | 150-Ω setting | — | 150 | — | — | 150 | — | Ω |
| t _{LTR} ⁽³³⁾ | — | — | — | 10 | — | — | 10 | μs |
| t _{LTD} ⁽³⁴⁾ | — | 4 | — | — | 4 | — | — | μs |
| t _{LTD_manual} ⁽³⁵⁾ | — | 4 | — | — | 4 | — | — | μs |
| t _{LTR_LTD_manual} ⁽³⁶⁾ | — | 15 | — | — | 15 | — | — | μs |
| Programmable ppm detector ⁽³⁷⁾ | — | ±62.5, 100, 125, 200, 250, 300, 500, and 1000 | | | | | | ppm |

⁽³⁰⁾ The differential eye opening specification at the receiver input pins assumes that you have disabled the **Receiver Equalization** feature. If you enable the **Receiver Equalization** feature, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

⁽³¹⁾ The AC coupled V_{ICM} is 650 mV for PCIe mode only.

⁽³²⁾ For standard protocol compliance, use AC coupling.

⁽³³⁾ t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

⁽³⁴⁾ t_{LTD} is time required for the receiver CDR to start recovering valid data after the rx_is_lockedto data signal goes high.

⁽³⁵⁾ t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the rx_is_lockedto data signal goes high when the CDR is functioning in the manual mode.

⁽³⁶⁾ t_{LTR_LTD_manual} is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx_is_lockedto ref signal goes high when the CDR is functioning in the manual mode.

⁽³⁷⁾ The rate match FIFO supports only up to ±300 parts per million (ppm).

| Symbol/Description | Condition | Transceiver Speed Grade 4 | | | Transceiver Speed Grade 6 | | | Unit |
|--|--|--|-----|-----|---------------------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Run length | — | — | — | 200 | — | — | 200 | UI |
| Programmable equalization AC and DC gain | AC gain setting = 0 to 3 ⁽³⁸⁾ DC gain setting = 0 to 1 | Refer to CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices and CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices diagrams. | | | | | | dB |

Table 1-23: Transmitter Specifications for Arria V GX and SX Devices

| Symbol/Description | Condition | Transceiver Speed Grade 4 | | | Transceiver Speed Grade 6 | | | Unit |
|---|---|---------------------------|-----|--------|---------------------------|-----|------|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Supported I/O standards | 1.5 V PCML | | | | | | | |
| Data rate | — | 611 | — | 6553.6 | 611 | — | 3125 | Mbps |
| V _{OCM} (AC coupled) | — | — | 650 | — | — | 650 | — | mV |
| V _{OCM} (DC coupled) | ≤ 3.2Gbps ⁽³²⁾ | 670 | 700 | 730 | 670 | 700 | 730 | mV |
| Differential on-chip termination resistors | 85-Ω setting | — | 85 | — | — | 85 | — | Ω |
| | 100-Ω setting | — | 100 | — | — | 100 | — | Ω |
| | 120-Ω setting | — | 120 | — | — | 120 | — | Ω |
| | 150-Ω setting | — | 150 | — | — | 150 | — | Ω |
| Intra-differential pair skew | TX V _{CM} = 0.65 V (AC coupled) and slew rate of 15 ps | — | — | 15 | — | — | 15 | ps |
| Intra-transceiver block transmitter channel-to-channel skew | ×6 PMA bonded mode | — | — | 180 | — | — | 180 | ps |

⁽³⁸⁾ The Quartus Prime software allows AC gain setting = 3 for design with data rate between 611 Mbps and 1.25 Gbps only.

| Symbol/Description | Condition | Transceiver Speed Grade 4 | | | Transceiver Speed Grade 6 | | | Unit |
|---|--------------------|---------------------------|-----|-----|---------------------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Inter-transceiver block transmitter channel-to-channel skew ⁽³⁹⁾ | ×N PMA bonded mode | — | — | 500 | — | — | 500 | ps |

Table 1-24: CMU PLL Specifications for Arria V GX and SX Devices

| Symbol/Description | Transceiver Speed Grade 4 | | Transceiver Speed Grade 6 | | Unit |
|---------------------------|---------------------------|--------|---------------------------|------|------|
| | Min | Max | Min | Max | |
| Supported data range | 611 | 6553.6 | 611 | 3125 | Mbps |
| fPLL supported data range | 611 | 3125 | 611 | 3125 | Mbps |

Table 1-25: Transceiver-FPGA Fabric Interface Specifications for Arria V GX and SX Devices

| Symbol/Description | Transceiver Speed Grade 4 and 6 | | Unit |
|-------------------------------------|---------------------------------|--------|------|
| | Min | Max | |
| Interface speed (single-width mode) | 25 | 187.5 | MHz |
| Interface speed (double-width mode) | 25 | 163.84 | MHz |

Related Information

- [CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain](#) on page 1-35
- [CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain](#) on page 1-36
- [Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines](#)
Provides more information about the power supply connection for different data rates.

⁽³⁹⁾ This specification is only applicable to channels on one side of the device across two transceiver banks.

Transceiver Specifications for Arria V GT and ST Devices

Table 1-26: Reference Clock Specifications for Arria V GT and ST Devices

| Symbol/Description | Condition | Transceiver Speed Grade 3 | | | Unit |
|--|---|---------------------------|------------|---------------------------|----------|
| | | Min | Typ | Max | |
| Supported I/O standards | 1.2 V PCML, 1.4 VPCML, 1.5 V PCML, 2.5 V PCML, Differential LVPECL ⁽⁴⁰⁾ , HCSL, and LVDS | | | | |
| Input frequency from REFCLK input pins | — | 27 | — | 710 | MHz |
| Rise time | Measure at ± 60 mV of differential signal ⁽⁴¹⁾ | — | — | 400 | ps |
| Fall time | Measure at ± 60 mV of differential signal ⁽⁴¹⁾ | — | — | 400 | ps |
| Duty cycle | — | 45 | — | 55 | % |
| Peak-to-peak differential input voltage | — | 200 | — | 300 ⁽⁴²⁾ /2000 | mV |
| Spread-spectrum modulating clock frequency | PCI Express (PCIe) | 30 | — | 33 | kHz |
| Spread-spectrum downspread | PCIe | — | 0 to -0.5% | — | — |
| On-chip termination resistors | — | — | 100 | — | Ω |
| V _{ICM} (AC coupled) | — | — | 1.2 | — | V |
| V _{ICM} (DC coupled) | HCSL I/O standard for the PCIe reference clock | 250 | — | 550 | mV |

⁽⁴⁰⁾ Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.

⁽⁴¹⁾ REFCLK performance requires to meet transmitter REFCLK phase noise specification.

⁽⁴²⁾ The maximum peak-to peak differential input voltage of 300 mV is allowed for DC coupled link.

| Symbol/Description | Condition | Transceiver Speed Grade 3 | | | Unit |
|---|--------------|---------------------------|---------------|------|----------|
| | | Min | Typ | Max | |
| Transmitter $_{REFCLK}$ phase noise ⁽⁴³⁾ | 10 Hz | — | — | -50 | dBc/Hz |
| | 100 Hz | — | — | -80 | dBc/Hz |
| | 1 KHz | — | — | -110 | dBc/Hz |
| | 10 KHz | — | — | -120 | dBc/Hz |
| | 100 KHz | — | — | -120 | dBc/Hz |
| | ≥ 1 MHz | — | — | -130 | dBc/Hz |
| R_{REF} | — | — | 2000 \pm 1% | — | Ω |

Table 1-27: Transceiver Clocks Specifications for Arria V GT and ST Devices

| Symbol/Description | Condition | Transceiver Speed Grade 3 | | | Unit |
|---|----------------------|---------------------------|-----|-----|------|
| | | Min | Typ | Max | |
| <code>fixedclk</code> clock frequency | PCIe Receiver Detect | — | 125 | — | MHz |
| Transceiver Reconfiguration Controller IP (<code>mgmt_clk_clk</code>) clock frequency | — | 75 | — | 125 | MHz |

Table 1-28: Receiver Specifications for Arria V GT and ST Devices

| Symbol/Description | Condition | Transceiver Speed Grade 3 | | | Unit |
|---|--|---------------------------|-----|---------|------|
| | | Min | Typ | Max | |
| Supported I/O Standards | 1.5 V PCML, 2.5 V PCML, LVPECL, and LVDS | | | | |
| Data rate (6-Gbps transceiver) ⁽⁴⁴⁾ | — | 611 | — | 6553.6 | Mbps |
| Data rate (10-Gbps transceiver) ⁽⁴⁴⁾ | — | 0.611 | — | 10.3125 | Gbps |

⁽⁴³⁾ The transmitter $_{REFCLK}$ phase jitter is 30 ps p-p (5 ps RMS) with bit error rate (BER) 10^{-12} , equivalent to 14 sigma.⁽⁴⁴⁾ To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

| Symbol/Description | Condition | Transceiver Speed Grade 3 | | | Unit |
|---|---------------------------------------|---------------------------|--------------------------|-----|---------------|
| | | Min | Typ | Max | |
| Absolute V_{MAX} for a receiver pin ⁽⁴⁵⁾ | — | — | — | 1.2 | V |
| Absolute V_{MIN} for a receiver pin | — | -0.4 | — | — | V |
| Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration | — | — | — | 1.6 | V |
| Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration | — | — | — | 2.2 | V |
| Minimum differential eye opening at the receiver serial input pins ⁽⁴⁶⁾ | — | 100 | — | — | mV |
| V_{ICM} (AC coupled) | — | — | 750 ⁽⁴⁷⁾ /800 | — | mV |
| V_{ICM} (DC coupled) | $\leq 3.2\text{Gbps}$ ⁽⁴⁸⁾ | 670 | 700 | 730 | mV |
| Differential on-chip termination resistors | 85- Ω setting | 85 | | | Ω |
| | 100- Ω setting | 100 | | | Ω |
| | 120- Ω setting | 120 | | | Ω |
| | 150- Ω setting | 150 | | | Ω |
| t_{LTR} ⁽⁴⁹⁾ | — | — | — | 10 | μs |
| t_{LTD} ⁽⁵⁰⁾ | — | 4 | — | — | μs |
| t_{LTD_manual} ⁽⁵¹⁾ | — | 4 | — | — | μs |

⁽⁴⁵⁾ The device cannot tolerate prolonged operation at this absolute maximum.

⁽⁴⁶⁾ The differential eye opening specification at the receiver input pins assumes that you have disabled the **Receiver Equalization** feature. If you enable the **Receiver Equalization** feature, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

⁽⁴⁷⁾ The AC coupled V_{ICM} is 750 mV for PCIe mode only.

⁽⁴⁸⁾ For standard protocol compliance, use AC coupling.

⁽⁴⁹⁾ t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

⁽⁵⁰⁾ t_{LTD} is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedto data` signal goes high.

| Symbol/Description | Condition | Transceiver Speed Grade 3 | | | Unit |
|---|--|---|-----|-----|---------|
| | | Min | Typ | Max | |
| $t_{LTR_LTD_manual}^{(52)}$ | — | 15 | — | — | μs |
| Programmable ppm detector ⁽⁵³⁾ | — | $\pm 62.5, 100, 125, 200, 250, 300, 500, \text{ and } 1000$ | | | ppm |
| Run length | — | — | — | 200 | UI |
| Programmable equalization AC and DC gain | AC gain setting = 0 to 3 ⁽⁵⁴⁾ DC gain setting = 0 to 1 | Refer to CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices and CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices diagrams. | | | |

Table 1-29: Transmitter Specifications for Arria V GT and ST Devices

| Symbol/Description | Condition | Transceiver Speed Grade 3 | | | Unit |
|---------------------------------|--------------------------------|---------------------------|-----|---------|------|
| | | Min | Typ | Max | |
| Supported I/O standards | | 1.5 V PCML | | | |
| Data rate (6-Gbps transceiver) | — | 611 | — | 6553.6 | Mbps |
| Data rate (10-Gbps transceiver) | — | 0.611 | — | 10.3125 | Gbps |
| V_{OCM} (AC coupled) | — | — | 650 | — | mV |
| V_{OCM} (DC coupled) | $\leq 3.2 \text{ Gbps}^{(48)}$ | 670 | 700 | 730 | mV |

⁽⁵¹⁾ t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedto data` signal goes high when the CDR is functioning in the manual mode.

⁽⁵²⁾ $t_{LTR_LTD_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedto ref` signal goes high when the CDR is functioning in the manual mode.

⁽⁵³⁾ The rate match FIFO supports only up to ± 300 ppm.

⁽⁵⁴⁾ The Quartus Prime software allows AC gain setting = 3 for design with data rate between 611 Mbps and 1.25 Gbps only.

| Symbol/Description | Condition | Transceiver Speed Grade 3 | | | Unit |
|---|--|---------------------------|-----|-----|----------|
| | | Min | Typ | Max | |
| Differential on-chip termination resistors | 85- Ω setting | — | 85 | — | Ω |
| | 100- Ω setting | — | 100 | — | Ω |
| | 120- Ω setting | — | 120 | — | Ω |
| | 150- Ω setting | — | 150 | — | Ω |
| Intra-differential pair skew | TX $V_{CM} = 0.65$ V (AC coupled) and slew rate of 15 ps | — | — | 15 | ps |
| Intra-transceiver block transmitter channel-to-channel skew | $\times 6$ PMA bonded mode | — | — | 180 | ps |
| Inter-transceiver block transmitter channel-to-channel skew ⁽⁵⁵⁾ | $\times N$ PMA bonded mode | — | — | 500 | ps |

Table 1-30: CMU PLL Specifications for Arria V GT and ST Devices

| Symbol/Description | Transceiver Speed Grade 3 | | Unit |
|---------------------------|---------------------------|---------|------|
| | Min | Max | |
| Supported data range | 0.611 | 10.3125 | Gbps |
| fPLL supported data range | 611 | 3125 | Mbps |

⁽⁵⁵⁾ This specification is only applicable to channels on one side of the device across two transceiver banks.

Table 1-31: Transceiver-FPGA Fabric Interface Specifications for Arria V GT and ST Devices

| Symbol/Description | Transceiver Speed Grade 3 | | Unit |
|-------------------------------------|---------------------------|---|------|
| | Min | Max | |
| Interface speed (PMA direct mode) | 50 | 153.6 ⁽⁵⁶⁾ , 161 ⁽⁵⁷⁾ | MHz |
| Interface speed (single-width mode) | 25 | 187.5 | MHz |
| Interface speed (double-width mode) | 25 | 163.84 | MHz |

Related Information

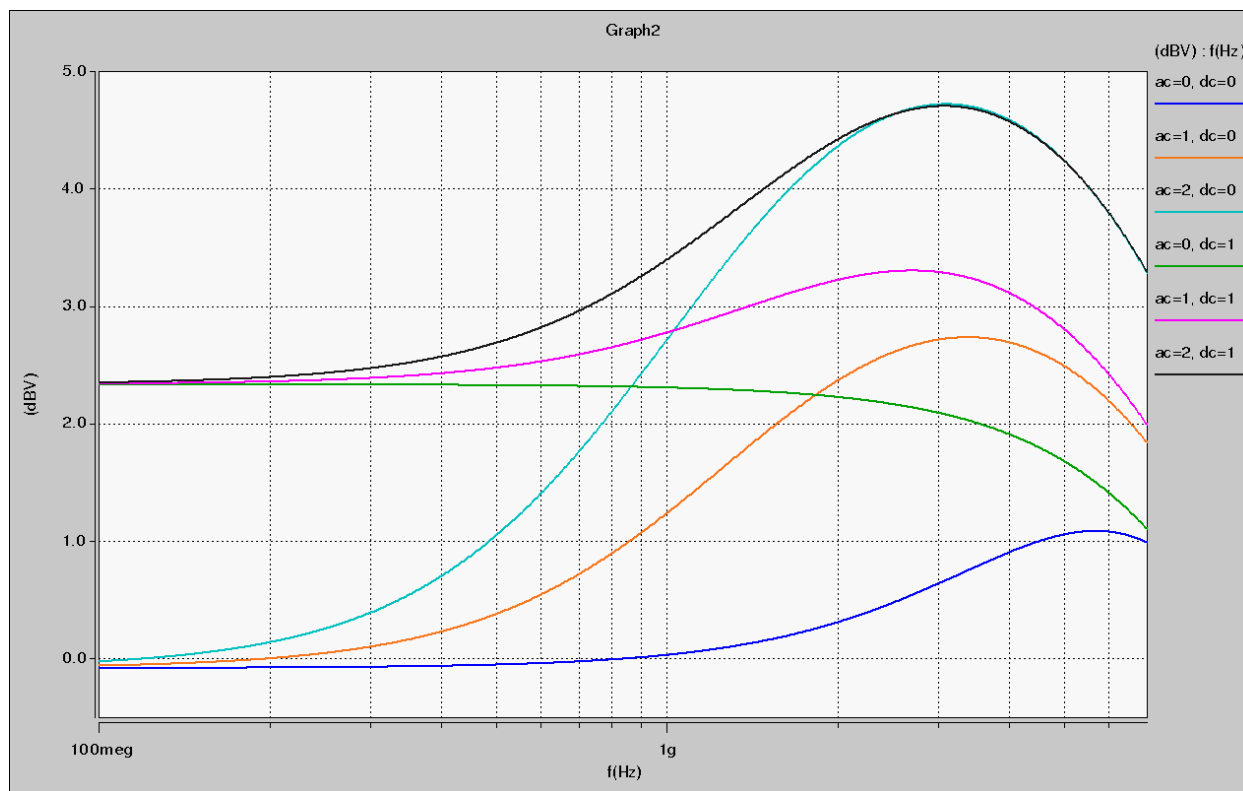
- [CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain](#) on page 1-35
- [CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain](#) on page 1-36

⁽⁵⁶⁾ The maximum frequency when core transceiver local routing is selected.

⁽⁵⁷⁾ The maximum frequency when core transceiver network routing (GCLK, RCLK, or PCLK) is selected.

CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain

Figure 1-2: Continuous Time-Linear Equalizer (CTLE) Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices



CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain

Figure 1-3: CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices



Typical TX V_{OD} Setting for Arria V Transceiver Channels with termination of 100 Ω

Table 1-32: Typical TX V_{OD} Setting for Arria V Transceiver Channels with termination of 100 Ω

| Symbol | V_{OD} Setting ⁽⁵⁸⁾ | V_{OD} Value (mV) | V_{OD} Setting ⁽⁵⁸⁾ | V_{OD} Value (mV) |
|---|----------------------------------|---------------------|----------------------------------|---------------------|
| V_{OD} differential peak-to-peak typical | 6 ⁽⁵⁹⁾ | 120 | 34 | 680 |
| | 7 ⁽⁵⁹⁾ | 140 | 35 | 700 |
| | 8 ⁽⁵⁹⁾ | 160 | 36 | 720 |
| | 9 | 180 | 37 | 740 |
| | 10 | 200 | 38 | 760 |
| | 11 | 220 | 39 | 780 |
| | 12 | 240 | 40 | 800 |
| | 13 | 260 | 41 | 820 |
| | 14 | 280 | 42 | 840 |
| | 15 | 300 | 43 | 860 |
| | 16 | 320 | 44 | 880 |
| | 17 | 340 | 45 | 900 |
| | 18 | 360 | 46 | 920 |
| | 19 | 380 | 47 | 940 |
| | 20 | 400 | 48 | 960 |
| | 21 | 420 | 49 | 980 |
| | 22 | 440 | 50 | 1000 |
| | 23 | 460 | 51 | 1020 |
| | 24 | 480 | 52 | 1040 |

⁽⁵⁸⁾ Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.

1-38 Transmitter Pre-Emphasis Levels

| Symbol | V _{OD} Setting ⁽⁵⁸⁾ | V _{OD} Value (mV) | V _{OD} Setting ⁽⁵⁸⁾ | V _{OD} Value (mV) |
|--------|---|----------------------------|---|----------------------------|
| | 25 | 500 | 53 | 1060 |
| | 26 | 520 | 54 | 1080 |
| | 27 | 540 | 55 | 1100 |
| | 28 | 560 | 56 | 1120 |
| | 29 | 580 | 57 | 1140 |
| | 30 | 600 | 58 | 1160 |
| | 31 | 620 | 59 | 1180 |
| | 32 | 640 | 60 | 1200 |
| | 33 | 660 | | |

Transmitter Pre-Emphasis Levels

The following table lists the simulation data on the transmitter pre-emphasis levels in dB for the first post tap under the following conditions:

- Low-frequency data pattern—five 1s and five 0s
- Data rate—2.5 Gbps

The levels listed are a representation of possible pre-emphasis levels under the specified conditions only and the pre-emphasis levels may change with data pattern and data rate.

Arria V devices only support 1st post tap pre-emphasis with the following conditions:

- The 1st post tap pre-emphasis settings must satisfy $|B| + |C| \leq 60$ where $|B| = V_{OD}$ setting with termination value, $R_{TERM} = 100 \Omega$ and $|C| = 1$ st post tap pre-emphasis setting.
- $|B| - |C| > 5$ for data rates < 5 Gbps and $|B| - |C| > 8.25$ for data rates > 5 Gbps.
- $(V_{MAX}/V_{MIN} - 1)\% < 600\%$, where $V_{MAX} = |B| + |C|$ and $V_{MIN} = |B| - |C|$.

Exception for PCIe Gen2 design: V_{OD} setting = 43 and pre-emphasis setting = 19 are allowed for PCIe Gen2 design with transmit de-emphasis - 6dB setting (`pipe_txdeemp = 1'b0`) using Altera PCIe Hard IP and PIPE IP cores.

⁽⁵⁸⁾ Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.

⁽⁵⁹⁾ Only valid for data rates ≤ 5 Gbps.

For example, when $V_{OD} = 800$ mV, the corresponding V_{OD} value setting is 40. The following conditions show that the 1st post tap pre-emphasis setting = 2 is valid:

- $|B| + |C| \leq 60 \rightarrow 40 + 2 = 42$
- $|B| - |C| > 5 \rightarrow 40 - 2 = 38$
- $(V_{MAX}/V_{MIN} - 1)\% < 600\% \rightarrow (42/38 - 1)\% = 10.52\%$

To predict the pre-emphasis level for your specific data rate and pattern, run simulations using the Arria V HSSI HSPICE models.

Table 1-33: Transmitter Pre-Emphasis Levels for Arria V Devices

| Quartus Prime 1st Post Tap Pre-Emphasis Setting | Quartus Prime V_{OD} Setting | | | | | | | Unit |
|---|--------------------------------|-------------|-------------|-------------|-------------|-------------|--------------|------|
| | 10 (200 mV) | 20 (400 mV) | 30 (600 mV) | 35 (700 mV) | 40 (800 mV) | 45 (900 mV) | 50 (1000 mV) | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | dB |
| 1 | 1.97 | 0.88 | 0.43 | 0.32 | 0.24 | 0.19 | 0.13 | dB |
| 2 | 3.58 | 1.67 | 0.95 | 0.76 | 0.61 | 0.5 | 0.41 | dB |
| 3 | 5.35 | 2.48 | 1.49 | 1.2 | 1 | 0.83 | 0.69 | dB |
| 4 | 7.27 | 3.31 | 2 | 1.63 | 1.36 | 1.14 | 0.96 | dB |
| 5 | — | 4.19 | 2.55 | 2.1 | 1.76 | 1.49 | 1.26 | dB |
| 6 | — | 5.08 | 3.11 | 2.56 | 2.17 | 1.83 | 1.56 | dB |
| 7 | — | 5.99 | 3.71 | 3.06 | 2.58 | 2.18 | 1.87 | dB |
| 8 | — | 6.92 | 4.22 | 3.47 | 2.93 | 2.48 | 2.11 | dB |
| 9 | — | 7.92 | 4.86 | 4 | 3.38 | 2.87 | 2.46 | dB |
| 10 | — | 9.04 | 5.46 | 4.51 | 3.79 | 3.23 | 2.77 | dB |
| 11 | — | 10.2 | 6.09 | 5.01 | 4.23 | 3.61 | — | dB |
| 12 | — | 11.56 | 6.74 | 5.51 | 4.68 | 3.97 | — | dB |
| 13 | — | 12.9 | 7.44 | 6.1 | 5.12 | 4.36 | — | dB |
| 14 | — | 14.44 | 8.12 | 6.64 | 5.57 | 4.76 | — | dB |
| 15 | — | — | 8.87 | 7.21 | 6.06 | 5.14 | — | dB |

1-40 Transceiver Compliance Specification

| Quartus Prime 1st Post Tap Pre-Emphasis Setting | Quartus Prime V _{OD} Setting | | | | | | | Unit |
|---|---------------------------------------|-------------|-------------|-------------|-------------|-------------|--------------|------|
| | 10 (200 mV) | 20 (400 mV) | 30 (600 mV) | 35 (700 mV) | 40 (800 mV) | 45 (900 mV) | 50 (1000 mV) | |
| 16 | — | — | 9.56 | 7.73 | 6.49 | — | — | dB |
| 17 | — | — | 10.43 | 8.39 | 7.02 | — | — | dB |
| 18 | — | — | 11.23 | 9.03 | 7.52 | — | — | dB |
| 19 | — | — | 12.18 | 9.7 | 8.02 | — | — | dB |
| 20 | — | — | 13.17 | 10.34 | 8.59 | — | — | dB |
| 21 | — | — | 14.2 | 11.1 | — | — | — | dB |
| 22 | — | — | 15.38 | 11.87 | — | — | — | dB |
| 23 | — | — | — | 12.67 | — | — | — | dB |
| 24 | — | — | — | 13.48 | — | — | — | dB |
| 25 | — | — | — | 14.37 | — | — | — | dB |
| 26 | — | — | — | — | — | — | — | dB |
| 27 | — | — | — | — | — | — | — | dB |
| 28 | — | — | — | — | — | — | — | dB |
| 29 | — | — | — | — | — | — | — | dB |
| 30 | — | — | — | — | — | — | — | dB |
| 31 | — | — | — | — | — | — | — | dB |

Related Information**[SPICE Models for Altera Devices](#)**

Provides the Arria V HSSI HSPICE models.

Transceiver Compliance Specification

The following table lists the physical medium attachment (PMA) specification compliance of all supported protocol for Arria V GX, GT, SX, and ST devices. For more information about the protocol parameter details and compliance specifications, contact your Altera Sales Representative.

Table 1-34: Transceiver Compliance Specification for All Supported Protocol for Arria V GX, GT, SX, and ST Devices

| Protocol | Sub-protocol | Data Rate (Mbps) |
|------------------------|--------------|------------------|
| PCIe | PCIe Gen1 | 2,500 |
| | PCIe Gen2 | 5,000 |
| | PCIe Cable | 2,500 |
| XAUI | XAUI 2135 | 3,125 |
| Serial RapidIO® (SRIO) | SRIO 1250 SR | 1,250 |
| | SRIO 1250 LR | 1,250 |
| | SRIO 2500 SR | 2,500 |
| | SRIO 2500 LR | 2,500 |
| | SRIO 3125 SR | 3,125 |
| | SRIO 3125 LR | 3,125 |
| | SRIO 5000 SR | 5,000 |
| | SRIO 5000 MR | 5,000 |
| | SRIO 5000 LR | 5,000 |
| | SRIO_6250_SR | 6,250 |
| | SRIO_6250_MR | 6,250 |
| | SRIO_6250_LR | 6,250 |

| Protocol | Sub-protocol | Data Rate (Mbps) |
|--------------------------------------|-------------------------------|------------------|
| Common Public Radio Interface (CPRI) | CPRI E6LV | 614.4 |
| | CPRI E6HV | 614.4 |
| | CPRI E6LVII | 614.4 |
| | CPRI E12LV | 1,228.8 |
| | CPRI E12HV | 1,228.8 |
| | CPRI E12LVII | 1,228.8 |
| | CPRI E24LV | 2,457.6 |
| | CPRI E24LVII | 2,457.6 |
| | CPRI E30LV | 3,072 |
| | CPRI E30LVII | 3,072 |
| | CPRI E48LVII | 4,915.2 |
| | CPRI E60LVII | 6,144 |
| | CPRI E96LVIII ⁽⁶⁰⁾ | 9,830.4 |
| | Gbps Ethernet (GbE) | GbE 1250 |
| OBSAI | OBSAI 768 | 768 |
| | OBSAI 1536 | 1,536 |
| | OBSAI 3072 | 3,072 |
| | OBSAI 6144 | 6,144 |
| Serial digital interface (SDI) | SDI 270 SD | 270 |
| | SDI 1485 HD | 1,485 |
| | SDI 2970 3G | 2,970 |

⁽⁶⁰⁾ You can achieve compliance with TX channel restriction of one HSSI channel per six-channel transceiver bank.

| Protocol | Sub-protocol | Data Rate (Mbps) |
|--|--------------|------------------|
| SONET | SONET 155 | 155.52 |
| | SONET 622 | 622.08 |
| | SONET 2488 | 2,488.32 |
| Gigabit-capable passive optical network (GPON) | GPON 155 | 155.52 |
| | GPON 622 | 622.08 |
| | GPON 1244 | 1,244.16 |
| | GPON 2488 | 2,488.32 |
| QSGMII | QSGMII 5000 | 5,000 |

Core Performance Specifications

Clock Tree Specifications

Table 1-35: Clock Tree Specifications for Arria V Devices

| Parameter | Performance | | | Unit |
|---------------------------------|-------------|----------|-----|------|
| | -I3, -C4 | -I5, -C5 | -C6 | |
| Global clock and Regional clock | 625 | 625 | 525 | MHz |
| Peripheral clock | 450 | 400 | 350 | MHz |

PLL Specifications

Table 1-36: PLL Specifications for Arria V Devices

This table lists the Arria V PLL block specifications. Arria V PLL block does not include HPS PLL.

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---------------------------|---|----------------|-----|-----|---------------------|------|
| f_{IN} | Input clock frequency | -3 speed grade | 5 | — | 800 ⁽⁶¹⁾ | MHz |
| | | -4 speed grade | 5 | — | 800 ⁽⁶¹⁾ | MHz |
| | | -5 speed grade | 5 | — | 750 ⁽⁶¹⁾ | MHz |
| | | -6 speed grade | 5 | — | 625 ⁽⁶¹⁾ | MHz |
| f_{INPFD} | Integer input clock frequency to the phase frequency detector (PFD) | — | 5 | — | 325 | MHz |
| f_{FINPFD} | Fractional input clock frequency to the PFD | — | 50 | — | 160 | MHz |
| f_{VCO} ⁽⁶²⁾ | PLL voltage-controlled oscillator (VCO) operating range | -3 speed grade | 600 | — | 1600 | MHz |
| | | -4 speed grade | 600 | — | 1600 | MHz |
| | | -5 speed grade | 600 | — | 1600 | MHz |
| | | -6 speed grade | 600 | — | 1300 | MHz |
| $t_{EINDUTY}$ | Input clock or external feedback clock input duty cycle | — | 40 | — | 60 | % |

⁽⁶¹⁾ This specification is limited in the Quartus Prime software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

⁽⁶²⁾ The VCO frequency reported by the Quartus Prime software takes into consideration the VCO post-scale counter κ value. Therefore, if the counter κ has a value of 2, the frequency reported can be lower than the f_{VCO} specification.

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|-------------------|--|----------------------|-----|-----|---------------------|------|
| f_{OUT} | Output frequency for internal global or regional clock | -3 speed grade | — | — | 500 ⁽⁶³⁾ | MHz |
| | | -4 speed grade | — | — | 500 ⁽⁶³⁾ | MHz |
| | | -5 speed grade | — | — | 500 ⁽⁶³⁾ | MHz |
| | | -6 speed grade | — | — | 400 ⁽⁶³⁾ | MHz |
| f_{OUT_EXT} | Output frequency for external clock output | -3 speed grade | — | — | 670 ⁽⁶³⁾ | MHz |
| | | -4 speed grade | — | — | 670 ⁽⁶³⁾ | MHz |
| | | -5 speed grade | — | — | 622 ⁽⁶³⁾ | MHz |
| | | -6 speed grade | — | — | 500 ⁽⁶³⁾ | MHz |
| $t_{OUTDUTY}$ | Duty cycle for external clock output (when set to 50%) | — | 45 | 50 | 55 | % |
| t_{FCOMP} | External feedback clock compensation time | — | — | — | 10 | ns |
| $t_{DYCONFIGCLK}$ | Dynamic configuration clock for <code>mgmt_clk</code> and <code>scanclk</code> | — | — | — | 100 | MHz |
| t_{LOCK} | Time required to lock from end-of-device configuration or deassertion of <code>areset</code> | — | — | — | 1 | ms |
| t_{DLOCK} | Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) | — | — | — | 1 | ms |
| f_{CLBW} | PLL closed-loop bandwidth | Low | — | 0.3 | — | MHz |
| | | Medium | — | 1.5 | — | MHz |
| | | High ⁽⁶⁴⁾ | — | 4 | — | MHz |
| t_{PLL_PSERR} | Accuracy of PLL phase shift | — | — | — | ±50 | ps |

⁽⁶³⁾ This specification is limited by the lower of the two: I/O f_{MAX} or F_{OUT} of the PLL.

⁽⁶⁴⁾ High bandwidth PLL settings are not supported in external feedback mode.

1-46 PLL Specifications

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|--|--|---------------------------------------|-----|-----|--------------------------|-----------|
| t_{ARESET} | Minimum pulse width on the <code>areset</code> signal | — | 10 | — | — | ns |
| $t_{\text{INCCJ}}^{(65)(66)}$ | Input clock cycle-to-cycle jitter | $F_{\text{REF}} \geq 100 \text{ MHz}$ | — | — | 0.15 | UI (p-p) |
| | | $F_{\text{REF}} < 100 \text{ MHz}$ | — | — | ± 750 | ps (p-p) |
| $t_{\text{OUTPJ_DC}}^{(67)}$ | Period jitter for dedicated clock output in integer PLL | $F_{\text{OUT}} \geq 100 \text{ MHz}$ | — | — | 175 | ps (p-p) |
| | | $F_{\text{OUT}} < 100 \text{ MHz}$ | — | — | 17.5 | mUI (p-p) |
| $t_{\text{FOUTPJ_DC}}^{(67)}$ | Period jitter for dedicated clock output in fractional PLL | $F_{\text{OUT}} \geq 100 \text{ MHz}$ | — | — | $250^{(68)}, 175^{(69)}$ | ps (p-p) |
| | | $F_{\text{OUT}} < 100 \text{ MHz}$ | — | — | $25^{(68)}, 17.5^{(69)}$ | mUI (p-p) |
| $t_{\text{OUTCCJ_DC}}^{(67)}$ | Cycle-to-cycle jitter for dedicated clock output in integer PLL | $F_{\text{OUT}} \geq 100 \text{ MHz}$ | — | — | 175 | ps (p-p) |
| | | $F_{\text{OUT}} < 100 \text{ MHz}$ | — | — | 17.5 | mUI (p-p) |
| $t_{\text{FOUTCCJ_DC}}^{(67)}$ | Cycle-to-cycle jitter for dedicated clock output in fractional PLL | $F_{\text{OUT}} \geq 100 \text{ MHz}$ | — | — | $250^{(68)}, 175^{(69)}$ | ps (p-p) |
| | | $F_{\text{OUT}} < 100 \text{ MHz}$ | — | — | $25^{(68)}, 17.5^{(69)}$ | mUI (p-p) |
| $t_{\text{OUTPJ_IO}}^{(67)(70)}$ | Period jitter for clock output on a regular I/O in integer PLL | $F_{\text{OUT}} \geq 100 \text{ MHz}$ | — | — | 600 | ps (p-p) |
| | | $F_{\text{OUT}} < 100 \text{ MHz}$ | — | — | 60 | mUI (p-p) |
| $t_{\text{FOUTPJ_IO}}^{(67)(68)(70)}$ | Period jitter for clock output on a regular I/O in fractional PLL | $F_{\text{OUT}} \geq 100 \text{ MHz}$ | — | — | 600 | ps (p-p) |
| | | $F_{\text{OUT}} < 100 \text{ MHz}$ | — | — | 60 | mUI (p-p) |

⁽⁶⁵⁾ A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

⁽⁶⁶⁾ F_{REF} is f_{IN}/N , specification applies when $N = 1$.

⁽⁶⁷⁾ Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Memory Output Clock Jitter Specification for Arria V Devices table.

⁽⁶⁸⁾ This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.05–0.95 must be $\geq 1000 \text{ MHz}$.

⁽⁶⁹⁾ This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.20–0.80 must be $\geq 1200 \text{ MHz}$.

⁽⁷⁰⁾ External memory interface clock output jitter specifications use a different measurement method, which are available in Memory Output Clock Jitter Specification for Arria V Devices table.

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---------------------------------------|--------|---------|------------|-----------|
| $t_{\text{OUTCCJ_IO}}^{(67)(70)}$ | Cycle-to-cycle jitter for clock output on a regular I/O in integer PLL | $F_{\text{OUT}} \geq 100 \text{ MHz}$ | — | — | 600 | ps (p-p) |
| | | $F_{\text{OUT}} < 100 \text{ MHz}$ | — | — | 60 | mUI (p-p) |
| $t_{\text{FOUTCCJ_IO}}^{(67)(68)(70)}$ | Cycle-to-cycle jitter for clock output on a regular I/O in fractional PLL | $F_{\text{OUT}} \geq 100 \text{ MHz}$ | — | — | 600 | ps (p-p) |
| | | $F_{\text{OUT}} < 100 \text{ MHz}$ | — | — | 60 | mUI (p-p) |
| $t_{\text{CASC_OUTPJ_DC}}^{(67)(71)}$ | Period jitter for dedicated clock output in cascaded PLLs | $F_{\text{OUT}} \geq 100 \text{ MHz}$ | — | — | 175 | ps (p-p) |
| | | $F_{\text{OUT}} < 100 \text{ MHz}$ | — | — | 17.5 | mUI (p-p) |
| t_{DRIFT} | Frequency drift after PFDENA is disabled for a duration of 100 μs | — | — | — | ± 10 | % |
| dK_{BIT} | Bit number of Delta Sigma Modulator (DSM) | — | 8 | 24 | 32 | bits |
| k_{VALUE} | Numerator of fraction | — | 128 | 8388608 | 2147483648 | — |
| f_{RES} | Resolution of VCO frequency | $f_{\text{INPFD}} = 100 \text{ MHz}$ | 390625 | 5.96 | 0.023 | Hz |

Related Information

[Memory Output Clock Jitter Specifications](#) on page 1-57

Provides more information about the external memory interface clock output jitter specifications.

⁽⁷¹⁾ The cascaded PLL specification is only applicable with the following conditions:

- Upstream PLL: $0.59 \text{ MHz} \leq \text{Upstream PLL BW} < 1 \text{ MHz}$
- Downstream PLL: $\text{Downstream PLL BW} > 2 \text{ MHz}$

DSP Block Performance Specifications

Table 1-37: DSP Block Performance Specifications for Arria V Devices

| | Mode | Performance | | | Unit |
|----------------------------|--|-------------|----------|-----|------|
| | | -I3, -C4 | -I5, -C5 | -C6 | |
| Modes using One DSP Block | Independent 9×9 multiplication | 370 | 310 | 220 | MHz |
| | Independent 18×19 multiplication | 370 | 310 | 220 | MHz |
| | Independent 18×25 multiplication | 370 | 310 | 220 | MHz |
| | Independent 20×24 multiplication | 370 | 310 | 220 | MHz |
| | Independent 27×27 multiplication | 310 | 250 | 200 | MHz |
| | Two 18×19 multiplier adder mode | 370 | 310 | 220 | MHz |
| | 18×18 multiplier added summed with 36-bit input | 370 | 310 | 220 | MHz |
| Modes using Two DSP Blocks | Complex 18×19 multiplication | 370 | 310 | 220 | MHz |

Memory Block Performance Specifications

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL and set to 50% output duty cycle. Use the Quartus Prime software to report timing for the memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in f_{MAX} .

Table 1-38: Memory Block Performance Specifications for Arria V Devices

| Memory | Mode | Resources Used | | Performance | | | Unit |
|------------|--|----------------|--------|-------------|----------|-----|------|
| | | ALUTs | Memory | -I3, -C4 | -I5, -C5 | -C6 | |
| MLAB | Single port, all supported widths | 0 | 1 | 500 | 450 | 400 | MHz |
| | Simple dual-port, all supported widths | 0 | 1 | 500 | 450 | 400 | MHz |
| | Simple dual-port with read and write at the same address | 0 | 1 | 400 | 350 | 300 | MHz |
| | ROM, all supported width | — | — | 500 | 450 | 400 | MHz |
| M10K Block | Single-port, all supported widths | 0 | 1 | 400 | 350 | 285 | MHz |
| | Simple dual-port, all supported widths | 0 | 1 | 400 | 350 | 285 | MHz |
| | Simple dual-port with the read-during-write option set to Old Data , all supported widths | 0 | 1 | 315 | 275 | 240 | MHz |
| | True dual port, all supported widths | 0 | 1 | 400 | 350 | 285 | MHz |
| | ROM, all supported widths | 0 | 1 | 400 | 350 | 285 | MHz |

Internal Temperature Sensing Diode Specifications

Table 1-39: Internal Temperature Sensing Diode Specifications for Arria V Devices

| Temperature Range | Accuracy | Offset Calibrated Option | Sampling Rate | Conversion Time | Resolution | Minimum Resolution with no Missing Codes |
|-------------------|----------|--------------------------|---------------|-----------------|------------|--|
| -40 to 100°C | ±8°C | No | 1 MHz | < 100 ms | 8 bits | 8 bits |

Periphery Performance

This section describes the periphery performance, high-speed I/O, and external memory interface.

Actual achievable frequency depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specifications

Table 1-40: High-Speed I/O Specifications for Arria V Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block. When J = 1 or 2, bypass the SERDES block.

For LVDS applications, you must use the PLLs in integer PLL mode.

The Arria V devices support the following output standards using true LVDS output buffer types on all I/O banks.

- True RSDS output standard with data rates of up to 360 Mbps
- True mini-LVDS output standard with data rates of up to 400 Mbps

| Symbol | | Condition | -I3, -C4 | | | -I5, -C5 | | | -C6 | | | Unit |
|--|---|--|-----------------|-----|---------------------|-----------------|-----|---------------------|-----------------|-----|---------------------|------|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{\text{HSCLK_in}}$ (input clock frequency) True Differential I/O Standards | | Clock boost factor W = 1 to 40 ⁽⁷²⁾ | 5 | — | 800 | 5 | — | 750 | 5 | — | 625 | MHz |
| $f_{\text{HSCLK_in}}$ (input clock frequency) Single-Ended I/O Standards ⁽⁷³⁾ | | Clock boost factor W = 1 to 40 ⁽⁷²⁾ | 5 | — | 625 | 5 | — | 625 | 5 | — | 500 | MHz |
| $f_{\text{HSCLK_in}}$ (input clock frequency) Single-Ended I/O Standards ⁽⁷⁴⁾ | | Clock boost factor W = 1 to 40 ⁽⁷²⁾ | 5 | — | 420 | 5 | — | 420 | 5 | — | 420 | MHz |
| $f_{\text{HSCLK_OUT}}$ (output clock frequency) | | — | 5 | — | 625 ⁽⁷⁵⁾ | 5 | — | 625 ⁽⁷⁵⁾ | 5 | — | 500 ⁽⁷⁵⁾ | MHz |
| Transmitter | True Differential I/O Standards - f_{HSDR} (data rate) | SERDES factor J = 3 to 10 ⁽⁷⁶⁾ | ⁽⁷⁷⁾ | — | 1250 | ⁽⁷⁷⁾ | — | 1250 | ⁽⁷⁷⁾ | — | 1050 | Mbps |

⁽⁷²⁾ Clock boost factor (W) is the ratio between the input data rate and the input clock rate.

⁽⁷³⁾ This applies to DPA and soft-CDR modes only.

⁽⁷⁴⁾ This applies to non-DPA mode only.

⁽⁷⁵⁾ This is achieved by using the LVDS clock network.

⁽⁷⁶⁾ The F_{max} specification is based on the fast clock used for serial data. The interface F_{max} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

⁽⁷⁷⁾ The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

| Symbol | Condition | -I3, -C4 | | | -I5, -C5 | | | -C6 | | | Unit |
|--|---|----------|-----|------|----------|-----|------|------|-----|------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| | SERDES factor $J \geq 8^{(76)(78)}$, LVDS TX with RX DPA | (77) | — | 1600 | (77) | — | 1500 | (77) | — | 1250 | Mbps |
| | SERDES factor $J = 1$ to 2, Uses DDR Registers | (77) | — | (79) | (77) | — | (79) | (77) | — | (79) | Mbps |
| Emulated Differential I/O Standards with Three External Output Resistor Network - f_{HSDR} (data rate) ⁽⁸⁰⁾ | SERDES factor $J = 4$ to $10^{(81)}$ | (77) | — | 945 | (77) | — | 945 | (77) | — | 945 | Mbps |
| Emulated Differential I/O Standards with One External Output Resistor Network - f_{HSDR} (data rate) ⁽⁸⁰⁾ | SERDES factor $J = 4$ to $10^{(81)}$ | (77) | — | 200 | (77) | — | 200 | (77) | — | 200 | Mbps |
| $t_{x \text{ Jitter}}$ - True Differential I/O Standards | Total Jitter for Data Rate 600 Mbps – 1.25 Gbps | — | — | 160 | — | — | 160 | — | — | 160 | ps |
| | Total Jitter for Data Rate < 600 Mbps | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | UI |

⁽⁷⁸⁾ The V_{CC} and V_{CCP} must be on a separate power layer and a maximum load of 5 pF for chip-to-chip interface.

⁽⁷⁹⁾ The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (f_{OUT}), provided you can close the design timing and the signal integrity simulation is clean.

⁽⁸⁰⁾ You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.

⁽⁸¹⁾ When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.

| Symbol | Condition | -I3, -C4 | | | -I5, -C5 | | | -C6 | | | Unit |
|---|--|----------|-----|------|----------|-----|------|-----|-----|------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $t_{x \text{ Jitter}}$ -Emulated Differential I/O Standards with Three External Output Resistor Network | Total Jitter for Data Rate 600 Mbps – 1.25 Gbps | — | — | 260 | — | — | 300 | — | — | 350 | ps |
| | Total Jitter for Data Rate < 600 Mbps | — | — | 0.16 | — | — | 0.18 | — | — | 0.21 | UI |
| $t_{x \text{ Jitter}}$ -Emulated Differential I/O Standards with One External Output Resistor Network | — | — | — | 0.15 | — | — | 0.15 | — | — | 0.15 | UI |
| t_{DUTY} | TX output clock duty cycle for both True and Emulated Differential I/O Standards | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | % |
| t_{RISE} and t_{FALL} | True Differential I/O Standards ⁽⁸²⁾ | — | — | 160 | — | — | 180 | — | — | 200 | ps |
| | Emulated Differential I/O Standards with Three External Output Resistor Network | — | — | 250 | — | — | 250 | — | — | 300 | ps |
| | Emulated Differential I/O Standards with One External Output Resistor Network | — | — | 500 | — | — | 500 | — | — | 500 | ps |

⁽⁸²⁾ This applies to default pre-emphasis and V_{OD} settings only.

| Symbol | | Condition | -I3, -C4 | | | -I5, -C5 | | | -C6 | | | Unit |
|---------------|--|--|-----------------|-------|-----------------|-----------------|-------|-----------------|-----------------|-------|-----------------|------|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| | TCCS | True Differential I/O Standards | — | — | 150 | — | — | 150 | — | — | 150 | ps |
| | | Emulated Differential I/O Standards | — | — | 300 | — | — | 300 | — | — | 300 | ps |
| Receiver | True Differential I/O Standards - f_{HSDRDPA} (data rate) | SERDES factor J = 3 to 10 ⁽⁷⁶⁾ | 150 | — | 1250 | 150 | — | 1250 | 150 | — | 1050 | Mbps |
| | | SERDES factor J ≥ 8 with DPA ⁽⁷⁶⁾⁽⁷⁸⁾ | 150 | — | 1600 | 150 | — | 1500 | 150 | — | 1250 | Mbps |
| | f_{HSDR} (data rate) | SERDES factor J = 3 to 10 | ⁽⁷⁷⁾ | — | ⁽⁸³⁾ | ⁽⁷⁷⁾ | — | ⁽⁸³⁾ | ⁽⁷⁷⁾ | — | ⁽⁸³⁾ | Mbps |
| | | SERDES factor J = 1 to 2, uses DDR registers | ⁽⁷⁷⁾ | — | ⁽⁷⁹⁾ | ⁽⁷⁷⁾ | — | ⁽⁷⁹⁾ | ⁽⁷⁷⁾ | — | ⁽⁷⁹⁾ | Mbps |
| DPA Mode | DPA run length | — | — | 10000 | — | — | 10000 | — | — | 10000 | UI | |
| Soft-CDR Mode | Soft-CDR ppm tolerance | — | — | 300 | — | — | 300 | — | — | 300 | ±ppm | |
| Non-DPA Mode | Sampling Window | — | — | 300 | — | — | 300 | — | — | 300 | ps | |

⁽⁸³⁾ You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

DPA Lock Time Specifications

Figure 1-4: Dynamic Phase Alignment (DPA) Lock Time Specifications with DPA PLL Calibration Enabled

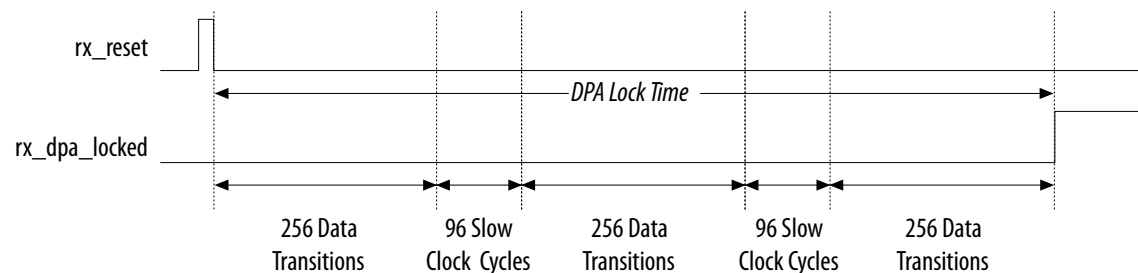


Table 1-41: DPA Lock Time Specifications for Arria V Devices

The specifications are applicable to both commercial and industrial grades. The DPA lock time is for one channel. One data transition is defined as a 0-to-1 or 1-to-0 transition.

| Standard | Training Pattern | Number of Data Transitions in One Repetition of the Training Pattern | Number of Repetitions per 256 Data Transitions ⁽⁸⁴⁾ | Maximum Data Transition |
|--------------------|--------------------|--|--|-------------------------|
| SPI-4 | 000000000111111111 | 2 | 128 | 640 |
| Parallel Rapid I/O | 00001111 | 2 | 128 | 640 |
| | 10010000 | 4 | 64 | 640 |
| Miscellaneous | 10101010 | 8 | 32 | 640 |
| | 01010101 | 8 | 32 | 640 |

⁽⁸⁴⁾ This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications

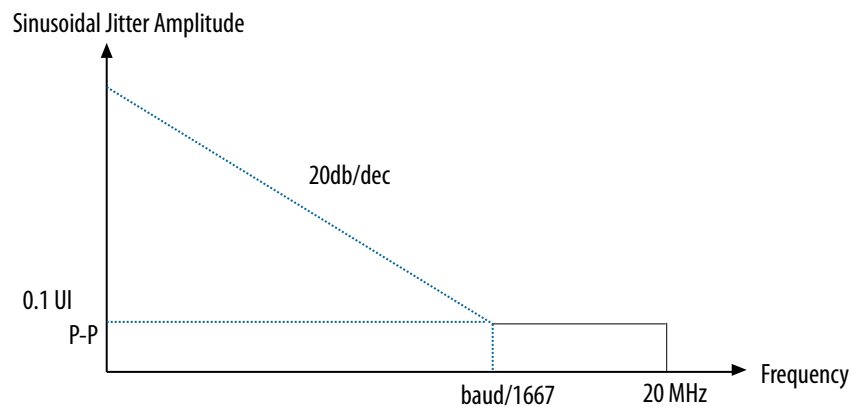
Figure 1-5: LVDS Soft-Clock Data Recovery (CDR)/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate Equal to 1.25 Gbps



Table 1-42: LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate Equal to 1.25 Gbps

| Jitter Frequency (Hz) | | Sinusoidal Jitter (UI) |
|-----------------------|------------|------------------------|
| F1 | 10,000 | 25.000 |
| F2 | 17,565 | 25.000 |
| F3 | 1,493,000 | 0.350 |
| F4 | 50,000,000 | 0.350 |

Figure 1-6: LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate Less than 1.25 Gbps



DLL Frequency Range Specifications

Table 1-43: DLL Frequency Range Specifications for Arria V Devices

| Parameter | -I3, -C4 | -I5, -C5 | -C6 | Unit |
|-------------------------------|-----------|-----------|-----------|------|
| DLL operating frequency range | 200 – 667 | 200 – 667 | 200 – 667 | MHz |

DQS Logic Block Specifications

Table 1-44: DQS Phase Shift Error Specifications for DLL-Delayed Clock (t_{DQS_PSEERR}) for Arria V Devices

This error specification is the absolute maximum and minimum error.

| Number of DQS Delay Buffer | -I3, -C4 | -I5, -C5 | -C6 | Unit |
|----------------------------|----------|----------|-----|------|
| 2 | 40 | 80 | 80 | ps |

Memory Output Clock Jitter Specifications

Table 1-45: Memory Output Clock Jitter Specifications for Arria V Devices

The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 SDRAM standard.

The memory output clock jitter is applicable when an input jitter of 30 ps (p-p) is applied with bit error rate (BER) 10^{-12} , equivalent to 14 sigma.

Altera recommends using the UniPHY intellectual property (IP) with PHYCLK connections for better jitter performance.

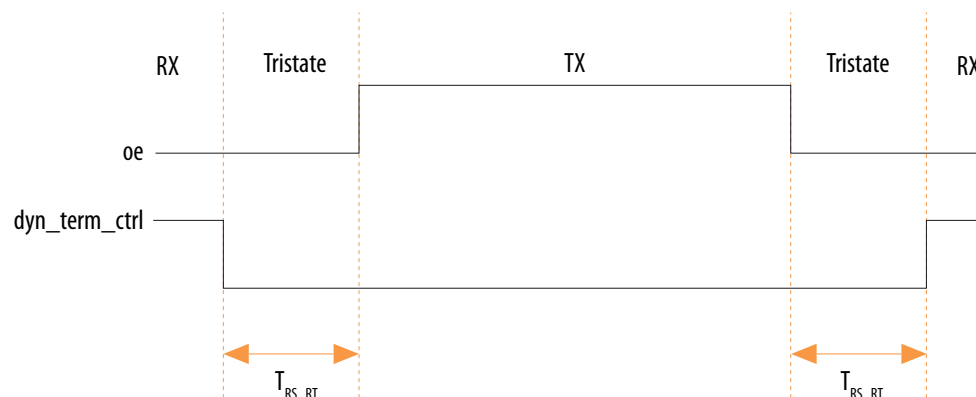
| Parameter | Clock Network | Symbol | -I3, -C4 | | -I5, -C5 | | -C6 | | Unit |
|------------------------------|---------------|----------------|----------|-----|----------|-----|-----|-----|------|
| | | | Min | Max | Min | Max | Min | Max | |
| Clock period jitter | PHYCLK | $t_{JIT(per)}$ | -41 | 41 | -50 | 50 | -55 | 55 | ps |
| Cycle-to-cycle period jitter | PHYCLK | $t_{JIT(cc)}$ | 63 | | 90 | | 94 | | ps |

OCT Calibration Block Specifications

Table 1-46: OCT Calibration Block Specifications for Arria V Devices

| Symbol | Description | Min | Typ | Max | Unit |
|----------------|---|-----|------|-----|--------|
| OCTUSRCLK | Clock required by OCT calibration blocks | — | — | 20 | MHz |
| T_{OCTCAL} | Number of OCTUSRCLK clock cycles required for R_S OCT/ R_T OCT calibration | — | 1000 | — | Cycles |
| $T_{OCTSHIFT}$ | Number of OCTUSRCLK clock cycles required for OCT code to shift out | — | 32 | — | Cycles |
| T_{RS_RT} | Time required between the <code>dyn_term_ctrl</code> and <code>oe</code> signal transitions in a bidirectional I/O buffer to dynamically switch between R_S OCT and R_T OCT | — | 2.5 | — | ns |

Figure 1-7: Timing Diagram for oe and dyn_term_ctrl Signals



Duty Cycle Distortion (DCD) Specifications

Table 1-47: Worst-Case DCD on Arria V I/O Pins

The output DCD cycle only applies to the I/O buffer. It does not cover the system DCD.

| Symbol | -I3, -C4 | | -C5, -I5 | | -C6 | | Unit |
|-------------------|----------|-----|----------|-----|-----|-----|------|
| | Min | Max | Min | Max | Min | Max | |
| Output Duty Cycle | 45 | 55 | 45 | 55 | 45 | 55 | % |

HPS Specifications

This section provides HPS specifications and timing for Arria V devices.

For HPS reset, the minimum reset pulse widths for the HPS cold and warm reset signals (HPS_nRST and HPS_nPOR) are six clock cycles of HPS_CLK1.

HPS Clock Performance

Table 1-48: HPS Clock Performance for Arria V Devices

| Symbol/Description | -I3 | -C4 | -C5, -I5 | -C6 | Unit |
|--|------|-----|----------|-----|------|
| mpu_base_clk (microprocessor unit clock) | 1050 | 925 | 800 | 700 | MHz |
| main_base_clk (L3/L4 interconnect clock) | 400 | 400 | 400 | 350 | MHz |
| h2f_user0_clk | 100 | 100 | 100 | 100 | MHz |
| h2f_user1_clk | 100 | 100 | 100 | 100 | MHz |
| h2f_user2_clk | 200 | 200 | 200 | 160 | MHz |

HPS PLL Specifications

HPS PLL VCO Frequency Range

Table 1-49: HPS PLL VCO Frequency Range for Arria V Devices

| Description | Speed Grade | Minimum | Maximum | Unit |
|-------------|---------------|---------|---------|------|
| VCO range | -C5, -I5, -C6 | 320 | 1,600 | MHz |
| | -C4 | 320 | 1,850 | MHz |
| | -I3 | 320 | 2,100 | MHz |

HPS PLL Input Clock Range

The HPS PLL input clock range is 10 – 50 MHz. This clock range applies to both HPS_CLK1 and HPS_CLK2 inputs.

Related Information

[Clock Select, Booting and Configuration chapter](#)

Provides more information about the clock range for different values of clock select (CSEL).

HPS PLL Input Jitter

Use the following equation to determine the maximum input jitter (peak-to-peak) the HPS PLLs can tolerate. The divide value (N) is the value programmed into the denominator field of the VCO register for each PLL. The PLL input reference clock is divided by this value. The range of the denominator is 1 to 64.

$$\text{Maximum input jitter} = \text{Input clock period} \times \text{Divide value (N)} \times 0.02$$

Table 1-50: Examples of Maximum Input Jitter

| Input Reference Clock Period | Divide Value (N) | Maximum Jitter | Unit |
|------------------------------|------------------|----------------|------|
| 40 ns | 1 | 0.8 | ns |
| 40 ns | 2 | 1.6 | ns |
| 40 ns | 4 | 3.2 | ns |

Quad SPI Flash Timing Characteristics**Table 1-51: Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Arria V Devices**

| Symbol | Description | Min | Typ | Max | Unit |
|--------------------------|--|---|-----------------------|---|------|
| F_{clk} | SCLK_OUT clock frequency (External clock) | — | — | 108 | MHz |
| $T_{\text{qspi_clk}}$ | QSPI_CLK clock period (Internal reference clock) | 2.32 | — | — | ns |
| $T_{\text{duty_cycle}}$ | SCLK_OUT duty cycle | 45 | — | 55 | % |
| T_{dssfrst} | Output delay QSPI_SS valid before first clock edge | — | 1/2 cycle of SCLK_OUT | — | ns |
| T_{dsslst} | Output delay QSPI_SS valid after last clock edge | -1 | — | 1 | ns |
| T_{dio} | I/O data output delay | -1 | — | 1 | ns |
| $T_{\text{din_start}}$ | Input data valid start | — | — | $(2 + R_{\text{delay}}) \times T_{\text{qspi_clk}} - 7.52$ ⁽⁸⁵⁾ | ns |
| $T_{\text{din_end}}$ | Input data valid end | $(2 + R_{\text{delay}}) \times T_{\text{qspi_clk}} - 1.21$ ⁽⁸⁵⁾ | — | — | ns |

Figure 1-8: Quad SPI Flash Timing Diagram

This timing diagram illustrates clock polarity mode 0 and clock phase mode 0.

**Related Information**

[Quad SPI Flash Controller Chapter, Arria V Hard Processor System Technical Reference Manual](#)

Provides more information about Rdelay.

SPI Timing Characteristics**Table 1-52: SPI Master Timing Requirements for Arria V Devices**

The setup and hold times can be used for Texas Instruments SSP mode and National Semiconductor Microwire mode.

| Symbol | Description | Min | Max | Unit |
|-----------|---|----------------------|-----|------|
| T_{clk} | CLK clock period | 16.67 | — | ns |
| T_{su} | SPI Master-in slave-out (MISO) setup time | 8.35 ⁽⁸⁶⁾ | — | ns |
| T_h | SPI MISO hold time | 1 | — | ns |

⁽⁸⁵⁾ R_{delay} is set by programming the register `qspiregs.rddatacap`. For the SoC EDS software version 13.1 and later, Altera provides automatic Quad SPI calibration in the preloader. For more information about R_{delay} , refer to the Quad SPI Flash Controller chapter in the Arria V Hard Processor System Technical Reference Manual.

⁽⁸⁶⁾ This value is based on `rx_sample_dly = 1` and `spi_m_clk = 120 MHz`. `spi_m_clk` is the internal clock that is used by SPI Master to derive its `SCLK_OUT`. These timings are based on `rx_sample_dly` of 1. This delay can be adjusted as needed to accommodate slower response times from the slave. Note that a delay of 0 is not allowed. The setup time can be used as a reference starting point. It is very crucial to do a calibration to get the correct `rx_sample_dly` value because each SPI slave device may have different output delay and each application board may have different path delay. For more information about `rx_sample_delay`, refer to the SPI Controller chapter in the Hard Processor System Technical Reference Manual.

1-62 SPI Timing Characteristics

| Symbol | Description | Min | Max | Unit |
|------------------------|---|-----|-----|------|
| $T_{\text{dutycycle}}$ | SPI_CLK duty cycle | 45 | 55 | % |
| T_{dssfrst} | Output delay SPI_SS valid before first clock edge | 8 | — | ns |
| T_{dsslst} | Output delay SPI_SS valid after last clock edge | 8 | — | ns |
| T_{dio} | Master-out slave-in (MOSI) output delay | -1 | 1 | ns |

Figure 1-9: SPI Master Timing Diagram

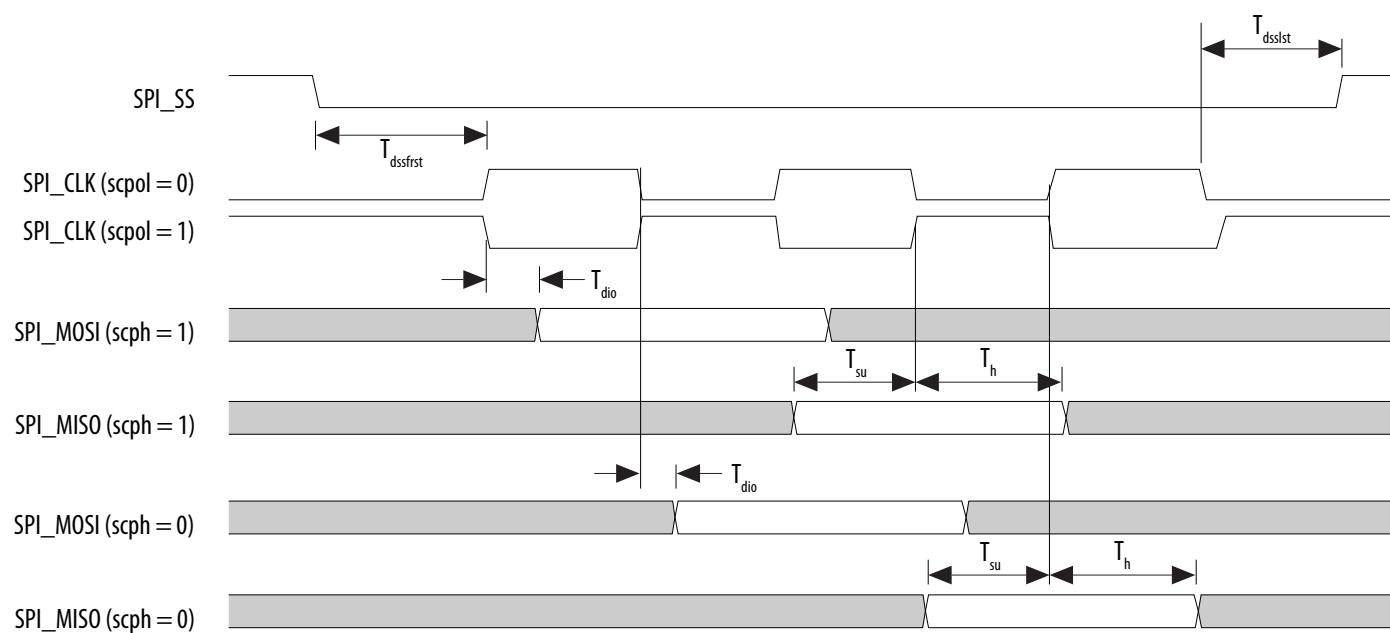


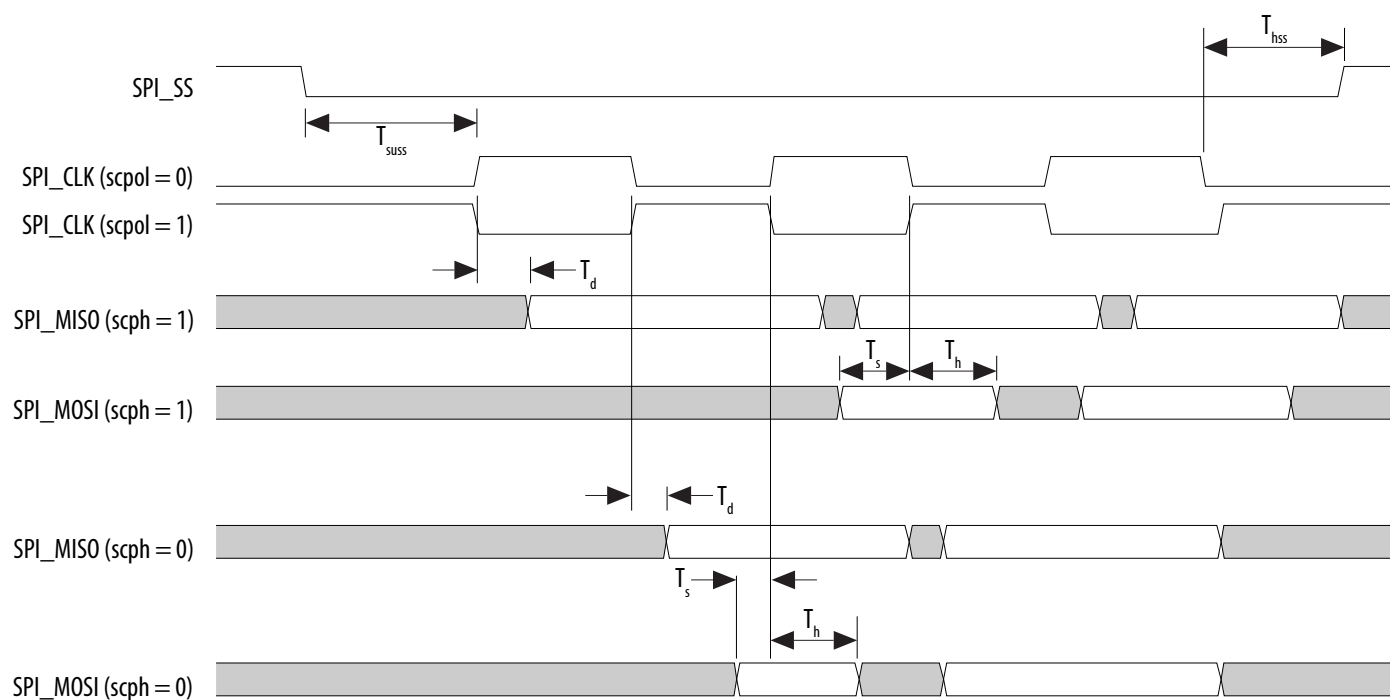
Table 1-53: SPI Slave Timing Requirements for Arria V Devices

The setup and hold times can be used for Texas Instruments SSP mode and National Semiconductor Microwire mode.

| Symbol | Description | Min | Max | Unit |
|------------------|------------------|-----|-----|------|
| T_{clk} | CLK clock period | 20 | — | ns |

| Symbol | Description | Min | Max | Unit |
|------------|---|-----|-----|------|
| T_s | MOSI Setup time | 5 | — | ns |
| T_h | MOSI Hold time | 5 | — | ns |
| T_{suss} | Setup time SPI_SS valid before first clock edge | 8 | — | ns |
| T_{hss} | Hold time SPI_SS valid after last clock edge | 8 | — | ns |
| T_d | MISO output delay | — | 6 | ns |

Figure 1-10: SPI Slave Timing Diagram



1-64 SD/MMC Timing Characteristics

Related Information

[SPI Controller, Arria V Hard Processor System Technical Reference Manual](#)

Provides more information about rx_sample_delay.

SD/MMC Timing Characteristics

Table 1-54: Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Arria V Devices

After power up or cold reset, the Boot ROM uses `drvsel = 3` and `smp1sel = 0` to execute the code. At the same time, the SD/MMC controller enters the Identification Phase followed by the Data Phase. During this time, the value of interface output clock `SDMMC_CLK_OUT` changes from a maximum of 400 kHz (Identification Phase) up to a maximum of 12.5 MHz (Data Phase), depending on the internal reference clock `SDMMC_CLK` and the `CSEL` setting. The value of `SDMMC_CLK` is based on the external oscillator frequency and has a maximum value of 50 MHz.

After the Boot ROM code exits and control is passed to the preloader, software can adjust the value of `drvsel` and `smp1sel` via the system manager. `drvsel` can be set from 1 to 7 and `smp1sel` can be set from 0 to 7. While the preloader is executing, the values for `SDMMC_CLK` and `SDMMC_CLK_OUT` increase to a maximum of 200 MHz and 50 MHz respectively.

The SD/MMC interface calibration support will be available in a future release of the preloader through the SoC EDS software update.

| Symbol | Description | Min | Max | Unit |
|--|--|--|--|------|
| T_{sdmmc_clk} (internal reference clock) | SDMMC_CLK clock period (Identification mode) | 20 | — | ns |
| | SDMMC_CLK clock period (Default speed mode) | 5 | — | ns |
| | SDMMC_CLK clock period (High speed mode) | 5 | — | ns |
| $T_{sdmmc_clk_out}$ (interface output clock) | SDMMC_CLK_OUT clock period (Identification mode) | 2500 | — | ns |
| | SDMMC_CLK_OUT clock period (Default speed mode) | 40 | — | ns |
| | SDMMC_CLK_OUT clock period (High speed mode) | 20 | — | ns |
| $T_{dutycycle}$ | SDMMC_CLK_OUT duty cycle | 45 | 55 | % |
| T_d | SDMMC_CMD/SDMMC_D output delay | $(T_{sdmmc_clk} \times drvsel)/2 - 1.23^{(87)}$ | $(T_{sdmmc_clk} \times drvsel)/2 + 1.69^{(87)}$ | ns |

| Symbol | Description | Min | Max | Unit |
|----------|------------------|--|-----|------|
| T_{su} | Input setup time | $1.05 - (T_{sdmmc_clk} \times \text{smp1sel})/2^{(88)}$ | — | ns |
| T_h | Input hold time | $(T_{sdmmc_clk} \times \text{smp1sel})/2^{(88)}$ | — | ns |

Figure 1-11: SD/MMC Timing Diagram

**Related Information**

[Booting and Configuration Chapter, Arria V Hard Processor System Technical Reference Manual](#)

Provides more information about CSEL pin settings in the SD/MMC Controller CSEL Pin Settings table.

USB Timing Characteristics

PHYs that support LPM mode may not function properly with the USB controller due to a timing issue. It is recommended that designers use the MicroChip USB3300 PHY device that has been proven to be successful on the development board.

Table 1-55: USB Timing Requirements for Arria V Devices

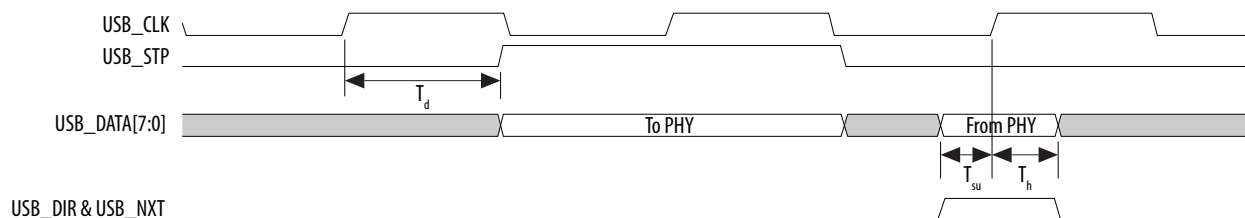
| Symbol | Description | Min | Typ | Max | Unit |
|-----------|----------------------|-----|-------|-----|------|
| T_{clk} | USB CLK clock period | — | 16.67 | — | ns |

⁽⁸⁷⁾ $drvsel$ is the drive clock phase shift select value.

⁽⁸⁸⁾ $smp1sel$ is the sample clock phase shift select value.

| Symbol | Description | Min | Typ | Max | Unit |
|----------|--|-----|-----|-----|------|
| T_d | CLK to USB_STP/USB_DATA[7:0] output delay | 4.4 | — | 11 | ns |
| T_{su} | Setup time for USB_DIR/USB_NXT/USB_DATA[7:0] | 2 | — | — | ns |
| T_h | Hold time for USB_DIR/USB_NXT/USB_DATA[7:0] | 1 | — | — | ns |

Figure 1-12: USB Timing Diagram



Ethernet Media Access Controller (EMAC) Timing Characteristics

Table 1-56: Reduced Gigabit Media Independent Interface (RGMII) TX Timing Requirements for Arria V Devices

| Symbol | Description | Min | Typ | Max | Unit |
|------------------------|--|-------|-----|------|------|
| T_{clk} (1000Base-T) | TX_CLK clock period | — | 8 | — | ns |
| T_{clk} (100Base-T) | TX_CLK clock period | — | 40 | — | ns |
| T_{clk} (10Base-T) | TX_CLK clock period | — | 400 | — | ns |
| T_{duty} | TX_CLK duty cycle | 45 | — | 55 | % |
| T_d | TX_CLK to TXD/TX_CTL output data delay | -0.85 | — | 0.15 | ns |

Figure 1-13: RGMII TX Timing Diagram



Table 1-57: RGMII RX Timing Requirements for Arria V Devices

| Symbol | Description | Min | Typ | Unit |
|------------------------|------------------------|-----|-----|------|
| T_{clk} (1000Base-T) | RX_CLK clock period | — | 8 | ns |
| T_{clk} (100Base-T) | RX_CLK clock period | — | 40 | ns |
| T_{clk} (10Base-T) | RX_CLK clock period | — | 400 | ns |
| T_{su} | RX_D/RX_CTL setup time | 1 | — | ns |
| T_h | RX_D/RX_CTL hold time | 1 | — | ns |

Figure 1-14: RGMII RX Timing Diagram

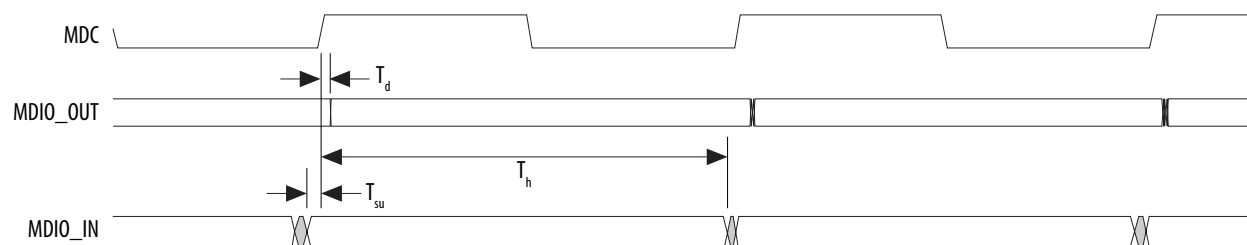


Table 1-58: Management Data Input/Output (MDIO) Timing Requirements for Arria V Devices

| Symbol | Description | Min | Typ | Unit |
|-----------|-------------------------------|-----|-----|------|
| T_{clk} | MDC clock period | — | 400 | ns |
| T_d | MDC to MDIO output data delay | 10 | — | ns |

| Symbol | Description | Min | Typ | Unit |
|--------|--------------------------|-----|-----|------|
| T_s | Setup time for MDIO data | 10 | — | ns |
| T_h | Hold time for MDIO data | 0 | — | ns |

Figure 1-15: MDIO Timing Diagram



I²C Timing Characteristics

Table 1-59: I²C Timing Requirements for Arria V Devices

| Symbol | Description | Standard Mode | | Fast Mode | | Unit |
|-----------------|---|---------------|------|-----------|-----|---------|
| | | Min | Max | Min | Max | |
| T_{clk} | Serial clock (SCL) clock period | 10 | — | 2.5 | — | μ s |
| $T_{clkhigh}$ | SCL high time | 4.7 | — | 0.6 | — | μ s |
| T_{clklow} | SCL low time | 4 | — | 1.3 | — | μ s |
| T_s | Setup time for serial data line (SDA) data to SCL | 0.25 | — | 0.1 | — | μ s |
| T_h | Hold time for SCL to SDA data | 0 | 3.45 | 0 | 0.9 | μ s |
| T_d | SCL to SDA output data delay | — | 0.2 | — | 0.2 | μ s |
| T_{su_start} | Setup time for a repeated start condition | 4.7 | — | 0.6 | — | μ s |
| T_{hd_start} | Hold time for a repeated start condition | 4 | — | 0.6 | — | μ s |
| T_{su_stop} | Setup time for a stop condition | 4 | — | 0.6 | — | μ s |

Figure 1-16: I²C Timing Diagram

NAND Timing Characteristics

Table 1-60: NAND ONFI 1.0 Timing Requirements for Arria V Devices

The NAND controller supports Open NAND FLASH Interface (ONFI) 1.0 Mode 5 timing as well as legacy NAND devices. This table lists the requirements for ONFI 1.0 mode 5 timing. The HPS NAND controller can meet this timing by programming the c4 output of the main HPS PLL and timing registers provided in the NAND controller.

| Symbol | Description | Min | Max | Unit |
|--------------------|---|-----|-----|------|
| $T_{wp}^{(89)}$ | Write enable pulse width | 10 | — | ns |
| $T_{wh}^{(89)}$ | Write enable hold time | 7 | — | ns |
| $T_{rp}^{(89)}$ | Read enable pulse width | 10 | — | ns |
| $T_{reh}^{(89)}$ | Read enable hold time | 7 | — | ns |
| $T_{clesu}^{(89)}$ | Command latch enable to write enable setup time | 10 | — | ns |
| $T_{cleh}^{(89)}$ | Command latch enable to write enable hold time | 5 | — | ns |
| $T_{cesu}^{(89)}$ | Chip enable to write enable setup time | 15 | — | ns |
| $T_{ceh}^{(89)}$ | Chip enable to write enable hold time | 5 | — | ns |
| $T_{alesu}^{(89)}$ | Address latch enable to write enable setup time | 10 | — | ns |
| $T_{aleh}^{(89)}$ | Address latch enable to write enable hold time | 5 | — | ns |
| $T_{dsu}^{(89)}$ | Data to write enable setup time | 10 | — | ns |

⁽⁸⁹⁾ Timing of the NAND interface is controlled through the NAND configuration registers.

1-70 NAND Timing Characteristics

| Symbol | Description | Min | Max | Unit |
|-----------------|------------------------------------|-----|-----|------|
| $T_{dh}^{(89)}$ | Data to write enable hold time | 5 | — | ns |
| T_{cea} | Chip enable to data access time | — | 25 | ns |
| T_{rea} | Read enable to data access time | — | 16 | ns |
| T_{rhz} | Read enable to data high impedance | — | 100 | ns |
| T_{rr} | Ready to read enable low | 20 | — | ns |

Figure 1-17: NAND Command Latch Timing Diagram

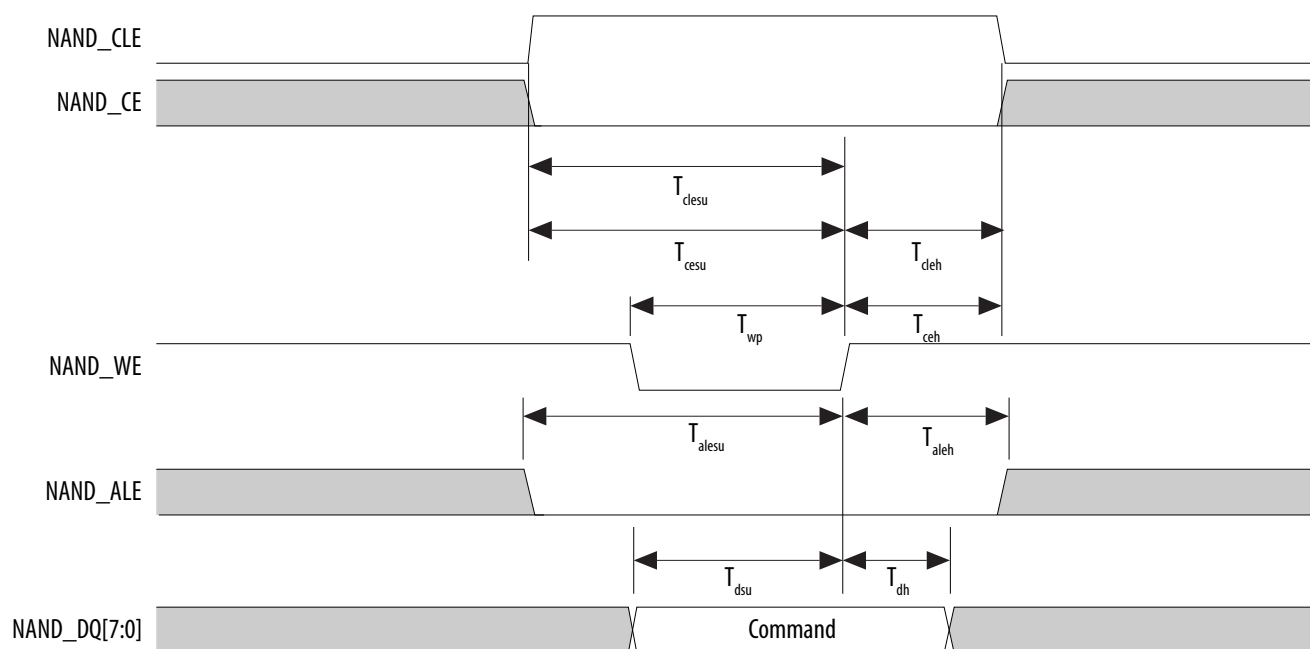


Figure 1-18: NAND Address Latch Timing Diagram

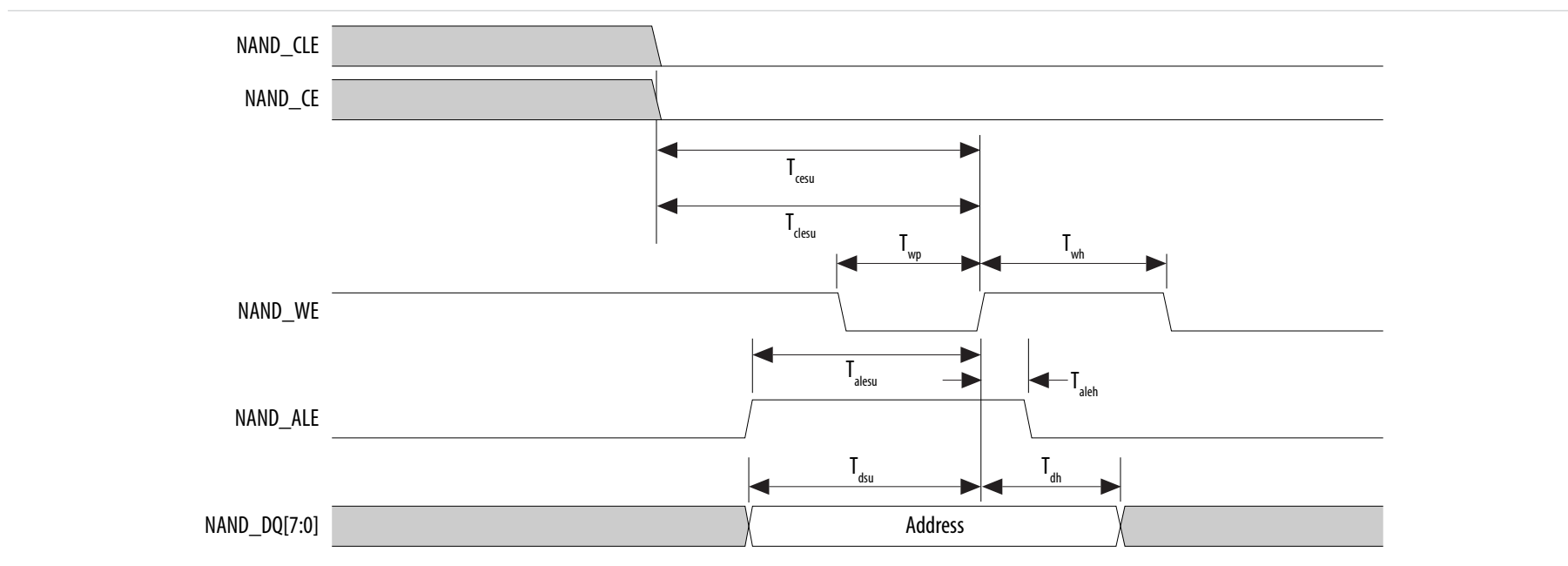


Figure 1-19: NAND Data Write Timing Diagram



Figure 1-20: NAND Data Read Timing Diagram



ARM Trace Timing Characteristics

Table 1-61: ARM Trace Timing Requirements for Arria V Devices

Most debugging tools have a mechanism to adjust the capture point of trace data.

| Description | Min | Max | Unit |
|---------------------------------|------|-----|------|
| CLK clock period | 12.5 | — | ns |
| CLK maximum duty cycle | 45 | 55 | % |
| CLK to D0 –D7 output data delay | –1 | 1 | ns |

UART Interface

The maximum UART baud rate is 6.25 megasymbols per second.

GPIO Interface

The minimum detectable general-purpose I/O (GPIO) pulse width is 2 μ s. The pulse width is based on a debounce clock frequency of 1 MHz.

HPS JTAG Timing Specifications

Table 1-62: HPS JTAG Timing Parameters and Values for Arria V Devices

| Symbol | Description | Min | Max | Unit |
|------------------|--|-----|--------------------|------|
| t_{JCP} | TCK clock period | 30 | — | ns |
| t_{JCH} | TCK clock high time | 14 | — | ns |
| t_{JCL} | TCK clock low time | 14 | — | ns |
| t_{JPSU} (TDI) | TDI JTAG port setup time | 2 | — | ns |
| t_{JPSU} (TMS) | TMS JTAG port setup time | 3 | — | ns |
| t_{JPH} | JTAG port hold time | 5 | — | ns |
| t_{JPCO} | JTAG port clock to output | — | 12 ⁽⁹⁰⁾ | ns |
| t_{JPZX} | JTAG port high impedance to valid output | — | 14 ⁽⁹⁰⁾ | ns |
| t_{JPXZ} | JTAG port valid output to high impedance | — | 14 ⁽⁹⁰⁾ | ns |

Configuration Specifications

This section provides configuration specifications and timing for Arria V devices.

POR Specifications

Table 1-63: Fast and Standard POR Delay Specification for Arria V Devices

| POR Delay | Minimum | Maximum | Unit |
|-----------|---------|--------------------|------|
| Fast | 4 | 12 ⁽⁹¹⁾ | ms |
| Standard | 100 | 300 | ms |

⁽⁹⁰⁾ A 1-ns adder is required for each V_{CCIO_HPS} voltage step down from 3.0 V. For example, t_{JPCO} = 13 ns if V_{CCIO_HPS} of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.

⁽⁹¹⁾ The maximum pulse width of the fast POR delay is 12 ms, providing enough time for the PCIe hard IP to initialize after the POR trip.

Related Information**MSEL Pin Settings**

Provides more information about POR delay based on MSEL pin settings for each configuration scheme.

FPGA JTAG Configuration Timing**Table 1-64: FPGA JTAG Timing Parameters and Values for Arria V Devices**

| Symbol | Description | Min | Max | Unit |
|-------------------------|--|-------------------------|--------------------|------|
| t _{JCP} | TCK clock period | 30, 167 ⁽⁹²⁾ | — | ns |
| t _{JCH} | TCK clock high time | 14 | — | ns |
| t _{JCL} | TCK clock low time | 14 | — | ns |
| t _{JPSU (TDI)} | TDI JTAG port setup time | 2 | — | ns |
| t _{JPSU (TMS)} | TMS JTAG port setup time | 3 | — | ns |
| t _{JPH} | JTAG port hold time | 5 | — | ns |
| t _{JPCO} | JTAG port clock to output | — | 12 ⁽⁹³⁾ | ns |
| t _{JPZX} | JTAG port high impedance to valid output | — | 14 ⁽⁹³⁾ | ns |
| t _{JPXZ} | JTAG port valid output to high impedance | — | 14 ⁽⁹³⁾ | ns |

FPP Configuration Timing**DCLK-to-DATA[] Ratio (r) for FPP Configuration**

Fast passive parallel (FPP) configuration requires a different DCLK-to-DATA[] ratio when you turn on encryption or the compression feature.

Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is *r* times the DATA[] rate in byte per second (Bps) or word per second (Wps). For example, in FPP ×16 where the *r* is 2, the DCLK frequency must be 2 times the DATA[] rate in Wps.

⁽⁹²⁾ The minimum TCK clock period is 167 ns if V_{CCBAT} is within the range 1.2 V – 1.5 V when you perform the volatile key programming.

⁽⁹³⁾ A 1-ns adder is required for each VCCIO voltage step down from 3.0 V. For example, t_{JPCO} = 13 ns if VCCIO of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.

1-76 FPP Configuration Timing when DCLK-to-DATA[] = 1

Table 1-65: DCLK-to-DATA[] Ratio for Arria V Devices

| Configuration Scheme | Encryption | Compression | DCLK-to-DATA[] Ratio (r) |
|----------------------|------------|-------------|--------------------------|
| FPP (8-bit wide) | Off | Off | 1 |
| | On | Off | 1 |
| | Off | On | 2 |
| | On | On | 2 |
| FPP (16-bit wide) | Off | Off | 1 |
| | On | Off | 2 |
| | Off | On | 4 |
| | On | On | 4 |

FPP Configuration Timing when DCLK-to-DATA[] = 1

When you enable decompression or the design security feature, the DCLK-to-DATA[] ratio varies for FPP ×8 and FPP ×16. For the respective DCLK-to-DATA[] ratio, refer to the DCLK-to-DATA[] Ratio for Arria V Devices table.

Table 1-66: FPP Timing Parameters When DCLK-to-DATA[] Ratio is 1 for Arria V Devices

| Symbol | Parameter | Minimum | Maximum | Unit |
|------------------------------------|---|---------|----------------------|------|
| t _{CF2CD} | nCONFIG low to CONF_DONE low | — | 600 | ns |
| t _{CF2ST0} | nCONFIG low to nSTATUS low | — | 600 | ns |
| t _{CFG} | nCONFIG low pulse width | 2 | — | μs |
| t _{STATUS} | nSTATUS low pulse width | 268 | 1506 ⁽⁹⁴⁾ | μs |
| t _{CF2ST1} | nCONFIG high to nSTATUS high | — | 1506 ⁽⁹⁵⁾ | μs |
| t _{CF2CK} ⁽⁹⁶⁾ | nCONFIG high to first rising edge on DCLK | 1506 | — | μs |

⁽⁹⁴⁾ You can obtain this value if you do not delay configuration by extending the nCONFIG or the nSTATUS low pulse width.

⁽⁹⁵⁾ You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.

⁽⁹⁶⁾ If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

| Symbol | Parameter | Minimum | Maximum | Unit |
|--------------------|---|---|---------|---------|
| $t_{ST2CK}^{(96)}$ | nSTATUS high to first rising edge of DCLK | 2 | — | μ s |
| t_{DSU} | DATA[] setup time before rising edge on DCLK | 5.5 | — | ns |
| t_{DH} | DATA[] hold time after rising edge on DCLK | 0 | — | ns |
| t_{CH} | DCLK high time | $0.45 \times 1/f_{MAX}$ | — | s |
| t_{CL} | DCLK low time | $0.45 \times 1/f_{MAX}$ | — | s |
| t_{CLK} | DCLK period | $1/f_{MAX}$ | — | s |
| f_{MAX} | DCLK frequency (FPP $\times 8/ \times 16$) | — | 125 | MHz |
| t_{CD2UM} | CONF_DONE high to user mode ⁽⁹⁷⁾ | 175 | 437 | μ s |
| t_{CD2CU} | CONF_DONE high to CLKUSR enabled | 4 \times maximum DCLK period | — | — |
| t_{CD2UMC} | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU} + (T_{init} \times CLKUSR \text{ period})$ | — | — |
| T_{init} | Number of clock cycles required for device initialization | 17,408 | — | Cycles |

Related Information**FPP Configuration Timing**

Provides the FPP configuration timing waveforms.

FPP Configuration Timing when DCLK-to-DATA[] >1**Table 1-67: FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Arria V Devices**

Use these timing parameters when you use the decompression and design security features.

| Symbol | Parameter | Minimum | Maximum | Unit |
|--------------|------------------------------|---------|---------|---------|
| t_{CF2CD} | nCONFIG low to CONF_DONE low | — | 600 | ns |
| t_{CF2ST0} | nCONFIG low to nSTATUS low | — | 600 | ns |
| t_{CFG} | nCONFIG low pulse width | 2 | — | μ s |

⁽⁹⁷⁾ The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

1-78 FPP Configuration Timing when DCLK-to-DATA[] >1

| Symbol | Parameter | Minimum | Maximum | Unit |
|---------------------|---|---|----------------------|---------|
| t_{STATUS} | nSTATUS low pulse width | 268 | 1506 ⁽⁹⁸⁾ | μ s |
| t_{CF2ST1} | nCONFIG high to nSTATUS high | — | 1506 ⁽⁹⁹⁾ | μ s |
| $t_{CF2CK}^{(100)}$ | nCONFIG high to first rising edge on DCLK | 1506 | — | μ s |
| $t_{ST2CK}^{(100)}$ | nSTATUS high to first rising edge of DCLK | 2 | — | μ s |
| t_{DSU} | DATA[] setup time before rising edge on DCLK | 5.5 | — | ns |
| t_{DH} | DATA[] hold time after rising edge on DCLK | $N - 1/f_{DCLK}^{(101)}$ | — | s |
| t_{CH} | DCLK high time | $0.45 \times 1/f_{MAX}$ | — | s |
| t_{CL} | DCLK low time | $0.45 \times 1/f_{MAX}$ | — | s |
| t_{CLK} | DCLK period | $1/f_{MAX}$ | — | s |
| f_{MAX} | DCLK frequency (FPP $\times 8/ \times 16$) | — | 125 | MHz |
| t_R | Input rise time | — | 40 | ns |
| t_F | Input fall time | — | 40 | ns |
| t_{CD2UM} | CONF_DONE high to user mode ⁽¹⁰²⁾ | 175 | 437 | μ s |
| t_{CD2CU} | CONF_DONE high to CLKUSR enabled | 4 \times maximum DCLK period | — | — |
| t_{CD2UMC} | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU} + (T_{init} \times CLKUSR \text{ period})$ | — | — |
| T_{init} | Number of clock cycles required for device initialization | 17,408 | — | Cycles |

Related Information**FPP Configuration Timing**

Provides the FPP configuration timing waveforms.

⁽⁹⁸⁾ This value can be obtained if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

⁽⁹⁹⁾ This value can be obtained if you do not delay configuration by externally holding nSTATUS low.

⁽¹⁰⁰⁾ If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

⁽¹⁰¹⁾ N is the DCLK-to-DATA[] ratio and f_{DCLK} is the DCLK frequency of the system.

⁽¹⁰²⁾ The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

AS Configuration Timing

Table 1-68: AS Timing Parameters for AS ×1 and ×4 Configurations in Arria V Devices

The minimum and maximum numbers apply to both the internal oscillator and CLKUSR when either one is used as the clock source for device configuration.

The t_{CF2CD} , t_{CF2ST0} , t_{CFG} , t_{STATUS} , and t_{CF2ST1} timing parameters are identical to the timing parameters for passive serial (PS) mode listed in PS Timing Parameters for Arria V Devices table. You can obtain the t_{CF2ST1} value if you do not delay configuration by externally holding nSTATUS low.

| Symbol | Parameter | Minimum | Maximum | Unit |
|--------------|---|--|---------|--------|
| t_{CO} | DCLK falling edge to the AS_DATA0/ASDO output | — | 2 | ns |
| t_{SU} | Data setup time before the falling edge on DCLK | 1.5 | — | ns |
| t_{DH} | Data hold time after the falling edge on DCLK | 0 | — | ns |
| t_{CD2UM} | CONF_DONE high to user mode | 175 | 437 | μs |
| t_{CD2CU} | CONF_DONE high to CLKUSR enabled | 4 × maximum DCLK period | — | — |
| t_{CD2UMC} | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU} + (T_{init} \times \text{CLKUSR period})$ | — | — |
| T_{init} | Number of clock cycles required for device initialization | 17,408 | — | Cycles |

Related Information

- [PS Configuration Timing](#) on page 1-80
- [AS Configuration Timing](#)
Provides the AS configuration timing waveform.

DCLK Frequency Specification in the AS Configuration Scheme

Table 1-69: DCLK Frequency Specification in the AS Configuration Scheme

This table lists the internal clock frequency specification for the AS configuration scheme. The DCLK frequency specification applies when you use the internal oscillator as the configuration clock source. The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

| Parameter | Minimum | Typical | Maximum | Unit |
|---|---------|---------|---------|------|
| DCLK frequency in AS configuration scheme | 5.3 | 7.9 | 12.5 | MHz |
| | 10.6 | 15.7 | 25.0 | MHz |
| | 21.3 | 31.4 | 50.0 | MHz |
| | 42.6 | 62.9 | 100.0 | MHz |

PS Configuration Timing

Table 1-70: PS Timing Parameters for Arria V Devices

| Symbol | Parameter | Minimum | Maximum | Unit |
|---------------------|---|---------|-----------------------|---------|
| t_{CF2CD} | nCONFIG low to CONF_DONE low | — | 600 | ns |
| t_{CF2ST0} | nCONFIG low to nSTATUS low | — | 600 | ns |
| t_{CFG} | nCONFIG low pulse width | 2 | — | μ s |
| t_{STATUS} | nSTATUS low pulse width | 268 | 1506 ⁽¹⁰³⁾ | μ s |
| t_{CF2ST1} | nCONFIG high to nSTATUS high | — | 1506 ⁽¹⁰⁴⁾ | μ s |
| $t_{CF2CK}^{(105)}$ | nCONFIG high to first rising edge on DCLK | 1506 | — | μ s |
| $t_{ST2CK}^{(105)}$ | nSTATUS high to first rising edge of DCLK | 2 | — | μ s |
| t_{DSU} | DATA[] setup time before rising edge on DCLK | 5.5 | — | ns |
| t_{DH} | DATA[] hold time after rising edge on DCLK | 0 | — | ns |

⁽¹⁰³⁾ You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

⁽¹⁰⁴⁾ You can obtain this value if you do not delay configuration by externally holding nSTATUS low.

⁽¹⁰⁵⁾ If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

| Symbol | Parameter | Minimum | Maximum | Unit |
|--------------|---|---|---------|---------|
| t_{CH} | DCLK high time | $0.45 \times 1/f_{MAX}$ | — | s |
| t_{CL} | DCLK low time | $0.45 \times 1/f_{MAX}$ | — | s |
| t_{CLK} | DCLK period | $1/f_{MAX}$ | — | s |
| f_{MAX} | DCLK frequency | — | 125 | MHz |
| t_{CD2UM} | CONF_DONE high to user mode ⁽¹⁰⁶⁾ | 175 | 437 | μ s |
| t_{CD2CU} | CONF_DONE high to CLKUSR enabled | 4 × maximum DCLK period | — | — |
| t_{CD2UMC} | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU} + (T_{init} \times CLKUSR \text{ period})$ | — | — |
| T_{init} | Number of clock cycles required for device initialization | 17,408 | — | Cycles |

Related Information**PS Configuration Timing**

Provides the PS configuration timing waveform.

Initialization**Table 1-71: Initialization Clock Source Option and the Maximum Frequency for Arria V Devices**

| Initialization Clock Source | Configuration Scheme | Maximum Frequency (MHz) | Minimum Number of Clock Cycles |
|-----------------------------|----------------------|-------------------------|--------------------------------|
| Internal Oscillator | AS, PS, and FPP | 12.5 | T_{init} |
| CLKUSR ⁽¹⁰⁷⁾ | PS and FPP | 125 | |
| | AS | 100 | |
| DCLK | PS and FPP | 125 | |

⁽¹⁰⁶⁾ The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

⁽¹⁰⁷⁾ To enable CLKUSR as the initialization clock source, turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus Prime software from the **General** panel of the **Device and Pin Options** dialog box.

Configuration Files

Table 1-72: Uncompressed .rbf Sizes for Arria V Devices

Use this table to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal file (**.hex**) or tabular text file (**.ttf**) format, have different file sizes.

For the different types of configuration file and file sizes, refer to the Quartus Prime software. However, for a specific version of the Quartus Prime software, any design targeted for the same device has the same uncompressed configuration file size.

The IOCSR raw binary file (**.rbf**) size is specifically for the Configuration via Protocol (CvP) feature.

| Variant | Member Code | Configuration .rbf Size (bits) | IOCSR .rbf Size (bits) |
|------------|-------------|--------------------------------|------------------------|
| Arria V GX | A1 | 71,015,712 | 439,960 |
| | A3 | 71,015,712 | 439,960 |
| | A5 | 101,740,800 | 446,360 |
| | A7 | 101,740,800 | 446,360 |
| | B1 | 137,785,088 | 457,368 |
| | B3 | 137,785,088 | 457,368 |
| | B5 | 185,915,808 | 463,128 |
| | B7 | 185,915,808 | 463,128 |
| Arria V GT | C3 | 71,015,712 | 439,960 |
| | C7 | 101,740,800 | 446,360 |
| | D3 | 137,785,088 | 457,368 |
| | D7 | 185,915,808 | 463,128 |
| Arria V SX | B3 | 185,903,680 | 450,968 |
| | B5 | 185,903,680 | 450,968 |
| Arria V ST | D3 | 185,903,680 | 450,968 |
| | D5 | 185,903,680 | 450,968 |

Minimum Configuration Time Estimation

Table 1-73: Minimum Configuration Time Estimation for Arria V Devices

The estimated values are based on the configuration .rbf sizes in Uncompressed .rbf Sizes for Arria V Devices table.

| Variant | Member Code | Active Serial ⁽¹⁰⁸⁾ | | | Fast Passive Parallel ⁽¹⁰⁹⁾ | | |
|------------|-------------|--------------------------------|------------|---------------------------------|--|------------|---------------------------------|
| | | Width | DCLK (MHz) | Minimum Configuration Time (ms) | Width | DCLK (MHz) | Minimum Configuration Time (ms) |
| Arria V GX | A1 | 4 | 100 | 178 | 16 | 125 | 36 |
| | A3 | 4 | 100 | 178 | 16 | 125 | 36 |
| | A5 | 4 | 100 | 255 | 16 | 125 | 51 |
| | A7 | 4 | 100 | 255 | 16 | 125 | 51 |
| | B1 | 4 | 100 | 344 | 16 | 125 | 69 |
| | B3 | 4 | 100 | 344 | 16 | 125 | 69 |
| | B5 | 4 | 100 | 465 | 16 | 125 | 93 |
| | B7 | 4 | 100 | 465 | 16 | 125 | 93 |
| Arria V GT | C3 | 4 | 100 | 178 | 16 | 125 | 36 |
| | C7 | 4 | 100 | 255 | 16 | 125 | 51 |
| | D3 | 4 | 100 | 344 | 16 | 125 | 69 |
| | D7 | 4 | 100 | 465 | 16 | 125 | 93 |
| Arria V SX | B3 | 4 | 100 | 465 | 16 | 125 | 93 |
| | B5 | 4 | 100 | 465 | 16 | 125 | 93 |
| Arria V ST | D3 | 4 | 100 | 465 | 16 | 125 | 93 |
| | D5 | 4 | 100 | 465 | 16 | 125 | 93 |

⁽¹⁰⁸⁾ DCLK frequency of 100 MHz using external CLKUSR.

⁽¹⁰⁹⁾ Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

Related Information[Configuration Files](#) on page 1-82

Remote System Upgrades

Table 1-74: Remote System Upgrade Circuitry Timing Specifications for Arria V Devices

| Parameter | Minimum | Unit |
|----------------------------|---------|------|
| $t_{RU_nCONFIG}^{(110)}$ | 250 | ns |
| $t_{RU_nRSTIMER}^{(111)}$ | 250 | ns |

Related Information

- [Remote System Upgrade State Machine](#)
Provides more information about configuration reset (RU_CONFIG) signal.
- [User Watchdog Timer](#)
Provides more information about reset_timer (RU_nRSTIMER) signal.

User Watchdog Internal Oscillator Frequency Specifications

Table 1-75: User Watchdog Internal Oscillator Frequency Specifications for Arria V Devices

| Parameter | Minimum | Typical | Maximum | Unit |
|---|---------|---------|---------|------|
| User watchdog internal oscillator frequency | 5.3 | 7.9 | 12.5 | MHz |

I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O timing and the Quartus Prime Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

⁽¹¹⁰⁾ This is equivalent to strobing the reconfiguration input of the ALTREMOTE_UPDATE IP core high for the minimum timing specification.

⁽¹¹¹⁾ This is equivalent to strobing the reset timer input of the ALTREMOTE_UPDATE IP core high for the minimum timing specification.

The Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

Related Information

[Arria V I/O Timing Spreadsheet](#)

Provides the Arria V Excel-based I/O timing spreadsheet.

Programmable IOE Delay

Table 1-76: I/O element (IOE) Programmable Delay for Arria V Devices

| Parameter ⁽¹¹²⁾) | Available Settings | Minimum Offset ⁽¹¹³⁾ | Fast Model | | Slow Model | | | | | Unit |
|---------------------------------|--------------------|---------------------------------|------------|------------|------------|-------|-------|-------|-------|------|
| | | | Industrial | Commercial | -C4 | -C5 | -C6 | -I3 | -I5 | |
| D1 | 32 | 0 | 0.508 | 0.517 | 0.870 | 1.063 | 1.063 | 0.872 | 1.057 | ns |
| D3 | 8 | 0 | 1.763 | 1.795 | 2.999 | 3.496 | 3.571 | 3.031 | 3.643 | ns |
| D4 | 32 | 0 | 0.508 | 0.518 | 0.869 | 1.063 | 1.063 | 1.063 | 1.057 | ns |
| D5 | 32 | 0 | 0.508 | 0.517 | 0.870 | 1.063 | 1.063 | 0.872 | 1.057 | ns |

⁽¹¹²⁾ You can set this value in the Quartus Prime software by selecting **D1**, **D3**, **D4**, and **D5** in the **Assignment Name** column of **Assignment Editor**.

⁽¹¹³⁾ Minimum offset does not include the intrinsic delay.

Programmable Output Buffer Delay

Table 1-77: Programmable Output Buffer Delay for Arria V Devices

This table lists the delay chain settings that control the rising and falling edge delays of the output buffer.

You can set the programmable output buffer delay in the Quartus Prime software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

| Symbol | Parameter | Typical | Unit |
|---------------------|----------------------------------|-------------|------|
| D _{OUTBUF} | Rising and/or falling edge delay | 0 (default) | ps |
| | | 50 | ps |
| | | 100 | ps |
| | | 150 | ps |

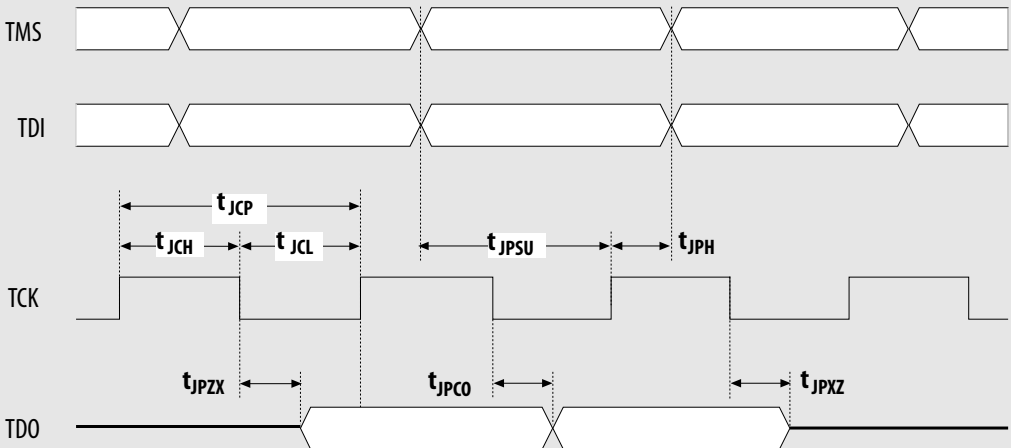
Glossary

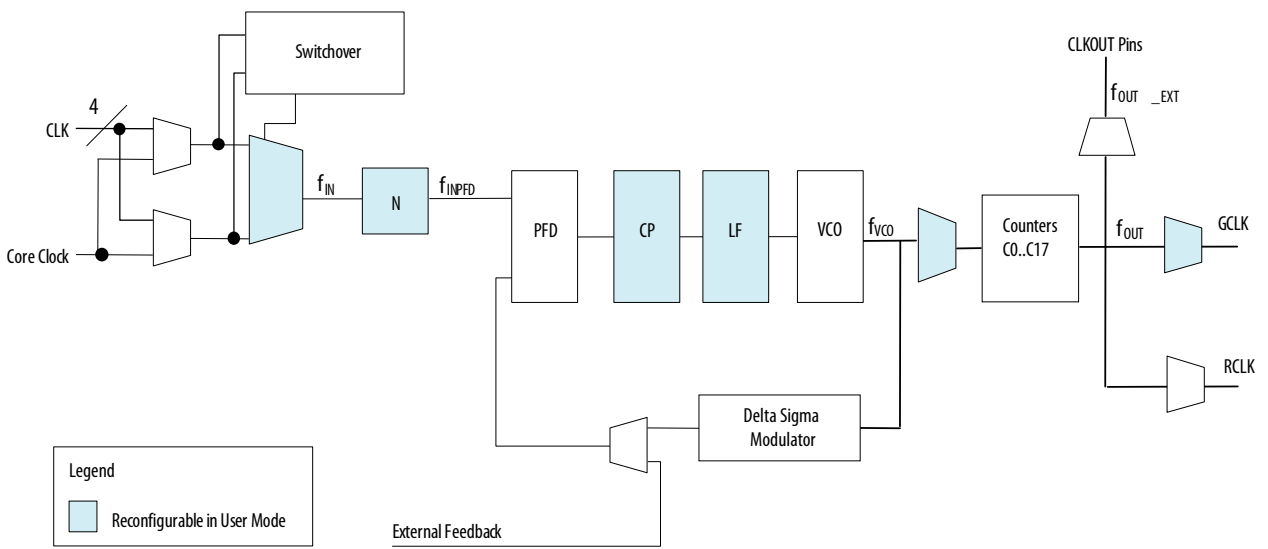
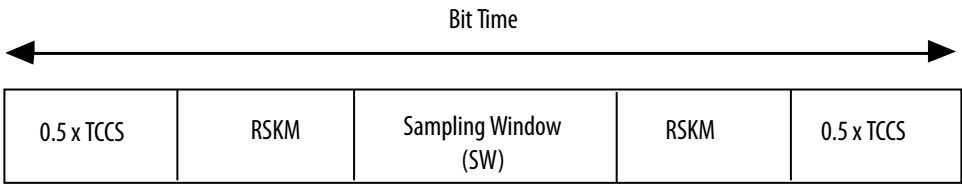
Table 1-78: Glossary

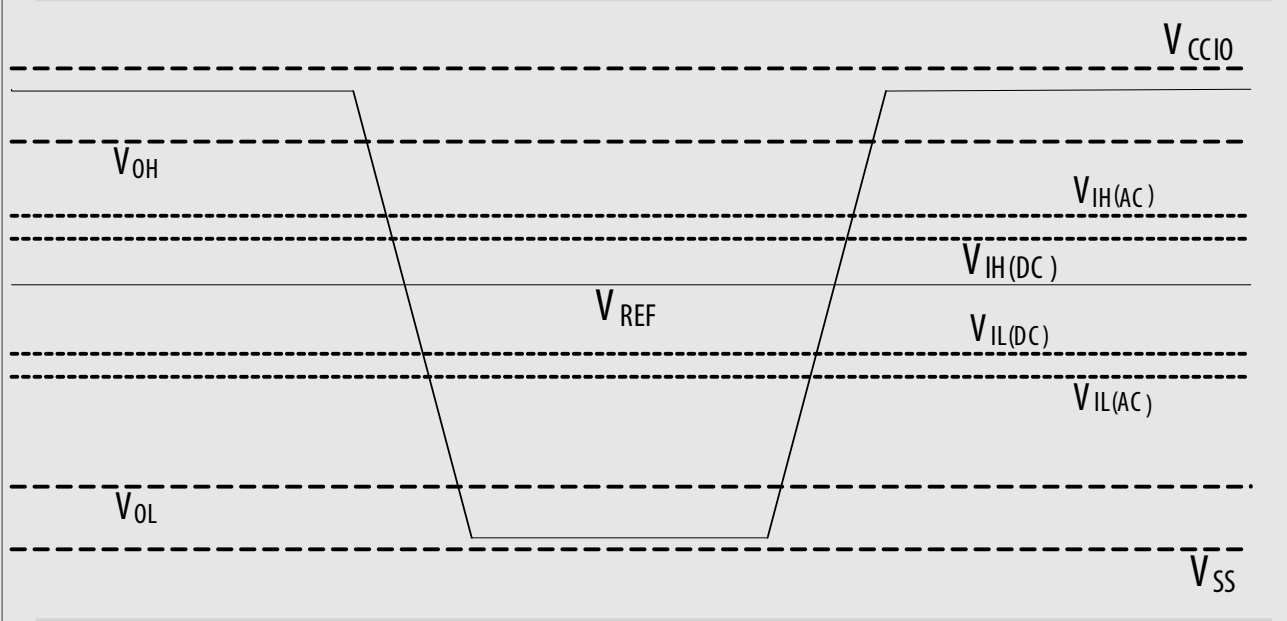
| Term | Definition |
|----------------------------|--------------------------|
| Differential I/O standards | Receiver Input Waveforms |

| Term | Definition |
|------|--|
| | <p>Single-Ended Waveform</p>  <p>Positive Channel (p) = V_{IH} Negative Channel (n) = V_{IL} Ground</p> <p>Differential Waveform</p>  <p>$p - n = 0V$</p> |
| | <p>Transmitter Output Waveforms</p> |

| Term | Definition |
|---------------|--|
| | <p>Single-Ended Waveform</p>  <p>Positive Channel (p) = V_{OH} Negative Channel (n) = V_{OL} Ground</p> <p>Differential Waveform</p>  <p>p - n = 0V V_{OD}</p> |
| f_{HSCLK} | Left/right PLL input clock frequency. |
| f_{HSDR} | High-speed I/O block—Maximum/minimum LVDS data transfer rate ($f_{HSDR} = 1/TUI$), non-DPA. |
| $f_{HSDRDPA}$ | High-speed I/O block—Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA} = 1/TUI$), DPA. |
| J | High-speed I/O block—Deserialization factor (width of parallel data bus). |

| Term | Definition |
|----------------------------|---|
| JTAG timing specifications | <p data-bbox="667 207 1003 240">JTAG Timing Specifications</p>  <p>The diagram illustrates the timing specifications for JTAG signals: TMS, TDI, TCK, and TDO. It shows the relationship between these signals during data capture and shift operations. The timing parameters are defined as follows:</p> <ul style="list-style-type: none"> t_{JCP}: Capture period t_{JCH}: Capture hold t_{JCL}: Capture latch t_{JPSU}: Program setup t_{JPH}: Program hold t_{JPZX}: Program zero t_{JPCO}: Program capture |

| Term | Definition |
|----------------------|--|
| PLL specifications | <p data-bbox="667 207 1024 240">Diagram of PLL specifications</p>  <p data-bbox="682 820 1155 868">Note: (1) Core Clock can only be fed by dedicated clock input pins or PLL outputs.</p> |
| R_L | Receiver differential input discrete resistor (external to the Arria V device). |
| Sampling window (SW) | <p data-bbox="667 990 1900 1055">Timing diagram—The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window, as shown:</p>  |

| Term | Definition |
|--|---|
| Single-ended voltage referenced I/O standard | <p>The JEDEC standard for the SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.</p> <p>The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing.</p> <p>Single-Ended Voltage Referenced I/O Standard</p>  |
| t_C | High-speed receiver/transmitter input and output clock period. |
| TCCS (channel-to-channel-skew) | The timing difference between the fastest and slowest output edges, including the t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table). |
| t_{DUTY} | High-speed I/O block—Duty cycle on high-speed transmitter output clock. |

| Term | Definition |
|----------------------------|---|
| t_{FALL} | Signal high-to-low transition time (80–20%) |
| t_{INCCJ} | Cycle-to-cycle jitter tolerance on the PLL clock input |
| $t_{\text{OUTPJ_IO}}$ | Period jitter on the GPIO driven by a PLL |
| $t_{\text{OUTPJ_DC}}$ | Period jitter on the dedicated clock output driven by a PLL |
| t_{RISE} | Signal low-to-high transition time (20–80%) |
| Timing Unit Interval (TUI) | The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = 1 / (Receiver Input Clock Frequency Multiplication Factor) = t_c/w) |
| $V_{\text{CM(DC)}}$ | DC common mode input voltage. |
| V_{ICM} | Input common mode voltage—The common mode of the differential signal at the receiver. |
| V_{ID} | Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver. |
| $V_{\text{DIF(AC)}}$ | AC differential input voltage—Minimum AC input differential voltage required for switching. |
| $V_{\text{DIF(DC)}}$ | DC differential input voltage— Minimum DC input differential voltage required for switching. |
| V_{IH} | Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high. |
| $V_{\text{IH(AC)}}$ | High-level AC input voltage |
| $V_{\text{IH(DC)}}$ | High-level DC input voltage |
| V_{IL} | Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low. |
| $V_{\text{IL(AC)}}$ | Low-level AC input voltage |
| $V_{\text{IL(DC)}}$ | Low-level DC input voltage |
| V_{OCM} | Output common mode voltage—The common mode of the differential signal at the transmitter. |
| V_{OD} | Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission line at the transmitter. |
| V_{SWING} | Differential input voltage |
| V_{X} | Input differential cross point voltage |

| Term | Definition |
|----------|---|
| V_{OX} | Output differential cross point voltage |
| W | High-speed I/O block—Clock boost factor |

Document Revision History

| Date | Version | Changes |
|-----------|------------|--|
| June 2016 | 2016.06.10 | <ul style="list-style-type: none"> Changed pin capacitance to maximum values. Updated SPI Master Timing Requirements for Arria V Devices table. <ul style="list-style-type: none"> Added T_{su} and T_h specifications. Removed T_{dinmax} specifications. Updated SPI Master Timing Diagram. Updated T_{clk} spec from maximum to minimum in I²C Timing Requirements for Arria V Devices table. |

1-94 Document Revision History

| Date | Version | Changes |
|---------------|------------|--|
| December 2015 | 2015.12.16 | <ul style="list-style-type: none"> • Updated Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Arria V Devices table. <ul style="list-style-type: none"> • Updated F_{clk}, $T_{duty\ cycle}$, and $T_{dss\ first}$ specifications. • Added T_{qspi_clk}, T_{din_start}, and T_{din_end} specifications. • Removed $T_{din\ max}$ specifications. • Updated the minimum specification for T_{clk} to 16.67 ns and removed the maximum specification in SPI Master Timing Requirements for Arria V Devices table. • Updated Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Arria V Devices table. <ul style="list-style-type: none"> • Updated T_{clk} to $T_{sdmmc_clk_out}$ symbol. • Updated $T_{sdmmc_clk_out}$ and T_d specifications. • Added T_{sdmmc_clk}, T_{su}, and T_h specifications. • Removed $T_{din\ max}$ specifications. • Updated the following diagrams: <ul style="list-style-type: none"> • Quad SPI Flash Timing Diagram • SD/MMC Timing Diagram • Updated configuration .rbf sizes for Arria V devices. • Changed instances of <i>Quartus II</i> to <i>Quartus Prime</i>. |

| Date | Version | Changes |
|-----------|------------|---|
| June 2015 | 2015.06.16 | <ul style="list-style-type: none"> • Added the supported data rates for the following output standards using true LVDS output buffer types in the High-Speed I/O Specifications for Arria V Devices table: <ul style="list-style-type: none"> • True RSDS output standard: data rates of up to 360 Mbps • True mini-LVDS output standard: data rates of up to 400 Mbps • Added note in the condition for Transmitter—Emulated Differential I/O Standards f_{HSDR} data rate parameter in the High-Speed I/O Specifications for Arria V Devices table. Note: When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported. • Changed Queued Serial Peripheral Interface (QSPI) to Quad Serial Peripheral Interface (SPI) Flash. • Updated T_h location in I²C Timing Diagram. • Updated T_{wp} location in NAND Address Latch Timing Diagram. • Corrected the unit for t_{DH} from ns to s in FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Arria V Devices table. • Updated the maximum value for t_{CO} from 4 ns to 2 ns in AS Timing Parameters for AS ×1 and ×4 Configurations in Arria V Devices table. • Moved the following timing diagrams to the Configuration, Design Security, and Remote System Upgrades in Arria V Devices chapter. <ul style="list-style-type: none"> • FPP Configuration Timing Waveform When DCLK-to-DATA[] Ratio is 1 • FPP Configuration Timing Waveform When DCLK-to-DATA[] Ratio is >1 • AS Configuration Timing Waveform • PS Configuration Timing Waveform |

| Date | Version | Changes |
|--------------|------------|---|
| January 2015 | 2015.01.30 | <ul style="list-style-type: none"> • Updated the description for $V_{CC_AUX_SHARED}$ to “HPS auxiliary power supply” in the following tables: <ul style="list-style-type: none"> • Absolute Maximum Ratings for Arria V Devices • HPS Power Supply Operating Conditions for Arria V SX and ST Devices • Added statement in I/O Standard Specifications: You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards. • Updated the conditions for transceiver reference clock rise time and fall time: Measure at ± 60 mV of differential signal. Added a note to the conditions: $REFCLK$ performance requires to meet transmitter $REFCLK$ phase noise specification. • Updated the description in Periphery Performance Specifications to mention that proper timing closure is required in design. • Updated HPS Clock Performance $main_base_clk$ specifications from 525 MHz (for -I3 speed grade) and 462 MHz (for -C4 speed grade) to 400 MHz. • Updated HPS PLL VCO maximum frequency to 1,600 MHz (for -C5, -I5, and -C6 speed grades), 1,850 MHz (for -C4 speed grade), and 2,100 MHz (for -I3 speed grade). • Changed the symbol for HPS PLL input jitter divide value from NR to N. • Removed “Slave select pulse width (Texas Instruments SSP mode)” parameter from the following tables: <ul style="list-style-type: none"> • SPI Master Timing Requirements for Arria V Devices • SPI Slave Timing Requirements for Arria V Devices • Added descriptions to USB Timing Characteristics section in HPS Specifications: PHYs that support LPM mode may not function properly with the USB controller due to a timing issue. It is recommended that designers use the MicroChip USB3300 PHY device that has been proven to be successful on the development board. • Added HPS JTAG timing specifications. • Updated FPGA JTAG timing specifications note as follows: A 1-ns adder is required for each V_{CCIO} voltage step down from 3.0 V. For example, $t_{PCO} = 13$ ns if V_{CCIO} of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V. • Updated the value in the V_{ICM} (AC Coupled) row and in note 6 from 650 mV to 750 mV in the Transceiver Specifications for Arria V GT and ST Devices table. |

| Date | Version | Changes |
|---------------|---------|---|
| July 2014 | 3.8 | <ul style="list-style-type: none"> • Added a note in Table 3, Table 4, and Table 5: The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements. • Updated V_{CC_HPS} specification in Table 5. • Added a note in Table 19: Differential inputs are powered by V_{CCPD} which requires 2.5 V. • Updated "Minimum differential eye opening at the receiver serial input pins" specification in Table 20 and Table 21. • Updated description in "HPS PLL Specifications" section. • Updated VCO range maximum specification in Table 39. • Updated T_d and T_h specifications in Table 45. • Added T_h specification in Table 47 and Figure 13. • Updated a note in Figure 20, Figure 21, and Figure 23 as follows: Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required. • Removed "Remote update only in AS mode" specification in Table 58. • Added DCLK device initialization clock source specification in Table 60. • Added description in "Configuration Files" section: The IOCSR .rbf size is specifically for the Configuration via Protocol (CvP) feature. • Removed $f_{MAX_RU_CLK}$ specification in Table 63. |
| February 2014 | 3.7 | <ul style="list-style-type: none"> • Updated $V_{CCRSTCLK_HPS}$ maximum specification in Table 1. • Added $V_{CC_AUX_SHARED}$ specification in Table 1. |
| December 2013 | 3.6 | <ul style="list-style-type: none"> • Added "HPS PLL Specifications". • Added Table 24, Table 39, and Table 40. • Updated Table 1, Table 3, Table 5, Table 19, Table 20, Table 21, Table 38, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, Table 48, Table 49, Table 50, Table 51, Table 55, Table 56, and Table 59. • Updated Figure 7, Figure 13, Figure 15, Figure 16, and Figure 19. • Removed table: GPIO Pulse Width for Arria V Devices. |

1-98 Document Revision History

| Date | Version | Changes |
|-------------|---------|---|
| August 2013 | 3.5 | <ul style="list-style-type: none"> Removed “Pending silicon characterization” note in Table 29. Updated Table 25. |
| August 2013 | 3.4 | <ul style="list-style-type: none"> Removed Preliminary tags for Table 1, Table 2, Table 3, Table 4, Table 5, Table 6, Table 7, Table 9, Table 12, Table 13, Table 14, Table 15, Table 16, Table 17, Table 18, Table 19, Table 20, Table 21, Table 22, Table 23, Table 24, Table 25, Table 26, Table 27, Table 28, Table 29, Table 30, Table 31, Table 35, Table 36, Table 51, Table 53, Table 54, Table 55, Table 56, Table 57, Table 60, Table 62, and Table 64. Updated Table 1, Table 3, Table 11, Table 19, Table 20, Table 21, Table 22, Table 25, and Table 29. |
| June 2013 | 3.3 | Updated Table 20, Table 21, Table 25, and Table 38. |
| May 2013 | 3.2 | <ul style="list-style-type: none"> Added Table 37. Updated Figure 8, Figure 9, Figure 20, Figure 22, and Figure 23. Updated Table 1, Table 5, Table 10, Table 13, Table 19, Table 20, Table 21, Table 23, Table 29, Table 39, Table 40, Table 46, Table 56, Table 57, Table 60, and Table 64. Updated industrial junction temperature range for –I3 speed grade in “PLL Specifications” section. |
| March 2013 | 3.1 | <ul style="list-style-type: none"> Added HPS reset information in the “HPS Specifications” section. Added Table 60. Updated Table 1, Table 3, Table 17, Table 20, Table 29, and Table 59. Updated Figure 21. |

| Date | Version | Changes |
|---------------|---------|--|
| November 2012 | 3.0 | <ul style="list-style-type: none"> Updated Table 2, Table 4, Table 9, Table 14, Table 16, Table 17, Table 20, Table 21, Table 25, Table 29, Table 36, Table 56, Table 57, and Table 60. Removed table: Transceiver Block Jitter Specifications for Arria V Devices. Added HPS information: <ul style="list-style-type: none"> Added “HPS Specifications” section. Added Table 38, Table 39, Table 40, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, Table 48, Table 49, and Table 50. Added Figure 7, Figure 8, Figure 9, Figure 10, Figure 11, Figure 12, Figure 13, Figure 14, Figure 15, Figure 16, Figure 17, Figure 18, and Figure 19. Updated Table 3 and Table 5. |
| October 2012 | 2.4 | <ul style="list-style-type: none"> Updated Arria V GX $V_{CCR_GXBL/R}$, $V_{CCT_GXBL/R}$, and $V_{CCL_GXBL/R}$ minimum and maximum values, and data rate in Table 4. Added receiver V_{ICM} (AC coupled) and V_{ICM} (DC coupled) values, and transmitter V_{OCM} (AC coupled) and V_{OCM} (DC coupled) values in Table 20 and Table 21. |
| August 2012 | 2.3 | Updated the SERDES factor condition in Table 30. |
| July 2012 | 2.2 | <ul style="list-style-type: none"> Updated the maximum voltage for V_I (DC input voltage) in Table 1. Updated Table 20 to include the Arria V GX -I3 speed grade. Updated the minimum value of the fixedclk clock frequency in Table 20 and Table 21. Updated the SERDES factor condition in Table 30. Updated Table 50 to include the IOE programmable delay settings for the Arria V GX -I3 speed grade. |
| June 2012 | 2.1 | Updated $V_{CCR_GXBL/R}$, $V_{CCT_GXBL/R}$, and $V_{CCL_GXBL/R}$ values in Table 4. |

1-100 Document Revision History

| Date | Version | Changes |
|---------------|---------|---|
| June 2012 | 2.0 | <ul style="list-style-type: none"> Updated for the Quartus II software v12.0 release: Restructured document. Updated “Supply Current and Power Consumption” section. Updated Table 20, Table 21, Table 24, Table 25, Table 26, Table 35, Table 39, Table 43, and Table 52. Added Table 22, Table 23, and Table 33. Added Figure 1–1 and Figure 1–2. Added “Initialization” and “Configuration Files” sections. |
| February 2012 | 1.3 | <ul style="list-style-type: none"> Updated Table 2–1. Updated Transceiver-FPGA Fabric Interface rows in Table 2–20. Updated V_{CCP} description. |
| December 2011 | 1.2 | Updated Table 2–1 and Table 2–3. |
| November 2011 | 1.1 | <ul style="list-style-type: none"> Updated Table 2–1, Table 2–19, Table 2–26, and Table 2–36. Added Table 2–5. Added Figure 2–4. |
| August 2011 | 1.0 | Initial release. |

2016.06.20

AV-51002



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This document covers the electrical and switching characteristics for Arria V GZ devices. Electrical characteristics include operating conditions and power consumption. Switching characteristics include transceiver specifications, core, and periphery performance. This document also describes I/O timing, including programmable I/O element (IOE) delay and programmable output buffer delay.

Related Information

[Arria V Device Overview](#)

For information regarding the densities and packages of devices in the Arria V GZ family.

Electrical Characteristics

Operating Conditions

When you use Arria V GZ devices, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of Arria V GZ devices, you must consider the operating requirements described in this datasheet.

Arria V GZ devices are offered in commercial and industrial temperature grades.

Commercial devices are offered in –3 (fastest) and –4 core speed grades. Industrial devices are offered in –3L and –4 core speed grades. Arria V GZ devices are offered in –2 and –3 transceiver speed grades.

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2-2 Absolute Maximum Ratings

Table 2-1: Commercial and Industrial Speed Grade Offering for Arria V GZ Devices

C = Commercial temperature grade; I = Industrial temperature grade.

Lower number refers to faster speed grade.

L = Low power devices.

| Transceiver Speed Grade | Core Speed Grade | | | |
|-------------------------|------------------|-----|-----|-----|
| | C3 | C4 | I3L | I4 |
| 2 | Yes | — | Yes | — |
| 3 | — | Yes | — | Yes |

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Arria V GZ devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

Caution: Conditions other than those listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 2-2: Absolute Maximum Ratings for Arria V GZ Devices

| Symbol | Description | Minimum | Maximum | Unit |
|---------------|--|---------|---------|------|
| V_{CC} | Power supply for core voltage and periphery circuitry | -0.5 | 1.35 | V |
| V_{CCPT} | Power supply for programmable power technology | -0.5 | 1.8 | V |
| V_{CCPGM} | Power supply for configuration pins | -0.5 | 3.9 | V |
| V_{CC_AUX} | Auxiliary supply for the programmable power technology | -0.5 | 3.4 | V |
| V_{CCBAT} | Battery back-up power supply for design security volatile key register | -0.5 | 3.9 | V |
| V_{CCPD} | I/O pre-driver power supply | -0.5 | 3.9 | V |
| V_{CCIO} | I/O power supply | -0.5 | 3.9 | V |

| Symbol | Description | Minimum | Maximum | Unit |
|-----------------------|--------------------------------|---------|---------|------|
| V _{CCD_FPLL} | PLL digital power supply | -0.5 | 1.8 | V |
| V _{CCA_FPLL} | PLL analog power supply | -0.5 | 3.4 | V |
| V _I | DC input voltage | -0.5 | 3.8 | V |
| T _J | Operating junction temperature | -55 | 125 | °C |
| T _{STG} | Storage temperature (No bias) | -65 | 150 | °C |
| I _{OUT} | DC output current per pin | -25 | 40 | mA |

Table 2-3: Transceiver Power Supply Absolute Conditions for Arria V GZ Devices

| Symbol | Description | Minimum | Maximum | Unit |
|-----------------------|---|---------|---------|------|
| V _{CCA_GXBL} | Transceiver channel PLL power supply (left side) | -0.5 | 3.75 | V |
| V _{CCA_GXBR} | Transceiver channel PLL power supply (right side) | -0.5 | 3.75 | V |
| V _{CCHIP_L} | Transceiver hard IP power supply (left side) | -0.5 | 1.35 | V |
| V _{CCHSSI_L} | Transceiver PCS power supply (left side) | -0.5 | 1.35 | V |
| V _{CCHSSI_R} | Transceiver PCS power supply (right side) | -0.5 | 1.35 | V |
| V _{CCR_GXBL} | Receiver analog power supply (left side) | -0.5 | 1.35 | V |
| V _{CCR_GXBR} | Receiver analog power supply (right side) | -0.5 | 1.35 | V |
| V _{CCT_GXBL} | Transmitter analog power supply (left side) | -0.5 | 1.35 | V |
| V _{CCT_GXBR} | Transmitter analog power supply (right side) | -0.5 | 1.35 | V |
| V _{CCH_GXBL} | Transmitter output buffer power supply (left side) | -0.5 | 1.8 | V |
| V _{CCH_GXBR} | Transmitter output buffer power supply (right side) | -0.5 | 1.8 | V |

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in the following table. They may also undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

2-4 Recommended Operating Conditions

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% of the duty cycle.

For example, a signal that overshoots to 3.95 V can be at 3.95 V for only ~21% over the lifetime of the device; for a device lifetime of 10 years, the overshoot duration amounts to ~2 years.

Table 2-4: Maximum Allowed Overshoot During Transitions for Arria V GZ Devices

| Symbol | Description | Condition (V) | Overshoot Duration as % @ $T_J = 100^\circ\text{C}$ | Unit |
|---------|------------------|---------------|---|------|
| Vi (AC) | AC input voltage | 3.8 | 100 | % |
| | | 3.85 | 64 | % |
| | | 3.9 | 36 | % |
| | | 3.95 | 21 | % |
| | | 4 | 12 | % |
| | | 4.05 | 7 | % |
| | | 4.1 | 4 | % |
| | | 4.15 | 2 | % |
| | | 4.2 | 1 | % |

Recommended Operating Conditions**Table 2-5: Recommended Operating Conditions for Arria V GZ Devices**

Power supply ramps must all be strictly monotonic, without plateaus.

| Symbol | Description | Condition | Minimum ⁽¹¹⁴⁾ | Typical | Maximum ⁽¹¹⁴⁾ | Unit |
|-----------------|--|-----------|--------------------------|---------|--------------------------|------|
| V _{CC} | Core voltage and periphery circuitry power supply ⁽¹¹⁵⁾ | — | 0.82 | 0.85 | 0.88 | V |

⁽¹¹⁴⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽¹¹⁵⁾ The V_{CC} core supply must be set to 0.9 V if the Partial Reconfiguration (PR) feature is used.

| Symbol | Description | Condition | Minimum ⁽¹¹⁴⁾ | Typical | Maximum ⁽¹¹⁴⁾ | Unit |
|-------------------------------------|--|-----------|--------------------------|---------|--------------------------|------|
| V _{CCPT} | Power supply for programmable power technology | — | 1.45 | 1.50 | 1.55 | V |
| V _{CC_AUX} | Auxiliary supply for the programmable power technology | — | 2.375 | 2.5 | 2.625 | V |
| V _{CCPD} ⁽¹¹⁶⁾ | I/O pre-driver (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | I/O pre-driver (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| V _{CCIO} | I/O buffers (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | I/O buffers (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| | I/O buffers (1.8 V) power supply | — | 1.71 | 1.8 | 1.89 | V |
| | I/O buffers (1.5 V) power supply | — | 1.425 | 1.5 | 1.575 | V |
| | I/O buffers (1.35 V) power supply | — | 1.283 | 1.35 | 1.45 | V |
| | I/O buffers (1.25 V) power supply | — | 1.19 | 1.25 | 1.31 | V |
| | I/O buffers (1.2 V) power supply | — | 1.14 | 1.2 | 1.26 | V |
| V _{CCPGM} | Configuration pins (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | Configuration pins (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| | Configuration pins (1.8 V) power supply | — | 1.71 | 1.8 | 1.89 | V |
| V _{CCA_FPLL} | PLL analog voltage regulator power supply | — | 2.375 | 2.5 | 2.625 | V |
| V _{CCD_FPLL} | PLL digital voltage regulator power supply | — | 1.45 | 1.5 | 1.55 | V |
| V _{CCBAT} ⁽¹¹⁷⁾ | Battery back-up power supply (For design security volatile key register) | — | 1.2 | — | 3.0 | V |

⁽¹¹⁴⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽¹¹⁶⁾ V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V.

⁽¹¹⁷⁾ If you do not use the design security feature in Arria V GZ devices, connect V_{CCBAT} to a 1.2- to 3.0-V power supply. Arria V GZ power-on-reset (POR) circuitry monitors V_{CCBAT}. Arria V GZ devices do not exit POR if V_{CCBAT} is not powered up.

2-6 Recommended Transceiver Power Supply Operating Conditions

| Symbol | Description | Condition | Minimum ⁽¹¹⁴⁾ | Typical | Maximum ⁽¹¹⁴⁾ | Unit |
|-------------------|--------------------------------|--------------|--------------------------|---------|--------------------------|------|
| V _I | DC input voltage | — | -0.5 | — | 3.6 | V |
| V _O | Output voltage | — | 0 | — | V _{CCIO} | V |
| T _J | Operating junction temperature | Commercial | 0 | — | 85 | °C |
| | | Industrial | -40 | — | 100 | °C |
| t _{RAMP} | Power supply ramp time | Standard POR | 200 μs | — | 100 ms | — |
| | | Fast POR | 200 μs | — | 4 ms | — |

Recommended Transceiver Power Supply Operating Conditions

Table 2-6: Recommended Transceiver Power Supply Operating Conditions for Arria V GZ Devices

| Symbol | Description | Minimum ⁽¹¹⁸⁾ | Typical | Maximum ⁽¹¹⁸⁾ | Unit |
|---------------------------------------|---|--------------------------|---------|--------------------------|------|
| V _{CCA_GXBL} (119), (120) | Transceiver channel PLL power supply (left side) | 2.85 | 3.0 | 3.15 | V |
| | | 2.375 | 2.5 | 2.625 | |
| V _{CCA_GXBR} (119), (120) | Transceiver channel PLL power supply (right side) | 2.85 | 3.0 | 3.15 | V |
| | | 2.375 | 2.5 | 2.625 | |
| V _{CCHIP_L} | Transceiver hard IP power supply (left side) | 0.82 | 0.85 | 0.88 | V |
| V _{CCHSSL_L} | Transceiver PCS power supply (left side) | 0.82 | 0.85 | 0.88 | V |
| V _{CCHSSL_R} | Transceiver PCS power supply (right side) | 0.82 | 0.85 | 0.88 | V |

⁽¹¹⁴⁾ The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽¹¹⁸⁾ This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽¹¹⁹⁾ This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.

⁽¹²⁰⁾ When using ATX PLLs, the supply must be 3.0 V.

| Symbol | Description | Minimum ⁽¹¹⁸⁾ | Typical | Maximum ⁽¹¹⁸⁾ | Unit |
|--|---|--------------------------|---------|--------------------------|------|
| V _{CCR_GXBL} ⁽¹²¹⁾ | Receiver analog power supply (left side) | 0.82 | 0.85 | 0.88 | V |
| | | 0.97 | 1.0 | 1.03 | |
| | | 1.03 | 1.05 | 1.07 | |
| V _{CCR_GXBR} ⁽¹²¹⁾ | Receiver analog power supply (right side) | 0.82 | 0.85 | 0.88 | V |
| | | 0.97 | 1.0 | 1.03 | |
| | | 1.03 | 1.05 | 1.07 | |
| V _{CCT_GXBL} ⁽¹²¹⁾ | Transmitter analog power supply (left side) | 0.82 | 0.85 | 0.88 | V |
| | | 0.97 | 1.0 | 1.03 | |
| | | 1.03 | 1.05 | 1.07 | |
| V _{CCT_GXBR} ⁽¹²¹⁾ | Transmitter analog power supply (right side) | 0.82 | 0.85 | 0.88 | V |
| | | 0.97 | 1.0 | 1.03 | |
| | | 1.03 | 1.05 | 1.07 | |
| V _{CCH_GXBL} | Transmitter output buffer power supply (left side) | 1.425 | 1.5 | 1.575 | V |
| V _{CCH_GXBR} | Transmitter output buffer power supply (right side) | 1.425 | 1.5 | 1.575 | V |

⁽¹¹⁸⁾ This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

⁽¹²¹⁾ This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps, and to 1.05 V if configured at a data rate > 10.3 Gbps when DFE is used. For data rate up to 6.5 Gbps, you can connect this supply to 0.85 V.

Transceiver Power Supply Requirements

Table 2-7: Transceiver Power Supply Voltage Requirements for Arria V GZ Devices

| Conditions | VCCR_GXB and VCCT_GXB ⁽¹²²⁾ | VCCA_GXB | VCCH_GXB | Unit |
|--|--|----------|----------|------|
| If BOTH of the following conditions are true: <ul style="list-style-type: none"> Data rate > 10.3 Gbps. DFE is used. | 1.05 | | | V |
| If ANY of the following conditions are true ⁽¹²³⁾ : <ul style="list-style-type: none"> ATX PLL is used. Data rate > 6.5Gbps. DFE (data rate ≤ 10.3 Gbps), AEQ, or EyeQ feature is used. | 1.0 | 3.0 | 1.5 | |
| If ALL of the following conditions are true: <ul style="list-style-type: none"> ATX PLL is not used. Data rate ≤ 6.5Gbps. DFE, AEQ, and EyeQ are not used. | 0.85 | 2.5 | | |

DC Characteristics

Supply Current

Standby current is the current drawn from the respective power rails used for power budgeting.

Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.

⁽¹²²⁾ If the VCCR_GXB and VCCT_GXB supplies are set to 1.0 V or 1.05 V, they cannot be shared with the VCC core supply. If the VCCR_GXB and VCCT_GXB are set to 0.85 V, they can be shared with the VCC core supply.

⁽¹²³⁾ Choose this power supply voltage requirement option if you plan to upgrade your design later with any of the listed conditions.

Related Information

- [PowerPlay Early Power Estimator User Guide](#)
For more information about the EPE tool.
- [PowerPlay Power Analysis](#)
For more information about PowerPlay power analysis.

Power Consumption

Altera offers two ways to estimate power consumption for a design—the Excel-based Early Power Estimator and the Quartus II PowerPlay Power Analyzer feature.

Note: You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

Related Information

- [PowerPlay Early Power Estimator User Guide](#)
For more information about the EPE tool.
- [PowerPlay Power Analysis](#)
For more information about PowerPlay power analysis.

I/O Pin Leakage Current**Table 2-8: I/O Pin Leakage Current for Arria V GZ Devices**

If $V_O = V_{CCIO}$ to $V_{CCIO_{MAX}}$, 100 μA of leakage current per I/O is expected.

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|----------|--------------------|---------------------------------|-----|-----|-----|---------|
| I_I | Input pin | $V_I = 0 V$ to $V_{CCIO_{MAX}}$ | -30 | — | 30 | μA |
| I_{OZ} | Tri-stated I/O pin | $V_O = 0 V$ to $V_{CCIO_{MAX}}$ | -30 | — | 30 | μA |

Bus Hold Specifications

Table 2-9: Bus Hold Parameters for Arria V GZ Devices

| Parameter | Symbol | Conditions | V_{CCIO} | | | | | | | | | | Unit |
|-------------------------|------------|--------------------------------|------------|------|-------|------|-------|------|-------|------|-------|------|---------|
| | | | 1.2 V | | 1.5 V | | 1.8 V | | 2.5 V | | 3.0 V | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Low sustaining current | I_{SUSL} | $V_{IN} > V_{IL}$ (maximum) | 22.5 | — | 25.0 | — | 30.0 | — | 50.0 | — | 70.0 | — | μA |
| High sustaining current | I_{SUSH} | $V_{IN} < V_{IH}$ (minimum) | -22.5 | — | -25.0 | — | -30.0 | — | -50.0 | — | -70.0 | — | μA |
| Low overdrive current | I_{ODL} | $0V < V_{IN} < V_{CCIO}$ | — | 120 | — | 160 | — | 200 | — | 300 | — | 500 | μA |
| High overdrive current | I_{ODH} | $0V < V_{IN} < V_{CCIO}$ | — | -120 | — | -160 | — | -200 | — | -300 | — | -500 | μA |
| Bus-hold trip point | V_{TRIP} | — | 0.45 | 0.95 | 0.50 | 1.00 | 0.68 | 1.07 | 0.70 | 1.70 | 0.80 | 2.00 | V |

On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block.

Table 2-10: OCT Calibration Accuracy Specifications for Arria V GZ Devices

OCT calibration accuracy is valid at the time of calibration only.

| Symbol | Description | Conditions | Calibration Accuracy | | Unit |
|---|--|--|----------------------|------------|------|
| | | | C3, I3L | C4, I4 | |
| 25- Ω R_S | Internal series termination with calibration (25- Ω setting) | $V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2$ V | ± 15 | ± 15 | % |
| 50- Ω R_S | Internal series termination with calibration (50- Ω setting) | $V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2$ V | ± 15 | ± 15 | % |
| 34- Ω and 40- Ω R_S | Internal series termination with calibration (34- Ω and 40- Ω setting) | $V_{CCIO} = 1.5, 1.35, 1.25, 1.2$ V | ± 15 | ± 15 | % |
| 48- Ω , 60- Ω , 80- Ω , and 240- Ω R_S | Internal series termination with calibration (48- Ω , 60- Ω , 80- Ω , and 240- Ω setting) | $V_{CCIO} = 1.2$ V | ± 15 | ± 15 | % |
| 50- Ω R_T | Internal parallel termination with calibration (50- Ω setting) | $V_{CCIO} = 2.5, 1.8, 1.5, 1.2$ V | -10 to +40 | -10 to +40 | % |
| 20- Ω , 30- Ω , 40- Ω , 60- Ω , and 120- Ω R_T | Internal parallel termination with calibration (20- Ω , 30- Ω , 40- Ω , 60- Ω , and 120- Ω setting) | $V_{CCIO} = 1.5, 1.35, 1.25$ V | -10 to +40 | -10 to +40 | % |
| 60- Ω and 120- Ω R_T | Internal parallel termination with calibration (60- Ω and 120- Ω setting) | $V_{CCIO} = 1.2$ | -10 to +40 | -10 to +40 | % |
| 25- Ω $R_{S_left_shift}$ | Internal left shift series termination with calibration (25- Ω $R_{S_left_shift}$ setting) | $V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2$ V | ± 15 | ± 15 | % |

Table 2-11: OCT Without Calibration Resistance Tolerance Specifications for Arria V GZ Devices

| Symbol | Description | Conditions | Resistance Tolerance | | Unit |
|-----------------------------|--|-----------------------------------|----------------------|--------|------|
| | | | C3, I3L | C4, I4 | |
| 25-Ω R, 50-Ω R _S | Internal series termination without calibration (25-Ω setting) | V _{CCIO} = 3.0 and 2.5 V | ±40 | ±40 | % |
| 25-Ω R _S | Internal series termination without calibration (25-Ω setting) | V _{CCIO} = 1.8 and 1.5 V | ±40 | ±40 | % |
| 25-Ω R _S | Internal series termination without calibration (25-Ω setting) | V _{CCIO} = 1.2 V | ±50 | ±50 | % |
| 50-Ω R _S | Internal series termination without calibration (50-Ω setting) | V _{CCIO} = 1.8 and 1.5 V | ±40 | ±40 | % |
| 50-Ω R _S | Internal series termination without calibration (50-Ω setting) | V _{CCIO} = 1.2 V | ±50 | ±50 | % |
| 100-Ω R _D | Internal differential termination (100-Ω setting) | V _{CCIO} = 2.5 V | ±25 | ±25 | % |

Figure 2-1: OCT Variation Without Re-Calibration for Arria V GZ Devices

$$R_{\text{OCT}} = R_{\text{SCAL}} \left(1 + \left(\frac{dR}{dT} \times \Delta T \right) \pm \left(\frac{dR}{dV} \times \Delta V \right) \right)$$

Notes:

1. The R_{OCT} value shows the range of OCT resistance with the variation of temperature and V_{CCIO}.
2. R_{SCAL} is the OCT resistance value at power-up.
3. ΔT is the variation of temperature with respect to the temperature at power-up.
4. ΔV is the variation of voltage with respect to the V_{CCIO} at power-up.
5. dR/dT is the percentage change of R_{SCAL} with temperature.
6. dR/dV is the percentage change of R_{SCAL} with voltage.

Table 2-12: OCT Variation after Power-Up Calibration for Arria V GZ DevicesValid for a V_{CCIO} range of $\pm 5\%$ and a temperature range of 0° to 85°C .

| Symbol | Description | V_{CCIO} (V) | Typical | Unit |
|--------|---|----------------|---------|---------------------|
| dR/dV | OCT variation with voltage without re-calibration | 3.0 | 0.0297 | %mV |
| | | 2.5 | 0.0344 | |
| | | 1.8 | 0.0499 | |
| | | 1.5 | 0.0744 | |
| | | 1.2 | 0.1241 | |
| dR/dT | OCT variation with temperature without re-calibration | 3.0 | 0.189 | %/ $^\circ\text{C}$ |
| | | 2.5 | 0.208 | |
| | | 1.8 | 0.266 | |
| | | 1.5 | 0.273 | |
| | | 1.2 | 0.317 | |

Pin Capacitance**Table 2-13: Pin Capacitance for Arria V GZ Devices**

| Symbol | Description | Maximum | Unit |
|-------------|--|---------|------|
| C_{IOTB} | Input capacitance on the top and bottom I/O pins | 6 | pF |
| C_{IOLR} | Input capacitance on the left and right I/O pins | 6 | pF |
| C_{OUTFB} | Input capacitance on dual-purpose clock output and feedback pins | 6 | pF |

Hot Socketing

Table 2-14: Hot Socketing Specifications for Arria V GZ Devices

| Symbol | Description | Maximum |
|--------------------|--|-----------------------|
| $I_{IOPIN (DC)}$ | DC current per I/O pin | 300 μ A |
| $I_{IOPIN (AC)}$ | AC current per I/O pin | 8 mA ⁽¹²⁴⁾ |
| $I_{XCVR-TX (DC)}$ | DC current per transceiver transmitter pin | 100 mA |
| $I_{XCVR-RX (DC)}$ | DC current per transceiver receiver pin | 50 mA |

Internal Weak Pull-Up Resistor

Table 2-15: Internal Weak Pull-Up Resistor for Arria V GZ Devices

All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins. The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 k Ω .

| Symbol | Description | V_{CCIO} Conditions (V) ⁽¹²⁵⁾ | Value ⁽¹²⁶⁾ | Unit |
|----------|---|--|------------------------|------------|
| R_{PU} | Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option. | 3.0 \pm 5% | 25 | k Ω |
| | | 2.5 \pm 5% | 25 | k Ω |
| | | 1.8 \pm 5% | 25 | k Ω |
| | | 1.5 \pm 5% | 25 | k Ω |
| | | 1.35 \pm 5% | 25 | k Ω |
| | | 1.25 \pm 5% | 25 | k Ω |
| | | 1.2 \pm 5% | 25 | k Ω |

⁽¹²⁴⁾ The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.

⁽¹²⁵⁾ The pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO} .

⁽¹²⁶⁾ These specifications are valid with a \pm 10% tolerance to cover changes over PVT.

I/O Standard Specifications

The V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL} , respectively.

Table 2-16: Single-Ended I/O Standards for Arria V GZ Devices

| I/O Standard | V_{CCIO} (V) | | | V_{IL} (V) | | V_{IH} (V) | | V_{OL} (V) | V_{OH} (V) | I_{OL} (mA) | I_{OH} (mA) |
|--------------|----------------|-----|-------|--------------|------------------------|------------------------|------------------|------------------------|------------------------|---------------|---------------|
| | Min | Typ | Max | Min | Max | Min | Max | Max | Min | | |
| LVTTL | 2.85 | 3 | 3.15 | -0.3 | 0.8 | 1.7 | 3.6 | 0.4 | 2.4 | 2 | -2 |
| LVC MOS | 2.85 | 3 | 3.15 | -0.3 | 0.8 | 1.7 | 3.6 | 0.2 | $V_{CCIO} - 0.2$ | 0.1 | -0.1 |
| 2.5 V | 2.375 | 2.5 | 2.625 | -0.3 | 0.7 | 1.7 | 3.6 | 0.4 | 2 | 1 | -1 |
| 1.8 V | 1.71 | 1.8 | 1.89 | -0.3 | $0.35 \times V_{CCIO}$ | $0.65 \times V_{CCIO}$ | $V_{CCIO} + 0.3$ | 0.45 | $V_{CCIO} - 0.45$ | 2 | -2 |
| 1.5 V | 1.425 | 1.5 | 1.575 | -0.3 | $0.35 \times V_{CCIO}$ | $0.65 \times V_{CCIO}$ | $V_{CCIO} + 0.3$ | $0.25 \times V_{CCIO}$ | $0.75 \times V_{CCIO}$ | 2 | -2 |
| 1.2 V | 1.14 | 1.2 | 1.26 | -0.3 | $0.35 \times V_{CCIO}$ | $0.65 \times V_{CCIO}$ | $V_{CCIO} + 0.3$ | $0.25 \times V_{CCIO}$ | $0.75 \times V_{CCIO}$ | 2 | -2 |

Table 2-17: Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Arria V GZ Devices

| I/O Standard | V_{CCIO} (V) | | | V_{REF} (V) | | | V_{TT} (V) | | |
|------------------------|----------------|-----|-------|------------------------|-----------------------|------------------------|------------------------|-----------------------|------------------------|
| | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | $0.49 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.51 \times V_{CCIO}$ | $V_{REF} - 0.04$ | V_{REF} | $V_{REF} + 0.04$ |
| SSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 | $V_{REF} - 0.04$ | V_{REF} | $V_{REF} + 0.04$ |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | $0.49 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.51 \times V_{CCIO}$ | $0.49 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.51 \times V_{CCIO}$ |

| I/O Standard | V_{CCIO} (V) | | | V_{REF} (V) | | | V_{TT} (V) | | |
|-------------------------|----------------|------|-------|------------------------|-----------------------|------------------------|------------------------|-----------------------|------------------------|
| | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |
| SSTL-135 Class I, II | 1.283 | 1.35 | 1.418 | $0.49 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.51 \times V_{CCIO}$ | $0.49 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.51 \times V_{CCIO}$ |
| SSTL-125 Class I, II | 1.19 | 1.25 | 1.26 | $0.49 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.51 \times V_{CCIO}$ | $0.49 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.51 \times V_{CCIO}$ |
| SSTL-12 Class I, II | 1.14 | 1.20 | 1.26 | $0.49 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.51 \times V_{CCIO}$ | $0.49 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.51 \times V_{CCIO}$ |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.85 | 0.9 | 0.95 | — | $V_{CCIO}/2$ | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.68 | 0.75 | 0.9 | — | $V_{CCIO}/2$ | — |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | $0.47 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.53 \times V_{CCIO}$ | — | $V_{CCIO}/2$ | — |
| HSUL-12 | 1.14 | 1.2 | 1.3 | $0.49 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | $0.51 \times V_{CCIO}$ | — | — | — |

Table 2-18: Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Arria V GZ Devices

| I/O Standard | $V_{IL(DC)}$ (V) | | $V_{IH(DC)}$ (V) | | $V_{IL(AC)}$ (V) | $V_{IH(AC)}$ (V) | V_{OL} (V) | V_{OH} (V) | I_{ol} (mA) | I_{oh} (mA) |
|-----------------|------------------|-------------------|-------------------|------------------|------------------|------------------|------------------|------------------|---------------|---------------|
| | Min | Max | Min | Max | Max | Min | Max | Min | | |
| SSTL-2 Class I | -0.3 | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | $V_{CCIO} + 0.3$ | $V_{REF} - 0.31$ | $V_{REF} + 0.31$ | $V_{TT} - 0.608$ | $V_{TT} + 0.608$ | 8.1 | -8.1 |
| SSTL-2 Class II | -0.3 | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | $V_{CCIO} + 0.3$ | $V_{REF} - 0.31$ | $V_{REF} + 0.31$ | $V_{TT} - 0.81$ | $V_{TT} + 0.81$ | 16.2 | -16.2 |
| SSTL-18 Class I | -0.3 | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | $V_{CCIO} + 0.3$ | $V_{REF} - 0.25$ | $V_{REF} + 0.25$ | $V_{TT} - 0.603$ | $V_{TT} + 0.603$ | 6.7 | -6.7 |

| I/O Standard | $V_{IL(DC)} (V)$ | | $V_{IH(DC)} (V)$ | | $V_{IL(AC)} (V)$ | $V_{IH(AC)} (V)$ | $V_{OL} (V)$ | $V_{OH} (V)$ | $I_{ol} (mA)$ | $I_{oh} (mA)$ |
|-------------------------|------------------|-------------------|-------------------|-------------------|-------------------|-------------------|------------------------|------------------------|---------------|---------------|
| | Min | Max | Min | Max | Max | Min | Max | Min | | |
| SSTL-18 Class II | -0.3 | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | $V_{CCIO} + 0.3$ | $V_{REF} - 0.25$ | $V_{REF} + 0.25$ | 0.28 | $V_{CCIO} - 0.28$ | 13.4 | -13.4 |
| SSTL-15 Class I | — | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | — | $V_{REF} - 0.175$ | $V_{REF} + 0.175$ | $0.2 \times V_{CCIO}$ | $0.8 \times V_{CCIO}$ | 8 | -8 |
| SSTL-15 Class II | — | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | — | $V_{REF} - 0.175$ | $V_{REF} + 0.175$ | $0.2 \times V_{CCIO}$ | $0.8 \times V_{CCIO}$ | 16 | -16 |
| SSTL-135 Class I, II | — | $V_{REF} - 0.09$ | $V_{REF} + 0.09$ | — | $V_{REF} - 0.16$ | $V_{REF} + 0.16$ | $0.2 * V_{CCIO}$ | $0.8 * V_{CCIO}$ | — | — |
| SSTL-125 Class I, II | — | $V_{REF} - 0.85$ | $V_{REF} + 0.85$ | — | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | $0.2 * V_{CCIO}$ | $0.8 * V_{CCIO}$ | — | — |
| SSTL-12 Class I, II | — | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | — | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | $0.2 * V_{CCIO}$ | $0.8 * V_{CCIO}$ | — | — |
| HSTL-18 Class I | — | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | — | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | 0.4 | $V_{CCIO} - 0.4$ | 8 | -8 |
| HSTL-18 Class II | — | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | — | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | 0.4 | $V_{CCIO} - 0.4$ | 16 | -16 |
| HSTL-15 Class I | — | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | — | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | 0.4 | $V_{CCIO} - 0.4$ | 8 | -8 |
| HSTL-15 Class II | — | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | — | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | 0.4 | $V_{CCIO} - 0.4$ | 16 | -16 |
| HSTL-12 Class I | -0.15 | $V_{REF} - 0.08$ | $V_{REF} + 0.08$ | $V_{CCIO} + 0.15$ | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | $0.25 \times V_{CCIO}$ | $0.75 \times V_{CCIO}$ | 8 | -8 |
| HSTL-12 Class II | -0.15 | $V_{REF} - 0.08$ | $V_{REF} + 0.08$ | $V_{CCIO} + 0.15$ | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | $0.25 \times V_{CCIO}$ | $0.75 \times V_{CCIO}$ | 16 | -16 |
| HSUL-12 | — | $V_{REF} - 0.13$ | $V_{REF} + 0.13$ | — | $V_{REF} - 0.22$ | $V_{REF} + 0.22$ | $0.1 \times V_{CCIO}$ | $0.9 \times V_{CCIO}$ | — | — |

Table 2-19: Differential SSTL I/O Standards for Arria V GZ Devices

| I/O Standard | V _{CCIO} (V) | | | V _{SWING(DC)} (V) | | V _{X(AC)} (V) | | | V _{SWING(AC)} (V) | |
|----------------------|-----------------------|------|-------|----------------------------|-------------------------|------------------------------|----------------------|------------------------------|--|--|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 0.3 | V _{CCIO} + 0.6 | V _{CCIO} /2 - 0.2 | — | V _{CCIO} /2 + 0.2 | 0.62 | V _{CCIO} + 0.6 |
| SSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.25 | V _{CCIO} + 0.6 | V _{CCIO} /2 - 0.175 | — | V _{CCIO} /2 + 0.175 | 0.5 | V _{CCIO} + 0.6 |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | ⁽¹²⁷⁾ | V _{CCIO} /2 - 0.15 | — | V _{CCIO} /2 + 0.15 | 0.35 | — |
| SSTL-135 Class I, II | 1.283 | 1.35 | 1.45 | 0.2 | ⁽¹²⁷⁾ | V _{CCIO} /2 - 0.15 | V _{CCIO} /2 | V _{CCIO} /2 + 0.15 | 2(V _{IH(AC)} - V _{REF}) | 2(V _{IL(AC)} - V _{REF}) |
| SSTL-125 Class I, II | 1.19 | 1.25 | 1.31 | 0.18 | ⁽¹²⁷⁾ | V _{CCIO} /2 - 0.15 | V _{CCIO} /2 | V _{CCIO} /2 + 0.15 | 2(V _{IH(AC)} - V _{REF}) | — |
| SSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.18 | — | V _{REF} - 0.15 | V _{CCIO} /2 | V _{REF} + 0.15 | -0.30 | 0.30 |

Table 2-20: Differential HSTL and HSUL I/O Standards for Arria V GZ Devices

| I/O Standard | V _{CCIO} (V) | | | V _{DIF(DC)} (V) | | V _{X(AC)} (V) | | | V _{CM(DC)} (V) | | | V _{DIF(AC)} (V) | |
|---------------------|-----------------------|-----|-------|--------------------------|-----|------------------------|-----|------|-------------------------|-----|------|--------------------------|-----|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Typ | Max | Min | Max |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.2 | — | 0.78 | — | 1.12 | 0.78 | — | 1.12 | 0.4 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | — | 0.68 | — | 0.9 | 0.68 | — | 0.9 | 0.4 | — |

⁽¹²⁷⁾ The maximum value for V_{SWING(DC)} is not defined. However, each single-ended signal needs to be within the respective single-ended limits (V_{IH(DC)} and V_{IL(DC)}).

| I/O Standard | V _{CCIO} (V) | | | V _{DIF(DC)} (V) | | V _{X(AC)} (V) | | | V _{CM(DC)} (V) | | | V _{DIF(AC)} (V) | |
|---------------------|-----------------------|-----|------|--------------------------|-------------------------|--------------------------------|-------------------------|--------------------------------|-------------------------|-------------------------|-------------------------|--------------------------|--------------------------|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Typ | Max | Min | Max |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.16 | V _{CCIO} + 0.3 | — | 0.5 × V _{CCIO} | — | 0.4 × V _{CCIO} | 0.5 × V _{CCIO} | 0.6 × V _{CCIO} | 0.3 | V _{CCIO} + 0.48 |
| HSUL-12 | 1.14 | 1.2 | 1.3 | 0.26 | 0.26 | 0.5 × V _{CCIO} - 0.12 | 0.5 × V _{CCIO} | 0.5 × V _{CCIO} + 0.12 | 0.4 × V _{CCIO} | 0.5 × V _{CCIO} | 0.6 × V _{CCIO} | 0.44 | 0.44 |

Table 2-21: Differential I/O Standard Specifications for Arria V GZ Devices

| I/O Standard | V _{CCIO} (V) ⁽¹²⁸⁾ | | | V _{ID} (mV) ⁽¹²⁹⁾ | | | V _{ICM(DC)} (V) | | | V _{OD} (V) ⁽¹³⁰⁾ | | | V _{OCM} (V) ⁽¹³⁰⁾ | | |
|-----------------------------|---|-----|-------|---------------------------------------|--------------------------|-----|--------------------------|-----------------------------|------|--------------------------------------|-----|-----|---------------------------------------|------|-------|
| | Min | Typ | Max | Min | Condition | Max | Min | Condition | Max | Min | Typ | Max | Min | Typ | Max |
| PCML | Transmitter, receiver, and input reference clock pins of the high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to the "Transceiver Performance Specifications" section. | | | | | | | | | | | | | | |
| 2.5 V LVDS ⁽¹³¹⁾ | 2.375 | 2.5 | 2.625 | 100 | V _{CM} = 1.25 V | — | 0.05 | D _{MAX} ≤ 700 Mbps | 1.8 | 0.247 | — | 0.6 | 1.125 | 1.25 | 1.375 |
| | | | | | | — | 1.05 | D _{MAX} > 700 Mbps | 1.55 | 0.247 | — | 0.6 | 1.125 | 1.25 | 1.375 |
| BLVDS ⁽¹³²⁾ | 2.375 | 2.5 | 2.625 | 100 | — | — | — | — | — | — | — | — | — | — | — |

⁽¹²⁸⁾ Differential inputs are powered by VCCPD which requires 2.5 V.⁽¹²⁹⁾ The minimum VID value is applicable over the entire common mode range, VCM.⁽¹³⁰⁾ RL range: 90 ≤ RL ≤ 110 Ω.⁽¹³¹⁾ For optimized LVDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.6 V for data rates above 700 Mbps, and 0 V to 1.85 V for data rates below 700 Mbps.⁽¹³²⁾ There are no fixed V_{ICM}, V_{OD}, and V_{OCM} specifications for BLVDS. They depend on the system topology.

| I/O Standard | V_{CCIO} (V) ⁽¹²⁸⁾ | | | V_{ID} (mV) ⁽¹²⁹⁾ | | | $V_{ICM(DC)}$ (V) | | | V_{OD} (V) ⁽¹³⁰⁾ | | | V_{OCM} (V) ⁽¹³⁰⁾ | | |
|---|---------------------------------|-----|-------|--------------------------------|-------------------|-----|-------------------|-------------------------|-------|-------------------------------|-----|-----|--------------------------------|-----|-----|
| | Min | Typ | Max | Min | Condition | Max | Min | Condition | Max | Min | Typ | Max | Min | Typ | Max |
| RSDS (HIO) ⁽¹³³⁾ | 2.375 | 2.5 | 2.625 | 100 | $V_{CM} = 1.25$ V | — | 0.3 | — | 1.4 | 0.1 | 0.2 | 0.6 | 0.5 | 1.2 | 1.4 |
| Mini-LVDS (HIO) ⁽¹³⁴⁾ | 2.375 | 2.5 | 2.625 | 200 | — | 600 | 0.4 | — | 1.325 | 0.25 | — | 0.6 | 1 | 1.2 | 1.4 |
| LVPECL ⁽¹³⁵⁾ , ⁽¹³⁶⁾ | — | — | — | 300 | — | — | 0.6 | $D_{MAX} \leq 700$ Mbps | 1.8 | — | — | — | — | — | — |
| | — | — | — | 300 | — | — | 1 | $D_{MAX} > 700$ Mbps | 1.6 | — | — | — | — | — | — |

Related Information[Glossary](#) on page 2-75⁽¹²⁸⁾ Differential inputs are powered by VCCPD which requires 2.5 V.⁽¹²⁹⁾ The minimum VID value is applicable over the entire common mode range, VCM.⁽¹³⁰⁾ RL range: $90 \leq RL \leq 110 \Omega$.⁽¹³³⁾ For optimized RSDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.45 V.⁽¹³⁴⁾ For optimized Mini-LVDS receiver performance, the receiver voltage input range must be between 0.3 V to 1.425 V.⁽¹³⁵⁾ LVPECL is only supported on dedicated clock input pins.⁽¹³⁶⁾ For optimized LVPECL receiver performance, the receiver voltage input range must be between 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.

Switching Characteristics

Transceiver Performance Specifications

Reference Clock

Table 2-22: Reference Clock Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

| Symbol/Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|--|--|---|-----|-----|---------------------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Reference Clock | | | | | | | | |
| Supported I/O Standards | Dedicated reference clock pin | 1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL | | | | | | |
| | RX reference clock pin | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS | | | | | | |
| Input Reference Clock Frequency (CMU PLL) ⁽¹³⁷⁾ | — | 40 | — | 710 | 40 | — | 710 | MHz |
| Input Reference Clock Frequency (ATX PLL) ⁽¹³⁷⁾ | — | 100 | — | 710 | 100 | — | 710 | MHz |
| Rise time | Measure at ± 60 mV of differential signal ⁽¹³⁸⁾ | — | — | 400 | — | — | 400 | ps |
| Fall time | Measure at ± 60 mV of differential signal ⁽¹³⁸⁾ | — | — | 400 | — | — | 400 | |

⁽¹³⁷⁾ The input reference clock frequency options depend on the data rate and the device speed grade.

⁽¹³⁸⁾ REFCLK performance requires to meet transmitter REFCLK phase noise specification.

2-22 Reference Clock

| Symbol/Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|--|--|-------------------------------|--------------|------|-------------------------------|--------------|------|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Duty cycle | — | 45 | — | 55 | 45 | — | 55 | % |
| Spread-spectrum modulating clock frequency | PCI Express® (PCIe) | 30 | — | 33 | 30 | — | 33 | kHz |
| Spread-spectrum downspread | PCIe | — | 0 to -0.5 | — | — | 0 to -0.5 | — | % |
| On-chip termination resistors | — | — | 100 | — | — | 100 | — | Ω |
| Absolute V_{MAX} | Dedicated reference clock pin | — | — | 1.6 | — | — | 1.6 | V |
| | RX reference clock pin | — | — | 1.2 | — | — | 1.2 | |
| Absolute V_{MIN} | — | -0.4 | — | — | -0.4 | — | — | V |
| Peak-to-peak differential input voltage | — | 200 | — | 1600 | 200 | — | 1600 | mV |
| V_{ICM} (AC coupled) | Dedicated reference clock pin | 1000/900/850 ⁽¹³⁹⁾ | | | 1000/900/850 ⁽¹³⁹⁾ | | | mV |
| | RX reference clock pin | 1.0/0.9/0.85 ⁽¹⁴⁰⁾ | | | 1.0/0.9/0.85 ⁽¹⁴⁰⁾ | | | mV |
| V_{ICM} (DC coupled) | HCSL I/O standard for PCIe reference clock | 250 | — | 550 | 250 | — | 550 | mV |

⁽¹³⁹⁾ The reference clock common mode voltage is equal to the V_{CCR_GXB} power supply level.⁽¹⁴⁰⁾ This supply follows V_{CCR_GXB}

| Symbol/Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|--|--------------------------|---------------------------|----------|------|---------------------------|----------|------|----------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Transmitter REFCLK Phase Noise (622 MHz) ⁽¹⁴¹⁾ | 100 Hz | — | — | -70 | — | — | -70 | dBc/Hz |
| | 1 kHz | — | — | -90 | — | — | -90 | dBc/Hz |
| | 10 kHz | — | — | -100 | — | — | -100 | dBc/Hz |
| | 100 kHz | — | — | -110 | — | — | -110 | dBc/Hz |
| | ≥1 MHz | — | — | -120 | — | — | -120 | dBc/Hz |
| Transmitter REFCLK Phase Jitter (100 MHz) ⁽¹⁴²⁾ | 10 kHz to 1.5 MHz (PCIe) | — | — | 3 | — | — | 3 | ps (rms) |
| R _{REF} | — | — | 1800 ±1% | — | — | 1800 ±1% | — | Ω |

Related Information[Arria V Device Overview](#)

For more information about device ordering codes.

⁽¹⁴¹⁾ To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).

⁽¹⁴²⁾ To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.

Transceiver Clocks

Table 2-23: Transceiver Clocks Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

| Symbol/Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|--|----------------------|---------------------------|------------|-----|---------------------------|------------|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| fixedclk clock frequency | PCIe Receiver Detect | — | 100 or 125 | — | — | 100 or 125 | — | MHz |
| Reconfiguration clock (mgmt_clk_clk) frequency | — | 100 | — | 125 | 100 | — | 125 | MHz |

Related Information

[Arria V Device Overview](#)

For more information about device ordering codes.

Receiver

Table 2-24: Receiver Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

| Symbol/Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|--|--|---------------------------|-----|------|---------------------------|-----|------|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Supported I/O Standards | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS | | | | | | | |
| Data rate (Standard PCS) ⁽¹⁴³⁾ , ⁽¹⁴⁴⁾ | — | 600 | — | 9900 | 600 | — | 8800 | Mbps |

⁽¹⁴³⁾ The line data rate may be limited by PCS-FPGA interface speed grade.

⁽¹⁴⁴⁾ To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

| Symbol/Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|--|---------------------------|----------------|-------|---------------------------|----------------|---------|----------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Data rate (10G PCS) ⁽¹⁴³⁾ , ⁽¹⁴⁴⁾ | — | 600 | — | 12500 | 600 | — | 10312.5 | Mbps |
| Absolute V_{MAX} for a receiver pin ⁽¹⁴⁵⁾ | — | — | — | 1.2 | — | — | 1.2 | V |
| Absolute V_{MIN} for a receiver pin | — | -0.4 | — | — | -0.4 | — | — | V |
| Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration | — | — | — | 1.6 | — | — | 1.6 | V |
| Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration ⁽¹⁴⁶⁾ | $V_{CCR_GXB} = 1.0\text{ V}$ ($V_{ICM} = 0.75\text{ V}$) | — | — | 1.8 | — | — | 1.8 | V |
| | $V_{CCR_GXB} = 0.85\text{ V}$ ($V_{ICM} = 0.6\text{ V}$) | — | — | 2.4 | — | — | 2.4 | V |
| Minimum differential eye opening at receiver serial input pins ⁽¹⁴⁷⁾⁽¹⁴⁸⁾ | — | 85 | — | — | 85 | — | — | mV |
| Differential on-chip termination resistors | 85- Ω setting | — | $85 \pm 30\%$ | — | — | $85 \pm 30\%$ | — | Ω |
| | 100- Ω setting | — | $100 \pm 30\%$ | — | — | $100 \pm 30\%$ | — | Ω |
| | 120- Ω setting | — | $120 \pm 30\%$ | — | — | $120 \pm 30\%$ | — | Ω |
| | 150- Ω setting | — | $150 \pm 30\%$ | — | — | $150 \pm 30\%$ | — | Ω |

⁽¹⁴⁵⁾ The device cannot tolerate prolonged operation at this absolute maximum.

⁽¹⁴⁶⁾ The maximum peak to peak differential input voltage V_{ID} after device configuration is equal to $4 \times (\text{absolute } V_{MAX} \text{ for receiver pin} - V_{ICM})$.

⁽¹⁴⁷⁾ The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

⁽¹⁴⁸⁾ Minimum eye opening of 85 mV is only for the unstressed input eye condition.

| Symbol/Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|--|---|---------------------------|-----|-----|---------------------------|-----|-----|---------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| V_{ICM} (AC and DC coupled) | $V_{CCR_GXB} = 0.85\text{ V}$ full bandwidth | — | 600 | — | — | 600 | — | mV |
| | $V_{CCR_GXB} = 0.85\text{ V}$ half bandwidth | — | 600 | — | — | 600 | — | mV |
| | $V_{CCR_GXB} = 1.0\text{ V}$ full bandwidth | — | 700 | — | — | 700 | — | mV |
| | $V_{CCR_GXB} = 1.0\text{ V}$ half bandwidth | — | 700 | — | — | 700 | — | mV |
| $t_{LTR}^{(149)}$ | — | — | — | 10 | — | — | 10 | μs |
| $t_{LTD}^{(150)}$ | — | 4 | — | — | 4 | — | — | μs |
| $t_{LTD_manual}^{(151)}$ | — | 4 | — | — | 4 | — | — | μs |
| $t_{LTR_LTD_manual}^{(152)}$ | — | 15 | — | — | 15 | — | — | μs |
| Programmable equalization (AC Gain) | Full bandwidth (6.25 GHz) Half bandwidth (3.125 GHz) | — | — | 16 | — | — | 16 | dB |

⁽¹⁴⁹⁾ t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

⁽¹⁵⁰⁾ t_{LTD} is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtoata` signal goes high.

⁽¹⁵¹⁾ t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtoata` signal goes high when the CDR is functioning in the manual mode.

⁽¹⁵²⁾ $t_{LTR_LTD_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedtoata` signal goes high when the CDR is functioning in the manual mode.

| Symbol/Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|----------------------|---------------------|---------------------------|-----|-----|---------------------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Programmable DC gain | DC gain setting = 0 | — | 0 | — | — | 0 | — | dB |
| | DC gain setting = 1 | — | 2 | — | — | 2 | — | dB |
| | DC gain setting = 2 | — | 4 | — | — | 4 | — | dB |
| | DC gain setting = 3 | — | 6 | — | — | 6 | — | dB |
| | DC gain setting = 4 | — | 8 | — | — | 8 | — | dB |

Related Information[Arria V Device Overview](#)

For more information about device ordering codes.

Transmitter**Table 2-25: Transmitter Specifications for Arria V GZ Devices**

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

| Symbol/Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|--------------------------|----------------------|---------------------------|-----|-------|---------------------------|-----|---------|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Supported I/O Standards | 1.4-V and 1.5-V PCML | | | | | | | |
| Data rate (Standard PCS) | — | 600 | — | 9900 | 600 | — | 8800 | Mbps |
| Data rate (10G PCS) | — | 600 | — | 12500 | 600 | — | 10312.5 | Mbps |

| Symbol/Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|--|---------------------------|---------------|-----|---------------------------|---------------|-----|----------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Differential on-chip termination resistors | 85- Ω setting | — | 85 \pm 20% | — | — | 85 \pm 20% | — | Ω |
| | 100- Ω setting | — | 100 \pm 20% | — | — | 100 \pm 20% | — | Ω |
| | 120- Ω setting | — | 120 \pm 20% | — | — | 120 \pm 20% | — | Ω |
| | 150- Ω setting | — | 150 \pm 20% | — | — | 150 \pm 20% | — | Ω |
| V_{OCM} (AC coupled) | 0.65-V setting | — | 650 | — | — | 650 | — | mV |
| V_{OCM} (DC coupled) | — | — | 650 | — | — | 650 | — | mV |
| Intra-differential pair skew | Tx V_{CM} = 0.5 V and slew rate of 15 ps | — | — | 15 | — | — | 15 | ps |
| Intra-transceiver block transmitter channel-to-channel skew | x6 PMA bonded mode | — | — | 120 | — | — | 120 | ps |
| Inter-transceiver block transmitter channel-to-channel skew | xN PMA bonded mode | — | — | 500 | — | — | 500 | ps |

Related Information[Arria V Device Overview](#)

For more information about device ordering codes.

CMU PLL

Table 2-26: CMU PLL Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

| Symbol/Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|--|------------|---------------------------|-----|-------|---------------------------|-----|---------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Supported data range | — | 600 | — | 12500 | 600 | — | 10312.5 | Mbps |
| $t_{\text{pll_powerdown}}$ ⁽¹⁵³⁾ | — | 1 | — | — | 1 | — | — | μs |
| $t_{\text{pll_lock}}$ ⁽¹⁵⁴⁾ | — | — | — | 10 | — | — | 10 | μs |

Related Information

[Arria V Device Overview](#)

For more information about device ordering codes.

⁽¹⁵³⁾ $t_{\text{pll_powerdown}}$ is the PLL powerdown minimum pulse width.

⁽¹⁵⁴⁾ $t_{\text{pll_lock}}$ is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.

ATX PLL

Table 2-27: ATX PLL Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

| Symbol/Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|--|---------------------------|---------------------------|-----|-------|---------------------------|-----|---------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Supported data rate range | VCO post-divider L = 2 | 8000 | — | 12500 | 8000 | — | 10312.5 | Mbps |
| | L = 4 | 4000 | — | 6600 | 4000 | — | 6600 | Mbps |
| | L = 8 ⁽¹⁵⁵⁾ | 2000 | — | 3300 | 2000 | — | 3300 | Mbps |
| $t_{\text{pll_powerdown}}$ ⁽¹⁵⁶⁾ | — | 1 | — | — | 1 | — | — | μs |
| $t_{\text{pll_lock}}$ ⁽¹⁵⁷⁾ | — | — | — | 10 | — | — | 10 | μs |

Related Information

- [Arria V Device Overview](#)
For more information about device ordering codes.
- [Transceiver Clocking in Arria V Devices](#)
For more information about clocking ATX PLLs.
- [Dynamic Reconfiguration in Arria V Devices](#)
For more information about reconfiguring ATX PLLs.

⁽¹⁵⁵⁾ This clock can be further divided by central or local clock dividers making it possible to use ATX PLL for data rates < 1 Gbps. For more information about ATX PLLs, refer to the Transceiver Clocking in Arria V Devices chapter and the Dynamic Reconfiguration in Arria V Devices chapter.

⁽¹⁵⁶⁾ $t_{\text{pll_powerdown}}$ is the PLL powerdown minimum pulse width.

⁽¹⁵⁷⁾ $t_{\text{pll_lock}}$ is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.

Fractional PLL

Table 2-28: Fractional PLL Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

| Symbol/Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|--|------------|---------------------------|-----|--------------------------------|---------------------------|-----|--------------------------------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Supported data range | — | 600 | — | 3250/ 3125 ⁽¹⁵⁸⁾ | 600 | — | 3250/ 3125 ⁽¹⁵⁸⁾ | Mbps |
| $t_{\text{pll_powerdown}}$ ⁽¹⁵⁹⁾ | — | 1 | — | — | 1 | — | — | μs |
| $t_{\text{pll_lock}}$ ⁽¹⁶⁰⁾ | — | — | — | 10 | — | — | 10 | μs |

Related Information

[Arria V Device Overview](#)

For more information about device ordering codes.

⁽¹⁵⁸⁾ When you use fPLL as a TXPLL of the transceiver.

⁽¹⁵⁹⁾ $t_{\text{pll_powerdown}}$ is the PLL powerdown minimum pulse width.

⁽¹⁶⁰⁾ $t_{\text{pll_lock}}$ is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.

Clock Network Data Rate

Table 2-29: Clock Network Maximum Data Rate Transmitter Specifications

Valid data rates below the maximum specified in this table depend on the reference clock frequency and the PLL counter settings. Check the MegaWizard message during the PHY IP instantiation.

| Clock Network | ATX PLL | | | CMU PLL ⁽¹⁶¹⁾ | | | fPLL | | |
|----------------------------------|------------------------|--------------------|---------------------------------------|--------------------------|--------------------|---------------------------------------|------------------------|--------------------|---------------------------------------|
| | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span |
| x1 ⁽¹⁶²⁾ | 12.5 | — | 6 | 12.5 | — | 6 | 3.125 | — | 3 |
| x6 ⁽¹⁶²⁾ | — | 12.5 | 6 | — | 12.5 | 6 | — | 3.125 | 6 |
| x6 PLL Feedback ⁽¹⁶³⁾ | — | 12.5 | Side-wide | — | 12.5 | Side-wide | — | — | — |
| xN (PCIe) | — | 8.0 | 8 | — | 5.0 | 8 | — | — | — |
| xN (Native PHY IP) | 8.0 | 8.0 | Up to 13 channels above and below PLL | 7.99 | 7.99 | Up to 13 channels above and below PLL | 3.125 | 3.125 | Up to 13 channels above and below PLL |
| | — | 8.01 to 9.8304 | Up to 7 channels above and below PLL | | | | | | |

⁽¹⁶¹⁾ ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.

⁽¹⁶²⁾ Channel span is within a transceiver bank.

⁽¹⁶³⁾ Side-wide channel bonding is allowed up to the maximum supported by the PHY IP.

Standard PCS Data Rate

Table 2-30: Standard PCS Approximate Maximum Date Rate (Gbps) for Arria V GZ Devices

The maximum data rate is also constrained by the transceiver speed grade. Refer to the “Commercial and Industrial Speed Grade Offering for Arria V GZ Devices” table for the transceiver speed grade.

| Mode ⁽¹⁶⁴⁾ | Transceiver Speed Grade | PMA Width | 20 | 20 | 16 | 16 | 10 | 10 | 8 | 8 |
|-----------------------|-------------------------|--------------------------|-----|-----|------|------|-----|-----|------|------|
| | | PCS/Core Width | 40 | 20 | 32 | 16 | 20 | 10 | 16 | 8 |
| FIFO | 2 | C3, I3L core speed grade | 9.9 | 9 | 7.84 | 7.2 | 5.3 | 4.7 | 4.24 | 3.76 |
| | 3 | C4, I4 core speed grade | 8.8 | 8.2 | 7.2 | 6.56 | 4.8 | 4.3 | 3.84 | 3.44 |
| Register | 2 | C3, I3L core speed grade | 9.9 | 9 | 7.92 | 7.2 | 4.9 | 4.5 | 3.92 | 3.6 |
| | 3 | C4, I4 core speed grade | 8.8 | 8.2 | 7.04 | 6.56 | 4.4 | 4.1 | 3.52 | 3.28 |

Related Information

[Operating Conditions](#) on page 2-1

⁽¹⁶⁴⁾ The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

10G PCS Data Rate**Table 2-31: 10G PCS Approximate Maximum Data Rate (Gbps) for Arria V GZ Devices**

| Mode ⁽¹⁶⁵⁾ | Transceiver Speed Grade | PMA Width | 64 | 40 | 40 | 40 | 32 | 32 |
|-----------------------|-------------------------|--------------------------|---------|---------|-------|---------|----------|-------|
| | | PCS Width | 64 | 66/67 | 50 | 40 | 64/66/67 | 32 |
| FIFO | 2 | C3, I3L core speed grade | 12.5 | 12.5 | 10.69 | 12.5 | 10.88 | 10.88 |
| | 3 | C4, I4 core speed grade | 10.3125 | 10.3125 | 10.69 | 10.3125 | 9.92 | 9.92 |
| Register | 2 | C3, I3L core speed grade | 12.5 | 12.5 | 10.69 | 12.5 | 10.88 | 10.88 |
| | 3 | C4, I4 core speed grade | 10.3125 | 10.3125 | 10.69 | 10.3125 | 9.92 | 9.92 |

⁽¹⁶⁵⁾ The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

Typical VOD Settings

Table 2-32: Typical V_{OD} Setting for Arria V GZ Channel, TX Termination = 100 Ω

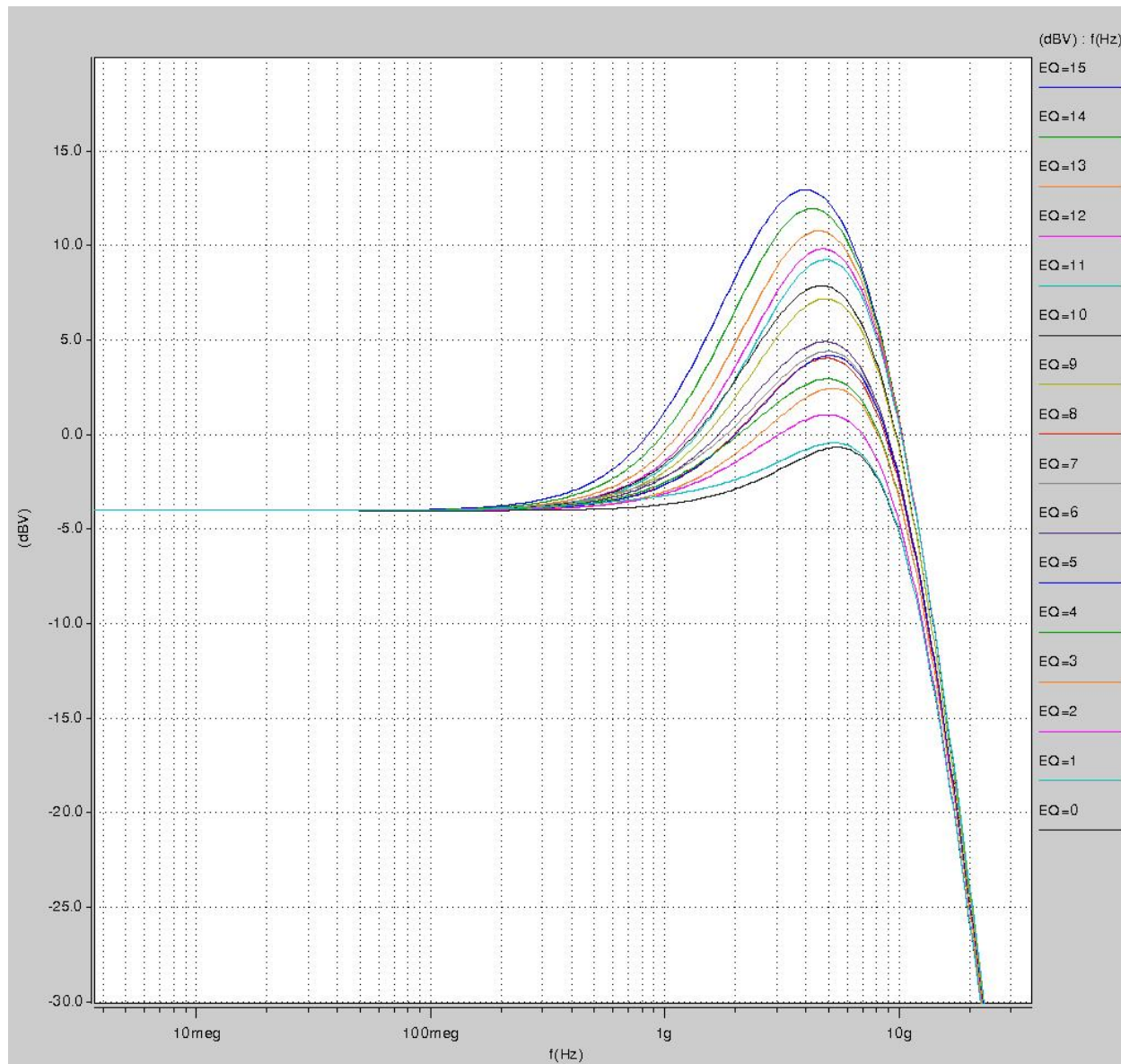
The tolerance is +/-20% for all VOD settings except for settings 2 and below.

| Symbol | V _{OD} Setting | V _{OD} Value (mV) | V _{OD} Setting | V _{OD} Value (mV) |
|---|-------------------------|----------------------------|-------------------------|----------------------------|
| V _{OD} differential peak to peak typical | 0 ⁽¹⁶⁶⁾ | 0 | 32 | 640 |
| | 1 ⁽¹⁶⁶⁾ | 20 | 33 | 660 |
| | 2 ⁽¹⁶⁶⁾ | 40 | 34 | 680 |
| | 3 ⁽¹⁶⁶⁾ | 60 | 35 | 700 |
| | 4 ⁽¹⁶⁶⁾ | 80 | 36 | 720 |
| | 5 ⁽¹⁶⁶⁾ | 100 | 37 | 740 |
| | 6 | 120 | 38 | 760 |
| | 7 | 140 | 39 | 780 |
| | 8 | 160 | 40 | 800 |
| | 9 | 180 | 41 | 820 |
| | 10 | 200 | 42 | 840 |
| | 11 | 220 | 43 | 860 |
| | 12 | 240 | 44 | 880 |
| | 13 | 260 | 45 | 900 |
| | 14 | 280 | 46 | 920 |

⁽¹⁶⁶⁾ If TX termination resistance = 100 Ω, this VOD setting is illegal.

| Symbol | V _{OD} Setting | V _{OD} Value (mV) | V _{OD} Setting | V _{OD} Value (mV) |
|---|-------------------------|----------------------------|-------------------------|----------------------------|
| V_{OD} differential peak to peak typical | 15 | 300 | 47 | 940 |
| | 16 | 320 | 48 | 960 |
| | 17 | 340 | 49 | 980 |
| | 18 | 360 | 50 | 1000 |
| | 19 | 380 | 51 | 1020 |
| | 20 | 400 | 52 | 1040 |
| | 21 | 420 | 53 | 1060 |
| | 22 | 440 | 54 | 1080 |
| | 23 | 460 | 55 | 1100 |
| | 24 | 480 | 56 | 1120 |
| | 25 | 500 | 57 | 1140 |
| | 26 | 520 | 58 | 1160 |
| | 27 | 540 | 59 | 1180 |
| | 28 | 560 | 60 | 1200 |
| | 29 | 580 | 61 | 1220 |
| | 30 | 600 | 62 | 1240 |
| | 31 | 620 | 63 | 1260 |

Figure 2-2: AC Gain Curves for Arria V GZ Channels (full bandwidth)



Core Performance Specifications

Clock Tree Specifications

Table 2-33: Clock Tree Performance for Arria V GZ Devices

| Symbol | Performance | | Unit |
|---------------------------|-------------|--------|------|
| | C3, I3L | C4, I4 | |
| Global and Regional Clock | 650 | 580 | MHz |
| Periphery Clock | 500 | 500 | MHz |

PLL Specifications

Table 2-34: PLL Specifications for Arria V GZ Devices

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------------|---|-----|-----|------|------|
| $f_{IN}^{(167)}$ | Input clock frequency (C3, I3L speed grade) | 5 | — | 800 | MHz |
| | Input clock frequency (C4, I4 speed grade) | 5 | — | 650 | MHz |
| f_{INPFD} | Input frequency to the PFD | 5 | — | 325 | MHz |
| f_{FINPFD} | Fractional Input clock frequency to the PFD | 50 | — | 160 | MHz |
| $f_{VCO}^{(168)}$ | PLL VCO operating range (C3, I3L speed grade) | 600 | — | 1600 | MHz |
| | PLL VCO operating range (C4, I4 speed grade) | 600 | — | 1300 | MHz |
| $t_{EINDUTY}$ | Input clock or external feedback clock input duty cycle | 40 | — | 60 | % |

⁽¹⁶⁷⁾ This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

⁽¹⁶⁸⁾ The VCO frequency reported by the Quartus II software in the **PLL Usage Summary** section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.

| Symbol | Parameter | Min | Typ | Max | Unit |
|------------------------|--|-----|-----|-----|------|
| $f_{OUT}^{(169)}$ | Output frequency for an internal global or regional clock (C3, I3L speed grade) | — | — | 650 | MHz |
| | Output frequency for an internal global or regional clock (C4, I4 speed grade) | — | — | 580 | MHz |
| $f_{OUT_EXT}^{(169)}$ | Output frequency for an external clock output (C3, I3L speed grade) | — | — | 667 | MHz |
| | Output frequency for an external clock output (C4, I4 speed grade) | — | — | 533 | MHz |
| $t_{OUTDUTY}$ | Duty cycle for a dedicated external clock output (when set to 50%) | 45 | 50 | 55 | % |
| t_{FCOMP} | External feedback clock compensation time | — | — | 10 | ns |
| $f_{DYCONFIGCLK}$ | Dynamic configuration clock for <code>mgmt_clk</code> and <code>scanclk</code> | — | — | 100 | MHz |
| t_{LOCK} | Time required to lock from the end-of-device configuration or deassertion of <code>areset</code> | — | — | 1 | ms |
| t_{DLOCK} | Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) | — | — | 1 | ms |
| f_{CLBW} | PLL closed-loop low bandwidth | — | 0.3 | — | MHz |
| | PLL closed-loop medium bandwidth | — | 1.5 | — | MHz |
| | PLL closed-loop high bandwidth ⁽¹⁷⁰⁾ | — | 4 | — | MHz |
| t_{PLL_PSERR} | Accuracy of PLL phase shift | — | — | ±50 | ps |
| t_{ARESET} | Minimum pulse width on the <code>areset</code> signal | 10 | — | — | ns |

⁽¹⁶⁹⁾ This specification is limited by the lower of the two: I/O f_{MAX} or f_{OUT} of the PLL.

⁽¹⁷⁰⁾ High bandwidth PLL settings are not supported in external feedback mode.

2-40 PLL Specifications

| Symbol | Parameter | Min | Typ | Max | Unit |
|-----------------------------------|---|------|-----|--|-----------|
| $t_{\text{INCCJ}}^{(171), (172)}$ | Input clock cycle-to-cycle jitter ($f_{\text{REF}} \geq 100$ MHz) | — | — | 0.15 | UI (p-p) |
| | Input clock cycle-to-cycle jitter ($f_{\text{REF}} < 100$ MHz) | -750 | — | +750 | ps (p-p) |
| $t_{\text{OUTPJ_DC}}^{(173)}$ | Period Jitter for dedicated clock output in integer PLL ($f_{\text{OUT}} \geq 100$ MHz) | — | — | 175 | ps (p-p) |
| | Period Jitter for dedicated clock output in integer PLL ($f_{\text{OUT}} < 100$ MHz) | — | — | 17.5 | mUI (p-p) |
| $t_{\text{FOUTPJ_DC}}^{(173)}$ | Period Jitter for dedicated clock output in fractional PLL ($f_{\text{OUT}} \geq 100$ MHz) | — | — | 250 ⁽¹⁷⁶⁾ , 175 ⁽¹⁷⁴⁾ | ps (p-p) |
| | Period Jitter for dedicated clock output in fractional PLL ($f_{\text{OUT}} < 100$ MHz) | — | — | 25 ⁽¹⁷⁶⁾ , 17.5 ⁽¹⁷⁴⁾ | mUI (p-p) |
| $t_{\text{OUTCCJ_DC}}^{(173)}$ | Cycle-to-cycle Jitter for a dedicated clock output in integer PLL ($f_{\text{OUT}} \geq 100$ MHz) | — | — | 175 | ps (p-p) |
| | Cycle-to-cycle Jitter for a dedicated clock output in integer PLL ($f_{\text{OUT}} < 100$ MHz) | — | — | 17.5 | mUI (p-p) |
| $t_{\text{FOUTCCJ_DC}}^{(173)}$ | Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{\text{OUT}} \geq 100$ MHz) | — | — | 250 ⁽¹⁷⁶⁾ , 175 ⁽¹⁷⁴⁾ | ps (p-p) |
| | Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{\text{OUT}} < 100$ MHz) | — | — | 25 ⁽¹⁷⁶⁾ , 17.5 ⁽¹⁷⁴⁾ | mUI (p-p) |

⁽¹⁷¹⁾ A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

⁽¹⁷²⁾ The f_{REF} is f_{IN}/N specification applies when $N = 1$.

⁽¹⁷³⁾ Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in the "Worst-Case DCD on Arria V GZ I/O Pins" table.

⁽¹⁷⁴⁾ This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.20–0.80 must be ≥ 1200 MHz.

| Symbol | Parameter | Min | Typ | Max | Unit |
|--|--|-----|-----|------|-----------|
| $t_{\text{OUTPJ_IO}}^{(173), (175)}$ | Period Jitter for a clock output on a regular I/O in integer PLL ($f_{\text{OUT}} \geq 100$ MHz) | — | — | 600 | ps (p-p) |
| | Period Jitter for a clock output on a regular I/O in integer PLL ($f_{\text{OUT}} < 100$ MHz) | — | — | 60 | mUI (p-p) |
| $t_{\text{FOUTPJ_IO}}^{(173), (175), (176)}$ | Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} \geq 100$ MHz) | — | — | 600 | ps (p-p) |
| | Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} < 100$ MHz) | — | — | 60 | mUI (p-p) |
| $t_{\text{OUTCCJ_IO}}^{(173), (175)}$ | Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{\text{OUT}} \geq 100$ MHz) | — | — | 600 | ps (p-p) |
| | Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{\text{OUT}} < 100$ MHz) | — | — | 60 | mUI (p-p) |
| $t_{\text{FOUTCCJ_IO}}^{(173), (175), (176)}$ | Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} \geq 100$ MHz) | — | — | 600 | ps (p-p) |
| | Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} < 100$ MHz) | — | — | 60 | mUI (p-p) |
| $t_{\text{CASC_OUTPJ_DC}}^{(173), (177)}$ | Period Jitter for a dedicated clock output in cascaded PLLs ($f_{\text{OUT}} \geq 100$ MHz) | — | — | 175 | ps (p-p) |
| | Period Jitter for a dedicated clock output in cascaded PLLs ($f_{\text{OUT}} < 100$ MHz) | — | — | 17.5 | mUI (p-p) |
| dK_{BIT} | Bit number of Delta Sigma Modulator (DSM) | 8 | 24 | 32 | Bits |

⁽¹⁷⁵⁾ The external memory interface clock output jitter specifications use a different measurement method, which is available in the "Memory Output Clock Jitter Specification for Arria V GZ Devices" table.

⁽¹⁷⁶⁾ This specification only covered fractional PLL for low bandwidth. The f_{VCO} for fractional value range 0.05–0.95 must be ≥ 1000 MHz.

⁽¹⁷⁷⁾ The cascaded PLL specification is only applicable with the following condition:

- Upstream PLL: $0.59\text{MHz} \leq \text{Upstream PLL BW} < 1$ MHz
- Downstream PLL: $\text{Downstream PLL BW} > 2$ MHz

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------------------|--|--------|---------|------------|------|
| k_{VALUE} | Numerator of Fraction | 128 | 8388608 | 2147483648 | — |
| f_{RES} | Resolution of VCO frequency ($f_{\text{INPFD}} = 100 \text{ MHz}$) | 390625 | 5.96 | 0.023 | Hz |

Related Information

- [Duty Cycle Distortion \(DCD\) Specifications](#) on page 2-56
- [DLL Range Specifications](#) on page 2-54

DSP Block Specifications**Table 2-35: DSP Block Performance Specifications for Arria V GZ Devices**

| Mode | Performance | | | Unit |
|--|-------------|-----|-----|------|
| | C3, I3L | C4 | I4 | |
| Modes using One DSP Block | | | | |
| Three 9×9 | 480 | 420 | | MHz |
| One 18×18 | 480 | 420 | 400 | MHz |
| Two partial 18×18 (or 16×16) | 480 | 420 | 400 | MHz |
| One 27×27 | 400 | 350 | | MHz |
| One 36×18 | 400 | 350 | | MHz |
| One sum of two 18×18 (One sum of two 16×16) | 400 | 350 | | MHz |
| One sum of square | 400 | 350 | | MHz |
| One 18×18 plus $36(a \times b) + c$ | 400 | 350 | | MHz |
| Modes using Two DSP Blocks | | | | |
| Three 18×18 | 400 | 350 | | MHz |
| One sum of four 18×18 | 380 | 300 | | MHz |

| Mode | Performance | | | Unit |
|-------------------------------------|-------------|-----|-----|------|
| | C3, I3L | C4 | I4 | |
| One sum of two 27×27 | 380 | 300 | 290 | MHz |
| One sum of two 36×18 | 380 | 300 | | MHz |
| One complex 18×18 | 400 | 350 | | MHz |
| One 36×36 | 380 | 300 | | MHz |
| Modes using Three DSP Blocks | | | | |
| One complex 18×25 | 340 | 275 | 265 | MHz |
| Modes using Four DSP Blocks | | | | |
| One complex 27×27 | 350 | 310 | | MHz |

Memory Block Specifications

Table 2-36: Memory Block Performance Specifications for Arria V GZ Devices

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to 50% output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in F_{MAX} .

| Memory | Mode | Resources Used | | Performance | | | | Unit |
|--------|--|----------------|--------|-------------|-----|-----|-----|------|
| | | ALUTs | Memory | C3 | C4 | I3L | I4 | |
| MLAB | Single port, all supported widths | 0 | 1 | 400 | 315 | 400 | 315 | MHz |
| | Simple dual-port, x32/x64 depth | 0 | 1 | 400 | 315 | 400 | 315 | MHz |
| | Simple dual-port, x16 depth ⁽¹⁷⁸⁾ | 0 | 1 | 533 | 400 | 533 | 400 | MHz |
| | ROM, all supported widths | 0 | 1 | 500 | 450 | 500 | 450 | MHz |

⁽¹⁷⁸⁾ The F_{MAX} specification is only achievable with Fitter options, **MLAB Implementation In 16-Bit Deep Mode** enabled.

| Memory | Mode | Resources Used | | Performance | | | | Unit |
|---------------|--|----------------|--------|-------------|-----|-----|-----|------|
| | | ALUTs | Memory | C3 | C4 | I3L | I4 | |
| M20K Block | Single-port, all supported widths | 0 | 1 | 650 | 550 | 500 | 450 | MHz |
| | Simple dual-port, all supported widths | 0 | 1 | 650 | 550 | 500 | 450 | MHz |
| | Simple dual-port with the read-during-write option set to Old Data , all supported widths | 0 | 1 | 455 | 400 | 455 | 400 | MHz |
| | Simple dual-port with ECC enabled, 512 × 32 | 0 | 1 | 400 | 350 | 400 | 350 | MHz |
| | Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32 | 0 | 1 | 500 | 450 | 500 | 450 | MHz |
| | True dual port, all supported widths | 0 | 1 | 650 | 550 | 500 | 450 | MHz |
| | ROM, all supported widths | 0 | 1 | 650 | 550 | 500 | 450 | MHz |

Temperature Sensing Diode Specifications

Table 2-37: Internal Temperature Sensing Diode Specification

| Temperature Range | Accuracy | Offset Calibrated Option | Sampling Rate | Conversion Time | Resolution | Minimum Resolution with no Missing Codes |
|-------------------|----------|--------------------------|----------------|-----------------|------------|--|
| -40°C to 100°C | ±8°C | No | 1 MHz, 500 kHz | < 100 ms | 8 bits | 8 bits |

Table 2-38: External Temperature Sensing Diode Specifications for Arria V GZ Devices

| Description | Min | Typ | Max | Unit |
|-----------------------------------|-------|-------|-------|------|
| I_{bias} , diode source current | 8 | — | 200 | μA |
| V_{bias} , voltage across diode | 0.3 | — | 0.9 | V |
| Series resistance | — | — | < 1 | Ω |
| Diode ideality factor | 1.006 | 1.008 | 1.010 | — |

Periphery Performance

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVC MOS** at 100 MHz interfacing frequency with a 10 pF load.

Note: The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

High-Speed Clock Specifications

Table 2-39: High-Speed Clock Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

For LVDS applications, you must use the PLLs in integer PLL mode.

Arria V GZ devices support the following output standards using true LVDS output buffer types on all I/O banks.

- True RSDS output standard with data rates of up to 230 Mbps
- True mini-LVDS output standard with data rates of up to 340 Mbps

| Symbol | Conditions | C3, I3L | | | C4, I4 | | | Unit |
|--|--|---------|-----|-----|--------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| $f_{\text{HCLK_in}}$ (input clock frequency) True Differential I/O Standards ⁽¹⁷⁹⁾ | Clock boost factor $W = 1$ to 40 ⁽¹⁸⁰⁾ | 5 | — | 625 | 5 | — | 525 | MHz |
| $f_{\text{HCLK_in}}$ (input clock frequency) Single Ended I/O Standards | Clock boost factor $W = 1$ to 40 ⁽¹⁸⁰⁾ | 5 | — | 625 | 5 | — | 525 | MHz |

⁽¹⁷⁹⁾ This only applies to DPA and soft-CDR modes.

⁽¹⁸⁰⁾ Clock Boost Factor (W) is the ratio between the input data rate to the input clock rate.

2-46 High-Speed Clock Specifications

| Symbol | Conditions | C3, I3L | | | C4, I4 | | | Unit |
|---|--|---------|-----|----------------------|--------|-----|----------------------|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| $f_{\text{HSCLK_in}}$ (input clock frequency) Single Ended I/O Standards | Clock boost factor $W = 1$ to 40 ⁽¹⁸⁰⁾ | 5 | — | 420 | 5 | — | 420 | MHz |
| $f_{\text{HSCLK_OUT}}$ (output clock frequency) | — | 5 | — | 625 ⁽¹⁸¹⁾ | 5 | — | 525 ⁽¹⁸¹⁾ | MHz |

⁽¹⁸¹⁾ This is achieved by using the LVDS clock network.

Transmitter High-Speed I/O Specifications

Table 2-40: Transmitter High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

| Symbol | Conditions | C3, I3L | | | C4, I4 | | | Unit |
|---|--|---------|-----|-------|--------|-----|-------|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| True Differential I/O Standards - f_{HSDR} (data rate) | SERDES factor J = 3 to 10 (182), (183) | (184) | — | 1250 | (184) | — | 1050 | Mbps |
| | SERDES factor J \geq 4 LVDS TX with DPA (185), (186), (187), (188) | (184) | — | 1600 | (184) | — | 1250 | Mbps |
| | SERDES factor J = 2, uses DDR Registers | (184) | — | (189) | (184) | — | (189) | Mbps |
| | SERDES factor J = 1, uses SDR Register | (184) | — | (189) | (184) | — | (189) | Mbps |

(182) If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.

(183) The F_{MAX} specification is based on the fast clock used for serial data. The interface F_{MAX} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

(184) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

(185) Arria V GZ RX LVDS will need DPA. For Arria V GZ TX LVDS, the receiver side component must have DPA.

(186) Requires package skew compensation with PCB trace length.

(187) Do not mix single-ended I/O buffer within LVDS I/O bank.

(188) Chip-to-chip communication only with a maximum load of 5 pF.

(189) The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (f_{OUT}) provided you can close the design timing and the signal integrity simulation is clean.

| Symbol | Conditions | C3, I3L | | | C4, I4 | | | Unit |
|---|---|---------|-----|-----|--------|-----|------|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Emulated Differential I/O Standards with Three External Output Resistor Networks - f_{HSDR} (data rate) (190) | SERDES factor J = 4 to 10 ⁽¹⁹¹⁾ | (184) | — | 840 | (184) | — | 840 | Mbps |
| $t_{\text{x Jitter}}$ - True Differential I/O Standards | Total Jitter for Data Rate 600 Mbps - 1.25 Gbps | — | — | 160 | — | — | 160 | ps |
| | Total Jitter for Data Rate < 600 Mbps | — | — | 0.1 | — | — | 0.1 | UI |
| $t_{\text{x Jitter}}$ - Emulated Differential I/O Standards with Three External Output Resistor Network | Total Jitter for Data Rate 600 Mbps - 1.25 Gbps | — | — | 300 | — | — | 325 | ps |
| | Total Jitter for Data Rate < 600 Mbps | — | — | 0.2 | — | — | 0.25 | UI |
| t_{DUTY} | Transmitter output clock duty cycle for both True and Emulated Differential I/O Standards | 45 | 50 | 55 | 45 | 50 | 55 | % |
| t_{RISE} & t_{FALL} | True Differential I/O Standards | — | — | 200 | — | — | 200 | ps |
| | Emulated Differential I/O Standards with three external output resistor networks | — | — | 250 | — | — | 300 | ps |
| TCCS | True Differential I/O Standards | — | — | 150 | — | — | 150 | ps |
| | Emulated Differential I/O Standards | — | — | 300 | — | — | 300 | ps |

⁽¹⁹⁰⁾ You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine leftover timing margin.

⁽¹⁹¹⁾ When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.

Receiver High-Speed I/O Specifications

Table 2-41: Receiver High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

| Symbol | Conditions | C3, I3L | | | C4, I4 | | | Unit |
|--|--|---------|-----|-------|--------|-----|-------|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| True Differential I/O Standards - f_{HSDRDPA} (data rate) | SERDES factor J = 3 to 10 (192), (193), (194), (195), (196), (197) | 150 | — | 1250 | 150 | — | 1050 | Mbps |
| | SERDES factor J \geq 4 LVDS RX with DPA (193), (195), (196), (197) | 150 | — | 1600 | 150 | — | 1250 | Mbps |
| | SERDES factor J = 2, uses DDR Registers | (198) | — | (199) | (198) | — | (199) | Mbps |
| | SERDES factor J = 1, uses SDR Register | (198) | — | (199) | (198) | — | (199) | Mbps |

⁽¹⁹²⁾ The F_{MAX} specification is based on the fast clock used for serial data. The interface F_{MAX} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

⁽¹⁹³⁾ Arria V GZ RX LVDS will need DPA. For Arria V GZ TX LVDS, the receiver side component must have DPA.

⁽¹⁹⁴⁾ Arria V GZ LVDS serialization and de-serialization factor needs to be x4 and above.

⁽¹⁹⁵⁾ Requires package skew compensation with PCB trace length.

⁽¹⁹⁶⁾ Do not mix single-ended I/O buffer within LVDS I/O bank.

⁽¹⁹⁷⁾ Chip-to-chip communication only with a maximum load of 5 pF.

⁽¹⁹⁸⁾ The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

⁽¹⁹⁹⁾ The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (f_{OUT}) provided you can close the design timing and the signal integrity simulation is clean.

| Symbol | Conditions | C3, I3L | | | C4, I4 | | | Unit |
|-------------------------------|--|---------|-----|-------|--------|-----|-------|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| f_{HSDR} (data rate) | SERDES factor J = 3 to 10 | (198) | — | (200) | (198) | — | (200) | Mbps |
| | SERDES factor J = 2, uses DDR Registers | (198) | — | (199) | (198) | — | (199) | Mbps |
| | SERDES factor J = 1, uses SDR Register | (198) | — | (199) | (198) | — | (199) | Mbps |

DPA Mode High-Speed I/O Specifications

Table 2-42: High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

| Symbol | Conditions | C3, I3L | | | C4, I4 | | | Unit |
|----------------|------------|---------|-----|-------|--------|-----|-------|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| DPA run length | — | — | — | 10000 | — | — | 10000 | UI |

Figure 2-3: DPA Lock Time Specification with DPA PLL Calibration Enabled



⁽²⁰⁰⁾ You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

Table 2-43: DPA Lock Time Specifications for Arria V GZ Devices

The DPA lock time is for one channel.

One data transition is defined as a 0-to-1 or 1-to-0 transition.

The DPA lock time stated in this table applies to both commercial and industrial grade.

| Standard | Training Pattern | Number of Data Transitions in One Repetition of the Training Pattern | Number of Repetitions per 256 Data Transitions ⁽²⁰¹⁾ | Maximum |
|--------------------|----------------------|--|---|----------------------|
| SPI-4 | 00000000001111111111 | 2 | 128 | 640 data transitions |
| Parallel Rapid I/O | 00001111 | 2 | 128 | 640 data transitions |
| | 10010000 | 4 | 64 | 640 data transitions |
| Miscellaneous | 10101010 | 8 | 32 | 640 data transitions |
| | 01010101 | 8 | 32 | 640 data transitions |

Soft CDR Mode High-Speed I/O Specifications

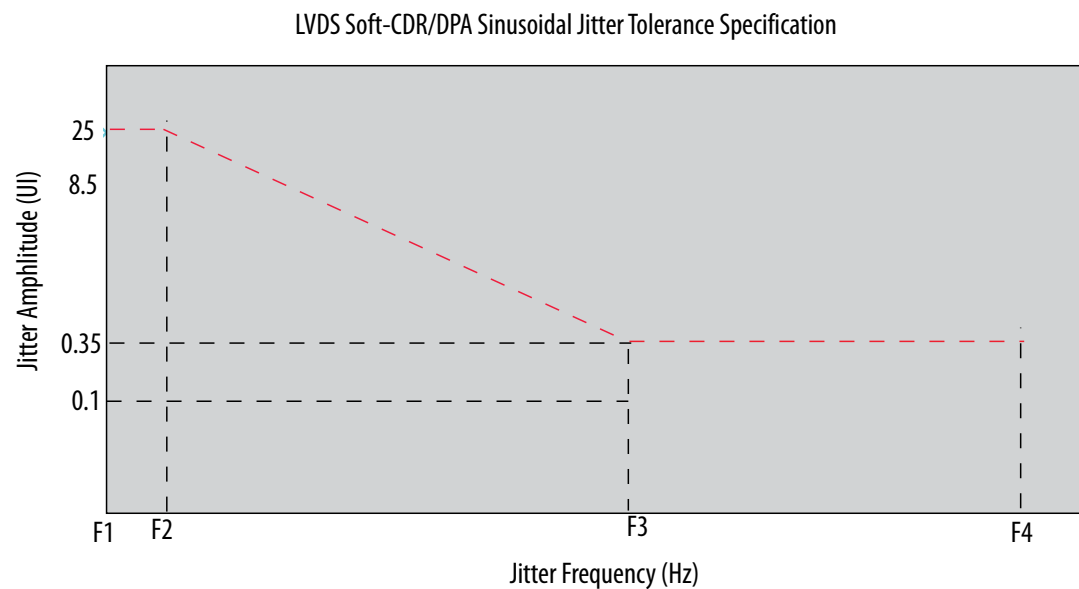
Table 2-44: High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

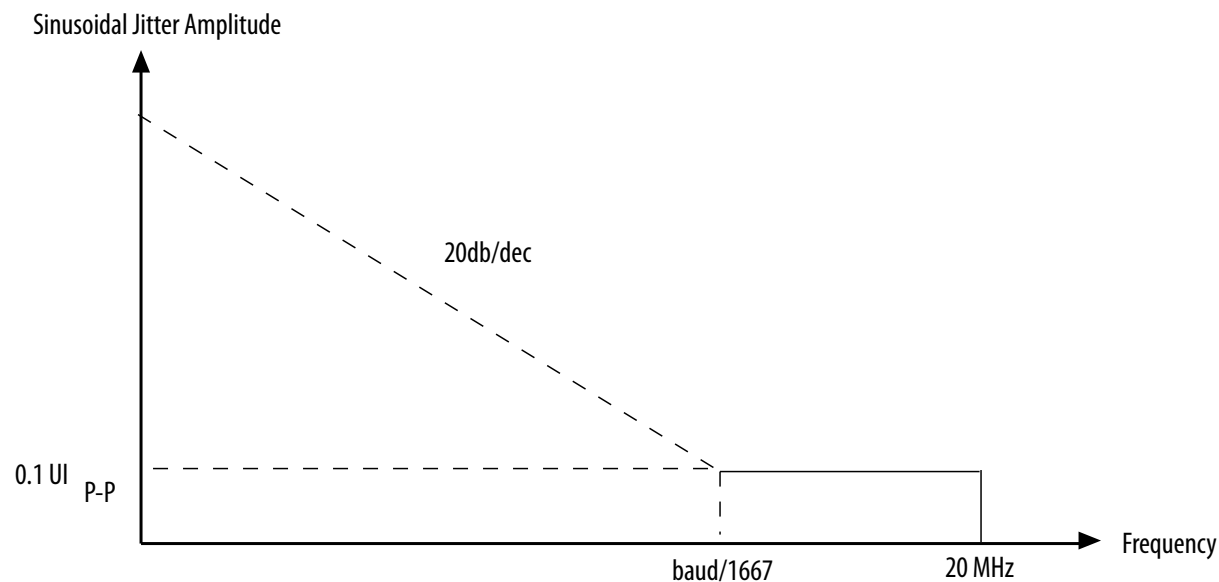
| Symbol | Conditions | C3, I3L | | | C4, I4 | | | Unit |
|------------------------|------------|---------|-----|-----|--------|-----|-----|-------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Soft-CDR ppm tolerance | — | — | — | 300 | — | — | 300 | ± ppm |

⁽²⁰¹⁾ This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 2-4: LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate ≥ 1.25 GbpsTable 2-45: LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate ≥ 1.25 Gbps

| | Jitter Frequency (Hz) | Sinusoidal Jitter (UI) |
|----|-----------------------|------------------------|
| F1 | 10,000 | 25.000 |
| F2 | 17,565 | 25.000 |
| F3 | 1,493,000 | 0.350 |
| F4 | 50,000,000 | 0.350 |

Figure 2-5: LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate < 1.25 Gbps



Non DPA Mode High-Speed I/O Specifications

Table 2-46: High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

| Symbol | Conditions | C3, I3L | | | C4, I4 | | | Unit |
|-----------------|------------|---------|-----|-----|--------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Sampling Window | — | — | — | 300 | — | — | 300 | ps |

DLL Range Specifications

Table 2-47: DLL Range Specifications for Arria V GZ Devices

Arria V GZ devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

| Parameter | C3, I3L | C4, I4 | Unit |
|-------------------------------|-----------|-----------|------|
| DLL operating frequency range | 300 – 890 | 300 – 890 | MHz |

DQS Logic Block Specifications

Table 2-48: DQS Phase Offset Delay Per Setting for Arria V GZ Devices

The typical value equals the average of the minimum and maximum values.

The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a –3 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is $[625 \text{ ps} + (10 \times 11 \text{ ps}) \pm 20 \text{ ps}] = 735 \text{ ps} \pm 20 \text{ ps}$.

| Speed Grade | Min | Max | Unit |
|-------------|-----|-----|------|
| C3, I3L | 8 | 15 | ps |
| C4, I4 | 8 | 16 | ps |

Table 2-49: DQS Phase Shift Error Specification for DLL-Delayed Clock ($t_{\text{DQS_PSERR}}$) for Arria V GZ Devices

This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a –3 speed grade is $\pm 84 \text{ ps}$ or $\pm 42 \text{ ps}$.

| Number of DQS Delay Buffers | C3, I3L | C4, I4 | Unit |
|-----------------------------|---------|--------|------|
| 1 | 30 | 32 | ps |
| 2 | 60 | 64 | ps |
| 3 | 90 | 96 | ps |
| 4 | 120 | 128 | ps |

Memory Output Clock Jitter Specifications

Table 2-50: Memory Output Clock Jitter Specification for Arria V GZ Devices

The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.

The clock jitter specification applies to the memory output clock pins clocked by an integer PLL.

The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) -12, equivalent to 14 sigma.

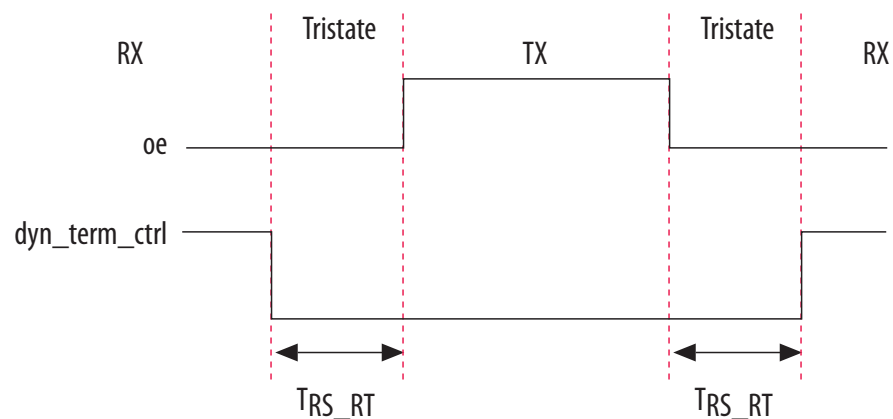
| Clock Network | Parameter | Symbol | C3, I3L | | C4, I4 | | Unit |
|---------------|------------------------------|-----------------|---------|------|--------|------|------|
| | | | Min | Max | Min | Max | |
| Regional | Clock period jitter | $t_{JIT(per)}$ | -55 | 55 | -55 | 55 | ps |
| | Cycle-to-cycle period jitter | $t_{JIT(cc)}$ | -110 | 110 | -110 | 110 | ps |
| | Duty cycle jitter | $t_{JIT(duty)}$ | -82.5 | 82.5 | -82.5 | 82.5 | ps |
| Global | Clock period jitter | $t_{JIT(per)}$ | -82.5 | 82.5 | -82.5 | 82.5 | ps |
| | Cycle-to-cycle period jitter | $t_{JIT(cc)}$ | -165 | 165 | -165 | 165 | ps |
| | Duty cycle jitter | $t_{JIT(duty)}$ | -90 | 90 | -90 | 90 | ps |
| PHY Clock | Clock period jitter | $t_{JIT(per)}$ | -30 | 30 | -35 | 35 | ps |
| | Cycle-to-cycle period jitter | $t_{JIT(cc)}$ | -60 | 60 | -70 | 70 | ps |
| | Duty cycle jitter | $t_{JIT(duty)}$ | -45 | 45 | -56 | 56 | ps |

OCT Calibration Block Specifications

Table 2-51: OCT Calibration Block Specifications for Arria V GZ Devices

| Symbol | Description | Min | Typ | Max | Unit |
|--------------|---|-----|------|-----|--------|
| OCTUSRCLK | Clock required by the OCT calibration blocks | — | — | 20 | MHz |
| T_{OCTCAL} | Number of OCTUSRCLK clock cycles required for OCT R_S/R_T calibration | — | 1000 | — | Cycles |

| Symbol | Description | Min | Typ | Max | Unit |
|-----------------------|---|-----|-----|-----|--------|
| T_{OCTSHIFT} | Number of OCTUSRCLK clock cycles required for the OCT code to shift out | — | 32 | — | Cycles |
| $T_{\text{RS_RT}}$ | Time required between the <code>dyn_term_ctrl</code> and <code>oe</code> signal transitions in a bidirectional I/O buffer to dynamically switch between OCT R_S and R_T (See the figure below.) | — | 2.5 | — | ns |

Figure 2-6: Timing Diagram for `oe` and `dyn_term_ctrl` Signals

Duty Cycle Distortion (DCD) Specifications

Table 2-52: Worst-Case DCD on Arria V GZ I/O Pins

The DCD numbers do not cover the core clock network.

| Symbol | C3, I3L | | C4, I4 | | Unit |
|-------------------|---------|-----|--------|-----|------|
| | Min | Max | Min | Max | |
| Output Duty Cycle | 45 | 55 | 45 | 55 | % |

Configuration Specification

POR Specifications

Table 2-53: Fast and Standard POR Delay Specification for Arria V GZ Devices

Select the POR delay based on the MSEL setting as described in the “Configuration Schemes for Arria V Devices” table in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

| POR Delay | Minimum (ms) | Maximum (ms) |
|-----------|--------------|---------------------|
| Fast | 4 | 12 ⁽²⁰²⁾ |
| Standard | 100 | 300 |

Related Information

[Configuration, Design Security, and Remote System Upgrades in Arria V Devices](#)

JTAG Configuration Specifications

Table 2-54: JTAG Timing Parameters and Values for Arria V GZ Devices

| Symbol | Description | Min | Max | Unit |
|------------------|--------------------------|----------------------|-----|------|
| t_{JCP} | TCK clock period | 30 | — | ns |
| t_{JCP} | TCK clock period | 167 ⁽²⁰³⁾ | — | ns |
| t_{JCH} | TCK clock high time | 14 | — | ns |
| t_{JCL} | TCK clock low time | 14 | — | ns |
| t_{JPSU} (TDI) | TDI JTAG port setup time | 2 | — | ns |
| t_{JPSU} (TMS) | TMS JTAG port setup time | 3 | — | ns |

⁽²⁰²⁾ The maximum pulse width of the fast POR delay is 12 ms, providing enough time for the PCIe hard IP to initialize after the POR trip.

⁽²⁰³⁾ The minimum TCK clock period is 167 ns if VCCBAT is within the range 1.2V-1.5V when you perform the volatile key programming.

| Symbol | Description | Min | Max | Unit |
|------------|--|-----|---------------------|------|
| t_{JPH} | JTAG port hold time | 5 | — | ns |
| t_{JPCO} | JTAG port clock to output | — | 11 ⁽²⁰⁴⁾ | ns |
| t_{JPZX} | JTAG port high impedance to valid output | — | 14 ⁽²⁰⁴⁾ | ns |
| t_{JPXZ} | JTAG port valid output to high impedance | — | 14 ⁽²⁰⁴⁾ | ns |

Fast Passive Parallel (FPP) Configuration Timing

DCLK-to-DATA[] Ratio (r) for FPP Configuration

FPP configuration requires a different DCLK-to-DATA[] ratio when you turn on encryption or the compression feature.

Table 2-55: DCLK-to-DATA[] Ratio for Arria V GZ Devices

Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is r times the data rate in bytes per second (Bps), or words per second (Wps). For example, in FPP ×16 when the DCLK-to-DATA[] ratio is 2, the DCLK frequency must be 2 times the data rate in Wps. Arria V GZ devices use the additional clock cycles to decrypt and decompress the configuration data.

| Configuration Scheme | Decompression | Design Security | DCLK-to-DATA[] Ratio |
|----------------------|---------------|-----------------|----------------------|
| FPP ×8 | Disabled | Disabled | 1 |
| | Disabled | Enabled | 1 |
| | Enabled | Disabled | 2 |
| | Enabled | Enabled | 2 |
| FPP ×16 | Disabled | Disabled | 1 |
| | Disabled | Enabled | 2 |
| | Enabled | Disabled | 4 |
| | Enabled | Enabled | 4 |

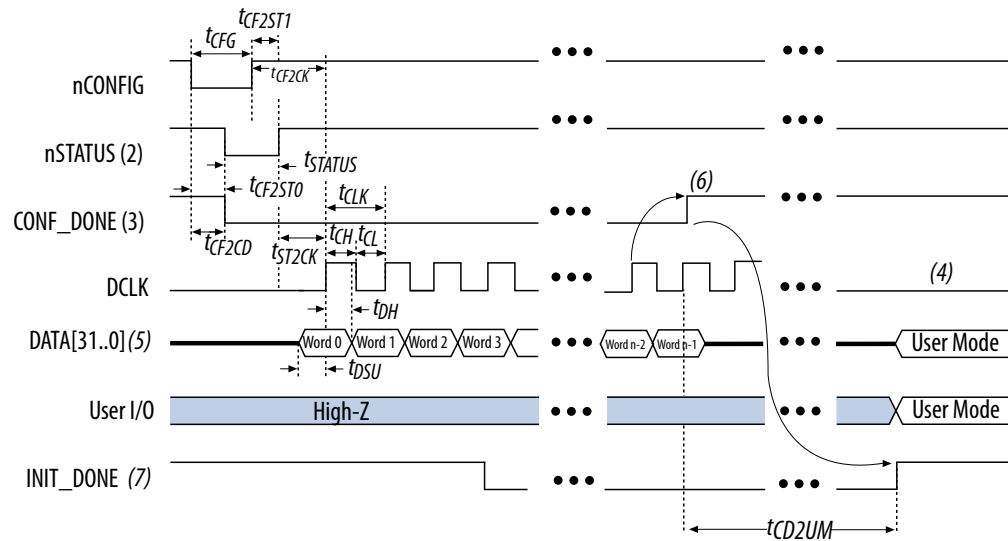
⁽²⁰⁴⁾ A 1-ns adder is required for each V_{CCIO} voltage step down from 3.0 V. For example, $t_{JPCO} = 12$ ns if V_{CCIO} of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

| Configuration Scheme | Decompression | Design Security | DCLK-to-DATA[] Ratio |
|----------------------|---------------|-----------------|----------------------|
| FPP ×32 | Disabled | Disabled | 1 |
| | Disabled | Enabled | 4 |
| | Enabled | Disabled | 8 |
| | Enabled | Enabled | 8 |

FPP Configuration Timing when DCLK to DATA[] = 1

Figure 2-7: FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is 1

Timing waveform for FPP configuration when using a MAX[®] II or MAX V device as an external host.



Notes:

1. The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
2. After power-up, the Arria V GZ device holds nSTATUS low for the time of the POR delay.
3. After power-up, before and during configuration, CONF_DONE is low.
4. Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
5. For FPP $\times 16$, use DATA[15..0]. For FPP $\times 8$, use DATA[7..0]. DATA[31..0] are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.
6. To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF_DONE is released high when the Arria V GZ device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
7. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Note: When you enable the decompression or design security feature, the DCLK-to-DATA[] ratio varies for FPP ×8, FPP ×16, and FPP ×32. For the respective DCLK-to-DATA[] ratio, refer to the "DCLK-to-DATA[] Ratio for Arria V GZ Devices" table.

Table 2-56: FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is 1

Use these timing parameters when the decompression and design security features are disabled.

| Symbol | Parameter | Minimum | Maximum | Unit |
|------------------------------|--|-------------------------|------------------------|------|
| t_{CF2CD} | nCONFIG low to CONF_DONE low | — | 600 | ns |
| t_{CF2ST0} | nCONFIG low to nSTATUS low | — | 600 | ns |
| t_{CFG} | nCONFIG low pulse width | 2 | — | μs |
| t_{STATUS} | nSTATUS low pulse width | 268 | 1,506 ⁽²⁰⁵⁾ | μs |
| t_{CF2ST1} | nCONFIG high to nSTATUS high | — | 1,506 ⁽²⁰⁶⁾ | μs |
| t_{CF2CK} (207) | nCONFIG high to first rising edge on DCLK | 1,506 | — | μs |
| t_{ST2CK} ⁽²⁰⁷⁾ | nSTATUS high to first rising edge of DCLK | 2 | — | μs |
| t_{DSU} | DATA[] setup time before rising edge on DCLK | 5.5 | — | ns |
| t_{DH} | DATA[] hold time after rising edge on DCLK | 0 | — | ns |
| t_{CH} | DCLK high time | $0.45 \times 1/f_{MAX}$ | — | s |
| t_{CL} | DCLK low time | $0.45 \times 1/f_{MAX}$ | — | s |
| t_{CLK} | DCLK period | $1/f_{MAX}$ | — | s |
| f_{MAX} | DCLK frequency (FPP ×8/×16) | — | 125 | MHz |
| | DCLK frequency (FPP ×32) | — | 100 | MHz |
| t_{CD2UM} | CONF_DONE high to user mode ⁽²⁰⁸⁾ | 175 | 437 | μs |

⁽²⁰⁵⁾ This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

⁽²⁰⁶⁾ This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

⁽²⁰⁷⁾ If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

⁽²⁰⁸⁾ The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

| Symbol | Parameter | Minimum | Maximum | Unit |
|------------------|---|---|---------|------|
| t_{CD2CU} | CONF_DONE high to CLKUSR enabled | $4 \times$ maximum DCLK period | — | — |
| t_{CD2UM} C | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU} +$ ($17,408 \times$ CLKUSR period) ⁽²⁰⁹⁾ | — | — |

Related Information

- [DCLK-to-DATA\[\] Ratio \(r\) for FPP Configuration](#) on page 2-58
- [Configuration, Design Security, and Remote System Upgrades in Arria V Devices](#)

⁽²⁰⁹⁾ To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the “Initialization” section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

FPP Configuration Timing when DCLK to DATA[] > 1

Figure 2-8: FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1 ,

Timing when using a MAX II device, MAX V device, or microprocessor as an external host.



Notes:

1. To find out the DCLK-to-DATA[] ratio for your system, refer to the "DCLK-to-DATA[] Ratio for Arria V GZ Devices" table.
2. The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
3. After power-up, the Arria V GZ device holds nSTATUS low for the time as specified by the POR delay.
4. After power-up, before and during configuration, CONF_DONE is low.
5. Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
6. "r" denotes the DCLK-to-DATA[] ratio. For the DCLK-to-DATA[] ratio based on the decompression and the design security feature enable settings, refer to the "DCLK-to-DATA[] Ratio for Arria V GZ Devices" table.
7. If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA[31..0] pins prior to sending the first DCLK rising edge.
8. To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF_DONE is released high after the Arria V GZ device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
9. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 2-57: FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is >1

Use these timing parameters when you use the decompression and design security features.

| Symbol | Parameter | Minimum | Maximum | Unit |
|------------------------------|--|---------------------------------|------------------------|---------|
| t_{CF2CD} | nCONFIG low to CONF_DONE low | — | 600 | ns |
| t_{CF2ST0} | nCONFIG low to nSTATUS low | — | 600 | ns |
| t_{CFG} | nCONFIG low pulse width | 2 | — | μ s |
| t_{STATUS} | nSTATUS low pulse width | 268 | 1,506 ⁽²¹⁰⁾ | μ s |
| t_{CF2ST1} | nCONFIG high to nSTATUS high | — | 1,506 ⁽²¹¹⁾ | μ s |
| t_{CF2CK} ⁽²¹²⁾ | nCONFIG high to first rising edge on DCLK | 1,506 | — | μ s |
| t_{ST2CK} ⁽²¹²⁾ | nSTATUS high to first rising edge of DCLK | 2 | — | μ s |
| t_{DSU} | DATA[] setup time before rising edge on DCLK | 5.5 | — | ns |
| t_{DH} | DATA[] hold time after rising edge on DCLK | $N-1/f_{DCLK}$ ⁽²¹³⁾ | — | s |
| t_{CH} | DCLK high time | $0.45 \times 1/f_{MAX}$ | — | s |
| t_{CL} | DCLK low time | $0.45 \times 1/f_{MAX}$ | — | s |
| t_{CLK} | DCLK period | $1/f_{MAX}$ | — | s |
| f_{MAX} | DCLK frequency (FPP $\times 8/\times 16$) | — | 125 | MHz |
| | DCLK frequency (FPP $\times 32$) | — | 100 | MHz |
| t_R | Input rise time | — | 40 | ns |
| t_F | Input fall time | — | 40 | ns |

⁽²¹⁰⁾ You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

⁽²¹¹⁾ You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.

⁽²¹²⁾ If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

⁽²¹³⁾ N is the DCLK-to-DATA ratio and f_{DCLK} is the DCLK frequency the system is operating.

| Symbol | Parameter | Minimum | Maximum | Unit |
|--------------|---|---|---------|---------|
| t_{CD2UM} | CONF_DONE high to user mode ⁽²¹⁴⁾ | 175 | 437 | μ s |
| t_{CD2CU} | CONF_DONE high to CLKUSR enabled | $4 \times$ maximum DCLK period | — | — |
| t_{CD2UMC} | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU} + (17,408 \times \text{CLKUSR period})$ ⁽²¹⁵⁾ | — | — |

Related Information

- [DCLK-to-DATA\[\] Ratio \(r\) for FPP Configuration](#) on page 2-58
- [Configuration, Design Security, and Remote System Upgrades in Arria V Devices](#)

⁽²¹⁴⁾ The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.

⁽²¹⁵⁾ To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the “Initialization” section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

Active Serial Configuration Timing

Figure 2-9: AS Configuration Timing

Timing waveform for the active serial (AS) x1 mode and AS x4 mode configuration timing.



Notes:

1. If you are using AS x4 mode, this signal represents the AS_DATA[3:0] and ERQ sends in 4-bits of data for each DCLK cycle.
2. The initialization clock can be from internal oscillator or CLKUSR pin.
3. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 2-58: AS Timing Parameters for AS x1 and AS x4 Configurations in Arria V GZ Devices

The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

t_{CF2CD} , t_{CF2ST0} , t_{CFG} , t_{STATUS} , and t_{CF2ST1} timing parameters are identical to the timing parameters for PS mode listed in the "PS Timing Parameters for Arria V GZ Devices" table.

| Symbol | Parameter | Minimum | Maximum | Unit |
|--------------|---|--|---------|---------|
| t_{CO} | DCLK falling edge to AS_DATA0/ASDO output | — | 4 | ns |
| t_{SU} | Data setup time before falling edge on DCLK | 1.5 | — | ns |
| t_{H} | Data hold time after falling edge on DCLK | 0 | — | ns |
| t_{CD2UM} | CONF_DONE high to user mode ⁽²¹⁶⁾ | 175 | 437 | μ s |
| t_{CD2CU} | CONF_DONE high to CLKUSR enabled | 4 × maximum DCLK period | — | — |
| t_{CD2UMC} | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU} + (17,408 \times \text{CLKUSR period})$ | — | — |

Table 2-59: DCLK Frequency Specification in the AS Configuration Scheme

This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.

The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

| Minimum | Typical | Maximum | Unit |
|---------|---------|---------|------|
| 5.3 | 7.9 | 12.5 | MHz |
| 10.6 | 15.7 | 25.0 | MHz |
| 21.3 | 31.4 | 50.0 | MHz |
| 42.6 | 62.9 | 100.0 | MHz |

⁽²¹⁶⁾ To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on this pin, refer to the "Initialization" section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

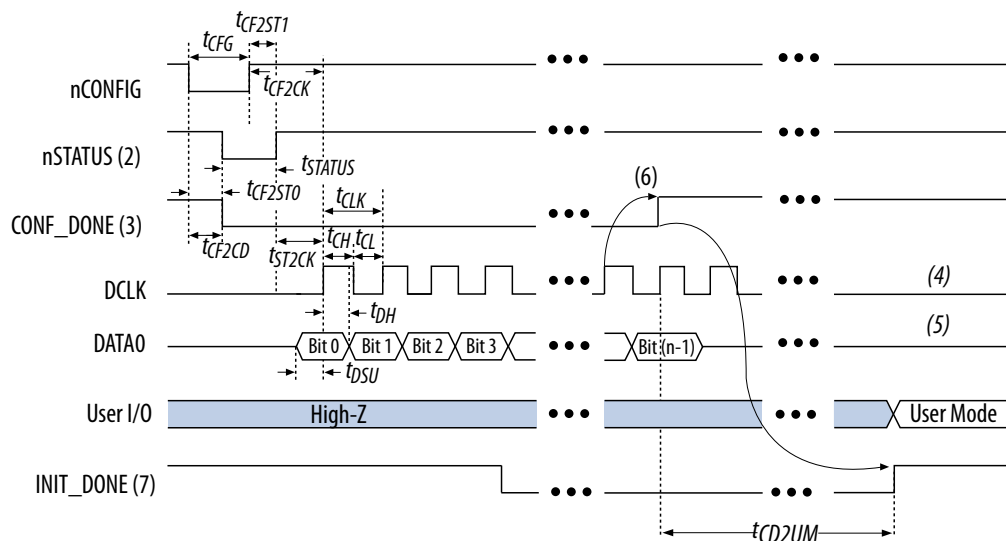
Related Information

- [Passive Serial Configuration Timing](#) on page 2-69
- [Configuration, Design Security, and Remote System Upgrades in Arria V Devices](#)

Passive Serial Configuration Timing

Figure 2-10: PS Configuration Timing Waveform

Timing waveform for a passive serial (PS) configuration when using a MAX II device, MAX V device, or microprocessor as an external host.



Notes:

1. The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
2. After power-up, the Arria V GZ device holds nSTATUS low for the time of the POR delay.
3. After power-up, before and during configuration, CONF_DONE is low.
4. Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
5. DATA0 is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the Device and Pins Option.
6. To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF_DONE is released high after the Arria V GZ device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
7. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 2-60: PS Timing Parameters for Arria V GZ Devices

| Symbol | Parameter | Minimum | Maximum | Unit |
|------------------------------|---|---|------------------------|---------|
| t_{CF2CD} | nCONFIG low to CONF_DONE low | — | 600 | ns |
| t_{CF2ST0} | nCONFIG low to nSTATUS low | — | 600 | ns |
| t_{CFG} | nCONFIG low pulse width | 2 | — | μ s |
| t_{STATUS} | nSTATUS low pulse width | 268 | 1,506 ⁽²¹⁷⁾ | μ s |
| t_{CF2ST1} | nCONFIG high to nSTATUS high | — | 1,506 ⁽²¹⁸⁾ | μ s |
| t_{CF2CK} (219) | nCONFIG high to first rising edge on DCLK | 1,506 | — | μ s |
| t_{ST2CK} ⁽²¹⁹⁾ | nSTATUS high to first rising edge of DCLK | 2 | — | μ s |
| t_{DSU} | DATA[] setup time before rising edge on DCLK | 5.5 | — | ns |
| t_{DH} | DATA[] hold time after rising edge on DCLK | 0 | — | ns |
| t_{CH} | DCLK high time | $0.45 \times 1/f_{MAX}$ | — | s |
| t_{CL} | DCLK low time | $0.45 \times 1/f_{MAX}$ | — | s |
| t_{CLK} | DCLK period | $1/f_{MAX}$ | — | s |
| f_{MAX} | DCLK frequency | — | 125 | MHz |
| t_{CD2UM} | CONF_DONE high to user mode ⁽²²⁰⁾ | 175 | 437 | μ s |
| t_{CD2CU} | CONF_DONE high to CLKUSR enabled | $4 \times$ maximum DCLK period | — | — |
| t_{CD2UMC} | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU} + (17,408 \times$ $CLKUSR period)$ ⁽²²¹⁾ | — | — |

⁽²¹⁷⁾ This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

⁽²¹⁸⁾ This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

⁽²¹⁹⁾ If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

⁽²²⁰⁾ The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

Related Information[Configuration, Design Security, and Remote System Upgrades in Arria V Devices](#)**Initialization****Table 2-61: Initialization Clock Source Option and the Maximum Frequency for Arria V GZ Devices**

| Initialization Clock Source | Configuration Schemes | Maximum Frequency (MHz) | Minimum Number of Clock Cycles |
|-----------------------------|-----------------------|-------------------------|--------------------------------|
| Internal Oscillator | AS, PS, FPP | 12.5 | 17,408 |
| CLKUSR ⁽²²²⁾ | PS, FPP | 125 | |
| | AS | 100 | |
| DCLK | PS, FPP | 125 | |

Configuration Files

Use the following table to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal file (**.hex**) or tabular text file (**.tff**) format, have different file sizes.

For the different types of configuration file and file sizes, refer to the Quartus II software. However, for a specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size.

⁽²²¹⁾ To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the “Initialization” section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

⁽²²²⁾ To enable CLKUSR as the initialization clock source, turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus II software from the **General** panel of the **Device and Pin Options** dialog box.

Table 2-62: Uncompressed .rbf Sizes for Arria V GZ Devices

| Variant | Member Code | Configuration .rbf Size (bits) | IOCSR .rbf Size (bits) ⁽²²³⁾ |
|------------|-------------|--------------------------------|---|
| Arria V GZ | E1 | 137,598,880 | 562,208 |
| | E3 | 137,598,880 | 562,208 |
| | E5 | 213,798,880 | 561,760 |
| | E7 | 213,798,880 | 561,760 |

Table 2-63: Minimum Configuration Time Estimation for Arria V GZ Devices

| Variant | Member Code | Active Serial ⁽²²⁴⁾ | | | Fast Passive Parallel ⁽²²⁵⁾ | | |
|------------|-------------|--------------------------------|------------|----------------------|--|------------|----------------------|
| | | Width | DCLK (MHz) | Min Config Time (ms) | Width | DCLK (MHz) | Min Config Time (ms) |
| Arria V GZ | E1 | 4 | 100 | 344 | 32 | 100 | 43 |
| | E3 | 4 | 100 | 344 | 32 | 100 | 43 |
| | E5 | 4 | 100 | 534 | 32 | 100 | 67 |
| | E7 | 4 | 100 | 534 | 32 | 100 | 67 |

Remote System Upgrades Circuitry Timing Specification

Table 2-64: Remote System Upgrade Circuitry Timing Specifications

| Parameter | Minimum | Maximum | Unit |
|-------------------------------------|---------|---------|------|
| $t_{RU_nCONFIG}$ ⁽²²⁶⁾ | 250 | — | ns |
| $t_{RU_nRSTIMER}$ ⁽²²⁷⁾ | 250 | — | ns |

⁽²²³⁾ The IOCSR .rbf size is specifically for the Configuration via Protocol (CvP) feature.

⁽²²⁴⁾ DCLK frequency of 100 MHz using external CLKUSR.

⁽²²⁵⁾ Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

Related Information

- **[Configuration, Design Security, and Remote System Upgrades in Arria V Devices](#)**
For more information about the reconfiguration input for the ALTREMOTE_UPDATE IP core, refer to the “User Watchdog Timer” section.
- **[Configuration, Design Security, and Remote System Upgrades in Arria V Devices](#)**
For more information about the `reset_timer` input for the ALTREMOTE_UPDATE IP core, refer to the “Remote System Upgrade State Machine” section.

User Watchdog Internal Oscillator Frequency Specification

Table 2-65: User Watchdog Internal Oscillator Frequency Specifications

| Minimum | Typical | Maximum | Unit |
|---------|---------|---------|------|
| 5.3 | 7.9 | 12.5 | MHz |

I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

Related Information

[Arria V Devices Documentation page](#)

For the Excel-based I/O Timing spreadsheet

⁽²²⁶⁾ This is equivalent to strobing the reconfiguration input of the ALTREMOTE_UPDATE IP core high for the minimum timing specification. For more information, refer to the “Remote System Upgrade State Machine” section in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

⁽²²⁷⁾ This is equivalent to strobing the `reset_timer` input of the ALTREMOTE_UPDATE IP core high for the minimum timing specification. For more information, refer to the “User Watchdog Timer” section in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

Programmable IOE Delay

Table 2-66: IOE Programmable Delay for Arria V GZ Devices

| Parameter ⁽²²⁸⁾ | Available Settings | Min Offset ⁽²²⁹⁾ | Fast Model | | Slow Model | | | | Unit |
|----------------------------|--------------------|-----------------------------|------------|------------|------------|-------|-------|-------|------|
| | | | Industrial | Commercial | C3 | C4 | I3L | I4 | |
| D1 | 64 | 0 | 0.464 | 0.493 | 0.924 | 1.011 | 0.921 | 1.006 | ns |
| D2 | 32 | 0 | 0.230 | 0.244 | 0.459 | 0.503 | 0.456 | 0.500 | ns |
| D3 | 8 | 0 | 1.587 | 1.699 | 2.992 | 3.192 | 3.047 | 3.257 | ns |
| D4 | 64 | 0 | 0.464 | 0.492 | 0.924 | 1.011 | 0.920 | 1.006 | ns |
| D5 | 64 | 0 | 0.464 | 0.493 | 0.924 | 1.011 | 0.921 | 1.006 | ns |
| D6 | 32 | 0 | 0.229 | 0.244 | 0.458 | 0.503 | 0.456 | 0.499 | ns |

Programmable Output Buffer Delay

Table 2-67: Programmable Output Buffer Delay for Arria V GZ Devices

You can set the programmable output buffer delay in the Quartus II software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

| Symbol | Parameter | Typical | Unit |
|---------------------|----------------------------------|-------------|------|
| D _{OUTBUF} | Rising and/or falling edge delay | 0 (default) | ps |
| | | 50 | ps |
| | | 100 | ps |
| | | 150 | ps |

⁽²²⁸⁾ You can set this value in the Quartus II software by selecting **D1**, **D2**, **D3**, **D4**, **D5**, and **D6** in the **Assignment Name** column of **Assignment Editor**.

⁽²²⁹⁾ Minimum offset does not include the intrinsic delay.

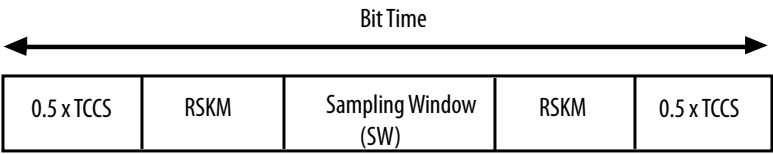
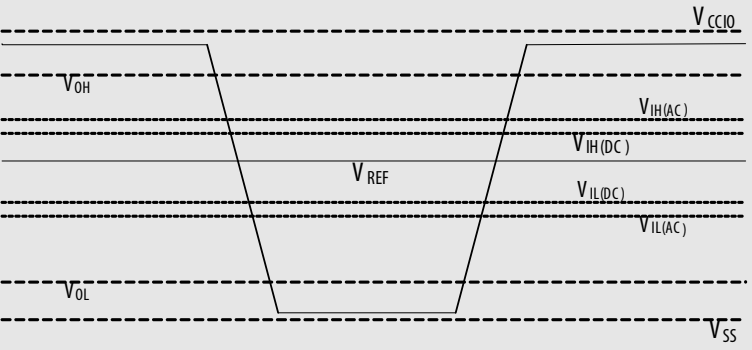
Glossary

Table 2-68: Glossary

| Term | Definition |
|----------------------------|--|
| Differential I/O Standards | <p>Receiver Input Waveforms</p>  <p>Single-Ended Waveform</p> <p>The diagram shows two signal channels, Positive Channel (p) and Negative Channel (n), relative to a common mode voltage V_{CM} and ground. The Positive Channel (p) is labeled V_{IH} and the Negative Channel (n) is labeled V_{IL}. The differential voltage between the two channels is labeled V_{ID}.</p> <p>Differential Waveform</p> <p>The diagram shows a differential signal waveform where the positive channel (p) is V_{IH} and the negative channel (n) is V_{IL}. The differential voltage is labeled V_{ID}. The common mode voltage is labeled $p - n = 0V$.</p> |
| | Transmitter Output Waveforms |

| Term | Definition |
|---------------|---|
| | <p>Single-Ended Waveform</p>  <p>Positive Channel (p) = V_{OH} Negative Channel (n) = V_{OL} Ground</p> <p>Differential Waveform</p>  <p>p - n = 0V</p> |
| f_{HSCLK} | Left and right PLL input clock frequency. |
| f_{HSDR} | High-speed I/O block—Maximum and minimum LVDS data transfer rate ($f_{HSDR} = 1/TUI$), non-DPA. |
| $f_{HSDRDPA}$ | High-speed I/O block—Maximum and minimum LVDS data transfer rate ($f_{HSDRDPA} = 1/TUI$), DPA. |
| J | High-speed I/O block—Deserialization factor (width of parallel data bus). |

| Term | Definition |
|-----------------------------------|---|
| <p>JTAG Timing Specifications</p> | <p>JTAG Timing Specifications:</p>  |
| <p>PLL Specifications</p> | <p>Diagram of PLL Specifications</p>  <p>Note: 1. Core Clock can only be fed by dedicated clock input pins or PLL outputs.</p> |
| <p>R_L</p> | <p>Receiver differential input discrete resistor (external to the Arria V GZ device).</p> |

| Term | Definition |
|--|---|
| SW (sampling window) | <p>Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown:</p>  |
| Single-ended voltage referenced I/O standard | <p>The JEDEC standard for SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.</p> <p>The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing:</p> <p>Single-Ended Voltage Referenced I/O Standard</p>  |
| t_C | High-speed receiver and transmitter input and output clock period. |

| Term | Definition |
|--------------------------------|---|
| TCCS (channel-to-channel-skew) | The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table). |
| t_{DUTY} | High-speed I/O block—Duty cycle on the high-speed transmitter output clock. |
| t_{FALL} | Signal high-to-low transition time (80-20%) |
| t_{INCCJ} | Cycle-to-cycle jitter tolerance on the PLL clock input. |
| t_{OUTPJ_IO} | Period jitter on the general purpose I/O driven by a PLL. |
| t_{OUTPJ_DC} | Period jitter on the dedicated clock output driven by a PLL. |
| t_{RISE} | Signal low-to-high transition time (20-80%) |
| Timing Unit Interval (TUI) | The timing budget allowed for skew, propagation delays, and the data sampling window. ($TUI = 1/(\text{receiver input clock frequency multiplication factor}) = t_C/w$) |
| $V_{CM(DC)}$ | DC common mode input voltage. |
| V_{ICM} | Input common mode voltage—The common mode of the differential signal at the receiver. |
| V_{ID} | Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver. |
| $V_{DIF(AC)}$ | AC differential input voltage—Minimum AC input differential voltage required for switching. |
| $V_{DIF(DC)}$ | DC differential input voltage— Minimum DC input differential voltage required for switching. |
| V_{IH} | Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high. |
| $V_{IH(AC)}$ | High-level AC input voltage |
| $V_{IH(DC)}$ | High-level DC input voltage |
| V_{IL} | Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low. |
| $V_{IL(AC)}$ | Low-level AC input voltage |
| $V_{IL(DC)}$ | Low-level DC input voltage |
| V_{OCM} | Output common mode voltage—The common mode of the differential signal at the transmitter. |

| Term | Definition |
|-------------|--|
| V_{OD} | Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter. |
| V_{SWING} | Differential input voltage |
| V_X | Input differential cross point voltage |
| V_{OX} | Output differential cross point voltage |
| W | High-speed I/O block—clock boost factor |

Document Revision History

| Date | Version | Changes |
|---------------|------------|--|
| June 2016 | 2016.06.20 | <ul style="list-style-type: none"> Changed column heading from "Value" to "Maximum" in the "Pin Capacitance for Arria V GZ Devices" table. Changed the minimum supported data rate range values from "1000" to "2000" in the "ATX PLL Specifications for Arria V GZ Devices" table. Added the supported data rates for the following output standards using true LVDS output buffer types in the "High-Speed Clock Specifications for Arria V GZ Devices" table: <ul style="list-style-type: none"> True RSDS output standard: data rates of up to 230 Mbps True mini-LVDS output standard: data rates of up to 340 Mbps |
| December 2015 | 2015.12.16 | <ul style="list-style-type: none"> Removed the CDR ppm tolerance specification from the "Receiver Specifications for Arria V GZ Devices" table. Removed transmitter rise and fall time specifications from the "Transmitter Specifications for Arria V GZ Devices" table. Changed the .rbf sizes in the "Uncompressed .rbf Sizes for Arria V GZ Devices" table. Added a footnote to the "Transmitter High-Speed I/O Specifications for Arria V GZ Devices" table. |

| Date | Version | Changes |
|---------------|------------|--|
| June 2015 | 2015.06.16 | <ul style="list-style-type: none"> Changed the conditions for the reference clock rise and fall time and added a note to the condition in the "Reference Clock Specifications for Arria V GZ Devices" table. Added a note to the "Minimum differential eye opening at receiver serial input pins" specification in the "Receiver Specifications for Arria V GZ Devices" table. |
| January 2015 | 2015.01.30 | <ul style="list-style-type: none"> Added 240-Ω to the "OCT Calibration Accuracy Specifications for Arria V GZ Devices" table. Changed the CDR PPM tolerance spec in the "Receiver Specifications for Arria V GZ Devices" table. Added additional max data rate for fPLL in the "Fractional PLL Specifications for Arria V GZ Devices" table. |
| July 2014 | 3.8 | <ul style="list-style-type: none"> Updated Table 21. Updated Table 22 V_{OCM} (DC Coupled) condition. Updated the DCLK note to Figure 6, Figure 7, and Figure 9. Added note to Table 5 and Table 6. Added the DCLK specification to Table 50. Added note to Table 51. Updated the list of parameters in Table 53. |
| February 2014 | 3.7 | Updated Table 28. |
| December 2013 | 3.6 | <ul style="list-style-type: none"> Updated Table 2, Table 13, Table 18, Table 19, Table 22, Table 30, Table 33, Table 37, Table 38, Table 45, Table 46, Table 47, Table 56, Table 49. Updated "PLL Specifications". |
| August 2013 | 3.5 | Updated Table 28. |
| August 2013 | 3.4 | <ul style="list-style-type: none"> Removed Preliminary tags for Table 2, Table 4, Table 5, Table 14, Table 27, Table 28, Table 29, Table 31, Table 32, Table 43, Table 45, Table 46, Table 47, Table 48, Table 49, Table 50, and Table 54. Updated Table 2 and Table 28. |
| June 2013 | 3.3 | Updated Table 23, Table 28, Table 51, and Table 55. |

| Date | Version | Changes |
|---------------|---------|---|
| May 2013 | 3.2 | <ul style="list-style-type: none">Added Table 23.Updated Table 5, Table 22, Table 26, and Table 57.Updated Figure 6, Figure 7, Figure 8, and Figure 9. |
| March 2013 | 3.1 | <ul style="list-style-type: none">Updated Table 2, Table 6, Table 7, Table 8, Table 19, Table 22, Table 26, Table 29, Table 52.Updated “Maximum Allowed Overshoot and Undershoot Voltage”. |
| December 2012 | 3.0 | Initial release. |

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