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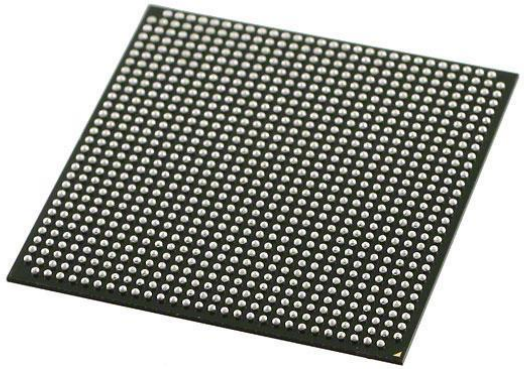

5ASXMB3E6F31C6N

# 3E6F31C6N Datasheet

| | |
|---|---|
| DiGi Electronics Part Number | 5ASXMB3E6F31C6N-DG |
| Manufacturer | Intel |
| Manufacturer Product Number | 5ASXMB3E6F31C6N |
| Description | IC SOC CORTEX-A9 700MHZ 896FBGA |
| Detailed Description | Dual ARM® Cortex®-A9 MPCore™ with CoreSight™ System On Chip (SOC) IC Arria V SX FPGA - 350K Logic Elements 700MHz 896-FBGA, FC (31x31) |

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RFQ Email: Info@DiGi-Electronics.com

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## Purchase and inquiry

| Manufacturer Product Number: | Manufacturer: |
| --- | --- |
| 5ASXMB3E6F31C6N | Intel |
| Series: | Product Status: |
| Arria V SX | Obsolete |
| Architecture: | Core Processor: |
| MCU, FPGA | Dual ARM® Cortex®-A9 MPCore™ with CoreSight™ |
| Flash Size: | RAM Size: |
| - | 64KB |
| Peripherals: | Connectivity: |
| DMA, POR, WDT | EBI/EMI, Ethernet, I²C, MMC/SD/SDIO, SPI, UART/USART, USB OTG |
| Speed: | Primary Attributes: |
| 700MHz | FPGA - 350K Logic Elements |
| Operating Temperature: | Package / Case: |
| 0°C ~ 85°C (TJ) | 896-BBGA, FCBGA |
| Supplier Device Package: | Number of I/O: |
| 896-FBGA, FC (31x31) | MCU - 208, FPGA - 250 |
| Base Product Number: | |
| 5ASXMB3 | |

## Environmental & Export classification

| RoHS Status: | Moisture Sensitivity Level (MSL): |
| --- | --- |
| RoHS Compliant | 3 (168 Hours) |
| ECCN: | HTSUS: |

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# Arria V Device Datasheet

Online Version
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AV-51002

ID: 683022
Version: 2019.04.26

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# 1. Arria® V GX, GT, SX, and ST Device Datasheet

This datasheet describes the electrical characteristics, switching characteristics, configuration specifications, and I/O timing for Arria® V devices.

Arria V devices are offered in commercial and industrial grades. Commercial devices are offered in –C4 (fastest), –C5, and –C6 speed grades. Industrial grade devices are offered in the –I3 and –I5 speed grades.

**Related Information**

Arria V Device Overview
Provides more information about the densities and packages of devices in the Arria V family.

## 1.1. Electrical Characteristics

The following sections describe the operating conditions and power consumption of Arria V devices.

### 1.1.1. Operating Conditions

Arria V devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Arria V devices, you must consider the operating requirements described in this section.

#### 1.1.1.1. Absolute Maximum Ratings

This section defines the maximum operating conditions for Arria V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms.

The functional operation of the device is not implied for these conditions.

***Caution:*** Conditions outside the range listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

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## Table 1. Absolute Maximum Ratings for Arria V Devices

| Symbol | Description | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Core voltage power supply | –0.50 | 1.43 | V |
| $V_{CCP}$ | Periphery circuitry, PCI Express* (PCIe*) hard IP block, and transceiver physical coding sublayer (PCS) power supply | –0.50 | 1.43 | V |
| $V_{CCPGM}$ | Configuration pins power supply | –0.50 | 3.90 | V |
| $V_{CC_AUX}$ | Auxiliary supply | –0.50 | 3.25 | V |
| $V_{CCBAT}$ | Battery back-up power supply for design security volatile key register | –0.50 | 3.90 | V |
| $V_{CCPD}$ | I/O pre-driver power supply | –0.50 | 3.90 | V |
| $V_{CCIO}$ | I/O power supply | –0.50 | 3.90 | V |
| $V_{CCD_FPLL}$ | Phase-locked loop (PLL) digital power supply | –0.50 | 1.80 | V |
| $V_{CCA_FPLL}$ | PLL analog power supply | –0.50 | 3.25 | V |
| $V_{CCA_GXB}$ | Transceiver high voltage power | –0.50 | 3.25 | V |
| $V_{CCH_GXB}$ | Transmitter output buffer power | –0.50 | 1.80 | V |
| $V_{CCR_GXB}$ | Receiver power | –0.50 | 1.50 | V |
| $V_{CCT_GXB}$ | Transmitter power | –0.50 | 1.50 | V |
| $V_{CCL_GXB}$ | Transceiver clock network power | –0.50 | 1.50 | V |
| $V_I$ | DC input voltage | –0.50 | 3.80 | V |
| $V_{CC_HPS}$ | HPS core voltage and periphery circuitry power supply | –0.50 | 1.43 | V |
| $V_{CCPD_HPS}$ | HPS I/O pre-driver power supply | –0.50 | 3.90 | V |
| $V_{CCIO_HPS}$ | HPS I/O power supply | –0.50 | 3.90 | V |
| $V_{CCRSTCLK_HPS}$ | HPS reset and clock input pins power supply | –0.50 | 3.90 | V |
| $V_{CCPLL_HPS}$ | HPS PLL analog power supply | –0.50 | 3.25 | V |
| $V_{CC_AUX_SHARED}$ | HPS auxiliary power supply | –0.50 | 3.25 | V |
| $I_{OUT}$ | DC output current per pin | –25 | 40 | mA |
| $T_J$ | Operating junction temperature | –55 | 125 | °C |
| $T_{STG}$ | Storage temperature (no bias) | –65 | 150 | °C |

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### 1.1.1.2. Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in the following table and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle.

For example, a signal that overshoots to 4.00 V can only be at 4.00 V for ~15% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 1.5 years.

**Table 2. Maximum Allowed Overshoot During Transitions for Arria V Devices**

This table lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime.

| Symbol | Description | Condition (V) | Overshoot Duration as % of High Time | Unit |
|---|---|---|---|---|
| Vi (AC) | AC input voltage | 3.8 | 100 | % |
| | | 3.85 | 68 | % |
| | | 3.9 | 45 | % |
| | | 3.95 | 28 | % |
| | | 4 | 15 | % |
| | | 4.05 | 13 | % |
| | | 4.1 | 11 | % |
| | | 4.15 | 9 | % |
| | | 4.2 | 8 | % |
| | | 4.25 | 7 | % |
| | | 4.3 | 5.4 | % |
| | | 4.35 | 3.2 | % |
| | | 4.4 | 1.9 | % |
| | | 4.45 | 1.1 | % |

*continued...*

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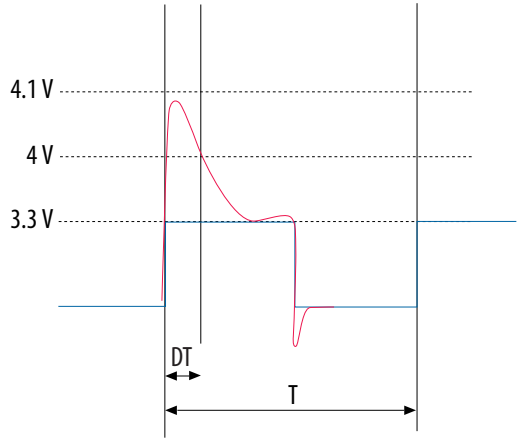
| Symbol | Description | Condition (V) | Overshoot Duration as % of High Time | Unit |
|---|---|---|---|---|
| | | 4.5 | 0.6 | % |
| | | 4.55 | 0.4 | % |
| | | 4.6 | 0.2 | % |

For an overshoot of 3.8 V, the percentage of high time for the overshoot can be as high as 100% over a 10-year period. Percentage of high time is calculated as ([delta T]/T) × 100. This 10-year period assumes that the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal.

**Figure 1. Arria V Devices Overshoot Duration**




### 1.1.1.3. Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Arria V devices.

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### 1.1.1.3.1. Recommended Operating Conditions

**Table 3. Recommended Operating Conditions for Arria V Devices**

This table lists the steady-state voltage values expected from Arria V devices. Power supply ramps must all be strictly monotonic, without plateaus.

| Symbol | Description | Condition | Minimum(1) | Typical | Maximum(1) | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Core voltage power supply | –C4, –I5, –C5, –C6 | 1.07 | 1.1 | 1.13 | V |
| | | –I3 | 1.12 | 1.15 | 1.18 | V |
| $V_{CCP}$ | Periphery circuitry, PCIe hard IP block, and transceiver PCS power supply | –C4, –I5, –C5, –C6 | 1.07 | 1.1 | 1.13 | V |
| | | –I3 | 1.12 | 1.15 | 1.18 | V |
| $V_{CCPGM}$ | Configuration pins power supply | 3.3 V | 3.135 | 3.3 | 3.465 | V |
| | | 3.0 V | 2.85 | 3.0 | 3.15 | V |
| | | 2.5 V | 2.375 | 2.5 | 2.625 | V |
| | | 1.8 V | 1.71 | 1.8 | 1.89 | V |
| $V_{CC_AUX}$ | Auxiliary supply | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCBAT}$(2) | Battery back-up power supply (For design security volatile key register) | — | 1.2 | — | 3.0 | V |
| $V_{CCPD}$(3) | I/O pre-driver power supply | 3.3 V | 3.135 | 3.3 | 3.465 | V |
| | | 3.0 V | 2.85 | 3.0 | 3.15 | V |
| | | 2.5 V | 2.375 | 2.5 | 2.625 | V |
| $V_{CCIO}$ | I/O buffers power supply | 3.3 V | 3.135 | 3.3 | 3.465 | V |

*continued...*

(1) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(2) If you do not use the design security feature in Arria V devices, connect $V_{CCBAT}$ to a 1.5-V, 2.5-V, or 3.0-V power supply. Arria V power-on reset (POR) circuitry monitors $V_{CCBAT}$. Arria V devices do not exit POR if $V_{CCBAT}$ is not powered up.

(3) $V_{CCPD}$ must be 2.5 V when $V_{CCIO}$ is 2.5, 1.8, 1.5, 1.35, 1.25, or 1.2 V. $V_{CCPD}$ must be 3.0 V when $V_{CCIO}$ is 3.0 V. $V_{CCPD}$ must be 3.3 V when $V_{CCIO}$ is 3.3 V.

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| Symbol | Description | Condition | Minimum(1) | Typical | Maximum(1) | Unit |
|---|---|---|---|---|---|---|
| | | 3.0 V | 2.85 | 3.0 | 3.15 | V |
| | | 2.5 V | 2.375 | 2.5 | 2.625 | V |
| | | 1.8 V | 1.71 | 1.8 | 1.89 | V |
| | | 1.5 V | 1.425 | 1.5 | 1.575 | V |
| | | 1.35 V | 1.283 | 1.35 | 1.418 | V |
| | | 1.25 V | 1.19 | 1.25 | 1.31 | V |
| | | 1.2 V | 1.14 | 1.2 | 1.26 | V |
| $V_{CCD_FPLL}$ | PLL digital voltage regulator power supply | — | 1.425 | 1.5 | 1.575 | V |
| $V_{CCA_FPLL}$ | PLL analog voltage regulator power supply | — | 2.375 | 2.5 | 2.625 | V |
| $V_I$ | DC input voltage | — | –0.5 | — | 3.6 | V |
| $V_O$ | Output voltage | — | 0 | — | $V_{CCIO}$ | V |
| $T_J$ | Operating junction temperature | Commercial | 0 | — | 85 | °C |
| | | Industrial | –40 | — | 100 | °C |
| $t_{RAMP}$(4) | Power supply ramp time | Standard POR | 200 µs | — | 100 ms | — |
| | | Fast POR | 200 µs | — | 4 ms | — |

(1) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(4) This is also applicable to HPS power supply. For HPS power supply, refer to $t_{RAMP}$ specifications for standard POR when HPS_PORSEL = 0 and $t_{RAMP}$ specifications for fast POR when HPS_PORSEL = 1.

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### 1.1.1.3.2. Transceiver Power Supply Operating Conditions

**Table 4. Transceiver Power Supply Operating Conditions for Arria V Devices**

| Symbol | Description | Minimum(5) | Typical | Maximum(5) | Unit |
|---|---|---|---|---|---|
| $V_{CCA_GXBL}$ | Transceiver high voltage power (left side) | 2.375 | 2.500 | 2.625 | V |
| $V_{CCA_GXBR}$ | Transceiver high voltage power (right side) | | | | |
| $V_{CCR_GXBL}$ | GX and SX speed grades—receiver power (left side) | 1.08/1.12 | 1.1/1.15(6) | 1.14/1.18 | V |
| $V_{CCR_GXBR}$ | GX and SX speed grades—receiver power (right side) | | | | |
| $V_{CCR_GXBL}$ | GT and ST speed grades—receiver power (left side) | 1.17 | 1.20 | 1.23 | V |
| $V_{CCR_GXBR}$ | GT and ST speed grades—receiver power (right side) | | | | |
| $V_{CCT_GXBL}$ | GX and SX speed grades—transmitter power (left side) | 1.08/1.12 | 1.1/1.15(6) | 1.14/1.18 | V |
| $V_{CCT_GXBR}$ | GX and SX speed grades—transmitter power (right side) | | | | |
| $V_{CCT_GXBL}$ | GT and ST speed grades—transmitter power (left side) | 1.17 | 1.20 | 1.23 | V |
| $V_{CCT_GXBR}$ | GT and ST speed grades—transmitter power (right side) | | | | |
| $V_{CCH_GXBL}$ | Transmitter output buffer power (left side) | 1.425 | 1.500 | 1.575 | V |
| $V_{CCH_GXBR}$ | Transmitter output buffer power (right side) | | | | |
| $V_{CCL_GXBL}$ | GX and SX speed grades—clock network power (left side) | 1.08/1.12 | 1.1/1.15(6) | 1.14/1.18 | V |
| $V_{CCL_GXBR}$ | GX and SX speed grades—clock network power (right side) | | | | |
| $V_{CCL_GXBL}$ | GT and ST speed grades—clock network power (left side) | 1.17 | 1.20 | 1.23 | V |
| $V_{CCL_GXBR}$ | GT and ST speed grades—clock network power (right side) | | | | |

(5) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(6) For data rate <=3.2 Gbps, connect $V_{CCR_GXBL/R}$, $V_{CCT_GXBL/R}$, or $V_{CCL_GXBL/R}$ to either 1.1-V or 1.15-V power supply. For data rate >3.2 Gbps, connect $V_{CCR_GXBL/R}$, $V_{CCT_GXBL/R}$, or $V_{CCL_GXBL/R}$ to a 1.15-V power supply. For details, refer to the *Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines*.

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### Related Information

Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines
Provides more information about the power supply connection for different data rates.

## 1.1.1.3.3. HPS Power Supply Operating Conditions

### Table 5. HPS Power Supply Operating Conditions for Arria V SX and ST Devices

This table lists the steady-state voltage and current values expected from Arria V system-on-a-chip (SoC) devices with Arm*-based hard processor system (HPS). Power supply ramps must all be strictly monotonic, without plateaus. Refer to *Recommended Operating Conditions for Arria V Devices* table for the steady-state voltage values expected from the FPGA portion of the Arria V SoC devices.

| Symbol | Description | Condition | Minimum(7) | Typical | Maximum(7) | Unit |
|---|---|---|---|---|---|---|
| $V_{CC_HPS}$ | HPS core voltage and periphery circuitry power supply | –C4, –I5, –C5, –C6 | 1.07 | 1.1 | 1.13 | V |
| | | –I3 | 1.12 | 1.15 | 1.18 | V |
| $V_{CCPD_HPS}$ (8) | HPS I/O pre-driver power supply | 3.3 V | 3.135 | 3.3 | 3.465 | V |
| | | 3.0 V | 2.85 | 3.0 | 3.15 | V |
| | | 2.5 V | 2.375 | 2.5 | 2.625 | V |
| $V_{CCIO_HPS}$ | HPS I/O buffers power supply | 3.3 V | 3.135 | 3.3 | 3.465 | V |
| | | 3.0 V | 2.85 | 3.0 | 3.15 | V |
| | | 2.5 V | 2.375 | 2.5 | 2.625 | V |
| | | 1.8 V | 1.71 | 1.8 | 1.89 | V |
| | | 1.5 V | 1.425 | 1.5 | 1.575 | V |
| | | 1.35 V (9) | 1.283 | 1.35 | 1.418 | V |

*continued...*

(7) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(8) $V_{CCPD_HPS}$ must be 2.5 V when $V_{CCIO_HPS}$ is 2.5, 1.8, 1.5, or 1.2 V. $V_{CCPD_HPS}$ must be 3.0 V when $V_{CCIO_HPS}$ is 3.0 V. $V_{CCPD_HPS}$ must be 3.3 V when $V_{CCIO_HPS}$ is 3.3 V.

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| Symbol | Description | Condition | Minimum(7) | Typical | Maximum(7) | Unit |
|---|---|---|---|---|---|---|
| | | 1.2 V | 1.14 | 1.2 | 1.26 | V |
| $V_{CCRSTCLK_HPS}$ | HPS reset and clock input pins power supply | 3.3 V | 3.135 | 3.3 | 3.465 | V |
| | | 3.0 V | 2.85 | 3.0 | 3.15 | V |
| | | 2.5 V | 2.375 | 2.5 | 2.625 | V |
| | | 1.8 V | 1.71 | 1.8 | 1.89 | V |
| $V_{CCPLL_HPS}$ | HPS PLL analog voltage regulator power supply | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CC_AUX_SHARED}$ | HPS auxiliary power supply | — | 2.375 | 2.5 | 2.625 | V |

**Related Information**

Recommended Operating Conditions on page 8
Provides the steady-state voltage values for the FPGA portion of the device.

## 1.1.1.4. DC Characteristics

### 1.1.1.4.1. Supply Current and Power Consumption

Intel offers two ways to estimate power for your design—the Excel-based Early Power Estimator (EPE) and the Intel® Quartus® Prime Power Analyzer feature.

Use the Excel-based EPE before you start your design to estimate the supply current for your design. The EPE provides a magnitude estimate of the device power because these currents vary greatly with the resources you use.

(7) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(9) $V_{CCIO_HPS}$ 1.35 V is supported for HPS row I/O bank only.

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The Intel Quartus Prime Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

**Related Information**

- Early Power Estimator User Guide
  Provides more information about power estimation tools.
- Power Analysis chapter, Intel Quartus Prime Handbook
  Provides more information about power estimation tools.

### 1.1.1.4.2. I/O Pin Leakage Current

**Table 6. I/O Pin Leakage Current for Arria V Devices**

| Symbol | Description | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_I$ | Input pin | $V_I$ = 0 V to $V_{CCIOMAX}$ | –30 | — | 30 | µA |
| $I_{OZ}$ | Tri-stated I/O pin | $V_O$ = 0 V to $V_{CCIOMAX}$ | –30 | — | 30 | µA |

### 1.1.1.4.3. Bus Hold Specifications

**Table 7. Bus Hold Parameters for Arria V Devices**

The bus-hold trip points are based on calculated input voltages from the JEDEC* standard.

| Parameter | Symbol | Condition | $V_{CCIO}$ (V) | | | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.2 | | 1.5 | | 1.8 | | 2.5 | | 3.0 | | 3.3 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Bus-hold, low, sustaining current | $I_{SUSL}$ | $V_{IN} > V_{IL}$ (max) | 8 | — | 12 | — | 30 | — | 50 | — | 70 | — | 70 | — | µA |
| Bus-hold, high, sustaining current | $I_{SUSH}$ | $V_{IN} < V_{IH}$ (min) | –8 | — | –12 | — | –30 | — | –50 | — | –70 | — | –70 | — | µA |

*continued...*

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| Parameter | Symbol | Condition | $V_{CCIO}$ (V) | | | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.2 | | 1.5 | | 1.8 | | 2.5 | | 3.0 | | 3.3 | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Bus-hold, low, overdrive current | $I_{ODL}$ | 0 V < $V_{IN}$ < $V_{CCIO}$ | — | 125 | — | 175 | — | 200 | — | 300 | — | 500 | — | 500 | µA |
| Bus-hold, high, overdrive current | $I_{ODH}$ | 0 V <$V_{IN}$ <$V_{CCIO}$ | — | –125 | — | –175 | — | –200 | — | –300 | — | –500 | — | –500 | µA |
| Bus-hold trip point | $V_{TRIP}$ | — | 0.3 | 0.9 | 0.375 | 1.125 | 0.68 | 1.07 | 0.7 | 1.7 | 0.8 | 2 | 0.8 | 2 | V |

### 1.1.1.4.4. OCT Calibration Accuracy Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.

**Table 8. OCT Calibration Accuracy Specifications for Arria V Devices**

Calibration accuracy for the calibrated on-chip series termination ($R_S$ OCT) and on-chip parallel termination ($R_T$ OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

| Symbol | Description | Condition (V) | Calibration Accuracy | | | Unit |
|---|---|---|---|---|---|---|
| | | | –I3, –C4 | –I5, –C5 | –C6 | |
| 25-Ω $R_S$ | Internal series termination with calibration (25-Ω setting) | $V_{CCIO}$ = 3.0, 2.5, 1.8, 1.5, 1.2 | ±15 | ±15 | ±15 | % |
| 50-Ω $R_S$ | Internal series termination with calibration (50-Ω setting) | $V_{CCIO}$ = 3.0, 2.5, 1.8, 1.5, 1.2 | ±15 | ±15 | ±15 | % |
| 34-Ω and 40-Ω $R_S$ | Internal series termination with calibration (34-Ω and 40-Ω setting) | $V_{CCIO}$ = 1.5, 1.35, 1.25, 1.2 | ±15 | ±15 | ±15 | % |
| 48-Ω, 60-Ω, and 80-Ω $R_S$ | Internal series termination with calibration (48-Ω, 60-Ω, and 80-Ω setting) | $V_{CCIO}$ = 1.2 | ±15 | ±15 | ±15 | % |
| 50-Ω $R_T$ | Internal parallel termination with calibration (50-Ω setting) | $V_{CCIO}$ = 2.5, 1.8, 1.5, 1.2 | –10 to +40 | –10 to +40 | –10 to +40 | % |

*continued...*

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| Symbol | Description | Condition (V) | Calibration Accuracy | | | Unit |
|---|---|---|---|---|---|---|
| | | | –I3, –C4 | –I5, –C5 | –C6 | |
| 20-Ω, 30-Ω, 40-Ω,60-Ω, and 120-Ω $R_T$ | Internal parallel termination with calibration (20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω setting) | $V_{CCIO}$ = 1.5, 1.35, 1.25 | –10 to +40 | –10 to +40 | –10 to +40 | % |
| 60-Ω and 120-Ω $R_T$ | Internal parallel termination with calibration (60-Ω and 120-Ω setting) | $V_{CCIO}$ = 1.2 | –10 to +40 | –10 to +40 | –10 to +40 | % |
| 25-Ω $R_{S_left_shift}$ | Internal left shift series termination with calibration (25-Ω $R_{S_left_shift}$ setting) | $V_{CCIO}$ = 3.0, 2.5, 1.8, 1.5, 1.2 | ±15 | ±15 | ±15 | % |

### 1.1.1.4.5. OCT Without Calibration Resistance Tolerance Specifications

**Table 9. OCT Without Calibration Resistance Tolerance Specifications for Arria V Devices**

This table lists the Arria V OCT without calibration resistance tolerance to PVT changes.

| Symbol | Description | Condition (V) | Resistance Tolerance | | | Unit |
|---|---|---|---|---|---|---|
| | | | –I3, –C4 | –I5, –C5 | –C6 | |
| 25-Ω $R_S$ | Internal series termination without calibration (25-Ω setting) | $V_{CCIO}$ = 3.0, 2.5 | ±30 | ±40 | ±40 | % |
| 25-Ω $R_S$ | Internal series termination without calibration (25-Ω setting) | $V_{CCIO}$ = 1.8, 1.5 | ±30 | ±40 | ±40 | % |
| 25-Ω $R_S$ | Internal series termination without calibration (25-Ω setting) | $V_{CCIO}$ = 1.2 | ±35 | ±50 | ±50 | % |
| 50-Ω $R_S$ | Internal series termination without calibration (50-Ω setting) | $V_{CCIO}$ = 3.0, 2.5 | ±30 | ±40 | ±40 | % |
| 50-Ω $R_S$ | Internal series termination without calibration (50-Ω setting) | $V_{CCIO}$ = 1.8, 1.5 | ±30 | ±40 | ±40 | % |
| 50-Ω $R_S$ | Internal series termination without calibration (50-Ω setting) | $V_{CCIO}$ = 1.2 | ±35 | ±50 | ±50 | % |
| 100-Ω $R_D$ | Internal differential termination (100-Ω setting) | $V_{CCIO}$ = 2.5 | ±25 | ±40 | ±40 | % |

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**Figure 2. Equation for OCT Variation Without Recalibration**

$$R_{OCT} = R_{SCAL}\left(1 + \left\langle \frac{dR}{dT} \times \Delta T \right\rangle \pm \left\langle \frac{dR}{dV} \times \Delta V \right\rangle\right)$$

The definitions for the equation are as follows:

- The $R_{OCT}$ value calculated shows the range of OCT resistance with the variation of temperature and $V_{CCIO}$.
- $R_{SCAL}$ is the OCT resistance value at power-up.
- ΔT is the variation of temperature with respect to the temperature at power up.
- ΔV is the variation of voltage with respect to the $V_{CCIO}$ at power up.
- dR/dT is the percentage change of $R_{SCAL}$ with temperature.
- dR/dV is the percentage change of $R_{SCAL}$ with voltage.

### 1.1.1.4.6. OCT Variation after Power-Up Calibration

**Table 10. OCT Variation after Power-Up Calibration for Arria V Devices**

This table lists OCT variation with temperature and voltage after power-up calibration. The OCT variation is valid for a $V_{CCIO}$ range of ±5% and a temperature range of 0°C to 85°C.

| Symbol | Description | $V_{CCIO}$ (V) | Value | Unit |
|---|---|---|---|---|
| dR/dV | OCT variation with voltage without recalibration | 3.0 | 0.100 | %/mV |
| | | 2.5 | 0.100 | |
| | | 1.8 | 0.100 | |
| | | 1.5 | 0.100 | |
| | | 1.35 | 0.150 | |
| | | 1.25 | 0.150 | |
| | | 1.2 | 0.150 | |
| dR/dT | OCT variation with temperature without recalibration | 3.0 | 0.189 | %/°C |
| | | 2.5 | 0.208 | |

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| Symbol | Description | $V_{CCIO}$ (V) | Value | Unit |
|---|---|---|---|---|
| | | 1.8 | 0.266 | |
| | | 1.5 | 0.273 | |
| | | 1.35 | 0.200 | |
| | | 1.25 | 0.200 | |
| | | 1.2 | 0.317 | |

### 1.1.1.4.7. Pin Capacitance

**Table 11. Pin Capacitance for Arria V Devices**

| Symbol | Description | Maximum | Unit |
|---|---|---|---|
| $C_{IOTB}$ | Input capacitance on top/bottom I/O pins | 6 | pF |
| $C_{IOLR}$ | Input capacitance on left/right I/O pins | 6 | pF |
| $C_{OUTFB}$ | Input capacitance on dual-purpose clock output/feedback pins | 6 | pF |
| $C_{IOVREF}$ | Input capacitance on $V_{REF}$ pins | 48 | pF |

### 1.1.1.4.8. Hot Socketing

**Table 12. Hot Socketing Specifications for Arria V Devices**

| Symbol | Description | Maximum | Unit |
|---|---|---|---|
| $I_{IOPIN\ (DC)}$ | DC current per I/O pin | 300 | µA |
| $I_{IOPIN\ (AC)}$ | AC current per I/O pin | 8(10) | mA |
| $I_{XCVR\text{-}TX\ (DC)}$ | DC current per transceiver transmitter (TX) pin | 100 | mA |
| $I_{XCVR\text{-}RX\ (DC)}$ | DC current per transceiver receiver (RX) pin | 50 | mA |

(10) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}|$ = C dv/dt, in which C is the I/O pin capacitance and dv/dt is the slew rate.

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### 1.1.1.4.9. Internal Weak Pull-Up Resistor

All I/O pins, except configuration, test, and JTAG pins, have an option to enable weak pull-up.

**Table 13. Internal Weak Pull-Up Resistor Values for Arria V Devices**

| Symbol | Description | Condition (V)[11] | Value[12] | Unit |
|---|---|---|---|---|
| $R_{PU}$ | Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you have enabled the programmable pull-up resistor option. | $V_{CCIO}$ = 3.3 ±5% | 25 | kΩ |
| | | $V_{CCIO}$ = 3.0 ±5% | 25 | kΩ |
| | | $V_{CCIO}$ = 2.5 ±5% | 25 | kΩ |
| | | $V_{CCIO}$ = 1.8 ±5% | 25 | kΩ |
| | | $V_{CCIO}$ = 1.5 ±5% | 25 | kΩ |
| | | $V_{CCIO}$ = 1.35 ±5% | 25 | kΩ |
| | | $V_{CCIO}$ = 1.25 ±5% | 25 | kΩ |
| | | $V_{CCIO}$ = 1.2 ±5% | 25 | kΩ |

**Related Information**

Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines
Provides more information about the pins that support internal weak pull-up and internal weak pull-down features.

## 1.1.1.5. I/O Standard Specifications

Tables in this section list the input voltage ($V_{IH}$ and $V_{IL}$), output voltage ($V_{OH}$ and $V_{OL}$), and current drive characteristics ($I_{OH}$ and $I_{OL}$) for various I/O standards supported by Arria V devices.

You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.

(11) Pin pull-up resistance values may be lower if an external source drives the pin higher than $V_{CCIO}$.

(12) Valid with ±10% tolerances to cover changes over PVT.

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### 1.1.1.5.1. Single-Ended I/O Standards

**Table 14. Single-Ended I/O Standards for Arria V Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{IL}$ (V) | | $V_{IH}$ (V) | | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{OL}$[13] (mA) | $I_{OH}$[13] (mA) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Max | Max | Min | | |
| 3.3-V LVTTL | 3.135 | 3.3 | 3.465 | –0.3 | 0.8 | 1.7 | 3.6 | 0.45 | 2.4 | 4 | –4 |
| 3.3-V LVCMOS | 3.135 | 3.3 | 3.465 | –0.3 | 0.8 | 1.7 | 3.6 | 0.2 | $V_{CCIO}$ – 0.2 | 2 | –2 |
| 3.0-V LVTTL | 2.85 | 3 | 3.15 | –0.3 | 0.8 | 1.7 | 3.6 | 0.4 | 2.4 | 2 | –2 |
| 3.0-V LVCMOS | 2.85 | 3 | 3.15 | –0.3 | 0.8 | 1.7 | 3.6 | 0.2 | $V_{CCIO}$ – 0.2 | 0.1 | –0.1 |
| 3.0-V PCI* | 2.85 | 3 | 3.15 | — | 0.3 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.1 × $V_{CCIO}$ | 0.9 × $V_{CCIO}$ | 1.5 | –0.5 |
| 3.0-V PCI-X | 2.85 | 3 | 3.15 | — | 0.35 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.1 × $V_{CCIO}$ | 0.9 × $V_{CCIO}$ | 1.5 | –0.5 |
| 2.5 V | 2.375 | 2.5 | 2.625 | –0.3 | 0.7 | 1.7 | 3.6 | 0.4 | 2 | 1 | –1 |
| 1.8 V | 1.71 | 1.8 | 1.89 | –0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.45 | $V_{CCIO}$ – 0.45 | 2 | –2 |
| 1.5 V | 1.425 | 1.5 | 1.575 | –0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 2 | –2 |
| 1.2 V | 1.14 | 1.2 | 1.26 | –0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 2 | –2 |

### 1.1.1.5.2. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications

**Table 15. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Arria V Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{REF}$ (V) | | | $V_{TT}$ (V) | | |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| SSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |

*continued...*

(13) To meet the $I_{OL}$ and $I_{OH}$ specifications, you must set the current strength settings accordingly. For example, to meet the 3.3-V LVTTL specification (4 mA), you should set the current strength settings to 4 mA. Setting at lower current strength may not meet the $I_{OL}$ and $I_{OH}$ specifications in the datasheet.

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| I/O Standard | $V_{CCIO}$ (V) | | | $V_{REF}$ (V) | | | $V_{TT}$ (V) | | |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ |
| SSTL-135 Class I, II | 1.283 | 1.35 | 1.418 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ |
| SSTL-125 Class I, II | 1.19 | 1.25 | 1.26 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.85 | 0.9 | 0.95 | — | $V_{CCIO}$/2 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.68 | 0.75 | 0.9 | — | $V_{CCIO}$/2 | — |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.47 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.53 × $V_{CCIO}$ | — | $V_{CCIO}$/2 | — |
| HSUL-12 | 1.14 | 1.2 | 1.3 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | — | — | — |

### 1.1.1.5.3. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications

**Table 16. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Arria V Devices**

| I/O Standard | $V_{IL(DC)}$ (V) | | $V_{IH(DC)}$ (V) | | $V_{IL(AC)}$ (V) | $V_{IH(AC)}$ (V) | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{OL}$[14] (mA) | $I_{OH}$[14] (mA) |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Max | Min | Max | Min | | |
| SSTL-2 Class I | –0.3 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.31 | $V_{REF}$ + 0.31 | $V_{TT}$ – 0.608 | $V_{TT}$ + 0.608 | 8.1 | –8.1 |
| SSTL-2 Class II | –0.3 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.31 | $V_{REF}$ + 0.31 | $V_{TT}$ – 0.81 | $V_{TT}$ + 0.81 | 16.2 | –16.2 |
| SSTL-18 Class I | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.25 | $V_{REF}$ + 0.25 | $V_{TT}$ – 0.603 | $V_{TT}$ + 0.603 | 6.7 | –6.7 |
| SSTL-18 Class II | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.25 | $V_{REF}$ + 0.25 | 0.28 | $V_{CCIO}$ – 0.28 | 13.4 | –13.4 |

*continued...*

(14) To meet the $I_{OL}$ and $I_{OH}$ specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the $I_{OL}$ and $I_{OH}$ specifications in the datasheet.

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| I/O Standard | $V_{IL(DC)}$ (V) | | $V_{IH(DC)}$ (V) | | $V_{IL(AC)}$ (V) | $V_{IH(AC)}$ (V) | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{OL}$[14] (mA) | $I_{OH}$[14] (mA) |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Max | Min | Max | Min | | |
| SSTL-15 Class I | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.175 | $V_{REF}$ + 0.175 | 0.2 × $V_{CCIO}$ | 0.8 × $V_{CCIO}$ | 8 | –8 |
| SSTL-15 Class II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.175 | $V_{REF}$ + 0.175 | 0.2 × $V_{CCIO}$ | 0.8 × $V_{CCIO}$ | 16 | –16 |
| SSTL-135 | — | $V_{REF}$ – 0.09 | $V_{REF}$ + 0.09 | — | $V_{REF}$ – 0.16 | $V_{REF}$ + 0.16 | 0.2 × $V_{CCIO}$ | 0.8 × $V_{CCIO}$ | — | — |
| SSTL-125 | — | $V_{REF}$ – 0.85 | $V_{REF}$ + 0.85 | — | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 0.2 × $V_{CCIO}$ | 0.8 × $V_{CCIO}$ | — | — |
| HSTL-18 Class I | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ – 0.4 | 8 | –8 |
| HSTL-18 Class II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ – 0.4 | 16 | –16 |
| HSTL-15 Class I | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ – 0.4 | 8 | –8 |
| HSTL-15 Class II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ – 0.4 | 16 | –16 |
| HSTL-12 Class I | –0.15 | $V_{REF}$ – 0.08 | $V_{REF}$ + 0.08 | $V_{CCIO}$ + 0.15 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 8 | –8 |
| HSTL-12 Class II | –0.15 | $V_{REF}$ – 0.08 | $V_{REF}$ + 0.08 | $V_{CCIO}$+ 0.15 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 16 | –16 |
| HSUL-12 | — | $V_{REF}$ – 0.13 | $V_{REF}$ + 0.13 | — | $V_{REF}$ – 0.22 | $V_{REF}$ + 0.22 | 0.1 × $V_{CCIO}$ | 0.9 × $V_{CCIO}$ | — | — |

(14) To meet the $I_{OL}$ and $I_{OH}$ specifications, you must set the current strength settings accordingly. For example, to meet the SSTL15CI specification (8 mA), you should set the current strength settings to 8 mA. Setting at lower current strength may not meet the $I_{OL}$ and $I_{OH}$ specifications in the datasheet.

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### 1.1.1.5.4. Differential SSTL I/O Standards

**Table 17. Differential SSTL I/O Standards for Arria V Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{SWING(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{SWING(AC)}$ (V) | |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 0.3 | $V_{CCIO}$ + 0.6 | $V_{CCIO}/2$ – 0.2 | — | $V_{CCIO}/2$ + 0.2 | 0.62 | $V_{CCIO}$ + 0.6 |
| SSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.25 | $V_{CCIO}$ + 0.6 | $V_{CCIO}/2$ – 0.175 | — | $V_{CCIO}/2$ + 0.175 | 0.5 | $V_{CCIO}$ + 0.6 |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | (15) | $V_{CCIO}/2$ – 0.15 | — | $V_{CCIO}/2$ + 0.15 | $2(V_{IH(AC)} – V_{REF})$ | $2(V_{IL(AC)} – V_{REF})$ |
| SSTL-135 | 1.283 | 1.35 | 1.45 | 0.18 | (15) | $V_{CCIO}/2$ – 0.15 | $V_{CCIO}/2$ | $V_{CCIO}/2$ + 0.15 | $2(V_{IH(AC)} – V_{REF})$ | $2(V_{IL(AC)} – V_{REF})$ |
| SSTL-125 | 1.19 | 1.25 | 1.31 | 0.18 | (15) | $V_{CCIO}/2$ – 0.15 | $V_{CCIO}/2$ | $V_{CCIO}/2$ + 0.15 | $2(V_{IH(AC)} – V_{REF})$ | $2(V_{IL(AC)} – V_{REF})$ |

### 1.1.1.5.5. Differential HSTL and HSUL I/O Standards

**Table 18. Differential HSTL and HSUL I/O Standards for Arria V Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{DIF(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{CM(DC)}$ (V) | | | $V_{DIF(AC)}$ (V) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Typ | Max | Min | Max |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.2 | — | 0.78 | — | 1.12 | 0.78 | — | 1.12 | 0.4 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | — | 0.68 | — | 0.9 | 0.68 | — | 0.9 | 0.4 | — |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.16 | $V_{CCIO}$ + 0.3 | — | 0.5 × $V_{CCIO}$ | — | 0.4 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.6 × $V_{CCIO}$ | 0.3 | $V_{CCIO}$ + 0.48 |
| HSUL-12 | 1.14 | 1.2 | 1.3 | 0.26 | 0.26 | 0.5 × $V_{CCIO}$ – 0.12 | 0.5 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ + 0.12 | 0.4 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.6 × $V_{CCIO}$ | 0.44 | 0.44 |

(15) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

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### 1.1.1.5.6. Differential I/O Standard Specifications

**Table 19. Differential I/O Standard Specifications for Arria V Devices**

Differential inputs are powered by $V_{CCPD}$ which requires 2.5 V.

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{ID}$ (mV)(16) | | | $V_{ICM(DC)}$ (V) | | | $V_{OD}$ (V)(17) | | | $V_{OCM}$ (V)(17)(18) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Condition | Max | Min | Condition | Max | Min | Typ | Max | Min | Typ | Max |
| PCML | Transmitter, receiver, and input reference clock pins of high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to *Transceiver Specifications for Arria V GX and SX Devices* and *Transceiver Specifications for Arria V GT and ST Devices* tables. | | | | | | | | | | | | | | |
| 2.5 V LVDS(19) | 2.375 | 2.5 | 2.625 | 100 | $V_{CM}$ = 1.25 V | — | 0.05 | $D_{MAX}$ ≤ 1.25 Gbps | 1.80 | 0.247 | — | 0.6 | 1.125 | 1.25 | 1.375 |
| | | | | | | — | 1.05 | $D_{MAX}$ > 1.25 Gbps | 1.55 | | | | | | |
| RSDS (HIO)(20) | 2.375 | 2.5 | 2.625 | 100 | $V_{CM}$ = 1.25 V | — | 0.25 | — | 1.45 | 0.1 | 0.2 | 0.6 | 0.5 | 1.2 | 1.4 |

*continued...*

(16) The minimum $V_{ID}$ value is applicable over the entire common mode range, $V_{CM}$.

(17) $R_L$ range: 90 ≤ $R_L$ ≤ 110 Ω.

(18) This applies to default pre-emphasis setting only.

(19) For optimized LVDS receiver performance, the receiver voltage input range must be within 1.0 V to 1.6 V for data rates above 1.25 Gbps and 0 V to 1.85 V for data rates below 1.25 Gbps.

(20) For optimized RSDS receiver performance, the receiver voltage input range must be within 0.25 V to 1.45 V.

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| I/O Standard | $V_{CCIO}$ (V) | | | $V_{ID}$ (mV)(16) | | | $V_{ICM(DC)}$ (V) | | | $V_{OD}$ (V)(17) | | | $V_{OCM}$ (V)(17)(18) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Condition | Max | Min | Condition | Max | Min | Typ | Max | Min | Typ | Max |
| Mini-LVDS (HIO) (21) | 2.375 | 2.5 | 2.625 | 200 | — | 600 | 0.300 | — | 1.425 | 0.25 | — | 0.6 | 1 | 1.2 | 1.4 |
| LVPECL(22) | — | — | — | 300 | — | — | 0.60 | $D_{MAX}$ ≤ 700 Mbps | 1.80 | — | — | — | — | — | — |
| | | | | | | | 1.00 | $D_{MAX}$ > 700 Mbps | 1.60 | | | | | | |

**Related Information**

- Transceiver Specifications for Arria V GX and SX Devices on page 25
  Provides the specifications for transmitter, receiver, and reference clock I/O pin.
- Transceiver Specifications for Arria V GT and ST Devices on page 30
  Provides the specifications for transmitter, receiver, and reference clock I/O pin.

## 1.2. Switching Characteristics

This section provides performance characteristics of Arria V core and periphery blocks.

(16) The minimum $V_{ID}$ value is applicable over the entire common mode range, $V_{CM}$.
(17) $R_L$ range: 90 ≤ $R_L$ ≤ 110 Ω.
(18) This applies to default pre-emphasis setting only.

(21) For optimized Mini-LVDS receiver performance, the receiver voltage input range must be within 0.3 V to 1.425 V.

(22) For optimized LVPECL receiver performance, the receiver voltage input range must be within 0.85 V to 1.75 V for data rates above 700 Mbps and 0.45 V to 1.95 V for data rates below 700 Mbps.

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## 1.2.1. Transceiver Performance Specifications

### 1.2.1.1. Transceiver Specifications for Arria V GX and SX Devices

**Table 20. Reference Clock Specifications for Arria V GX and SX Devices**

| Symbol/Description | Condition | Transceiver Speed Grade 4 | | | Transceiver Speed Grade 6 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Supported I/O standards | 1.2 V PCML, 1.4 V PCML,1.5 V PCML, 2.5 V PCML, Differential LVPECL(23), HCSL, and LVDS | | | | | | | |
| Input frequency from REFCLK input pins | — | 27 | — | 710 | 27 | — | 710 | MHz |
| Rise time | Measure at ±60 mV of differential signal(24) | — | — | 400 | — | — | 400 | ps |
| Fall time | Measure at ±60 mV of differential signal(24) | — | — | 400 | — | — | 400 | ps |
| Duty cycle | — | 45 | — | 55 | 45 | — | 55 | % |
| Peak-to-peak differential input voltage | — | 200 | — | 300(25)/ 2000 | 200 | — | 300(25)/ 2000 | mV |
| Spread-spectrum modulating clock frequency | PCIe | 30 | — | 33 | 30 | — | 33 | kHz |
| Spread-spectrum downspread | PCIe | — | 0 to –0.5% | — | — | 0 to –0.5% | — | — |
| On-chip termination resistors | — | — | 100 | — | — | 100 | — | Ω |
| $V_{ICM}$ (AC coupled) | — | — | 1.1/1.15(26) | — | — | 1.1/1.15(26) | — | V |

*continued...*

(23) Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.

(24) REFCLK performance requires to meet transmitter REFCLK phase noise specification.

(25) The maximum peak-to peak differential input voltage of 300 mV is allowed for DC coupled link.

(26) For data rate ≤3.2 Gbps, connect $V_{CCR_GXBL/R}$ to either 1.1-V or 1.15-V power supply. For data rate >3.2 Gbps, connect $V_{CCR_GXBL/R}$ to a 1.15-V power supply. For details, refer to the *Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines*.

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| Symbol/Description | Condition | Transceiver Speed Grade 4 | | | Transceiver Speed Grade 6 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| $V_{ICM}$ (DC coupled) | HCSL I/O standard for the PCIe reference clock | 250 | — | 550 | 250 | — | 550 | mV |
| Transmitter REFCLK phase noise(27) | 10 Hz | — | — | –50 | — | — | –50 | dBc/Hz |
| | 100 Hz | — | — | –80 | — | — | –80 | dBc/Hz |
| | 1 KHz | — | — | –110 | — | — | –110 | dBc/Hz |
| | 10 KHz | — | — | –120 | — | — | –120 | dBc/Hz |
| | 100 KHz | — | — | –120 | — | — | –120 | dBc/Hz |
| | ≥1 MHz | — | — | –130 | — | — | –130 | dBc/Hz |
| $R_{REF}$ | — | — | 2000 ±1% | — | — | 2000 ±1% | — | Ω |

## Table 21. Transceiver Clocks Specifications for Arria V GX and SX Devices

| Symbol/Description | Condition | Transceiver Speed Grade 4 | | | Transceiver Speed Grade 6 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| `fixedclk` clock frequency | PCIe Receiver Detect | — | 125 | — | — | 125 | — | MHz |
| Transceiver Reconfiguration Controller Intel FPGA IP (`mgmt_clk_clk`) clock frequency | — | 75 | — | 125 | 75 | — | 125 | MHz |

## Table 22. Receiver Specifications for Arria V GX and SX Devices

| Symbol/Description | Condition | Transceiver Speed Grade 4 | | | Transceiver Speed Grade 6 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Supported I/O standards | 1.5 V PCML, 2.5 V PCML, LVPECL, and LVDS | | | | | | | |
| Data rate(28) | — | 611 | — | 6553.6 | 611 | — | 3125 | Mbps |

*continued...*

(27) The transmitter REFCLK phase jitter is 30 ps p-p at bit error rate (BER) $10^{-12}$.

(28) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

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| Symbol/Description | Condition | Transceiver Speed Grade 4 | | | Transceiver Speed Grade 6 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Absolute $V_{MAX}$ for a receiver pin(29) | — | — | — | 1.2 | — | — | 1.2 | V |
| Absolute $V_{MIN}$ for a receiver pin | — | –0.4 | — | — | –0.4 | — | — | V |
| Maximum peak-to-peak differential input voltage $V_{ID}$ (diff p-p) before device configuration | — | — | — | 1.6 | — | — | 1.6 | V |
| Maximum peak-to-peak differential input voltage $V_{ID}$ (diff p-p) after device configuration | — | — | — | 2.2 | — | — | 2.2 | V |
| Minimum differential eye opening at the receiver serial input pins(30) | — | 100 | — | — | 100 | — | — | mV |
| $V_{ICM}$ (AC coupled) | — | — | 0.7/0.75/0.8 (31) | — | — | 0.7/0.75/0.8 (31) | — | mV |
| $V_{ICM}$ (DC coupled) | ≤ 3.2Gbps(32) | 670 | 700 | 730 | 670 | 700 | 730 | mV |
| Differential on-chip termination resistors | 85-Ω setting | — | 85 | — | — | 85 | — | Ω |
| | 100-Ω setting | — | 100 | — | — | 100 | — | Ω |
| | 120-Ω setting | — | 120 | — | — | 120 | — | Ω |
| | 150-Ω setting | — | 150 | — | — | 150 | — | Ω |

***continued...***

(29) The device cannot tolerate prolonged operation at this absolute maximum.

(30) The differential eye opening specification at the receiver input pins assumes that you have disabled the **Receiver Equalization** feature. If you enable the **Receiver Equalization** feature, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(31) The AC coupled $V_{ICM}$ = 700 mV for Arria V GX and SX in PCIe mode only. The AC coupled $V_{ICM}$ = 750 mV for Arria V GT and ST in PCIe mode only.

(32) For standard protocol compliance, use AC coupling.

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| Symbol/Description | Condition | Transceiver Speed Grade 4 | | | Transceiver Speed Grade 6 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| $t_{LTR}$(33) | — | — | — | 10 | — | — | 10 | µs |
| $t_{LTD}$(34) | — | 4 | — | — | 4 | — | — | µs |
| $t_{LTD_manual}$(35) | — | 4 | — | — | 4 | — | — | µs |
| $t_{LTR_LTD_manual}$(36) | — | 15 | — | — | 15 | — | — | µs |
| Programmable ppm detector(37) | — | ±62.5, 100, 125, 200, 250, 300, 500, and 1000 | | | | | | ppm |
| Run length | — | — | — | 200 | — | — | 200 | UI |
| Programmable equalization AC and DC gain | AC gain setting = 0 to 3(38)<br>DC gain setting = 0 to 1 | Refer to *CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices* and *CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices* diagrams. | | | | | | dB |

## Table 23. Transmitter Specifications for Arria V GX and SX Devices

| Symbol/Description | Condition | Transceiver Speed Grade 4 | | | Transceiver Speed Grade 6 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Supported I/O standards | 1.5 V PCML | | | | | | | |
| Data rate | — | 611 | — | 6553.6 | 611 | — | 3125 | Mbps |

*continued...*

(33) $t_{LTR}$ is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

(34) $t_{LTD}$ is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high.

(35) $t_{LTD_manual}$ is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high when the CDR is functioning in the manual mode.

(36) $t_{LTR_LTD_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedtoref` signal goes high when the CDR is functioning in the manual mode.

(37) The rate match FIFO supports only up to ±300 parts per million (ppm).

(38) The Intel Quartus Prime software allows AC gain setting = 3 for design with data rate between 611 Mbps and 1.25 Gbps only.

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| Symbol/Description | Condition | Transceiver Speed Grade 4 | | | Transceiver Speed Grade 6 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| $V_{OCM}$ (AC coupled) | — | — | 650 | — | — | 650 | — | mV |
| $V_{OCM}$ (DC coupled) | ≤ 3.2Gbps(32) | 670 | 700 | 730 | 670 | 700 | 730 | mV |
| Differential on-chip termination resistors | 85-Ω setting | — | 85 | — | — | 85 | — | Ω |
| | 100-Ω setting | — | 100 | — | — | 100 | — | Ω |
| | 120-Ω setting | — | 120 | — | — | 120 | — | Ω |
| | 150-Ω setting | — | 150 | — | — | 150 | — | Ω |
| Intra-differential pair skew | TX $V_{CM}$ = 0.65 V (AC coupled) and slew rate of 15 ps | — | — | 15 | — | — | 15 | ps |
| Intra-transceiver block transmitter channel-to-channel skew | ×6 PMA bonded mode | — | — | 180 | — | — | 180 | ps |
| Inter-transceiver block transmitter channel-to-channel skew(39) | ×*N* PMA bonded mode | — | — | 500 | — | — | 500 | ps |

## Table 24. CMU PLL Specifications for Arria V GX and SX Devices

| Symbol/Description | Transceiver Speed Grade 4 | | Transceiver Speed Grade 6 | | Unit |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| Supported data range | 611 | 6553.6 | 611 | 3125 | Mbps |
| fPLL supported data range | 611 | 3125 | 611 | 3125 | Mbps |

## Table 25. Transceiver-FPGA Fabric Interface Specifications for Arria V GX and SX Devices

| Symbol/Description | Transceiver Speed Grade 4 and 6 | | Unit |
|---|---|---|---|
| | Min | Max | |
| Interface speed (single-width mode) | 25 | 187.5 | MHz |
| Interface speed (double-width mode) | 25 | 163.84 | MHz |

(39) This specification is only applicable to channels on one side of the device across two transceiver banks.

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**Related Information**

- CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain on page 36
- CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain on page 37
- Arria V GT, GX, ST, and SX Device Family Pin Connection Guidelines
  Provides more information about the power supply connection for different data rates.

### 1.2.1.2. Transceiver Specifications for Arria V GT and ST Devices

**Table 26. Reference Clock Specifications for Arria V GT and ST Devices**

| Symbol/Description | Condition | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Supported I/O standards | 1.2 V PCML, 1.4 VPCML, 1.5 V PCML, 2.5 V PCML, Differential LVPECL(40), HCSL, and LVDS | | | | |
| Input frequency from REFCLK input pins | — | 27 | — | 710 | MHz |
| Rise time | Measure at ±60 mV of differential signal(41) | — | — | 400 | ps |
| Fall time | Measure at ±60 mV of differential signal(41) | — | — | 400 | ps |
| Duty cycle | — | 45 | — | 55 | % |
| Peak-to-peak differential input voltage | — | 200 | — | 300(42)/2000 | mV |
| Spread-spectrum modulating clock frequency | PCIe | 30 | — | 33 | kHz |
| Spread-spectrum downspread | PCIe | — | 0 to –0.5% | — | — |
| On-chip termination resistors | — | — | 100 | — | Ω |
| $V_{ICM}$ (AC coupled) | — | — | 1.2 | — | V |

*continued...*

(40) Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.

(41) REFCLK performance requires to meet transmitter REFCLK phase noise specification.

(42) The maximum peak-to peak differential input voltage of 300 mV is allowed for DC coupled link.

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| Symbol/Description | Condition | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{ICM}$ (DC coupled) | HCSL I/O standard for the PCIe reference clock | 250 | — | 550 | mV |
| Transmitter REFCLK phase noise(43) | 10 Hz | — | — | –50 | dBc/Hz |
| | 100 Hz | — | — | –80 | dBc/Hz |
| | 1 KHz | — | — | –110 | dBc/Hz |
| | 10 KHz | — | — | –120 | dBc/Hz |
| | 100 KHz | — | — | –120 | dBc/Hz |
| | ≥ 1 MHz | — | — | –130 | dBc/Hz |
| $R_{REF}$ | — | — | 2000 ±1% | — | Ω |

## Table 27. Transceiver Clocks Specifications for Arria V GT and ST Devices

| Symbol/Description | Condition | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| `fixedclk` clock frequency | PCIe Receiver Detect | — | 125 | — | MHz |
| Transceiver Reconfiguration Controller Intel FPGA IP (`mgmt_clk_clk`) clock frequency | — | 75 | — | 125 | MHz |

## Table 28. Receiver Specifications for Arria V GT and ST Devices

| Symbol/Description | Condition | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Supported I/O Standards | 1.5 V PCML, 2.5 V PCML, LVPECL, and LVDS | | | | |
| Data rate (6-Gbps transceiver)(44) | — | 611 | — | 6553.6 | Mbps |

*continued...*

(43) The transmitter REFCLK phase jitter is 30 ps p-p (5 ps RMS) with bit error rate (BER) $10^{-12}$, equivalent to 14 sigma.

(44) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

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| Symbol/Description | Condition | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Data rate (10-Gbps transceiver)(44) | — | 0.611 | — | 10.3125 | Gbps |
| Absolute $V_{MAX}$ for a receiver pin(45) | — | — | — | 1.2 | V |
| Absolute $V_{MIN}$ for a receiver pin | — | –0.4 | — | — | V |
| Maximum peak-to-peak differential input voltage $V_{ID}$ (diff p-p) before device configuration | — | — | — | 1.6 | V |
| Maximum peak-to-peak differential input voltage $V_{ID}$ (diff p-p) after device configuration | — | — | — | 2.2 | V |
| Minimum differential eye opening at the receiver serial input pins(46) | — | 100 | — | — | mV |
| $V_{ICM}$ (AC coupled) | — | — | 750(47)/800 | — | mV |
| $V_{ICM}$ (DC coupled) | ≤ 3.2Gbps(48) | 670 | 700 | 730 | mV |
| Differential on-chip termination resistors | 85-Ω setting | 85 | | | Ω |
| | 100-Ω setting | 100 | | | Ω |
| | 120-Ω setting | 120 | | | Ω |
| | 150-Ω setting | 150 | | | Ω |
| $t_{LTR}$(49) | — | — | — | 10 | µs |

continued...

(45) The device cannot tolerate prolonged operation at this absolute maximum.

(46) The differential eye opening specification at the receiver input pins assumes that you have disabled the **Receiver Equalization** feature. If you enable the **Receiver Equalization** feature, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(47) The AC coupled $V_{ICM}$ is 750 mV for PCIe mode only.

(48) For standard protocol compliance, use AC coupling.

(49) $t_{LTR}$ is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

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| Symbol/Description | Condition | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $t_{LTD}$[50] | — | 4 | — | — | µs |
| $t_{LTD_manual}$[51] | — | 4 | — | — | µs |
| $t_{LTR_LTD_manual}$[52] | — | 15 | — | — | µs |
| Programmable ppm detector[53] | — | ±62.5, 100, 125, 200, 250, 300, 500, and 1000 | | | ppm |
| Run length | — | — | — | 200 | UI |
| Programmable equalization AC and DC gain | AC gain setting = 0 to 3[54]<br>DC gain setting = 0 to 1 | Refer to *CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices* and *CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices* diagrams. | | | |

## Table 29. Transmitter Specifications for Arria V GT and ST Devices

| Symbol/Description | Condition | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Supported I/O standards | 1.5 V PCML | | | | |
| Data rate (6-Gbps transceiver) | — | 611 | — | 6553.6 | Mbps |
| Data rate (10-Gbps transceiver) | — | 0.611 | — | 10.3125 | Gbps |
| $V_{OCM}$ (AC coupled) | — | — | 650 | — | mV |

***continued...***

(50) $t_{LTD}$ is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high.

(51) $t_{LTD_manual}$ is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high when the CDR is functioning in the manual mode.

(52) $t_{LTR_LTD_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedtoref` signal goes high when the CDR is functioning in the manual mode.

(53) The rate match FIFO supports only up to ±300 ppm.

(54) The Intel Quartus Prime software allows AC gain setting = 3 for design with data rate between 611 Mbps and 1.25 Gbps only.

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| Symbol/Description | Condition | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $V_{OCM}$ (DC coupled) | ≤ 3.2 Gbps(48) | 670 | 700 | 730 | mV |
| Differential on-chip termination resistors | 85-Ω setting | — | 85 | — | Ω |
| | 100-Ω setting | — | 100 | — | Ω |
| | 120-Ω setting | — | 120 | — | Ω |
| | 150-Ω setting | — | 150 | — | Ω |
| Intra-differential pair skew | TX $V_{CM}$ = 0.65 V (AC coupled) and slew rate of 15 ps | — | — | 15 | ps |
| Intra-transceiver block transmitter channel-to-channel skew | ×6 PMA bonded mode | — | — | 180 | ps |
| Inter-transceiver block transmitter channel-to-channel skew(55) | ×*N* PMA bonded mode | — | — | 500 | ps |

## Table 30. CMU PLL Specifications for Arria V GT and ST Devices

| Symbol/Description | Transceiver Speed Grade 3 | | Unit |
|---|---|---|---|
| | Min | Max | |
| Supported data range | 0.611 | 10.3125 | Gbps |
| fPLL supported data range | 611 | 3125 | Mbps |

(55) This specification is only applicable to channels on one side of the device across two transceiver banks.

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**Table 31. Transceiver-FPGA Fabric Interface Specifications for Arria V GT and ST Devices**

| Symbol/Description | Transceiver Speed Grade 3 | | Unit |
|---|---|---|---|
| | Min | Max | |
| Interface speed (PMA direct mode) | 50 | 153.6(56), 161(57) | MHz |
| Interface speed (single-width mode) | 25 | 187.5 | MHz |
| Interface speed (double-width mode) | 25 | 163.84 | MHz |

**Related Information**

- CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain on page 36
- CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain on page 37

(56) The maximum frequency when core transceiver local routing is selected.

(57) The maximum frequency when core transceiver network routing (GCLK, RCLK, or PCLK) is selected.

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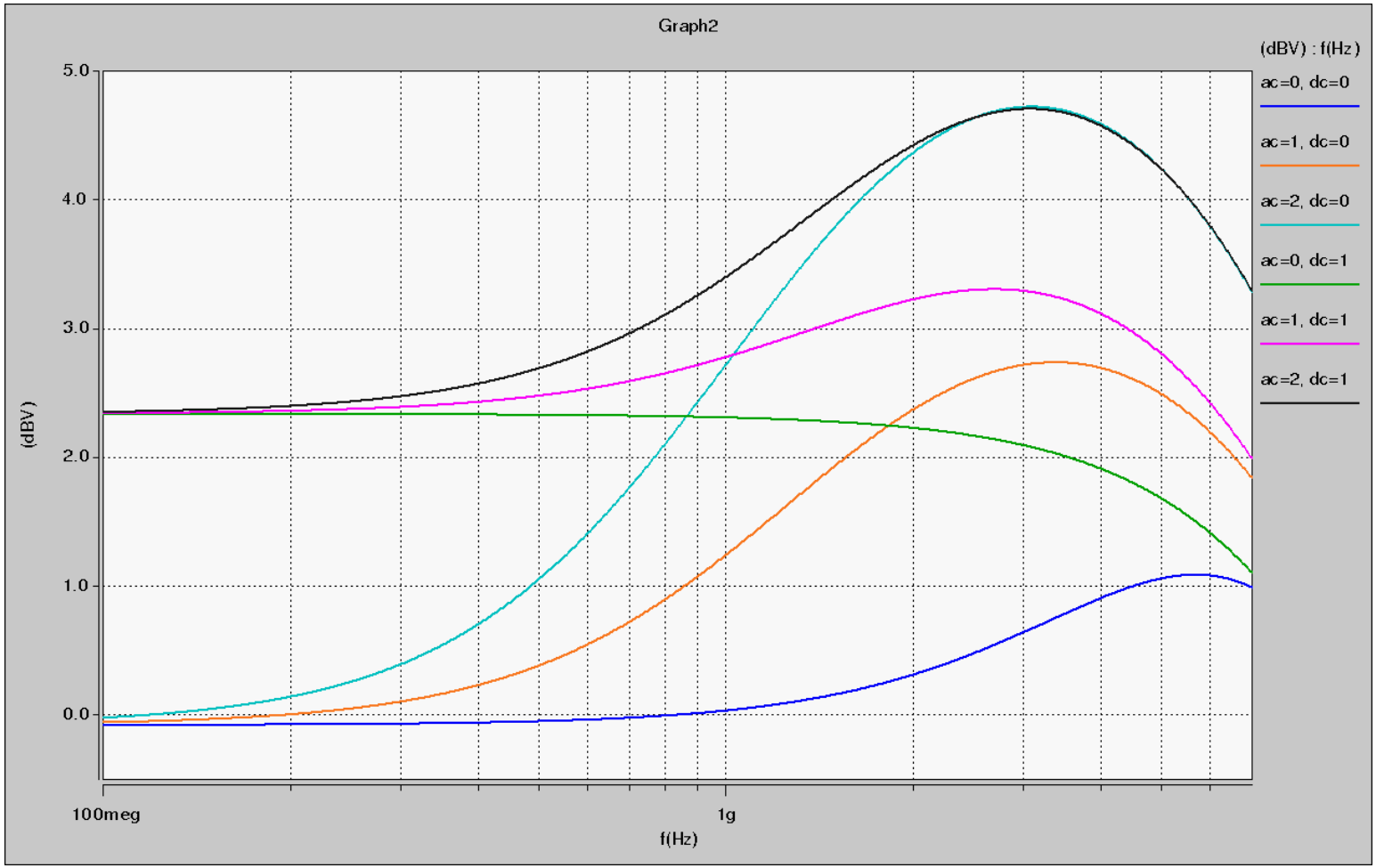
### 1.2.1.3. CTLE Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain

**Figure 3. Continuous Time-Linear Equalizer (CTLE) Response at Data Rates > 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices**



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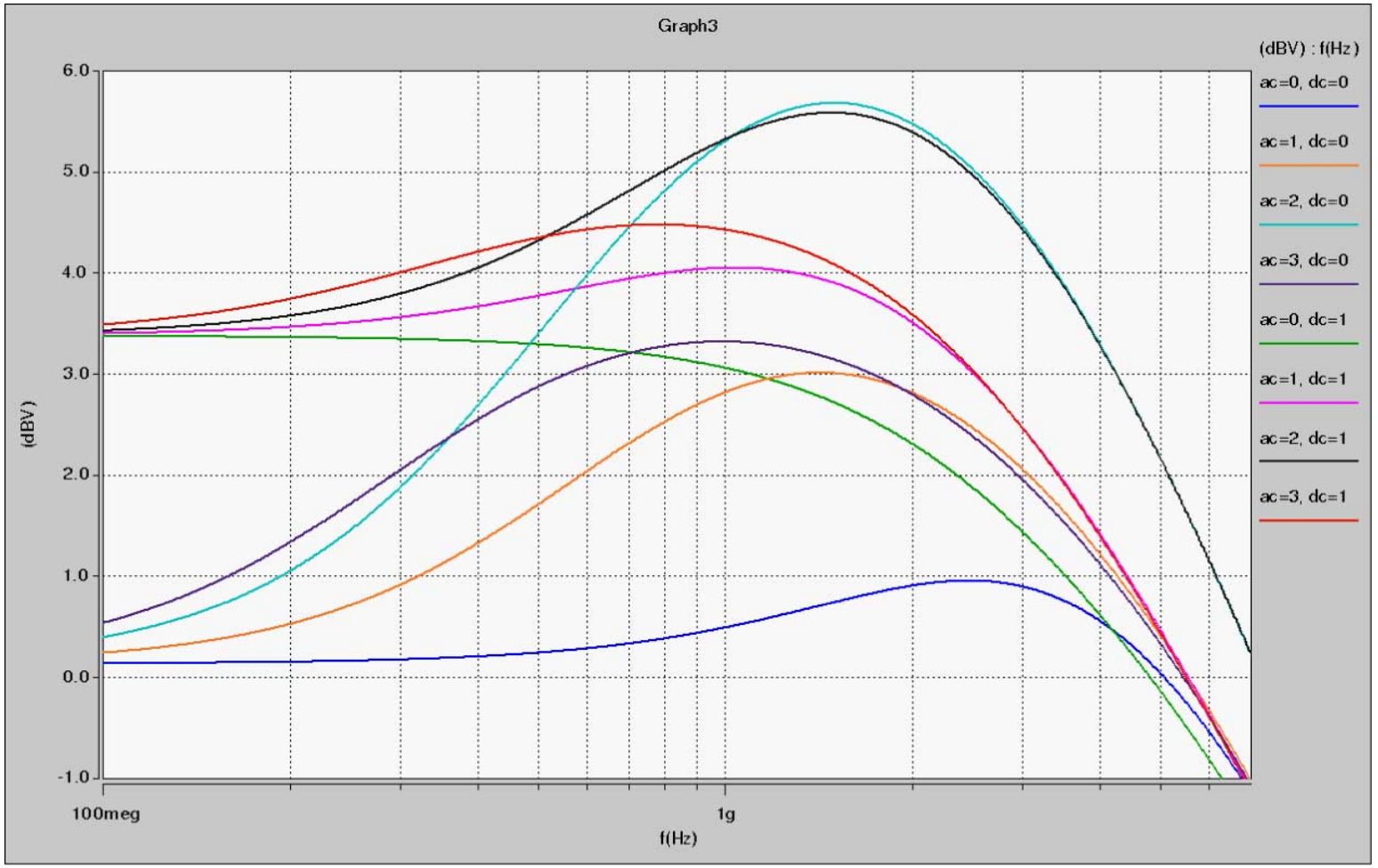
### 1.2.1.4. CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain

**Figure 4. CTLE Response at Data Rates ≤ 3.25 Gbps across Supported AC Gain and DC Gain for Arria V GX, GT, SX, and ST Devices**



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### 1.2.1.5. Typical TX $V_{OD}$ Setting for Arria V Transceiver Channels with termination of 100 Ω

**Table 32. Typical TX $V_{OD}$ Setting for Arria V Transceiver Channels with termination of 100 Ω**

| Symbol | $V_{OD}$ Setting[58] | $V_{OD}$ Value (mV) | $V_{OD}$ Setting[58] | $V_{OD}$ Value (mV) |
|---|---|---|---|---|
| $V_{OD}$ differential peak-to-peak typical | 6[59] | 120 | 34 | 680 |
| | 7[59] | 140 | 35 | 700 |
| | 8[59] | 160 | 36 | 720 |
| | 9 | 180 | 37 | 740 |
| | 10 | 200 | 38 | 760 |
| | 11 | 220 | 39 | 780 |
| | 12 | 240 | 40 | 800 |
| | 13 | 260 | 41 | 820 |
| | 14 | 280 | 42 | 840 |
| | 15 | 300 | 43 | 860 |
| | 16 | 320 | 44 | 880 |
| | 17 | 340 | 45 | 900 |
| | 18 | 360 | 46 | 920 |
| | 19 | 380 | 47 | 940 |
| | 20 | 400 | 48 | 960 |
| | 21 | 420 | 49 | 980 |
| | 22 | 440 | 50 | 1000 |
| | 23 | 460 | 51 | 1020 |
| | 24 | 480 | 52 | 1040 |

*continued...*

(58) Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.

(59) Only valid for data rates ≤ 5 Gbps.

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| Symbol | $V_{OD}$ Setting[58] | $V_{OD}$ Value (mV) | $V_{OD}$ Setting[58] | $V_{OD}$ Value (mV) |
|---|---|---|---|---|
| | 25 | 500 | 53 | 1060 |
| | 26 | 520 | 54 | 1080 |
| | 27 | 540 | 55 | 1100 |
| | 28 | 560 | 56 | 1120 |
| | 29 | 580 | 57 | 1140 |
| | 30 | 600 | 58 | 1160 |
| | 31 | 620 | 59 | 1180 |
| | 32 | 640 | 60 | 1200 |
| | 33 | 660 | | |

### 1.2.1.6. Transmitter Pre-Emphasis Levels

The following table lists the simulation data on the transmitter pre-emphasis levels in dB for the first post tap under the following conditions:

- Low-frequency data pattern—five 1s and five 0s
- Data rate—2.5 Gbps

The levels listed are a representation of possible pre-emphasis levels under the specified conditions only and the pre-emphasis levels may change with data pattern and data rate.

Arria V devices only support 1st post tap pre-emphasis with the following conditions:

- The 1st post tap pre-emphasis settings must satisfy $|B| + |C| \leq 60$ where $|B| = V_{OD}$ setting with termination value, $R_{TERM} = 100\ \Omega$ and $|C|$ = 1st post tap pre-emphasis setting.
- $|B| - |C| > 5$ for data rates < 5 Gbps and $|B| - |C| > 8.25$ for data rates > 5 Gbps.
- $(V_{MAX}/V_{MIN} - 1)\% < 600\%$, where $V_{MAX} = |B| + |C|$ and $V_{MIN} = |B| - |C|$.

(58) Convert these values to their binary equivalent form if you are using the dynamic reconfiguration mode for PMA analog controls.

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Exception for PCIe Gen2 design: $V_{OD}$ setting = 43 and pre-emphasis setting = 19 are allowed for PCIe Gen2 design with transmit de-emphasis –6dB setting (`pipe_txdeemp` = 1'b0) using Arria V Hard IP for PCI Express Intel FPGA IP and PHY for PCI Express (PIPE) Intel FPGA IP cores.

For example, when $V_{OD}$ = 800 mV, the corresponding $V_{OD}$ value setting is 40. The following conditions show that the 1st post tap pre-emphasis setting = 2 is valid:

- $|B| + |C| \leq 60 \rightarrow 40 + 2 = 42$
- $|B| - |C| > 5 \rightarrow 40 - 2 = 38$
- $(V_{MAX}/V_{MIN} - 1)\% < 600\% \rightarrow (42/38 - 1)\% = 10.52\%$

To predict the pre-emphasis level for your specific data rate and pattern, run simulations using the Arria V HSSI HSPICE models.

**Table 33. Transmitter Pre-Emphasis Levels for Arria V Devices**

| Intel Quartus Prime 1st Post Tap Pre-Emphasis Setting | Intel Quartus Prime $V_{OD}$ Setting | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | 10 (200 mV) | 20 (400 mV) | 30 (600 mV) | 35 (700 mV) | 40 (800 mV) | 45 (900 mV) | 50 (1000 mV) | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | dB |
| 1 | 1.97 | 0.88 | 0.43 | 0.32 | 0.24 | 0.19 | 0.13 | dB |
| 2 | 3.58 | 1.67 | 0.95 | 0.76 | 0.61 | 0.5 | 0.41 | dB |
| 3 | 5.35 | 2.48 | 1.49 | 1.2 | 1 | 0.83 | 0.69 | dB |
| 4 | 7.27 | 3.31 | 2 | 1.63 | 1.36 | 1.14 | 0.96 | dB |
| 5 | — | 4.19 | 2.55 | 2.1 | 1.76 | 1.49 | 1.26 | dB |
| 6 | — | 5.08 | 3.11 | 2.56 | 2.17 | 1.83 | 1.56 | dB |
| 7 | — | 5.99 | 3.71 | 3.06 | 2.58 | 2.18 | 1.87 | dB |
| 8 | — | 6.92 | 4.22 | 3.47 | 2.93 | 2.48 | 2.11 | dB |
| 9 | — | 7.92 | 4.86 | 4 | 3.38 | 2.87 | 2.46 | dB |
| 10 | — | 9.04 | 5.46 | 4.51 | 3.79 | 3.23 | 2.77 | dB |
| 11 | — | 10.2 | 6.09 | 5.01 | 4.23 | 3.61 | — | dB |
| 12 | — | 11.56 | 6.74 | 5.51 | 4.68 | 3.97 | — | dB |

*continued...*

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| Intel Quartus Prime 1st Post Tap Pre-Emphasis Setting | Intel Quartus Prime $V_{OD}$ Setting | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | 10 (200 mV) | 20 (400 mV) | 30 (600 mV) | 35 (700 mV) | 40 (800 mV) | 45 (900 mV) | 50 (1000 mV) | |
| 13 | — | 12.9 | 7.44 | 6.1 | 5.12 | 4.36 | — | dB |
| 14 | — | 14.44 | 8.12 | 6.64 | 5.57 | 4.76 | — | dB |
| 15 | — | — | 8.87 | 7.21 | 6.06 | 5.14 | — | dB |
| 16 | — | — | 9.56 | 7.73 | 6.49 | — | — | dB |
| 17 | — | — | 10.43 | 8.39 | 7.02 | — | — | dB |
| 18 | — | — | 11.23 | 9.03 | 7.52 | — | — | dB |
| 19 | — | — | 12.18 | 9.7 | 8.02 | — | — | dB |
| 20 | — | — | 13.17 | 10.34 | 8.59 | — | — | dB |
| 21 | — | — | 14.2 | 11.1 | — | — | — | dB |
| 22 | — | — | 15.38 | 11.87 | — | — | — | dB |
| 23 | — | — | — | 12.67 | — | — | — | dB |
| 24 | — | — | — | 13.48 | — | — | — | dB |
| 25 | — | — | — | 14.37 | — | — | — | dB |
| 26 | — | — | — | — | — | — | — | dB |
| 27 | — | — | — | — | — | — | — | dB |
| 28 | — | — | — | — | — | — | — | dB |
| 29 | — | — | — | — | — | — | — | dB |
| 30 | — | — | — | — | — | — | — | dB |
| 31 | — | — | — | — | — | — | — | dB |

## Related Information

SPICE Models for Intel Devices
Provides the Arria V HSSI HSPICE models.

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### 1.2.1.7. Transceiver Compliance Specification

The following table lists the physical medium attachment (PMA) specification compliance of all supported protocol for Arria V GX, GT, SX, and ST devices. For more information about the protocol parameter details and compliance specifications, contact your Intel Sales Representative.

**Table 34. Transceiver Compliance Specification for All Supported Protocol for Arria V GX, GT, SX, and ST Devices**

| Protocol | Sub-protocol | Data Rate (Mbps) |
|---|---|---|
| PCIe | PCIe Gen1 | 2,500 |
| | PCIe Gen2 | 5,000 |
| | PCIe Cable | 2,500 |
| XAUI | XAUI 2135 | 3,125 |
| Serial RapidIO® (SRIO) | SRIO 1250 SR | 1,250 |
| | SRIO 1250 LR | 1,250 |
| | SRIO 2500 SR | 2,500 |
| | SRIO 2500 LR | 2,500 |
| | SRIO 3125 SR | 3,125 |
| | SRIO 3125 LR | 3,125 |
| | SRIO 5000 SR | 5,000 |
| | SRIO 5000 MR | 5,000 |
| | SRIO 5000 LR | 5,000 |
| | SRIO_6250_SR | 6,250 |
| | SRIO_6250_MR | 6,250 |
| | SRIO_6250_LR | 6,250 |
| Common Public Radio Interface (CPRI) | CPRI E6LV | 614.4 |
| | CPRI E6HV | 614.4 |
| | CPRI E6LVII | 614.4 |
| | CPRI E12LV | 1,228.8 |

*continued...*

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| Protocol | Sub-protocol | Data Rate (Mbps) |
|---|---|---|
| | CPRI E12HV | 1,228.8 |
| | CPRI E12LVII | 1,228.8 |
| | CPRI E24LV | 2,457.6 |
| | CPRI E24LVII | 2,457.6 |
| | CPRI E30LV | 3,072 |
| | CPRI E30LVII | 3,072 |
| | CPRI E48LVII | 4,915.2 |
| | CPRI E60LVII | 6,144 |
| | CPRI E96LVIII(60) | 9,830.4 |
| Gbps Ethernet (GbE) | GbE 1250 | 1,250 |
| OBSAI | OBSAI 768 | 768 |
| | OBSAI 1536 | 1,536 |
| | OBSAI 3072 | 3,072 |
| | OBSAI 6144 | 6,144 |
| Serial digital interface (SDI) | SDI 270 SD | 270 |
| | SDI 1485 HD | 1,485 |
| | SDI 2970 3G | 2,970 |
| SONET | SONET 155 | 155.52 |
| | SONET 622 | 622.08 |
| | SONET 2488 | 2,488.32 |
| Gigabit-capable passive optical network (GPON) | GPON 155 | 155.52 |
| | GPON 622 | 622.08 |

***continued...***

(60) You can achieve compliance with TX channel restriction of one HSSI channel per six-channel transceiver bank.

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| Protocol | Sub-protocol | Data Rate (Mbps) |
|---|---|---|
| | GPON 1244 | 1,244.16 |
| | GPON 2488 | 2,488.32 |
| QSGMII | QSGMII 5000 | 5,000 |

## 1.2.2. Core Performance Specifications

### 1.2.2.1. Clock Tree Specifications

**Table 35. Clock Tree Specifications for Arria V Devices**

| Parameter | Performance | | | Unit |
|---|---|---|---|---|
| | –I3, –C4 | –I5, –C5 | –C6 | |
| Global clock and Regional clock | 625 | 625 | 525 | MHz |
| Peripheral clock | 450 | 400 | 350 | MHz |

### 1.2.2.2. PLL Specifications

**Table 36. PLL Specifications for Arria V Devices**

This table lists the Arria V PLL block specifications. Arria V PLL block does not include HPS PLL.

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{IN}$ | Input clock frequency | –3 speed grade | 5 | — | 800(61) | MHz |
| | | –4 speed grade | 5 | — | 800(61) | MHz |
| | | –5 speed grade | 5 | — | 750(61) | MHz |
| | | –6 speed grade | 5 | — | 625(61) | MHz |
| $f_{INPFD}$ | Integer input clock frequency to the phase frequency detector (PFD) | — | 5 | — | 325 | MHz |

continued...

(61) This specification is limited in the Intel Quartus Prime software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

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| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{FINPFD}$ | Fractional input clock frequency to the PFD | — | 50 | — | 160 | MHz |
| $f_{VCO}$(62) | PLL voltage-controlled oscillator (VCO) operating range | –3 speed grade | 600 | — | 1600 | MHz |
| | | –4 speed grade | 600 | — | 1600 | MHz |
| | | –5 speed grade | 600 | — | 1600 | MHz |
| | | –6 speed grade | 600 | — | 1300 | MHz |
| $t_{EINDUTY}$ | Input clock or external feedback clock input duty cycle | — | 40 | — | 60 | % |
| $f_{OUT}$ | Output frequency for internal global or regional clock | –3 speed grade | — | — | 500(63) | MHz |
| | | –4 speed grade | — | — | 500(63) | MHz |
| | | –5 speed grade | — | — | 500(63) | MHz |
| | | –6 speed grade | — | — | 400(63) | MHz |
| $f_{OUT_EXT}$ | Output frequency for external clock output | –3 speed grade | — | — | 670(63) | MHz |
| | | –4 speed grade | — | — | 670(63) | MHz |
| | | –5 speed grade | — | — | 622(63) | MHz |
| | | –6 speed grade | — | — | 500(63) | MHz |
| $t_{OUTDUTY}$ | Duty cycle for external clock output (when set to 50%) | — | 45 | 50 | 55 | % |
| $t_{FCOMP}$ | External feedback clock compensation time | — | — | — | 10 | ns |
| $t_{DYCONFIGCLK}$ | Dynamic configuration clock for `mgmt_clk` and `scanclk` | — | — | — | 100 | MHz |
| $t_{LOCK}$ | Time required to lock from end-of-device configuration or deassertion of `areset` | — | — | — | 1 | ms |

***continued...***

(62) The VCO frequency reported by the Intel Quartus Prime software takes into consideration the VCO post divider value. Therefore, if the VCO post divider value is 2, the frequency reported can be lower than the $f_{VCO}$ specification.

(63) This specification is limited by the lower of the two: I/O $f_{MAX}$ or $F_{OUT}$ of the PLL.

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| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{DLOCK}$ | Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) | — | — | — | 1 | ms |
| $f_{CLBW}$ | PLL closed-loop bandwidth | Low | — | 0.3 | — | MHz |
| | | Medium | — | 1.5 | — | MHz |
| | | High(64) | — | 4 | — | MHz |
| $t_{PLL_PSERR}$ | Accuracy of PLL phase shift | — | — | — | ±50 | ps |
| $t_{ARESET}$ | Minimum pulse width on the areset signal | — | 10 | — | — | ns |
| $t_{INCCJ}$(65)(66) | Input clock cycle-to-cycle jitter | $F_{REF}$ ≥ 100 MHz | — | — | 0.15 | UI (p-p) |
| | | $F_{REF}$ < 100 MHz | — | — | ±750 | ps (p-p) |
| $t_{OUTPJ_DC}$(67) | Period jitter for dedicated clock output in integer PLL | $F_{OUT}$ ≥ 100 MHz | — | — | 175 | ps (p-p) |
| | | $F_{OUT}$ < 100 MHz | — | — | 17.5 | mUI (p-p) |
| $t_{FOUTPJ_DC}$(67) | Period jitter for dedicated clock output in fractional PLL | $F_{OUT}$ ≥ 100 MHz | — | — | 250(68), 175(69) | ps (p-p) |
| | | $F_{OUT}$ < 100 MHz | — | — | 25(68), 17.5(69) | mUI (p-p) |

continued...

(64) High bandwidth PLL settings are not supported in external feedback mode.

(65) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

(66) $F_{REF}$ is $f_{IN}/N$, specification applies when $N = 1$.

(67) Peak-to-peak jitter with a probability level of $10^{-12}$ (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Memory Output Clock Jitter Specification for Arria V Devices table.

(68) This specification only covered fractional PLL for low bandwidth. The $f_{VCO}$ for fractional value range 0.05–0.95 must be ≥ 1000 MHz.

(69) This specification only covered fractional PLL for low bandwidth. The $f_{VCO}$ for fractional value range 0.20–0.80 must be ≥ 1200 MHz.

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| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{OUTCCJ_DC}$[67] | Cycle-to-cycle jitter for dedicated clock output in integer PLL | $F_{OUT}$ ≥ 100 MHz | — | — | 175 | ps (p-p) |
| | | $F_{OUT}$ < 100 MHz | — | — | 17.5 | mUI (p-p) |
| $t_{FOUTCCJ_DC}$[67] | Cycle-to-cycle jitter for dedicated clock output in fractional PLL | $F_{OUT}$ ≥ 100 MHz | — | — | 250[68], 175[69] | ps (p-p) |
| | | $F_{OUT}$ < 100 MHz | — | — | 25[68], 17.5[69] | mUI (p-p) |
| $t_{OUTPJ_IO}$[67][70] | Period jitter for clock output on a regular I/O in integer PLL | $F_{OUT}$ ≥ 100 MHz | — | — | 600 | ps (p-p) |
| | | $F_{OUT}$ < 100 MHz | — | — | 60 | mUI (p-p) |
| $t_{FOUTPJ_IO}$[67][68][70] | Period jitter for clock output on a regular I/O in fractional PLL | $F_{OUT}$ ≥ 100 MHz | — | — | 600 | ps (p-p) |
| | | $F_{OUT}$ < 100 MHz | — | — | 60 | mUI (p-p) |
| $t_{OUTCCJ_IO}$[67][70] | Cycle-to-cycle jitter for clock output on a regular I/O in integer PLL | $F_{OUT}$ ≥ 100 MHz | — | — | 600 | ps (p-p) |
| | | $F_{OUT}$ < 100 MHz | — | — | 60 | mUI (p-p) |
| $t_{FOUTCCJ_IO}$[67][68][70] | Cycle-to-cycle jitter for clock output on a regular I/O in fractional PLL | $F_{OUT}$ ≥ 100 MHz | — | — | 600 | ps (p-p) |
| | | $F_{OUT}$ < 100 MHz | — | — | 60 | mUI (p-p) |
| $t_{CASC_OUTPJ_DC}$[67][71] | Period jitter for dedicated clock output in cascaded PLLs | $F_{OUT}$ ≥ 100 MHz | — | — | 175 | ps (p-p) |
| | | $F_{OUT}$ < 100 MHz | — | — | 17.5 | mUI (p-p) |
| $t_{DRIFT}$ | Frequency drift after PFDENA is disabled for a duration of 100 µs | — | — | — | ±10 | % |
| $dK_{BIT}$ | Bit number of Delta Sigma Modulator (DSM) | — | 8 | 24 | 32 | bits |
| $k_{VALUE}$ | Numerator of fraction | — | 128 | 8388608 | 2147483648 | — |
| $f_{RES}$ | Resolution of VCO frequency | $f_{INPFD}$ = 100 MHz | 390625 | 5.96 | 0.023 | Hz |

(70) External memory interface clock output jitter specifications use a different measurement method, which are available in Memory Output Clock Jitter Specification for Arria V Devices table.

(71) The cascaded PLL specification is only applicable with the following conditions:
- Upstream PLL: 0.59 MHz ≤ Upstream PLL BW < 1 MHz
- Downstream PLL: Downstream PLL BW > 2 MHz

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**Related Information**

Memory Output Clock Jitter Specifications on page 56
Provides more information about the external memory interface clock output jitter specifications.

### 1.2.2.3. DSP Block Performance Specifications

**Table 37. DSP Block Performance Specifications for Arria V Devices**

| Mode | | Performance | | | Unit |
|---|---|---|---|---|---|
| | | –I3, –C4 | –I5, –C5 | –C6 | |
| Modes using One DSP Block | Independent 9 × 9 multiplication | 370 | 310 | 220 | MHz |
| | Independent 18 × 19 multiplication | 370 | 310 | 220 | MHz |
| | Independent 18 × 25 multiplication | 370 | 310 | 220 | MHz |
| | Independent 20 × 24 multiplication | 370 | 310 | 220 | MHz |
| | Independent 27 × 27 multiplication | 310 | 250 | 200 | MHz |
| | Two 18 × 19 multiplier adder mode | 370 | 310 | 220 | MHz |
| | 18 × 18 multiplier added summed with 36-bit input | 370 | 310 | 220 | MHz |
| Modes using Two DSP Blocks | Complex 18 × 19 multiplication | 370 | 310 | 220 | MHz |

### 1.2.2.4. Memory Block Performance Specifications

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL and set to 50% output duty cycle. Use the Intel Quartus Prime software to report timing for the memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in $f_{MAX}$.

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**Table 38. Memory Block Performance Specifications for Arria V Devices**

| Memory | Mode | Resources Used | | Performance | | | Unit |
|---|---|---|---|---|---|---|---|
| | | ALUTs | Memory | –I3, –C4 | –I5, –C5 | –C6 | |
| MLAB | Single port, all supported widths | 0 | 1 | 500 | 450 | 400 | MHz |
| | Simple dual-port, all supported widths | 0 | 1 | 500 | 450 | 400 | MHz |
| | Simple dual-port with read and write at the same address | 0 | 1 | 400 | 350 | 300 | MHz |
| | ROM, all supported width | — | — | 500 | 450 | 400 | MHz |
| M10K Block | Single-port, all supported widths | 0 | 1 | 400 | 350 | 285 | MHz |
| | Simple dual-port, all supported widths | 0 | 1 | 400 | 350 | 285 | MHz |
| | Simple dual-port with the read-during-write option set to **Old Data**, all supported widths | 0 | 1 | 315 | 275 | 240 | MHz |
| | True dual port, all supported widths | 0 | 1 | 400 | 350 | 285 | MHz |
| | ROM, all supported widths | 0 | 1 | 400 | 350 | 285 | MHz |

### 1.2.2.5. Internal Temperature Sensing Diode Specifications

**Table 39. Internal Temperature Sensing Diode Specifications for Arria V Devices**

| Temperature Range | Accuracy | Offset Calibrated Option | Sampling Rate | Conversion Time(72) | Resolution | Minimum Resolution with no Missing Codes |
|---|---|---|---|---|---|---|
| –40 to 100°C | ±8°C | No | 1 MHz | < 100 ms | 8 bits | 8 bits |

**Related Information**

Intel FPGA Temperature Sensor IP Core User Guide
Provides more information about the temperature sensing operation.

## 1.2.3. Periphery Performance

This section describes the periphery performance, high-speed I/O, and external memory interface.

(72) For more details about the temperature sensing operations, refer to the *Intel FPGA Temperature Sensor IP Core User Guide*.

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Actual achievable frequency depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

### 1.2.3.1. High-Speed I/O Specifications

#### Table 40. High-Speed I/O Specifications for Arria V Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block. When J = 1 or 2, bypass the SERDES block.

For LVDS applications, you must use the PLLs in integer PLL mode.

The Arria V devices support the following output standards using true LVDS output buffer types on all I/O banks.

- True RSDS output standard with data rates of up to 360 Mbps
- True mini-LVDS output standard with data rates of up to 400 Mbps

| Symbol | | Condition | –I3, –C4 | | | –I5, –C5 | | | –C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSCLK_in}$ (input clock frequency) True Differential I/O Standards | | Clock boost factor W = 1 to 40(73) | 5 | — | 800 | 5 | — | 750 | 5 | — | 625 | MHz |
| $f_{HSCLK_in}$ (input clock frequency) Single-Ended I/O Standards(74) | | Clock boost factor W = 1 to 40(73) | 5 | — | 625 | 5 | — | 625 | 5 | — | 500 | MHz |
| $f_{HSCLK_in}$ (input clock frequency) Single-Ended I/O Standards(75) | | Clock boost factor W = 1 to 40(73) | 5 | — | 420 | 5 | — | 420 | 5 | — | 420 | MHz |
| $f_{HSCLK_OUT}$ (output clock frequency) | | — | 5 | — | 625(76) | 5 | — | 625(76) | 5 | — | 500(76) | MHz |
| Transmitter | True Differential I/O Standards - $f_{HSDR}$ (data rate) | SERDES factor J =3 to 10(77) | (78) | — | 1250 | (78) | — | 1250 | (78) | — | 1050 | Mbps |

continued...

(73) Clock boost factor (W) is the ratio between the input data rate and the input clock rate.

(74) This applies to DPA and soft-CDR modes only.

(75) This applies to non-DPA mode only.

(76) This is achieved by using the LVDS clock network.

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| Symbol | | Condition | –I3, –C4 | | | –I5, –C5 | | | –C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| | | SERDES factor J ≥ 8(77) (79), LVDS TX with RX DPA | (78) | — | 1600 | (78) | — | 1500 | (78) | — | 1250 | Mbps |
| | | SERDES factor J = 1 to 2, Uses DDR Registers | (78) | — | (80) | (78) | — | (80) | (78) | — | (80) | Mbps |
| | Emulated Differential I/O Standards with Three External Output Resistor Network - $f_{HSDR}$ (data rate) (81) | SERDES factor J = 4 to 10(82) | (78) | — | 945 | (78) | — | 945 | (78) | — | 945 | Mbps |
| | Emulated Differential I/O Standards with One External Output Resistor Network - $f_{HSDR}$ (data rate)(81) | SERDES factor J = 4 to 10(82) | (78) | — | 200 | (78) | — | 200 | (78) | — | 200 | Mbps |
| | $t_{x\ Jitter}$ -True Differential I/O Standards | Total Jitter for Data Rate 600 Mbps – 1.25 Gbps | — | — | 160 | — | — | 160 | — | — | 160 | ps |
| | | Total Jitter for Data Rate < 600 Mbps | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | UI |

*continued...*

(77) The $F_{max}$ specification is based on the fast clock used for serial data. The interface $F_{max}$ is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

(78) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

(79) The $V_{CC}$ and $V_{CCP}$ must be on a separate power layer and a maximum load of 5 pF for chip-to-chip interface.

(80) The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency ($f_{OUT}$), provided you can close the design timing and the signal integrity simulation is clean.

(81) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.

(82) When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.

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| Symbol | | Condition | –I3, –C4 | | | –I5, –C5 | | | –C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| | $t_{x\ Jitter}$ -Emulated Differential I/O Standards with Three External Output Resistor Network | Total Jitter for Data Rate 600 Mbps – 1.25 Gbps | — | — | 260 | — | — | 300 | — | — | 350 | ps |
| | | Total Jitter for Data Rate < 600 Mbps | — | — | 0.16 | — | — | 0.18 | — | — | 0.21 | UI |
| | $t_{x\ Jitter}$ -Emulated Differential I/O Standards with One External Output Resistor Network | — | — | — | 0.15 | — | — | 0.15 | — | — | 0.15 | UI |
| | $t_{DUTY}$ | TX output clock duty cycle for both True and Emulated Differential I/O Standards | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | % |
| | $t_{RISE}$ and $t_{FALL}$ | True Differential I/O Standards(83) | — | — | 160 | — | — | 180 | — | — | 200 | ps |
| | | Emulated Differential I/O Standards with Three External Output Resistor Network | — | — | 250 | — | — | 250 | — | — | 300 | ps |
| | | Emulated Differential I/O Standards with One External Output Resistor Network | — | — | 500 | — | — | 500 | — | — | 500 | ps |
| | TCCS | True Differential I/O Standards | — | — | 150 | — | — | 150 | — | — | 150 | ps |
| | | Emulated Differential I/O Standards | — | — | 300 | — | — | 300 | — | — | 300 | ps |
| Receiver | True Differential I/O Standards - $f_{HSDRDPA}$ (data rate) | SERDES factor J =3 to 10(77) | 150 | — | 1250 | 150 | — | 1250 | 150 | — | 1050 | Mbps |
| | | SERDES factor J ≥ 8 with DPA(77)(79) | 150 | — | 1600 | 150 | — | 1500 | 150 | — | 1250 | Mbps |

continued...

(83) This applies to default pre-emphasis and $V_{OD}$ settings only.

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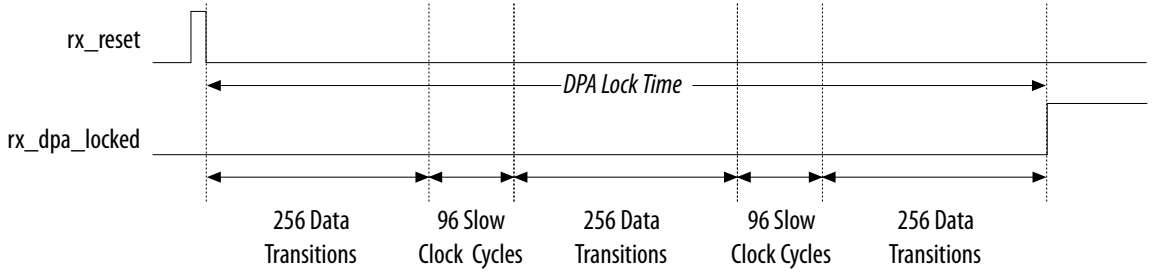
| Symbol | | Condition | –I3, –C4 | | | –I5, –C5 | | | –C6 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| | $f_{HSDR}$ (data rate) | SERDES factor J = 3 to 10 | (78) | — | (84) | (78) | — | (84) | (78) | — | (84) | Mbps |
| | | SERDES factor J = 1 to 2, uses DDR registers | (78) | — | (80) | (78) | — | (80) | (78) | — | (80) | Mbps |
| DPA Mode | DPA run length | — | — | — | 10000 | — | — | 10000 | — | — | 10000 | UI |
| Soft-CDR Mode | Soft-CDR ppm tolerance | — | — | — | 300 | — | — | 300 | — | — | 300 | ±ppm |
| Non-DPA Mode | Sampling Window | — | — | — | 300 | — | — | 300 | — | — | 300 | ps |

### 1.2.3.2. DPA Lock Time Specifications

**Figure 5. Dynamic Phase Alignment (DPA) Lock Time Specifications with DPA PLL Calibration Enabled**




(84) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

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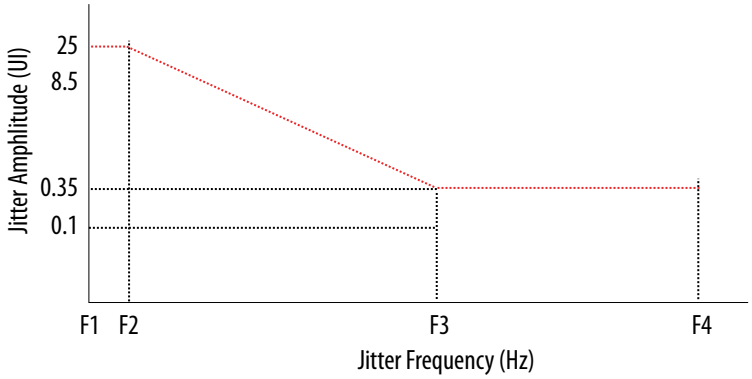
**Table 41. DPA Lock Time Specifications for Arria V Devices**

The specifications are applicable to both commercial and industrial grades. The DPA lock time is for one channel. One data transition is defined as a 0-to-1 or 1-to-0 transition.

| Standard | Training Pattern | Number of Data Transitions in One Repetition of the Training Pattern | Number of Repetitions per 256 Data Transitions(85) | Maximum Data Transition |
|---|---|---|---|---|
| SPI-4 | 00000000001111111111 | 2 | 128 | 640 |
| Parallel Rapid I/O | 00001111 | 2 | 128 | 640 |
| | 10010000 | 4 | 64 | 640 |
| Miscellaneous | 10101010 | 8 | 32 | 640 |
| | 01010101 | 8 | 32 | 640 |

## 1.2.3.3. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specifications

**Figure 6. LVDS Soft-Clock Data Recovery (CDR)/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate Equal to 1.25 Gbps**




(85) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

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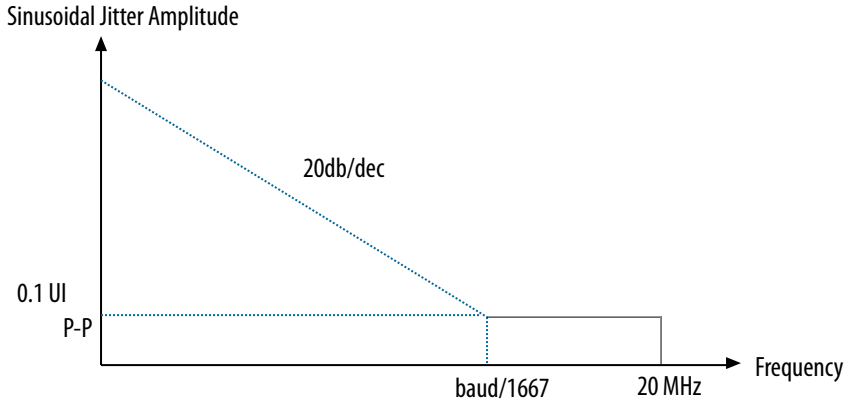
**Table 42. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate Equal to 1.25 Gbps**

| Jitter Frequency (Hz) | | Sinusoidal Jitter (UI) |
|---|---|---|
| F1 | 10,000 | 25.000 |
| F2 | 17,565 | 25.000 |
| F3 | 1,493,000 | 0.350 |
| F4 | 50,000,000 | 0.350 |

**Figure 7. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate Less than 1.25 Gbps**




## 1.2.3.4. DLL Frequency Range Specifications

**Table 43. DLL Frequency Range Specifications for Arria V Devices**

| Parameter | –I3, –C4 | –I5, –C5 | –C6 | Unit |
|---|---|---|---|---|
| DLL operating frequency range | 200 – 667 | 200 – 667 | 200 – 667 | MHz |

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## 1.2.3.5. DQS Logic Block Specifications

### Table 44. DQS Phase Shift Error Specifications for DLL-Delayed Clock ($t_{DQS_PSERR}$) for Arria V Devices

This error specification is the absolute maximum and minimum error.

| Number of DQS Delay Buffer | –I3, –C4 | –I5, –C5 | –C6 | Unit |
|---|---|---|---|---|
| 2 | 40 | 80 | 80 | ps |

## 1.2.3.6. Memory Output Clock Jitter Specifications

### Table 45. Memory Output Clock Jitter Specifications for Arria V Devices

The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 SDRAM standard.

The memory output clock jitter is applicable when an input jitter of 30 ps (p-p) is applied with bit error rate (BER) $10^{-12}$, equivalent to 14 sigma.

Intel recommends using the UniPHY IP cores with PHYCLK connections for better jitter performance.

| Parameter | Clock Network | Symbol | –I3, –C4 | | –I5, –C5 | | –C6 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| Clock period jitter | PHYCLK | $t_{JIT(per)}$ | –41 | 41 | –50 | 50 | –55 | 55 | ps |
| Cycle-to-cycle period jitter | PHYCLK | $t_{JIT(cc)}$ | 63 | | 90 | | 94 | | ps |

## 1.2.3.7. OCT Calibration Block Specifications

### Table 46. OCT Calibration Block Specifications for Arria V Devices

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| OCTUSRCLK | Clock required by OCT calibration blocks | — | — | 20 | MHz |
| $T_{OCTCAL}$ | Number of OCTUSRCLK clock cycles required for $R_S$ OCT/$R_T$ OCT calibration | — | 1000 | — | Cycles |
| $T_{OCTSHIFT}$ | Number of OCTUSRCLK clock cycles required for OCT code to shift out | — | 32 | — | Cycles |
| $T_{RS_RT}$ | Time required between the dyn_term_ctrl and oe signal transitions in a bidirectional I/O buffer to dynamically switch between $R_S$ OCT and $R_T$ OCT | — | 2.5 | — | ns |

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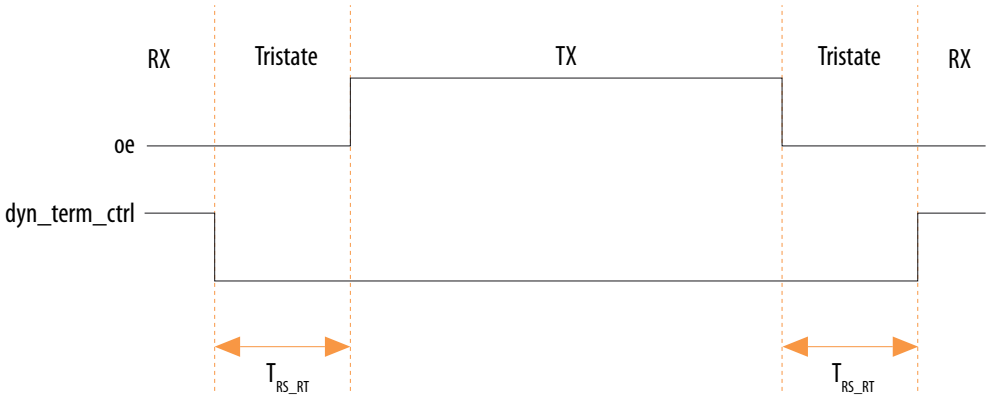
**Figure 8. Timing Diagram for oe and dyn_term_ctrl Signals**




### 1.2.3.8. Duty Cycle Distortion (DCD) Specifications

**Table 47. Worst-Case DCD on Arria V I/O Pins**

The output DCD cycle only applies to the I/O buffer. It does not cover the system DCD.

| Symbol | –I3, –C4 | | –C5, –I5 | | –C6 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| Output Duty Cycle | 45 | 55 | 45 | 55 | 45 | 55 | % |

## 1.2.4. HPS Specifications

This section provides HPS specifications and timing for Arria V devices.

For HPS reset, the minimum reset pulse widths for the HPS cold and warm reset signals (HPS_nRST and HPS_nPOR) are six clock cycles of HPS_CLK1.

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### 1.2.4.1. HPS Clock Performance

**Table 48. HPS Clock Performance for Arria V Devices**

| Symbol/Description | –I3 | –C4 | –C5, –I5 | –C6 | Unit |
|---|---|---|---|---|---|
| mpu_base_clk (microprocessor unit clock) | 1050 | 925 | 800 | 700 | MHz |
| main_base_clk (L3/L4 interconnect clock) | 400 | 400 | 400 | 350 | MHz |
| h2f_user0_clk | 100 | 100 | 100 | 100 | MHz |
| h2f_user1_clk | 100 | 100 | 100 | 100 | MHz |
| h2f_user2_clk | 200 | 200 | 200 | 160 | MHz |

### 1.2.4.2. HPS PLL Specifications

#### 1.2.4.2.1. HPS PLL VCO Frequency Range

**Table 49. HPS PLL VCO Frequency Range for Arria V Devices**

| Description | Speed Grade | Minimum | Maximum | Unit |
|---|---|---|---|---|
| VCO range | –C5, –I5, –C6 | 320 | 1,600 | MHz |
| | –C4 | 320 | 1,850 | MHz |
| | –I3 | 320 | 2,100 | MHz |

#### 1.2.4.2.2. HPS PLL Input Clock Range

The HPS PLL input clock range is 10 – 50 MHz. This clock range applies to both HPS_CLK1 and HPS_CLK2 inputs.

**Related Information**

Clock Select, Booting and Configuration chapter
Provides more information about the clock range for different values of clock select (CSEL).

#### 1.2.4.2.3. HPS PLL Input Jitter

Use the following equation to determine the maximum input jitter (peak-to-peak) the HPS PLLs can tolerate. The divide value (N) is the value programmed into the denominator field of the VCO register for each PLL. The PLL input reference clock is divided by this value. The range of the denominator is 1 to 64.

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Maximum input jitter = Input clock period × Divide value (N) × 0.02

**Table 50. Examples of Maximum Input Jitter**

| Input Reference Clock Period | Divide Value (N) | Maximum Jitter | Unit |
|---|---|---|---|
| 40 ns | 1 | 0.8 | ns |
| 40 ns | 2 | 1.6 | ns |
| 40 ns | 4 | 3.2 | ns |

### 1.2.4.3. Quad SPI Flash Timing Characteristics

**Table 51. Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Arria V Devices**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $F_{clk}$ | SCLK_OUT clock frequency (External clock) | — | — | 108 | MHz |
| $T_{qspi_clk}$ | QSPI_CLK clock period (Internal reference clock) | 2.32 | — | — | ns |
| $T_{dutycycle}$ | SCLK_OUT duty cycle | 45 | — | 55 | % |
| $T_{dssfrst}$ | Output delay QSPI_SS valid before first clock edge | — | 1/2 cycle of SCLK_OUT | — | ns |
| $T_{dsslst}$ | Output delay QSPI_SS valid after last clock edge | –1 | — | 1 | ns |
| $T_{dio}$ | I/O data output delay | –1 | — | 1 | ns |
| $T_{din_start}$ | Input data valid start | — | — | $(2 + R_{delay}) \times T_{qspi_clk} - 7.52$ (86) | ns |
| $T_{din_end}$ | Input data valid end | $(2 + R_{delay}) \times T_{qspi_clk} - 1.21$ (86) | — | — | ns |

(86) $R_{delay}$ is set by programming the register `qspiregs.rddatacap`. For the SoC EDS software version 13.1 and later, Intel provides automatic Quad SPI calibration in the preloader. For more information about $R_{delay}$, refer to the *Quad SPI Flash Controller* chapter in the *Arria V Hard Processor System Technical Reference Manual*.

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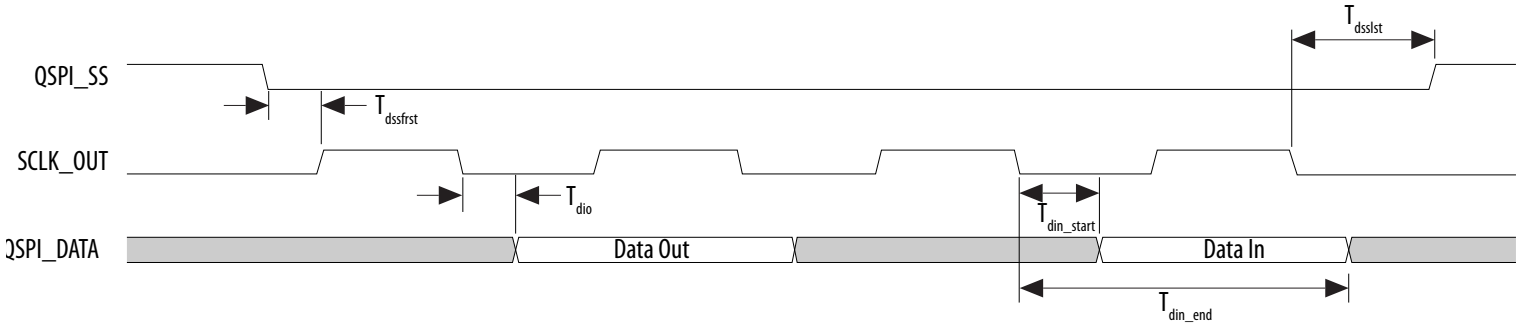
**Figure 9. Quad SPI Flash Timing Diagram**

This timing diagram illustrates clock polarity mode 0 and clock phase mode 0.




**Related Information**

Quad SPI Flash Controller Chapter, Arria V Hard Processor System Technical Reference Manual
Provides more information about $R_{delay}$.

## 1.2.4.4. SPI Timing Characteristics

**Table 52. SPI Master Timing Requirements for Arria V Devices**

The setup and hold times can be used for Texas Instruments SSP mode and National Semiconductor Microwire mode.

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $T_{clk}$ | CLK clock period | 16.67 | — | ns |
| $T_{su}$ | SPI Master-in slave-out (MISO) setup time | 8.35 (87) | — | ns |
| $T_h$ | SPI MISO hold time | 1 | — | ns |

*continued...*

(87) This value is based on `rx_sample_dly` = 1 and `spi_m_clk` = 120 MHz. `spi_m_clk` is the internal clock that is used by SPI Master to derive it's SCLK_OUT. These timings are based on `rx_sample_dly` of 1. This delay can be adjusted as needed to accommodate slower response times from the slave. Note that a delay of 0 is not allowed. The setup time can be used as a reference starting point. It is very crucial to do a calibration to get the correct `rx_sample_dly` value because each SPI slave device may have different output delay and each application board may have different path delay. For more information about `rx_sample_delay`, refer to the *SPI Controller* chapter in the *Hard Processor System Technical Reference Manual*.

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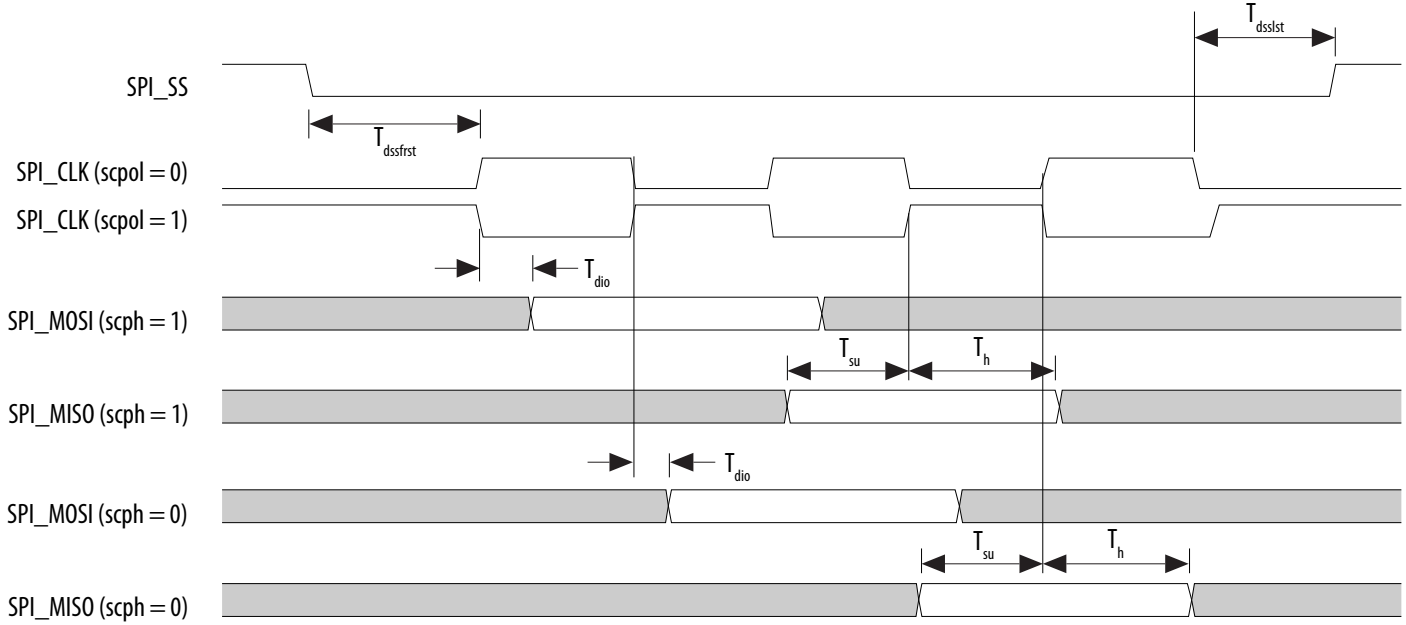
| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $T_{dutycycle}$ | SPI_CLK duty cycle | 45 | 55 | % |
| $T_{dssfrst}$ | Output delay SPI_SS valid before first clock edge | 8 | — | ns |
| $T_{dsslst}$ | Output delay SPI_SS valid after last clock edge | 8 | — | ns |
| $T_{dio}$ | Master-out slave-in (MOSI) output delay | –1 | 1 | ns |

**Figure 10. SPI Master Timing Diagram**



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## Table 53. SPI Slave Timing Requirements for Arria V Devices

The setup and hold times can be used for Texas Instruments SSP mode and National Semiconductor Microwire mode.

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $T_{clk}$ | CLK clock period | 20 | — | ns |
| $T_s$ | MOSI Setup time | 5 | — | ns |
| $T_h$ | MOSI Hold time | 5 | — | ns |
| $T_{suss}$ | Setup time SPI_SS valid before first clock edge | 8 | — | ns |
| $T_{hss}$ | Hold time SPI_SS valid after last clock edge | 8 | — | ns |
| $T_d$ | MISO output delay | — | 6 | ns |

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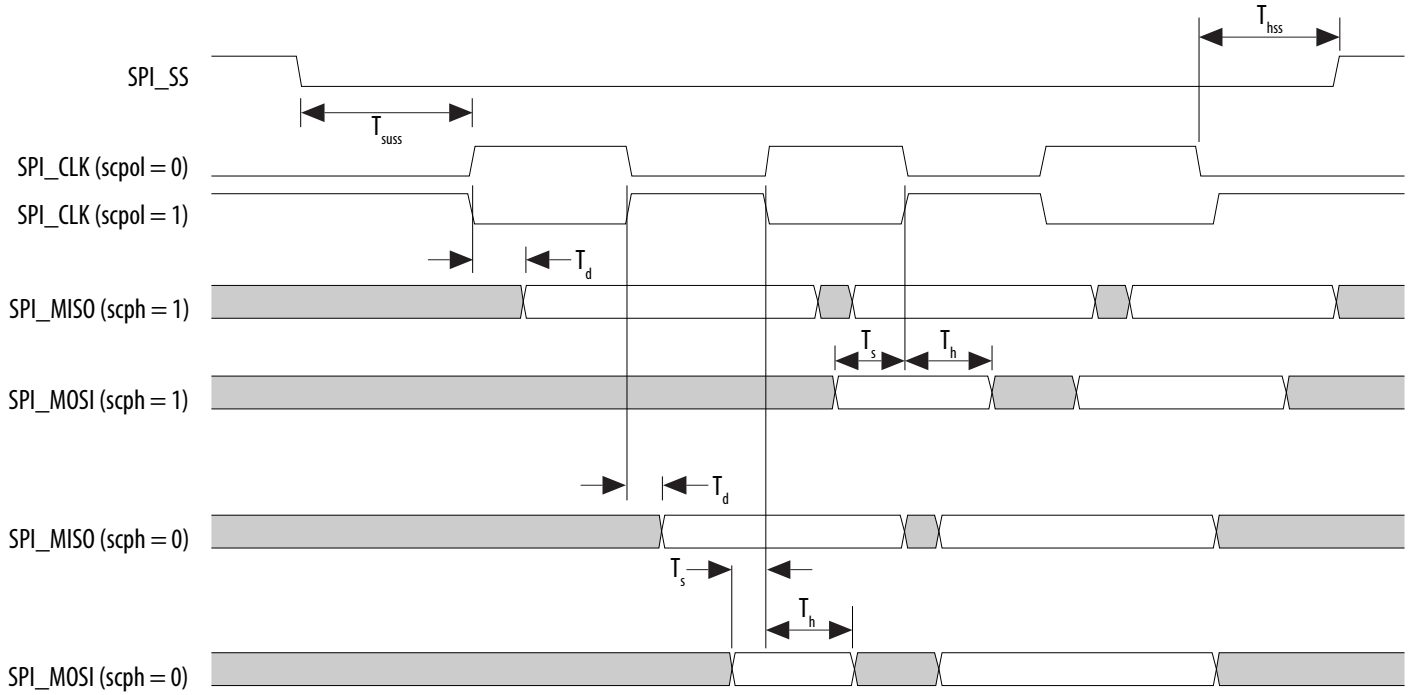
**Figure 11. SPI Slave Timing Diagram**




## Related Information

SPI Controller, Arria V Hard Processor System Technical Reference Manual
Provides more information about `rx_sample_delay`.

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### 1.2.4.5. SD/MMC Timing Characteristics

#### Table 54. Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Arria V Devices

After power up or cold reset, the Boot ROM uses `drvsel` = 3 and `smplsel` = 0 to execute the code. At the same time, the SD/MMC controller enters the Identification Phase followed by the Data Phase. During this time, the value of interface output clock SDMMC_CLK_OUT changes from a maximum of 400 kHz (Identification Phase) up to a maximum of 12.5 MHz (Data Phase), depending on the internal reference clock SDMMC_CLK and the CSEL setting. The value of SDMMC_CLK is based on the external oscillator frequency and has a maximum value of 50 MHz.

After the Boot ROM code exits and control is passed to the preloader, software can adjust the value of `drvsel` and `smplsel` via the system manager. `drvsel` can be set from 1 to 7 and `smplsel` can be set from 0 to 7. While the preloader is executing, the values for SDMMC_CLK and SDMMC_CLK_OUT increase to a maximum of 200 MHz and 50 MHz respectively.

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $T_{sdmmc_clk}$ (internal reference clock) | SDMMC_CLK clock period (Identification mode) | 20 | — | ns |
| | SDMMC_CLK clock period (Default speed mode) | 5 | — | ns |
| | SDMMC_CLK clock period (High speed mode) | 5 | — | ns |
| $T_{sdmmc_clk_out}$ (interface output clock) | SDMMC_CLK_OUT clock period (Identification mode) | 2500 | — | ns |
| | SDMMC_CLK_OUT clock period (Default speed mode) | 40 | — | ns |
| | SDMMC_CLK_OUT clock period (High speed mode) | 20 | — | ns |
| $T_{dutycycle}$ | SDMMC_CLK_OUT duty cycle | 45 | 55 | % |
| $T_d$ | SDMMC_CMD/SDMMC_D output delay | ($T_{sdmmc_clk}$ × `drvsel`)/2 – 1.23 (88) | ($T_{sdmmc_clk}$ × `drvsel`)/2 + 1.69 (88) | ns |
| $T_{su}$ | Input setup time | 1.05 – ($T_{sdmmc_clk}$ × `smplsel`)/2 (89) | — | ns |
| $T_h$ | Input hold time | ($T_{sdmmc_clk}$ × `smplsel`)/2 (89) | — | ns |

(88) `drvsel` is the drive clock phase shift select value.

(89) `smplsel` is the sample clock phase shift select value.

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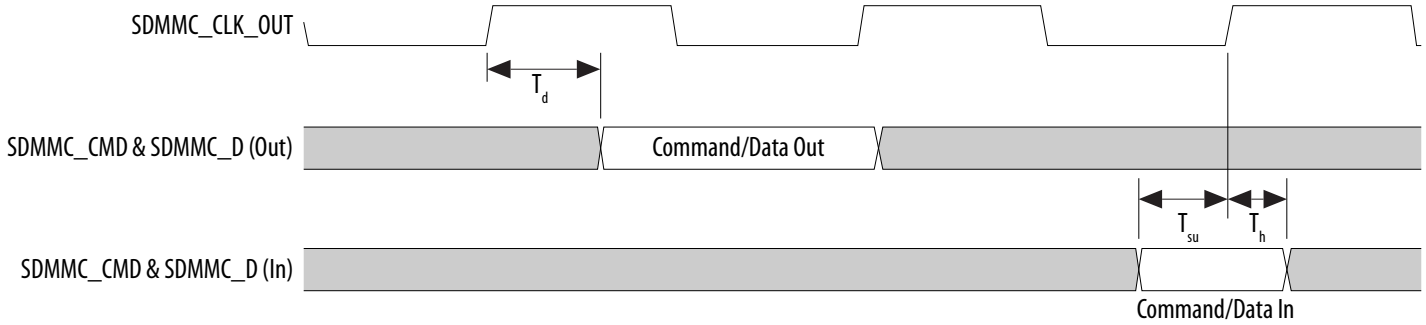
**Figure 12. SD/MMC Timing Diagram**




### Related Information

Booting and Configuration Chapter, Arria V Hard Processor System Technical Reference Manual
Provides more information about CSEL pin settings in the *SD/MMC Controller CSEL Pin Settings* table.

## 1.2.4.6. USB Timing Characteristics

PHYs that support LPM mode may not function properly with the USB controller due to a timing issue. It is recommended that designers use the MicroChip USB3300 PHY device that has been proven to be successful on the development board.

**Table 55. USB Timing Requirements for Arria V Devices**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{clk}$ | USB CLK clock period | — | 16.67 | — | ns |
| $T_d$ | CLK to USB_STP/USB_DATA[7:0] output delay | 4.4 | — | 11 | ns |
| $T_{su}$ | Setup time for USB_DIR/USB_NXT/USB_DATA[7:0] | 2 | — | — | ns |
| $T_h$ | Hold time for USB_DIR/USB_NXT/USB_DATA[7:0] | 1 | — | — | ns |

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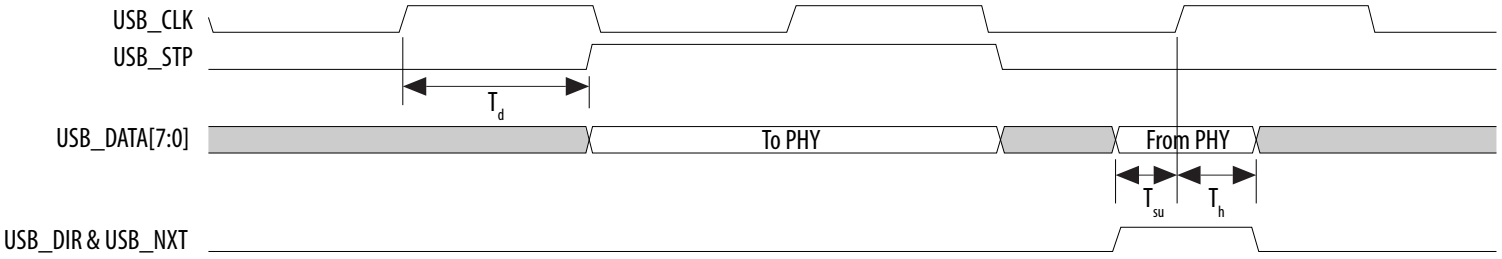
**Figure 13. USB Timing Diagram**

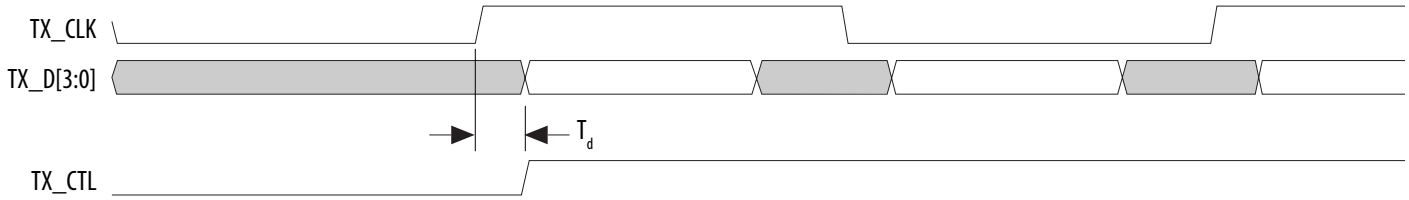



## 1.2.4.7. Ethernet Media Access Controller (EMAC) Timing Characteristics

**Table 56. Reduced Gigabit Media Independent Interface (RGMII) TX Timing Requirements for Arria V Devices**

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{clk}$ (1000Base-T) | TX_CLK clock period | — | 8 | — | ns |
| $T_{clk}$ (100Base-T) | TX_CLK clock period | — | 40 | — | ns |
| $T_{clk}$ (10Base-T) | TX_CLK clock period | — | 400 | — | ns |
| $T_{dutycycle}$ | TX_CLK duty cycle | 45 | — | 55 | % |
| $T_d$ | TX_CLK to TXD/TX_CTL output data delay | –0.85 | — | 0.15 | ns |

**Figure 14. RGMII TX Timing Diagram**



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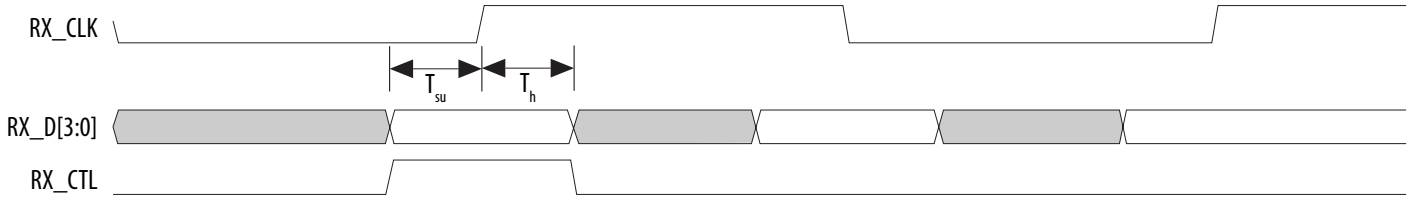
### Table 57. RGMII RX Timing Requirements for Arria V Devices

| Symbol | Description | Min | Typ | Unit |
|---|---|---|---|---|
| $T_{clk}$ (1000Base-T) | RX_CLK clock period | — | 8 | ns |
| $T_{clk}$ (100Base-T) | RX_CLK clock period | — | 40 | ns |
| $T_{clk}$ (10Base-T) | RX_CLK clock period | — | 400 | ns |
| $T_{su}$ | RX_D/RX_CTL setup time | 1 | — | ns |
| $T_h$ | RX_D/RX_CTL hold time | 1 | — | ns |

### Figure 15. RGMII RX Timing Diagram




### Table 58. Management Data Input/Output (MDIO) Timing Requirements for Arria V Devices

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{clk}$ | MDC clock period | — | 400 | — | ns |
| $T_d$ | MDC to MDIO output data delay | 10 | — | 20 | ns |
| $T_s$ | Setup time for MDIO data | 10 | — | — | ns |
| $T_h$ | Hold time for MDIO data | 0 | — | — | ns |

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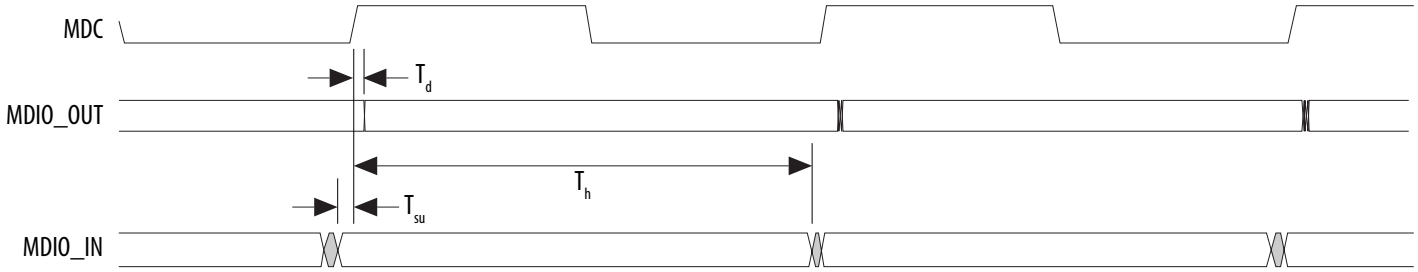
**Figure 16. MDIO Timing Diagram**




## 1.2.4.8. I²C Timing Characteristics

**Table 59. I²C Timing Requirements for Arria V Devices**

| Symbol | Description | Standard Mode | | Fast Mode | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $T_{clk}$ | Serial clock (SCL) clock period | 10 | — | 2.5 | — | µs |
| $T_{clkhigh}$ | SCL high time | 4.7 | — | 0.6 | — | µs |
| $T_{clklow}$ | SCL low time | 4 | — | 1.3 | — | µs |
| $T_s$ | Setup time for serial data line (SDA) data to SCL | 0.25 | — | 0.1 | — | µs |
| $T_h$ | Hold time for SCL to SDA data | 0 | 3.45 | 0 | 0.9 | µs |
| $T_d$ | SCL to SDA output data delay | — | 0.2 | — | 0.2 | µs |
| $T_{su_start}$ | Setup time for a repeated start condition | 4.7 | — | 0.6 | — | µs |
| $T_{hd_start}$ | Hold time for a repeated start condition | 4 | — | 0.6 | — | µs |
| $T_{su_stop}$ | Setup time for a stop condition | 4 | — | 0.6 | — | µs |

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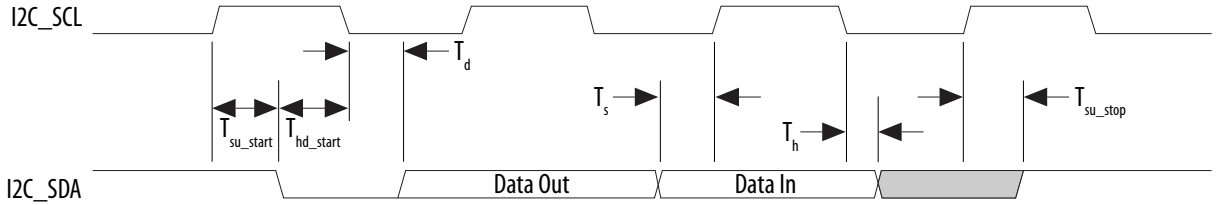
**Figure 17. I²C Timing Diagram**




## 1.2.4.9. NAND Timing Characteristics

**Table 60. NAND ONFI 1.0 Timing Requirements for Arria V Devices**

The NAND controller supports Open NAND FLASH Interface (ONFI) 1.0 Mode 5 timing as well as legacy NAND devices. This table lists the requirements for ONFI 1.0 mode 5 timing. The HPS NAND controller can meet this timing by programming the C4 output of the main HPS PLL and timing registers provided in the NAND controller.

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $T_{wp}$ (90) | Write enable pulse width | 10 | — | ns |
| $T_{wh}$ (90) | Write enable hold time | 7 | — | ns |
| $T_{rp}$ (90) | Read enable pulse width | 10 | — | ns |
| $T_{reh}$ (90) | Read enable hold time | 7 | — | ns |
| $T_{clesu}$ (90) | Command latch enable to write enable setup time | 10 | — | ns |
| $T_{cleh}$ (90) | Command latch enable to write enable hold time | 5 | — | ns |
| $T_{cesu}$ (90) | Chip enable to write enable setup time | 15 | — | ns |
| $T_{ceh}$ (90) | Chip enable to write enable hold time | 5 | — | ns |
| $T_{alesu}$ (90) | Address latch enable to write enable setup time | 10 | — | ns |
| $T_{aleh}$ (90) | Address latch enable to write enable hold time | 5 | — | ns |
| $T_{dsu}$ (90) | Data to write enable setup time | 10 | — | ns |
| $T_{dh}$ (90) | Data to write enable hold time | 5 | — | ns |

*continued...*

(90) Timing of the NAND interface is controlled through the NAND configuration registers.

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| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $T_{cea}$ | Chip enable to data access time | — | 25 | ns |
| $T_{rea}$ | Read enable to data access time | — | 16 | ns |
| $T_{rhz}$ | Read enable to data high impedance | — | 100 | ns |
| $T_{rr}$ | Ready to read enable low | 20 | — | ns |

**Figure 18. NAND Command Latch Timing Diagram**

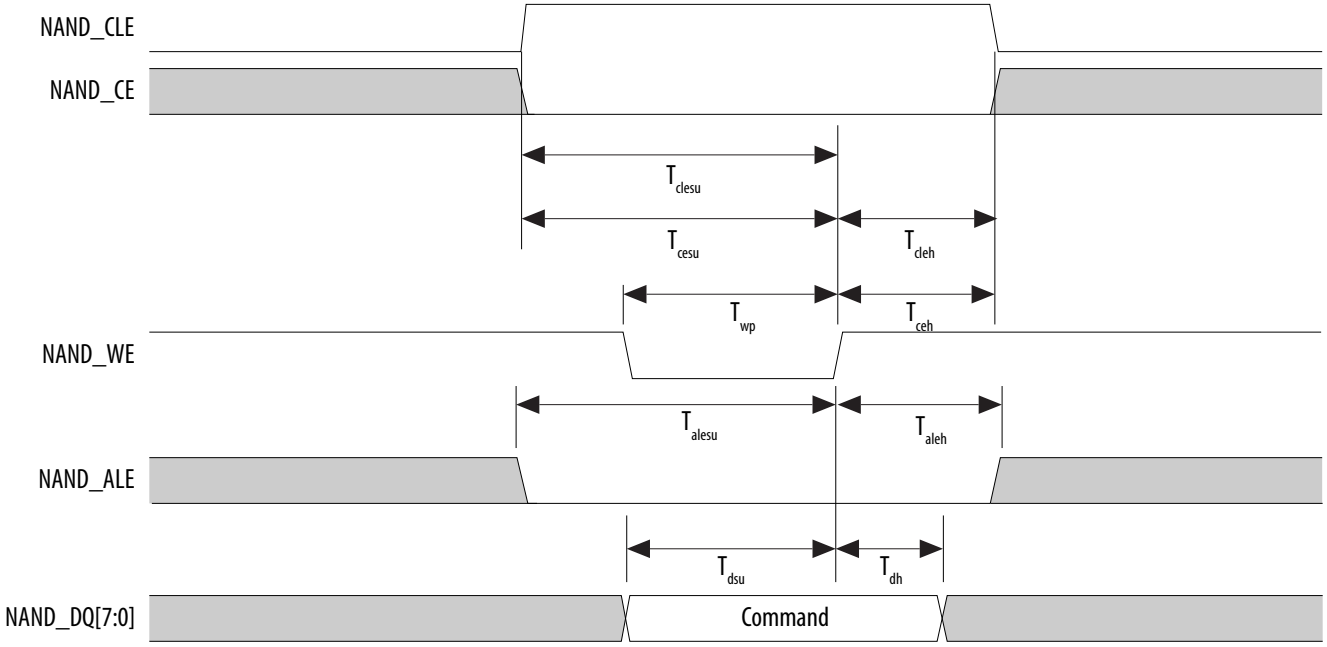

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**Figure 19. NAND Address Latch Timing Diagram**

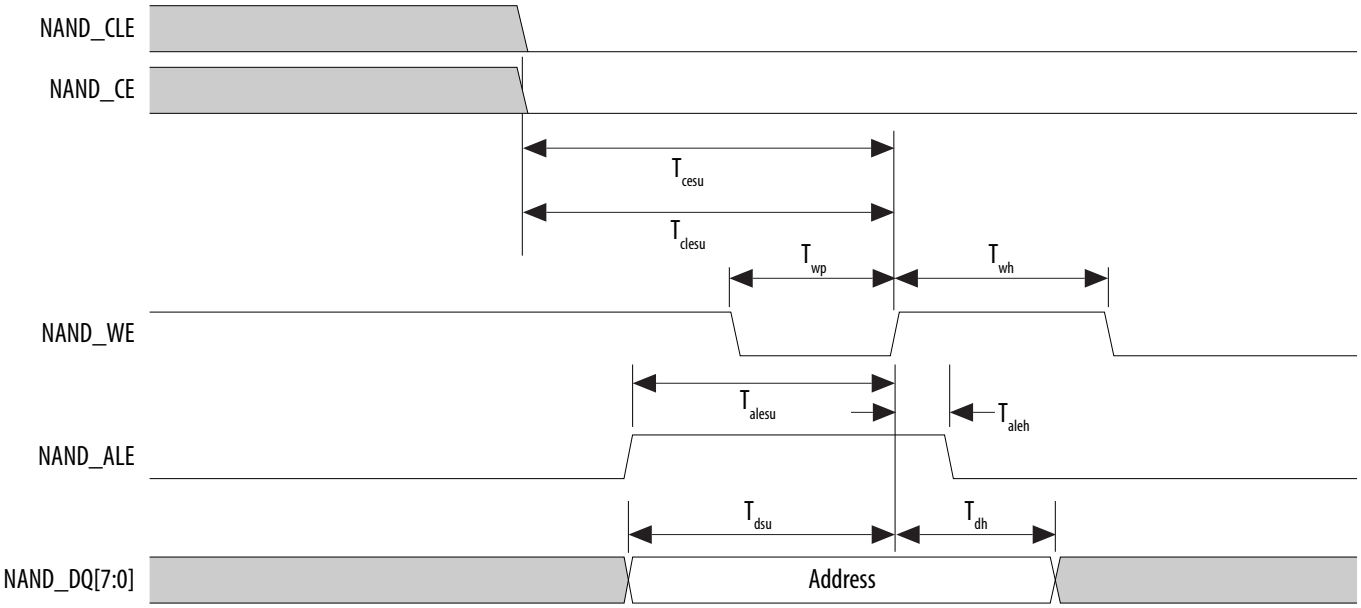

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**Figure 20. NAND Data Write Timing Diagram**

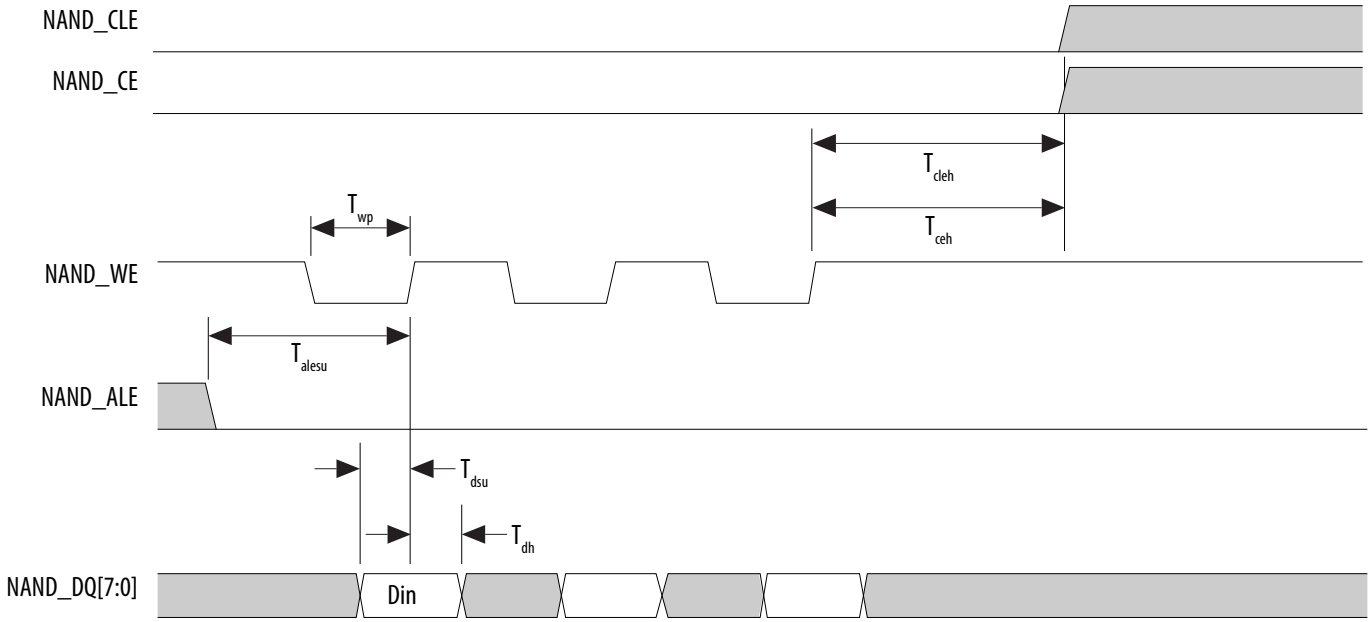

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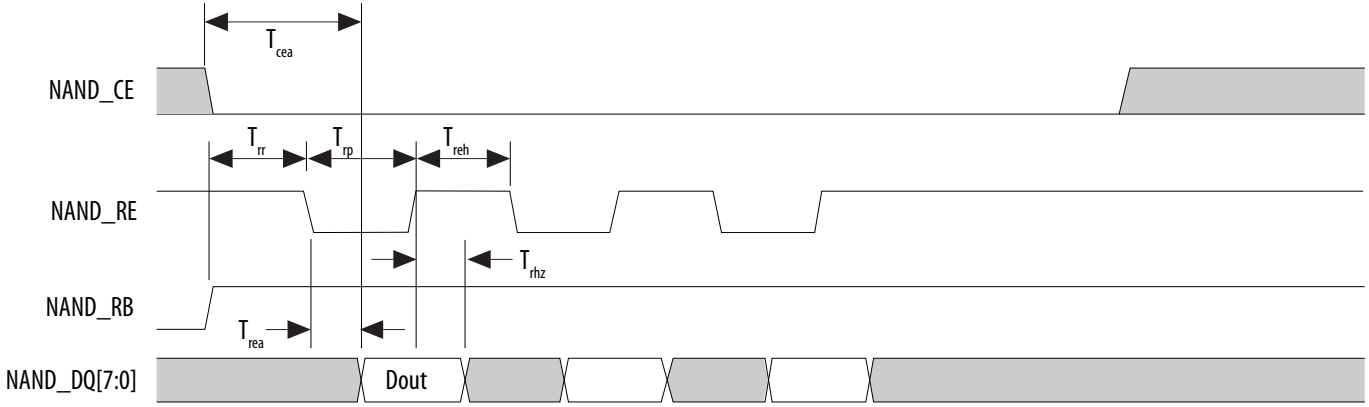
**Figure 21. NAND Data Read Timing Diagram**




## 1.2.4.10. Arm Trace Timing Characteristics

**Table 61. Arm Trace Timing Requirements for Arria V Devices**

Most debugging tools have a mechanism to adjust the capture point of trace data.

| Description | Min | Max | Unit |
|---|---|---|---|
| CLK clock period | 12.5 | — | ns |
| CLK maximum duty cycle | 45 | 55 | % |
| CLK to D0 –D7 output data delay | –1 | 1 | ns |

## 1.2.4.11. UART Interface

The maximum UART baud rate is 6.25 megasymbols per second.

## 1.2.4.12. GPIO Interface

The minimum detectable general-purpose I/O (GPIO) pulse width is 2 µs. The pulse width is based on a debounce clock frequency of 1 MHz.

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### 1.2.4.13. HPS JTAG Timing Specifications

**Table 62. HPS JTAG Timing Parameters and Values for Arria V Devices**

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JCP}$ | TCK clock period | 30 | — | ns |
| $t_{JCH}$ | TCK clock high time | 14 | — | ns |
| $t_{JCL}$ | TCK clock low time | 14 | — | ns |
| $t_{JPSU\ (TDI)}$ | TDI JTAG port setup time | 2 | — | ns |
| $t_{JPSU\ (TMS)}$ | TMS JTAG port setup time | 3 | — | ns |
| $t_{JPH}$ | JTAG port hold time | 5 | — | ns |
| $t_{JPCO}$ | JTAG port clock to output | — | 12(91) | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output | — | 14(91) | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | — | 14(91) | ns |

## 1.3. Configuration Specifications

This section provides configuration specifications and timing for Arria V devices.

### 1.3.1. POR Specifications

**Table 63. Fast and Standard POR Delay Specification for Arria V Devices**

| POR Delay | Minimum | Maximum | Unit |
|---|---|---|---|
| Fast | 4 | 12(92) | ms |
| Standard | 100 | 300 | ms |

(91) A 1-ns adder is required for each $V_{CCIO\ _HPS}$ voltage step down from 3.0 V. For example, $t_{JPCO}$= 13 ns if $V_{CCIO\ _HPS}$ of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.

(92) The maximum pulse width of the fast POR delay is 12 ms, providing enough time for the PCIe hard IP to initialize after the POR trip.

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**Related Information**

MSEL Pin Settings
Provides more information about POR delay based on MSEL pin settings for each configuration scheme.

## 1.3.2. FPGA JTAG Configuration Timing

**Table 64. FPGA JTAG Timing Parameters and Values for Arria V Devices**

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JCP}$ | TCK clock period | 30, 167(93) | — | ns |
| $t_{JCH}$ | TCK clock high time | 14 | — | ns |
| $t_{JCL}$ | TCK clock low time | 14 | — | ns |
| $t_{JPSU\ (TDI)}$ | TDI JTAG port setup time | 2 | — | ns |
| $t_{JPSU\ (TMS)}$ | TMS JTAG port setup time | 3 | — | ns |
| $t_{JPH}$ | JTAG port hold time | 5 | — | ns |
| $t_{JPCO}$ | JTAG port clock to output | — | 12(94) | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output | — | 14(94) | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | — | 14(94) | ns |

## 1.3.3. FPP Configuration Timing

### 1.3.3.1. DCLK-to-DATA[] Ratio (r) for FPP Configuration

Fast passive parallel (FPP) configuration requires a different DCLK-to-DATA[] ratio when you turn on encryption or the compression feature.

(93) The minimum TCK clock period is 167 ns if $V_{CCBAT}$ is within the range 1.2 V – 1.5 V when you perform the volatile key programming.

(94) A 1-ns adder is required for each VCCIO voltage step down from 3.0 V. For example, tJPCO= 13 ns if VCCIO of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.

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Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is *r* times the DATA[] rate in byte per second (Bps) or word per second (Wps). For example, in FPP ×16 where the *r* is 2, the DCLK frequency must be 2 times the DATA[] rate in Wps.

**Table 65. DCLK-to-DATA[] Ratio for Arria V Devices**

| Configuration Scheme | Encryption | Compression | DCLK-to-DATA[] Ratio (r) |
|---|---|---|---|
| FPP (8-bit wide) | Off | Off | 1 |
| | On | Off | 1 |
| | Off | On | 2 |
| | On | On | 2 |
| FPP (16-bit wide) | Off | Off | 1 |
| | On | Off | 2 |
| | Off | On | 4 |
| | On | On | 4 |

### 1.3.3.2. FPP Configuration Timing when DCLK-to-DATA[] = 1

When you enable decompression or the design security feature, the DCLK-to-DATA[] ratio varies for FPP ×8 and FPP ×16. For the respective DCLK-to-DATA[] ratio, refer to the *DCLK-to-DATA[] Ratio for Arria V Devices* table.

**Table 66. FPP Timing Parameters When DCLK-to-DATA[] Ratio is 1 for Arria V Devices**

| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{CF2CD}$ | nCONFIG low to CONF_DONE low | — | 600 | ns |
| $t_{CF2ST0}$ | nCONFIG low to nSTATUS low | — | 600 | ns |
| $t_{CFG}$ | nCONFIG low pulse width | 2 | — | µs |
| $t_{STATUS}$ | nSTATUS low pulse width | 268 | 1506(95) | µs |

*continued...*

(95) You can obtain this value if you do not delay configuration by extending the nCONFIG or the nSTATUS low pulse width.

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| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{CF2ST1}$ | nCONFIG high to nSTATUS high | — | 1506(96) | µs |
| $t_{CF2CK}$(97) | nCONFIG high to first rising edge on DCLK | 1506 | — | µs |
| $t_{ST2CK}$(97) | nSTATUS high to first rising edge of DCLK | 2 | — | µs |
| $t_{DSU}$ | DATA[] setup time before rising edge on DCLK | 5.5 | — | ns |
| $t_{DH}$ | DATA[] hold time after rising edge on DCLK | 0 | — | ns |
| $t_{CH}$ | DCLK high time | 0.45 × 1/$f_{MAX}$ | — | s |
| $t_{CL}$ | DCLK low time | 0.45 × 1/$f_{MAX}$ | — | s |
| $t_{CLK}$ | DCLK period | 1/$f_{MAX}$ | — | s |
| $f_{MAX}$ | DCLK frequency (FPP ×8/ ×16) | — | 125 | MHz |
| $t_{CD2UM}$ | CONF_DONE high to user mode(98) | 175 | 437 | µs |
| $t_{CD2CU}$ | CONF_DONE high to CLKUSR enabled | 4× maximum DCLK period | — | — |
| $t_{CD2UMC}$ | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU}$ + ($T_{init}$ × CLKUSR period) | — | — |
| $T_{init}$ | Number of clock cycles required for device initialization | 8,576 | — | Cycles |

## Related Information

FPP Configuration Timing
Provides the FPP configuration timing waveforms.

(96) You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.

(97) If nSTATUS is monitored, follow the $t_{ST2CK}$ specification. If nSTATUS is not monitored, follow the $t_{CF2CK}$ specification.

(98) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

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### 1.3.3.3. FPP Configuration Timing when DCLK-to-DATA[] >1

**Table 67. FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Arria V Devices**

Use these timing parameters when you use the decompression and design security features.

| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{CF2CD}$ | nCONFIG low to CONF_DONE low | — | 600 | ns |
| $t_{CF2ST0}$ | nCONFIG low to nSTATUS low | — | 600 | ns |
| $t_{CFG}$ | nCONFIG low pulse width | 2 | — | µs |
| $t_{STATUS}$ | nSTATUS low pulse width | 268 | 1506(99) | µs |
| $t_{CF2ST1}$ | nCONFIG high to nSTATUS high | — | 1506(100) | µs |
| $t_{CF2CK}$(101) | nCONFIG high to first rising edge on DCLK | 1506 | — | µs |
| $t_{ST2CK}$(101) | nSTATUS high to first rising edge of DCLK | 2 | — | µs |
| $t_{DSU}$ | DATA[] setup time before rising edge on DCLK | 5.5 | — | ns |
| $t_{DH}$ | DATA[] hold time after rising edge on DCLK | $N - 1/f_{DCLK}$(102) | — | s |
| $t_{CH}$ | DCLK high time | $0.45 \times 1/f_{MAX}$ | — | s |
| $t_{CL}$ | DCLK low time | $0.45 \times 1/f_{MAX}$ | — | s |
| $t_{CLK}$ | DCLK period | $1/f_{MAX}$ | — | s |
| $f_{MAX}$ | DCLK frequency (FPP ×8/ ×16) | — | 125 | MHz |
| $t_R$ | Input rise time | — | 40 | ns |
| $t_F$ | Input fall time | — | 40 | ns |

*continued...*

(99) This value can be obtained if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(100) This value can be obtained if you do not delay configuration by externally holding nSTATUS low.

(101) If nSTATUS is monitored, follow the $t_{ST2CK}$ specification. If nSTATUS is not monitored, follow the $t_{CF2CK}$ specification.

(102) *N* is the DCLK-to-DATA[] ratio and $f_{DCLK}$ is the DCLK frequency of the system.

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| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{CD2UM}$ | CONF_DONE high to user mode(103) | 175 | 437 | µs |
| $t_{CD2CU}$ | CONF_DONE high to CLKUSR enabled | 4 × maximum DCLK period | — | — |
| $t_{CD2UMC}$ | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU}$ + ($T_{init}$ × CLKUSR period) | — | — |
| $T_{init}$ | Number of clock cycles required for device initialization | 8,576 | — | Cycles |

**Related Information**

FPP Configuration Timing
Provides the FPP configuration timing waveforms.

## 1.3.4. Active Serial (AS) Configuration Timing

### Table 68. AS Timing Parameters for AS ×1 and ×4 Configurations in Arria V Devices

The minimum and maximum numbers apply to both the internal oscillator and CLKUSR when either one is used as the clock source for device configuration.

The $t_{CF2CD}$, $t_{CF2ST0}$, $t_{CFG}$, $t_{STATUS}$, and $t_{CF2ST1}$ timing parameters are identical to the timing parameters for passive serial (PS) mode listed in *PS Timing Parameters for Arria V Devices* table. You can obtain the $t_{CF2ST1}$ value if you do not delay configuration by externally holding nSTATUS low.

| Symbol | Parameter | Condition | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| $t_{CO}$ (104) | DCLK falling edge to the AS_DATA0/ASDO output | — | — | 2 | ns |
| $t_{SU}$(105) | Data setup time before the falling edge on DCLK | — | 1.5 | — | ns |
| $t_{DH}$(105) | Data hold time after the falling edge on DCLK | –3 speed grade | 1.7 | — | ns |
| | | –4 speed grade | 2.0 | — | ns |

*continued...*

(103) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

(104) Load capacitance for DCLK = 6 pF and AS_DATA/ASDO = 8 pF. Intel recommends obtaining the $t_{CO}$ for a given link (including receiver, transmission lines, connectors, termination resistors, and other components) through IBIS or HSPICE simulation.

(105) To evaluate the data setup ($t_{SU}$) and data hold time ($t_{DH}$) slack on your board in order to ensure you are meeting the $t_{SU}$ and $t_{DH}$ requirement, Intel recommends following the guideline in the "Evaluating Data Setup and Hold Timing Slack" chapter in *AN822: Intel FPGA Configuration Device Migration Guideline*.

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| Symbol | Parameter | Condition | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| | | –5 speed grade | 2.3 | — | ns |
| | | –6 speed grade | 2.6 | — | ns |
| $t_{CD2UM}$ | CONF_DONE high to user mode | — | 175 | 437 | µs |
| $t_{CD2CU}$ | CONF_DONE high to CLKUSR enabled | — | 4 × maximum DCLK period | — | — |
| $t_{CD2UMC}$ | CONF_DONE high to user mode with CLKUSR option on | — | $t_{CD2CU}$ + ($T_{init}$ × CLKUSR period) | — | — |
| $T_{init}$ | Number of clock cycles required for device initialization | — | 8,576 | — | Cycles |

**Related Information**

- Passive Serial (PS) Configuration Timing on page 81
- AS Configuration Timing
  Provides the AS configuration timing waveform.
- Evaluating Data Setup and Hold Timing Slack chapter, AN822: Intel FPGA Configuration Device Migration Guideline

## 1.3.5. DCLK Frequency Specification in the AS Configuration Scheme

### Table 69. DCLK Frequency Specification in the AS Configuration Scheme

This table lists the internal clock frequency specification for the AS configuration scheme. The DCLK frequency specification applies when you use the internal oscillator as the configuration clock source. The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

| Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|
| DCLK frequency in AS configuration scheme | 5.3 | 7.9 | 12.5 | MHz |
| | 10.6 | 15.7 | 25.0 | MHz |
| | 21.3 | 31.4 | 50.0 | MHz |
| | 42.6 | 62.9 | 100.0 | MHz |

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## 1.3.6. Passive Serial (PS) Configuration Timing

### Table 70. PS Timing Parameters for Arria V Devices

| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{CF2CD}$ | nCONFIG low to CONF_DONE low | — | 600 | ns |
| $t_{CF2ST0}$ | nCONFIG low to nSTATUS low | — | 600 | ns |
| $t_{CFG}$ | nCONFIG low pulse width | 2 | — | µs |
| $t_{STATUS}$ | nSTATUS low pulse width | 268 | 1506(106) | µs |
| $t_{CF2ST1}$ | nCONFIG high to nSTATUS high | — | 1506(107) | µs |
| $t_{CF2CK}$(108) | nCONFIG high to first rising edge on DCLK | 1506 | — | µs |
| $t_{ST2CK}$(108) | nSTATUS high to first rising edge of DCLK | 2 | — | µs |
| $t_{DSU}$ | DATA[] setup time before rising edge on DCLK | 5.5 | — | ns |
| $t_{DH}$ | DATA[] hold time after rising edge on DCLK | 0 | — | ns |
| $t_{CH}$ | DCLK high time | 0.45 × 1/$f_{MAX}$ | — | s |
| $t_{CL}$ | DCLK low time | 0.45 × 1/$f_{MAX}$ | — | s |
| $t_{CLK}$ | DCLK period | 1/$f_{MAX}$ | — | s |
| $f_{MAX}$ | DCLK frequency | — | 125 | MHz |
| $t_{CD2UM}$ | CONF_DONE high to user mode(109) | 175 | 437 | µs |

*continued...*

(106) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(107) You can obtain this value if you do not delay configuration by externally holding nSTATUS low.

(108) If nSTATUS is monitored, follow the $t_{ST2CK}$ specification. If nSTATUS is not monitored, follow the $t_{CF2CK}$ specification.

(109) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

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| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{CD2CU}$ | CONF_DONE high to CLKUSR enabled | 4 × maximum DCLK period | — | — |
| $t_{CD2UMC}$ | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU}$ + ($T_{init}$ × CLKUSR period) | — | — |
| $T_{init}$ | Number of clock cycles required for device initialization | 8,576 | — | Cycles |

**Related Information**

PS Configuration Timing
Provides the PS configuration timing waveform.

## 1.3.7. Initialization

**Table 71. Initialization Clock Source Option and the Maximum Frequency for Arria V Devices**

| Initialization Clock Source | Configuration Scheme | Maximum Frequency (MHz) | Minimum Number of Clock Cycles |
|---|---|---|---|
| Internal Oscillator | AS, PS, and FPP | 12.5 | $T_{init}$ |
| CLKUSR(110) | PS and FPP | 125 | |
| | AS | 100 | |
| DCLK | PS and FPP | 125 | |

(110) To enable CLKUSR as the initialization clock source, turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Intel Quartus Prime software from the **General** panel of the **Device and Pin Options** dialog box.

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## 1.3.8. Configuration Files

### Table 72. Uncompressed .rbf Sizes for Arria V Devices

Use this table to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal file (`.hex`) or tabular text file (`.ttf`) format, have different file sizes.

For the different types of configuration file and file sizes, refer to the Intel Quartus Prime software. However, for a specific version of the Intel Quartus Prime software, any design targeted for the same device has the same uncompressed configuration file size.

The IOCSR raw binary file (`.rbf`) size is specifically for the Configuration via Protocol (CvP) feature.

| Variant | Member Code | Configuration .rbf Size (bits) | IOCSR .rbf Size (bits) |
|---|---|---|---|
| Arria V GX | A1 | 71,015,712 | 439,960 |
| | A3 | 71,015,712 | 439,960 |
| | A5 | 101,740,800 | 446,360 |
| | A7 | 101,740,800 | 446,360 |
| | B1 | 137,785,088 | 457,368 |
| | B3 | 137,785,088 | 457,368 |
| | B5 | 185,915,808 | 463,128 |
| | B7 | 185,915,808 | 463,128 |
| Arria V GT | C3 | 71,015,712 | 439,960 |
| | C7 | 101,740,800 | 446,360 |
| | D3 | 137,785,088 | 457,368 |
| | D7 | 185,915,808 | 463,128 |
| Arria V SX | B3 | 185,903,680 | 450,968 |
| | B5 | 185,903,680 | 450,968 |
| Arria V ST | D3 | 185,903,680 | 450,968 |
| | D5 | 185,903,680 | 450,968 |

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## 1.3.9. Minimum Configuration Time Estimation

### Table 73. Minimum Configuration Time Estimation for Arria V Devices

The estimated values are based on the configuration `.rbf` sizes in Uncompressed .rbf Sizes for Arria V Devices table.

| Variant | Member Code | Active Serial(111) | | | Fast Passive Parallel(112) | | |
|---|---|---|---|---|---|---|---|
| | | Width | DCLK (MHz) | Minimum Configuration Time (ms) | Width | DCLK (MHz) | Minimum Configuration Time (ms) |
| Arria V GX | A1 | 4 | 100 | 178 | 16 | 125 | 36 |
| | A3 | 4 | 100 | 178 | 16 | 125 | 36 |
| | A5 | 4 | 100 | 255 | 16 | 125 | 51 |
| | A7 | 4 | 100 | 255 | 16 | 125 | 51 |
| | B1 | 4 | 100 | 344 | 16 | 125 | 69 |
| | B3 | 4 | 100 | 344 | 16 | 125 | 69 |
| | B5 | 4 | 100 | 465 | 16 | 125 | 93 |
| | B7 | 4 | 100 | 465 | 16 | 125 | 93 |
| Arria V GT | C3 | 4 | 100 | 178 | 16 | 125 | 36 |
| | C7 | 4 | 100 | 255 | 16 | 125 | 51 |
| | D3 | 4 | 100 | 344 | 16 | 125 | 69 |
| | D7 | 4 | 100 | 465 | 16 | 125 | 93 |
| Arria V SX | B3 | 4 | 100 | 465 | 16 | 125 | 93 |
| | B5 | 4 | 100 | 465 | 16 | 125 | 93 |
| Arria V ST | D3 | 4 | 100 | 465 | 16 | 125 | 93 |
| | D5 | 4 | 100 | 465 | 16 | 125 | 93 |

(111) DCLK frequency of 100 MHz using external CLKUSR.

(112) Maximum FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

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**Related Information**

Configuration Files on page 83

## 1.3.10. Remote System Upgrades

**Table 74. Remote System Upgrade Circuitry Timing Specifications for Arria V Devices**

| Parameter | Minimum | Unit |
|---|---|---|
| $t_{RU_nCONFIG}$(113) | 250 | ns |
| $t_{RU_nRSTIMER}$(114) | 250 | ns |

**Related Information**

- Remote System Upgrade State Machine
  Provides more information about configuration reset (RU_CONFIG) signal.
- User Watchdog Timer
  Provides more information about reset_timer (RU_nRSTIMER) signal.

## 1.3.11. User Watchdog Internal Oscillator Frequency Specifications

**Table 75. User Watchdog Internal Oscillator Frequency Specifications for Arria V Devices**

| Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|
| User watchdog internal oscillator frequency | 5.3 | 7.9 | 12.5 | MHz |

# 1.4. I/O Timing

Intel offers two ways to determine I/O timing—the Excel-based I/O timing and the Intel Quartus Prime Timing Analyzer.

(113) This is equivalent to strobing the reconfiguration input of the Remote Update Intel FPGA IP core high for the minimum timing specification.

(114) This is equivalent to strobing the reset timer input of the Remote Update Intel FPGA IP core high for the minimum timing specification.

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Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

The Intel Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

**Related Information**

Arria V I/O Timing Spreadsheet
Provides the Arria V Excel-based I/O timing spreadsheet.

## 1.4.1. Programmable IOE Delay

**Table 76. I/O element (IOE) Programmable Delay for Arria V Devices**

| Parameter[115] | Available Settings | Minimum Offset[116] | Fast Model | | Slow Model | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | –C4 | –C5 | –C6 | –I3 | –I5 | |
| D1 | 32 | 0 | 0.508 | 0.517 | 0.870 | 1.063 | 1.063 | 0.872 | 1.057 | ns |
| D3 | 8 | 0 | 1.763 | 1.795 | 2.999 | 3.496 | 3.571 | 3.031 | 3.643 | ns |
| D4 | 32 | 0 | 0.508 | 0.518 | 0.869 | 1.063 | 1.063 | 1.063 | 1.057 | ns |
| D5 | 32 | 0 | 0.508 | 0.517 | 0.870 | 1.063 | 1.063 | 0.872 | 1.057 | ns |

(115) You can set this value in the Intel Quartus Prime software by selecting **D1**, **D3**, **D4**, and **D5** in the **Assignment Name** column of **Assignment Editor**.

(116) Minimum offset does not include the intrinsic delay.

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## 1.4.2. Programmable Output Buffer Delay

### Table 77. Programmable Output Buffer Delay for Arria V Devices

This table lists the delay chain settings that control the rising and falling edge delays of the output buffer.

You can set the programmable output buffer delay in the Intel Quartus Prime software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

| Symbol | Parameter | Typical | Unit |
|---|---|---|---|
| $D_{OUTBUF}$ | Rising and/or falling edge delay | 0 (default) | ps |
| | | 50 | ps |
| | | 100 | ps |
| | | 150 | ps |

## 1.5. Glossary

### Table 78. Glossary

| Term | Definition |
|---|---|
| Differential I/O standards | Receiver Input Waveforms |

*continued...*

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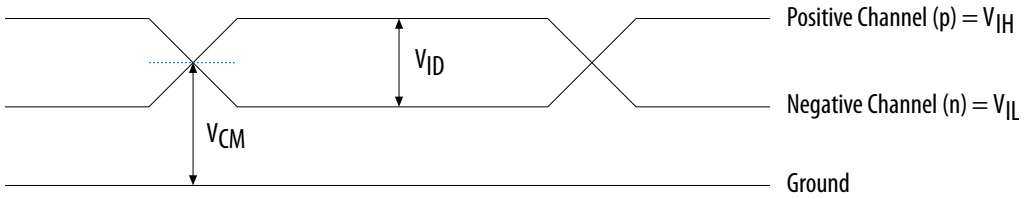
| Term | Definition |
|---|---|
| | **Single-Ended Waveform**<br>  <br><br>**Differential Waveform**<br> <br><br>Transmitter Output Waveforms |

continued...

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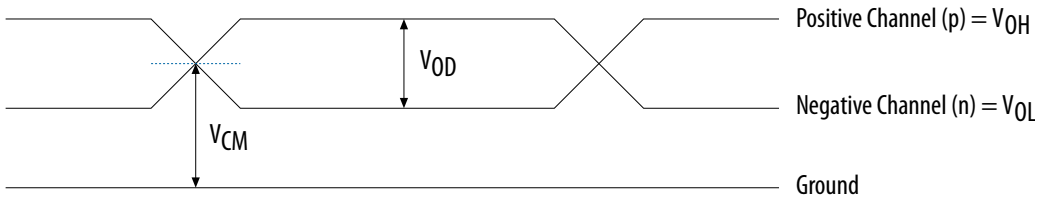
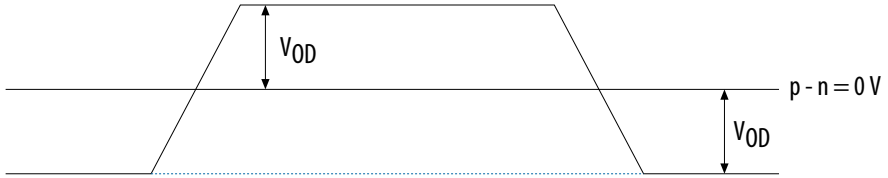
| Term | Definition |
|---|---|
| | **Single-Ended Waveform**<br>  <br><br>**Differential Waveform**<br>  <br> |
| $f_{HSCLK}$ | Left/right PLL input clock frequency. |
| $f_{HSDR}$ | High-speed I/O block—Maximum/minimum LVDS data transfer rate ($f_{HSDR}$ =1/TUI). |
| J | High-speed I/O block—Deserialization factor (width of parallel data bus). |
| JTAG timing specifications | JTAG Timing Specifications |

*continued...*

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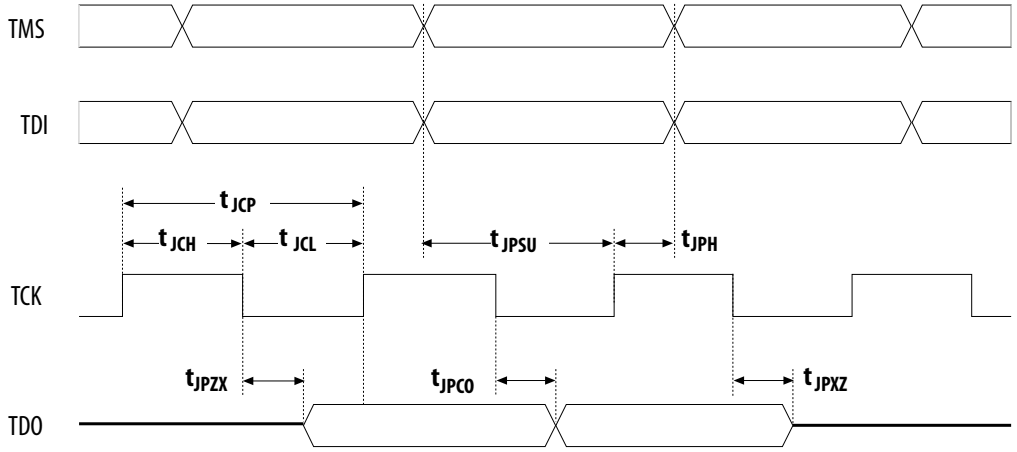
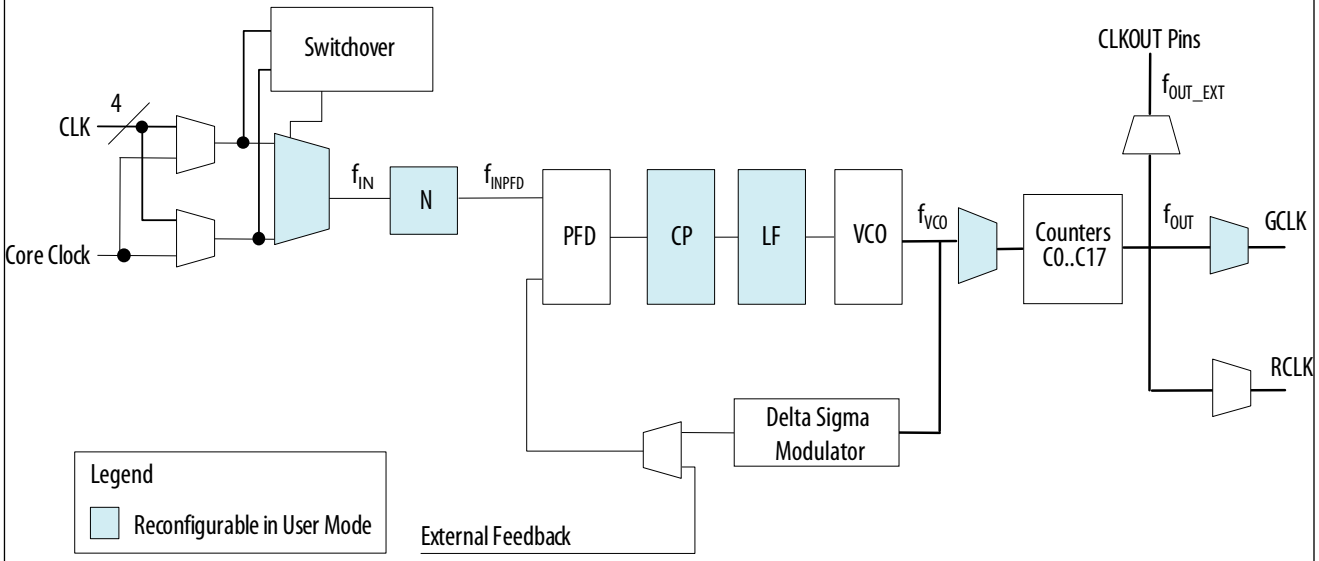
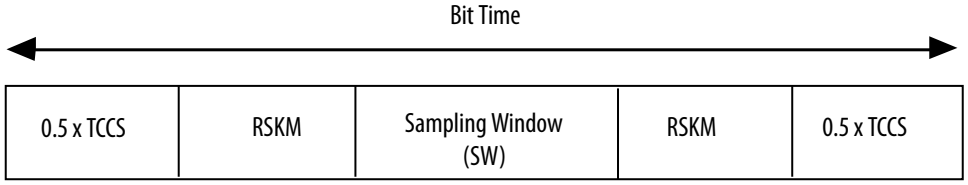
| Term | Definition |
|---|---|
| |  |
| PLL specifications | Diagram of PLL specifications |

continued...

| Term | Definition |
|---|---|
| |  <br>Note:<br>(1) Core Clock can only be fed by dedicated clock input pins or PLL outputs. |
| $R_L$ | Receiver differential input discrete resistor (external to the Arria V device). |
| Sampling window (SW) | Timing diagram—The period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window, as shown:<br>  |

*continued...*

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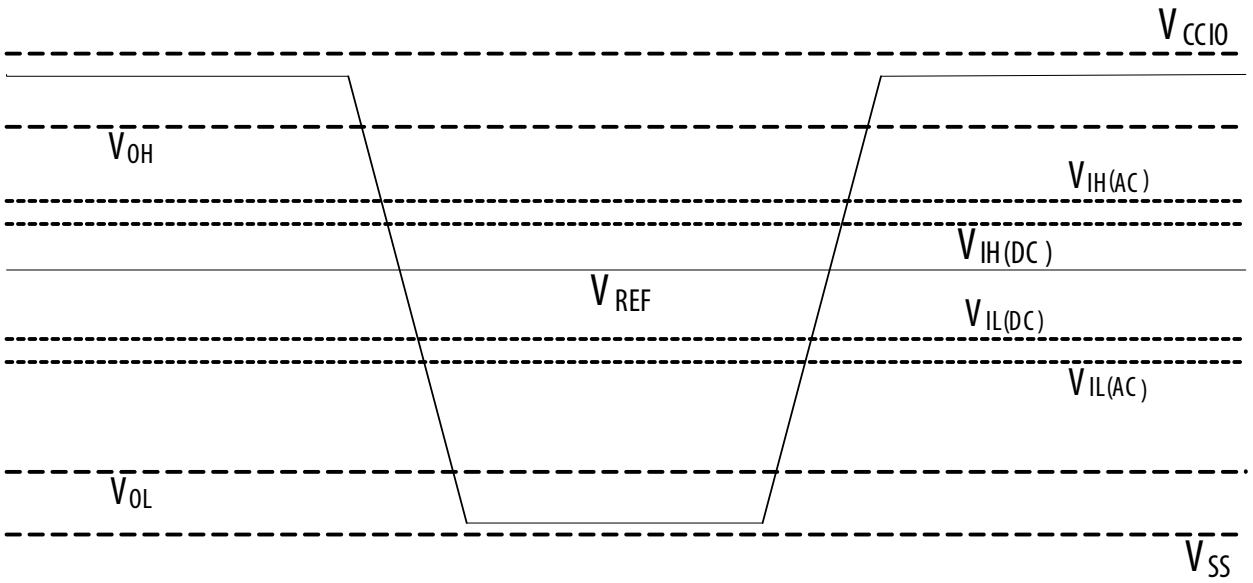
| Term | Definition |
|---|---|
| Single-ended voltage referenced I/O standard | The JEDEC standard for the SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.<br>The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing.<br>Single-Ended Voltage Referenced I/O Standard<br>  |
| $t_C$ | High-speed receiver/transmitter input and output clock period. |
| TCCS (channel-to-channel-skew) | The timing difference between the fastest and slowest output edges, including the $t_{CO}$ variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table). |
| $t_{DUTY}$ | High-speed I/O block—Duty cycle on high-speed transmitter output clock. |
| $t_{FALL}$ | Signal high-to-low transition time (80–20%) |
| $t_{INCCJ}$ | Cycle-to-cycle jitter tolerance on the PLL clock input |

continued...

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| Term | Definition |
|---|---|
| $t_{OUTPJ_IO}$ | Period jitter on the GPIO driven by a PLL |
| $t_{OUTPJ_DC}$ | Period jitter on the dedicated clock output driven by a PLL |
| $t_{RISE}$ | Signal low-to-high transition time (20–80%) |
| Timing Unit Interval (TUI) | The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = $t_C$/w) |
| $V_{CM(DC)}$ | DC common mode input voltage. |
| $V_{ICM}$ | Input common mode voltage—The common mode of the differential signal at the receiver. |
| $V_{ID}$ | Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver. |
| $V_{DIF(AC)}$ | AC differential input voltage—Minimum AC input differential voltage required for switching. |
| $V_{DIF(DC)}$ | DC differential input voltage— Minimum DC input differential voltage required for switching. |
| $V_{IH}$ | Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high. |
| $V_{IH(AC)}$ | High-level AC input voltage |
| $V_{IH(DC)}$ | High-level DC input voltage |
| $V_{IL}$ | Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low. |
| $V_{IL(AC)}$ | Low-level AC input voltage |
| $V_{IL(DC)}$ | Low-level DC input voltage |
| $V_{OCM}$ | Output common mode voltage—The common mode of the differential signal at the transmitter. |
| $V_{OD}$ | Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission line at the transmitter. |
| $V_{SWING}$ | Differential input voltage |
| $V_X$ | Input differential cross point voltage |
| $V_{OX}$ | Output differential cross point voltage |
| W | High-speed I/O block—Clock boost factor |

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## 1.6. Arria V GX, GT, SX, and ST Device Datasheet Revision History

| Document Version | Changes |
|---|---|
| 2019.04.26 | • Added a note for Conversion Time in the *Internal Temperature Sensing Diode Specifications for Arria V Devices* table.<br>• Updated $t_{DH}$ specifications in the *AS Timing Parameters for AS ×1 and ×4 Configurations in Arria V Devices* table. |
| 2019.01.25 | • Added *Arria V Devices Overshoot Duration* diagram.<br>• Changed "VCO post-scale counter K value" to "VCO post divider value" in the $f_{VCO}$ note in the *PLL Specifications for Arria V Devices* table.<br>• Updated the *AS Timing Parameters for AS ×1 and ×4 Configurations in Arria V Devices* table.<br>— Updated $t_{DH}$ specifications. These specifications are applicable to the commercial and industrial grade devices.<br>— Added note to $t_{CO}$, $t_{SU}$, and $t_{DH}$.<br>• Removed PowerPlay text from tool name.<br>• Renamed IP cores as per Intel rebranding. |

| Date | Version | Changes |
|---|---|---|
| December 2016 | 2016.12.09 | • Updated $V_{ICM}$ (AC coupled) specifications in Receiver Specifications for Arria V GX and SX Devices table.<br>• Added maximum specification for $T_d$ in Management Data Input/Output (MDIO) Timing Requirements for Arria V Devices table.<br>• Updated $T_{init}$ specifications in the following tables:<br>— FPP Timing Parameters When DCLK-to-DATA[] Ratio is 1 for Arria V Devices<br>— FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Arria V Devices<br>— AS Timing Parameters for AS ×1 and ×4 Configurations in Arria V Devices<br>— PS Timing Parameters for Arria V Devices |
| June 2016 | 2016.06.10 | • Changed pin capacitance to maximum values.<br>• Updated SPI Master Timing Requirements for Arria V Devices table.<br>— Added $T_{su}$ and $T_h$ specifications.<br>— Removed $T_{dinmax}$ specifications.<br>• Updated SPI Master Timing Diagram.<br>• Updated $T_{clk}$ spec from maximum to minimum in $I^2C$ Timing Requirements for Arria V Devices table. |

*continued...*

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| Date | Version | Changes |
|---|---|---|
| December 2015 | 2015.12.16 | • Updated Quad Serial Peripheral Interface (SPI) Flash Timing Requirements for Arria V Devices table.<br>— Updated $F_{clk}$, $T_{dutycycle}$, and $T_{dssfrst}$ specifications.<br>— Added $T_{qspi_clk}$, $T_{din_start}$, and $T_{din_end}$ specifications.<br>— Removed $T_{dinmax}$ specifications.<br>• Updated the minimum specification for $T_{clk}$ to 16.67 ns and removed the maximum specification in SPI Master Timing Requirements for Arria V Devices table.<br>• Updated Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Arria V Devices table.<br>— Updated $T_{clk}$ to $T_{sdmmc_clk_out}$ symbol.<br>— Updated $T_{sdmmc_clk_out}$ and $T_d$ specifications.<br>— Added $T_{sdmmc_clk}$, $T_{su}$, and $T_h$ specifications.<br>— Removed $T_{dinmax}$ specifications.<br>• Updated the following diagrams:<br>— Quad SPI Flash Timing Diagram<br>— SD/MMC Timing Diagram<br>• Updated configuration .rbf sizes for Arria V devices.<br>• Changed instances of *Quartus II* to *Quartus Prime*. |
| June 2015 | 2015.06.16 | • Added the supported data rates for the following output standards using true LVDS output buffer types in the High-Speed I/O Specifications for Arria V Devices table:<br>— True RSDS output standard: data rates of up to 360 Mbps<br>— True mini-LVDS output standard: data rates of up to 400 Mbps<br>• Added note in the condition for Transmitter—Emulated Differential I/O Standards $f_{HSDR}$ data rate parameter in the High-Speed I/O Specifications for Arria V Devices table. Note: When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.<br>• Changed Queued Serial Peripheral Interface (QSPI) to Quad Serial Peripheral Interface (SPI) Flash.<br>• Updated $T_h$ location in $I^2C$ Timing Diagram.<br>• Updated $T_{wp}$ location in NAND Address Latch Timing Diagram.<br>• Corrected the unit for $t_{DH}$ from ns to s in FPP Timing Parameters When DCLK-to-DATA[] Ratio is >1 for Arria V Devices table.<br>• Updated the maximum value for $t_{CO}$ from 4 ns to 2 ns in AS Timing Parameters for AS ×1 and ×4 Configurations in Arria V Devices table.<br>• Moved the following timing diagrams to the Configuration, Design Security, and Remote System Upgrades in Arria V Devices chapter.<br>— FPP Configuration Timing Waveform When DCLK-to-DATA[] Ratio is 1<br>— FPP Configuration Timing Waveform When DCLK-to-DATA[] Ratio is >1<br>— AS Configuration Timing Waveform<br>— PS Configuration Timing Waveform |

***continued...***

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| Date | Version | Changes |
|---|---|---|
| January 2015 | 2015.01.30 | • Updated the description for $V_{CC_AUX_SHARED}$ to "HPS auxiliary power supply" in the following tables:<br>— Absolute Maximum Ratings for Arria V Devices<br>— HPS Power Supply Operating Conditions for Arria V SX and ST Devices<br>• Added statement in I/O Standard Specifications: You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.<br>• Updated the conditions for transceiver reference clock rise time and fall time: Measure at ±60 mV of differential signal. Added a note to the conditions: REFCLK performance requires to meet transmitter REFCLK phase noise specification.<br>• Updated the description in Periphery Performance Specifications to mention that proper timing closure is required in design.<br>• Updated HPS Clock Performance main_base_clk specifications from 525 MHz (for –I3 speed grade) and 462 MHz (for –C4 speed grade) to 400 MHz.<br>• Updated HPS PLL VCO maximum frequency to 1,600 MHz (for –C5, –I5, and –C6 speed grades), 1,850 MHz (for –C4 speed grade), and 2,100 MHz (for –I3 speed grade).<br>• Changed the symbol for HPS PLL input jitter divide value from NR to N.<br>• Removed "Slave select pulse width (Texas Instruments SSP mode)" parameter from the following tables:<br>— SPI Master Timing Requirements for Arria V Devices<br>— SPI Slave Timing Requirements for Arria V Devices<br>• Added descriptions to USB Timing Characteristics section in HPS Specifications: PHYs that support LPM mode may not function properly with the USB controller due to a timing issue. It is recommended that designers use the MicroChip USB3300 PHY device that has been proven to be successful on the development board.<br>• Added HPS JTAG timing specifications.<br>• Updated FPGA JTAG timing specifications note as follows: A 1-ns adder is required for each $V_{CCIO}$ voltage step down from 3.0 V. For example, $t_{JPCO}$ = 13 ns if $V_{CCIO}$ of the TDO I/O bank = 2.5 V, or 14 ns if it equals 1.8 V.<br>• Updated the value in the $V_{ICM}$ (AC Coupled) row and in note 6 from 650 mV to 750 mV in the Transceiver Specifications for Arria V GT and ST Devices table. |
| July 2014 | 3.8 | • Added a note in Table 3, Table 4, and Table 5: The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.<br>• Updated $V_{CC_HPS}$ specification in Table 5.<br>• Added a note in Table 19: Differential inputs are powered by $V_{CCPD}$ which requires 2.5 V.<br>• Updated "Minimum differential eye opening at the receiver serial input pins" specification in Table 20 and Table 21.<br>• Updated description in "HPS PLL Specifications" section.<br>• Updated VCO range maximum specification in Table 39.<br>• Updated $T_d$ and $T_h$ specifications in Table 45.<br>• Added $T_h$ specification in Table 47 and Figure 13.<br>• Updated a note in Figure 20, Figure 21, and Figure 23 as follows: Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.<br>• Removed "Remote update only in AS mode" specification in Table 58. |

*continued...*

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| Date | Version | Changes |
|---|---|---|
| | | • Added DCLK device initialization clock source specification in Table 60.<br>• Added description in "Configuration Files" section: The IOCSR `.rbf` size is specifically for the Configuration via Protocol (CvP) feature.<br>• Removed $f_{MAX_RU_CLK}$ specification in Table 63. |
| February 2014 | 3.7 | • Updated $V_{CCRSTCLK_HPS}$ maximum specification in Table 1.<br>• Added $V_{CC_AUX_SHARED}$ specification in Table 1. |
| December 2013 | 3.6 | • Added "HPS PLL Specifications".<br>• Added Table 24, Table 39, and Table 40.<br>• Updated Table 1, Table 3, Table 5, Table 19, Table 20, Table 21, Table 38, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, Table 48, Table 49, Table 50, Table 51, Table 55, Table 56, and Table 59.<br>• Updated Figure 7, Figure 13, Figure 15, Figure 16, and Figure 19.<br>• Removed table: GPIO Pulse Width for Arria V Devices. |
| August 2013 | 3.5 | • Removed "Pending silicon characterization" note in Table 29.<br>• Updated Table 25. |
| August 2013 | 3.4 | • Removed Preliminary tags for Table 1, Table 2, Table 3, Table 4, Table 5, Table 6, Table 7, Table 9, Table 12, Table 13, Table 14, Table 15, Table 16, Table 17, Table 18, Table 19, Table 20, Table 21, Table 22, Table 23, Table 24, Table 25, Table 26, Table 27, Table 28, Table 29, Table 30, Table 31, Table 35, Table 36, Table 51, Table 53, Table 54, Table 55, Table 56, Table 57, Table 60, Table 62, and Table 64.<br>• Updated Table 1, Table 3, Table 11, Table 19, Table 20, Table 21, Table 22, Table 25, and Table 29. |
| June 2013 | 3.3 | Updated Table 20, Table 21, Table 25, and Table 38. |
| May 2013 | 3.2 | • Added Table 37.<br>• Updated Figure 8, Figure 9, Figure 20, Figure 22, and Figure 23.<br>• Updated Table 1, Table 5, Table 10, Table 13, Table 19, Table 20, Table 21, Table 23, Table 29, Table 39, Table 40, Table 46, Table 56, Table 57, Table 60, and Table 64.<br>• Updated industrial junction temperature range for –I3 speed grade in "PLL Specifications" section. |
| March 2013 | 3.1 | • Added HPS reset information in the "HPS Specifications" section.<br>• Added Table 60.<br>• Updated Table 1, Table 3, Table 17, Table 20, Table 29, and Table 59.<br>• Updated Figure 21. |

***continued...***

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| Date | Version | Changes |
|---|---|---|
| November 2012 | 3.0 | • Updated Table 2, Table 4, Table 9, Table 14, Table 16, Table 17, Table 20, Table 21, Table 25, Table 29, Table 36, Table 56, Table 57, and Table 60.<br>• Removed table: Transceiver Block Jitter Specifications for Arria V Devices.<br>• Added HPS information:<br>— Added "HPS Specifications" section.<br>— Added Table 38, Table 39, Table 40, Table 41, Table 42, Table 43, Table 44, Table 45, Table 46, Table 47, Table 48, Table 49, and Table 50.<br>— Added Figure 7, Figure 8, Figure 9, Figure 10, Figure 11, Figure 12, Figure 13, Figure 14, Figure 15, Figure 16, Figure 17, Figure 18, and Figure 19.<br>— Updated Table 3 and Table 5. |
| October 2012 | 2.4 | • Updated Arria V GX $V_{CCR_GXBL/R}$, $V_{CCT_GXBL/R}$, and $V_{CCL_GXBL/R}$ minimum and maximum values, and data rate in Table 4.<br>• Added receiver $V_{ICM}$ (AC coupled) and $V_{ICM}$ (DC coupled) values, and transmitter $V_{OCM}$ (AC coupled) and $V_{OCM}$ (DC coupled) values in Table 20 and Table 21. |
| August 2012 | 2.3 | Updated the SERDES factor condition in Table 30. |
| July 2012 | 2.2 | • Updated the maximum voltage for $V_I$ (DC input voltage) in Table 1.<br>• Updated Table 20 to include the Arria V GX -I3 speed grade.<br>• Updated the minimum value of the fixedclk clock frequency in Table 20 and Table 21.<br>• Updated the SERDES factor condition in Table 30.<br>• Updated Table 50 to include the IOE programmable delay settings for the Arria V GX -I3 speed grade. |
| June 2012 | 2.1 | Updated $V_{CCR_GXBL/R}$, $V_{CCT_GXBL/R}$, and $V_{CCL_GXBL/R}$ values in Table 4. |
| June 2012 | 2.0 | • Updated for the Quartus II software v12.0 release:<br>• Restructured document.<br>• Updated "Supply Current and Power Consumption" section.<br>• Updated Table 20, Table 21, Table 24, Table 25, Table 26, Table 35, Table 39, Table 43, and Table 52.<br>• Added Table 22, Table 23, and Table 33.<br>• Added Figure 1–1 and Figure 1–2.<br>• Added "Initialization" and "Configuration Files" sections. |
| February 2012 | 1.3 | • Updated Table 2–1.<br>• Updated Transceiver-FPGA Fabric Interface rows in Table 2–20.<br>• Updated $V_{CCP}$ description. |

*continued...*

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| Date | Version | Changes |
|---|---|---|
| December 2011 | 1.2 | Updated Table 2–1 and Table 2–3. |
| November 2011 | 1.1 | • Updated Table 2–1, Table 2–19, Table 2–26, and Table 2–36.<br>• Added Table 2–5.<br>• Added Figure 2–4. |
| August 2011 | 1.0 | Initial release. |

683022 | 2019.04.26

Send Feedback

# 2. Arria V GZ Device Datasheet

This document covers the electrical and switching characteristics for Arria V GZ devices. Electrical characteristics include operating conditions and power consumption. Switching characteristics include transceiver specifications, core, and periphery performance. This document also describes I/O timing, including programmable I/O element (IOE) delay and programmable output buffer delay.

**Related Information**

Arria V Device Overview
For information regarding the densities and packages of devices in the Arria V GZ family.

## 2.1. Electrical Characteristics

### 2.1.1. Operating Conditions

When you use Arria V GZ devices, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of Arria V GZ devices, you must consider the operating requirements described in this datasheet.

Arria V GZ devices are offered in commercial and industrial temperature grades.

Commercial devices are offered in –3 (fastest) and –4 core speed grades. Industrial devices are offered in –3L and –4 core speed grades. Arria V GZ devices are offered in –2 and –3 transceiver speed grades.

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**Table 79. Commercial and Industrial Speed Grade Offering for Arria V GZ Devices**

C = Commercial temperature grade; I = Industrial temperature grade.

Lower number refers to faster speed grade.

L = Low power devices.

| Transceiver Speed Grade | Core Speed Grade | | | |
|---|---|---|---|---|
| | C3 | C4 | I3L | I4 |
| 2 | Yes | — | Yes | — |
| 3 | — | Yes | — | Yes |

### 2.1.1.1. Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Arria V GZ devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

***Caution:*** Conditions other than those listed in the following table may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

**Table 80. Absolute Maximum Ratings for Arria V GZ Devices**

| Symbol | Description | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Power supply for core voltage and periphery circuitry | –0.5 | 1.35 | V |
| $V_{CCPT}$ | Power supply for programmable power technology | –0.5 | 1.8 | V |
| $V_{CCPGM}$ | Power supply for configuration pins | –0.5 | 3.9 | V |
| $V_{CC_AUX}$ | Auxiliary supply for the programmable power technology | –0.5 | 3.4 | V |
| $V_{CCBAT}$ | Battery back-up power supply for design security volatile key register | –0.5 | 3.9 | V |
| $V_{CCPD}$ | I/O pre-driver power supply | –0.5 | 3.9 | V |
| $V_{CCIO}$ | I/O power supply | –0.5 | 3.9 | V |
| $V_{CCD_FPLL}$ | PLL digital power supply | –0.5 | 1.8 | V |
| $V_{CCA_FPLL}$ | PLL analog power supply | –0.5 | 3.4 | V |

*continued...*

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| Symbol | Description | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $V_I$ | DC input voltage | –0.5 | 3.8 | V |
| $T_J$ | Operating junction temperature | –55 | 125 | °C |
| $T_{STG}$ | Storage temperature (No bias) | –65 | 150 | °C |
| $I_{OUT}$ | DC output current per pin | –25 | 40 | mA |

**Table 81. Transceiver Power Supply Absolute Conditions for Arria V GZ Devices**

| Symbol | Description | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $V_{CCA_GXBL}$ | Transceiver channel PLL power supply (left side) | –0.5 | 3.75 | V |
| $V_{CCA_GXBR}$ | Transceiver channel PLL power supply (right side) | –0.5 | 3.75 | V |
| $V_{CCHIP_L}$ | Transceiver hard IP power supply (left side) | –0.5 | 1.35 | V |
| $V_{CCHSSI_L}$ | Transceiver PCS power supply (left side) | –0.5 | 1.35 | V |
| $V_{CCHSSI_R}$ | Transceiver PCS power supply (right side) | –0.5 | 1.35 | V |
| $V_{CCR_GXBL}$ | Receiver analog power supply (left side) | –0.5 | 1.35 | V |
| $V_{CCR_GXBR}$ | Receiver analog power supply (right side) | –0.5 | 1.35 | V |
| $V_{CCT_GXBL}$ | Transmitter analog power supply (left side) | –0.5 | 1.35 | V |
| $V_{CCT_GXBR}$ | Transmitter analog power supply (right side) | –0.5 | 1.35 | V |
| $V_{CCH_GXBL}$ | Transmitter output buffer power supply (left side) | –0.5 | 1.8 | V |
| $V_{CCH_GXBR}$ | Transmitter output buffer power supply (right side) | –0.5 | 1.8 | V |

### 2.1.1.2. Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in the following table. They may also undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% of the duty cycle.

For example, a signal that overshoots to 3.95 V can be at 3.95 V for only ~21% over the lifetime of the device; for a device lifetime of 10 years, the overshoot duration amounts to ~2 years.

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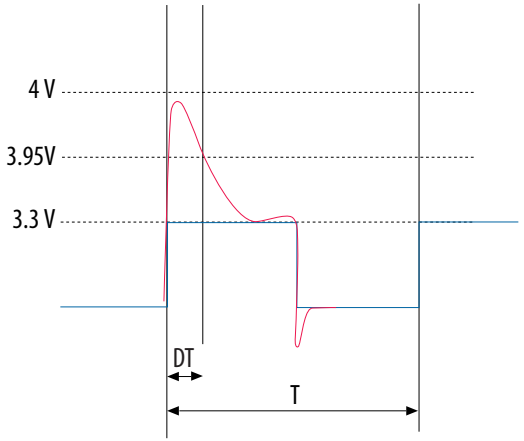
**Table 82. Maximum Allowed Overshoot During Transitions for Arria V GZ Devices**

| Symbol | Description | Condition (V) | Overshoot Duration as % @ $T_J$ = 100°C | Unit |
|---|---|---|---|---|
| Vi (AC) | AC input voltage | 3.8 | 100 | % |
| | | 3.85 | 64 | % |
| | | 3.9 | 36 | % |
| | | 3.95 | 21 | % |
| | | 4 | 12 | % |
| | | 4.05 | 7 | % |
| | | 4.1 | 4 | % |
| | | 4.15 | 2 | % |
| | | 4.2 | 1 | % |

For an overshoot of 3.8 V, the percentage of high time for the overshoot can be as high as 100% over a 10-year period. Percentage of high time is calculated as ([delta T]/T) × 100. This 10-year period assumes that the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal.

**Figure 22. Arria V GZ Devices Overshoot Duration**



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### 2.1.1.3. Recommended Operating Conditions

**Table 83. Recommended Operating Conditions for Arria V GZ Devices**

Power supply ramps must all be strictly monotonic, without plateaus.

| Symbol | Description | Condition | Minimum(117) | Typical | Maximum (117) | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Core voltage and periphery circuitry power supply (118) | — | 0.82 | 0.85 | 0.88 | V |
| $V_{CCPT}$ | Power supply for programmable power technology | — | 1.45 | 1.50 | 1.55 | V |
| $V_{CC_AUX}$ | Auxiliary supply for the programmable power technology | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCPD}$ (119) | I/O pre-driver (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | I/O pre-driver (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| $V_{CCIO}$ | I/O buffers (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | I/O buffers (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| | I/O buffers (1.8 V) power supply | — | 1.71 | 1.8 | 1.89 | V |
| | I/O buffers (1.5 V) power supply | — | 1.425 | 1.5 | 1.575 | V |
| | I/O buffers (1.35 V) power supply | — | 1.283 | 1.35 | 1.45 | V |
| | I/O buffers (1.25 V) power supply | — | 1.19 | 1.25 | 1.31 | V |
| | I/O buffers (1.2 V) power supply | — | 1.14 | 1.2 | 1.26 | V |
| $V_{CCPGM}$ | Configuration pins (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | Configuration pins (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| | Configuration pins (1.8 V) power supply | — | 1.71 | 1.8 | 1.89 | V |
| $V_{CCA_FPLL}$ | PLL analog voltage regulator power supply | — | 2.375 | 2.5 | 2.625 | V |

*continued...*

(117) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(118) The $V_{CC}$ core supply must be set to 0.9 V if the Partial Reconfiguration (PR) feature is used.

(119) $V_{CCPD}$ must be 2.5 V when $V_{CCIO}$ is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V. $V_{CCPD}$ must be 3.0 V when $V_{CCIO}$ is 3.0 V.

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| Symbol | Description | Condition | Minimum(117) | Typical | Maximum (117) | Unit |
|---|---|---|---|---|---|---|
| $V_{CCD_FPLL}$ | PLL digital voltage regulator power supply | — | 1.45 | 1.5 | 1.55 | V |
| $V_{CCBAT}$ (120) | Battery back-up power supply (For design security volatile key register) | — | 1.2 | — | 3.0 | V |
| $V_I$ | DC input voltage | — | –0.5 | — | 3.6 | V |
| $V_O$ | Output voltage | — | 0 | — | $V_{CCIO}$ | V |
| $T_J$ | Operating junction temperature | Commercial | 0 | — | 85 | °C |
| | | Industrial | –40 | — | 100 | °C |
| $t_{RAMP}$ | Power supply ramp time | Standard POR | 200 µs | — | 100 ms | — |
| | | Fast POR | 200 µs | — | 4 ms | — |

### 2.1.1.3.1. Recommended Transceiver Power Supply Operating Conditions

**Table 84. Recommended Transceiver Power Supply Operating Conditions for Arria V GZ Devices**

| Symbol | Description | Minimum (121) | Typical | Maximum(121) | Unit |
|---|---|---|---|---|---|
| $V_{CCA_GXBL}$ (122), (123) | Transceiver channel PLL power supply (left side) | 2.85 | 3.0 | 3.15 | V |
| | | 2.375 | 2.5 | 2.625 | |
| $V_{CCA_GXBR}$ (122), (123) | Transceiver channel PLL power supply (right side) | 2.85 | 3.0 | 3.15 | V |

*continued...*

(117) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(120) If you do not use the design security feature in Arria V GZ devices, connect $V_{CCBAT}$ to a 1.2- to 3.0-V power supply. Arria V GZ power-on-reset (POR) circuitry monitors $V_{CCBAT}$. Arria V GZ devices do not exit POR if $V_{CCBAT}$ is not powered up.

(121) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(122) This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.

(123) When using ATX PLLs, the supply must be 3.0 V.

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| Symbol | Description | Minimum (121) | Typical | Maximum(121) | Unit |
|---|---|---|---|---|---|
| | | 2.375 | 2.5 | 2.625 | |
| $V_{CCHIP_L}$ | Transceiver hard IP power supply (left side) | 0.82 | 0.85 | 0.88 | V |
| $V_{CCHSSI_L}$ | Transceiver PCS power supply (left side) | 0.82 | 0.85 | 0.88 | V |
| $V_{CCHSSI_R}$ | Transceiver PCS power supply (right side) | 0.82 | 0.85 | 0.88 | V |
| $V_{CCR_GXBL}$ (124) | Receiver analog power supply (left side) | 0.82 | 0.85 | 0.88 | V |
| | | 0.97 | 1.0 | 1.03 | |
| | | 1.03 | 1.05 | 1.07 | |
| $V_{CCR_GXBR}$ (124) | Receiver analog power supply (right side) | 0.82 | 0.85 | 0.88 | V |
| | | 0.97 | 1.0 | 1.03 | |
| | | 1.03 | 1.05 | 1.07 | |
| $V_{CCT_GXBL}$ (124) | Transmitter analog power supply (left side) | 0.82 | 0.85 | 0.88 | V |
| | | 0.97 | 1.0 | 1.03 | |
| | | 1.03 | 1.05 | 1.07 | |
| $V_{CCT_GXBR}$ (124) | Transmitter analog power supply (right side) | 0.82 | 0.85 | 0.88 | V |
| | | 0.97 | 1.0 | 1.03 | |
| | | 1.03 | 1.05 | 1.07 | |
| $V_{CCH_GXBL}$ | Transmitter output buffer power supply (left side) | 1.425 | 1.5 | 1.575 | V |
| $V_{CCH_GXBR}$ | Transmitter output buffer power supply (right side) | 1.425 | 1.5 | 1.575 | V |

(121) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

(124) This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps, and to 1.05 V if configured at a data rate > 10.3 Gbps when DFE is used. For data rate up to 6.5 Gbps, you can connect this supply to 0.85 V.

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#### 2.1.1.3.2. Transceiver Power Supply Requirements

**Table 85. Transceiver Power Supply Voltage Requirements for Arria V GZ Devices**

| Conditions | VCCR_GXB and VCCT_GXB (125) | VCCA_GXB | VCCH_GXB | Unit |
|---|---|---|---|---|
| If BOTH of the following conditions are true:<br>• Data rate > 10.3 Gbps.<br>• DFE is used. | 1.05 | 3.0 | 1.5 | V |
| If ANY of the following conditions are true (126) :<br>• ATX PLL is used.<br>• Data rate > 6.5Gbps.<br>• DFE (data rate ≤ 10.3 Gbps), AEQ, or EyeQ feature is used. | 1.0 | | | |
| If ALL of the following conditions are true:<br>• ATX PLL is not used.<br>• Data rate ≤ 6.5Gbps.<br>• DFE, AEQ, and EyeQ are not used. | 0.85 | 2.5 | | |

### 2.1.1.4. DC Characteristics

#### 2.1.1.4.1. Supply Current

Standby current is the current drawn from the respective power rails used for power budgeting.

Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.

**Related Information**

- Early Power Estimator User Guide
  For more information about the EPE tool.
- Power Analysis chapter, Intel Quartus Prime Handbook
  For more information about power analysis.

(125) If the VCCR_GXB and VCCT_GXB supplies are set to 1.0 V or 1.05 V, they cannot be shared with the VCC core supply. If the VCCR_GXB and VCCT_GXB are set to 0.85 V, they can be shared with the VCC core supply.

(126) Choose this power supply voltage requirement option if you plan to upgrade your design later with any of the listed conditions.

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### 2.1.1.4.2. Power Consumption

Intel offers two ways to estimate power consumption for a design—the Excel-based Early Power Estimator and the Intel Quartus Prime Power Analyzer feature.

*Note:* You typically use the interactive Excel-based EPE before designing the FPGA to get a magnitude estimate of the device power. The Intel Quartus Prime Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

#### Related Information

- Early Power Estimator User Guide
  For more information about the EPE tool.
- Power Analysis chapter, Intel Quartus Prime Handbook
  For more information about power analysis.

### 2.1.1.4.3. I/O Pin Leakage Current

**Table 86. I/O Pin Leakage Current for Arria V GZ Devices**

If $V_O = V_{CCIO}$ to $V_{CCIOMax}$, 100 µA of leakage current per I/O is expected.

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_I$ | Input pin | $V_I$ = 0 V to $V_{CCIOMAX}$ | –30 | — | 30 | µA |
| $I_{OZ}$ | Tri-stated I/O pin | $V_O$ = 0 V to $V_{CCIOMAX}$ | –30 | — | 30 | µA |

### 2.1.1.4.4. Bus Hold Specifications

**Table 87. Bus Hold Parameters for Arria V GZ Devices**

| Parameter | Symbol | Conditions | $V_{CCIO}$ | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.2 V | | 1.5 V | | 1.8 V | | 2.5 V | | 3.0 V | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Low sustaining current | $I_{SUSL}$ | $V_{IN} > V_{IL}$ | 22.5 | — | 25.0 | — | 30.0 | — | 50.0 | — | 70.0 | — | µA |

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| Parameter | Symbol | Conditions | $V_{CCIO}$ | | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1.2 V | | 1.5 V | | 1.8 V | | 2.5 V | | 3.0 V | | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| | | (maximum) | | | | | | | | | | | |
| High sustaining current | $I_{SUSH}$ | $V_{IN} < V_{IH}$ (minimum) | –22.5 | — | –25.0 | — | –30.0 | — | –50.0 | — | –70.0 | — | µA |
| Low overdrive current | $I_{ODL}$ | $0V < V_{IN} < V_{CCIO}$ | — | 120 | — | 160 | — | 200 | — | 300 | — | 500 | µA |
| High overdrive current | $I_{ODH}$ | $0V < V_{IN} < V_{CCIO}$ | — | –120 | — | –160 | — | –200 | — | –300 | — | –500 | µA |
| Bus-hold trip point | $V_{TRIP}$ | — | 0.45 | 0.95 | 0.50 | 1.00 | 0.68 | 1.07 | 0.70 | 1.70 | 0.80 | 2.00 | V |

### 2.1.1.4.5. On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block.

**Table 88. OCT Calibration Accuracy Specifications for Arria V GZ Devices**

OCT calibration accuracy is valid at the time of calibration only.

| Symbol | Description | Conditions | Calibration Accuracy | | Unit |
|---|---|---|---|---|---|
| | | | C3, I3L | C4, I4 | |
| 25-Ω $R_S$ | Internal series termination with calibration (25-Ω setting) | $V_{CCIO}$ = 3.0, 2.5, 1.8, 1.5, 1.2 V | ±15 | ±15 | % |
| 50-Ω $R_S$ | Internal series termination with calibration (50-Ω setting) | $V_{CCIO}$ = 3.0, 2.5, 1.8, 1.5, 1.2 V | ±15 | ±15 | % |
| 34-Ω and 40-Ω $R_S$ | Internal series termination with calibration (34-Ω and 40-Ω setting) | $V_{CCIO}$ = 1.5, 1.35, 1.25, 1.2 V | ±15 | ±15 | % |
| 48-Ω, 60-Ω, 80-Ω, and 240-Ω $R_S$ | Internal series termination with calibration (48-Ω, 60-Ω, 80-Ω, and 240-Ω setting) | $V_{CCIO}$ = 1.2 V | ±15 | ±15 | % |
| 50-Ω $R_T$ | Internal parallel termination with calibration (50-Ω setting) | $V_{CCIO}$ = 2.5, 1.8, 1.5, 1.2 V | –10 to +40 | –10 to +40 | % |

*continued...*

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| Symbol | Description | Conditions | Calibration Accuracy | | Unit |
|---|---|---|---|---|---|
| | | | C3, I3L | C4, I4 | |
| 20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω $R_T$ | Internal parallel termination with calibration (20-Ω , 30-Ω, 40-Ω, 60-Ω, and 120-Ω setting) | $V_{CCIO}$ = 1.5, 1.35, 1.25 V | –10 to +40 | –10 to +40 | % |
| 60-Ω and 120-Ω $R_T$ | Internal parallel termination with calibration (60-Ω and 120-Ω setting) | $V_{CCIO}$ = 1.2 | –10 to +40 | –10 to +40 | % |
| 25-Ω $R_{S_left_shift}$ | Internal left shift series termination with calibration (25-Ω $R_{S_left_shift}$ setting) | $V_{CCIO}$ = 3.0, 2.5, 1.8, 1.5, 1.2 V | ±15 | ±15 | % |

## Table 89. OCT Without Calibration Resistance Tolerance Specifications for Arria V GZ Devices

| Symbol | Description | Conditions | Resistance Tolerance | | Unit |
|---|---|---|---|---|---|
| | | | C3, I3L | C4, I4 | |
| 25-Ω R, 50-Ω $R_S$ | Internal series termination without calibration (25-Ω setting) | $V_{CCIO}$ = 3.0 and 2.5 V | ±40 | ±40 | % |
| 25-Ω $R_S$ | Internal series termination without calibration (25-Ω setting) | $V_{CCIO}$ = 1.8 and 1.5 V | ±40 | ±40 | % |
| 25-Ω $R_S$ | Internal series termination without calibration (25-Ω setting) | $V_{CCIO}$ = 1.2 V | ±50 | ±50 | % |
| 50-Ω $R_S$ | Internal series termination without calibration (50-Ω setting) | $V_{CCIO}$ = 1.8 and 1.5 V | ±40 | ±40 | % |
| 50-Ω $R_S$ | Internal series termination without calibration (50-Ω setting) | $V_{CCIO}$ = 1.2 V | ±50 | ±50 | % |
| 100-Ω $R_D$ | Internal differential termination (100-Ω setting) | $V_{CCIO}$ = 2.5 V | ±25 | ±25 | % |

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**Figure 23. OCT Variation Without Re-Calibration for Arria V GZ Devices**

$$R_{OCT} = R_{SCAL}\left(1 + \left(\frac{dR}{dT} \times \triangle T\right) \pm \left(\frac{dR}{dV} \times \triangle V\right)\right)$$

Notes:
1. The $R_{OCT}$ value shows the range of OCT resistance with the variation of temperature and $V_{CCIO}$.
2. $R_{SCAL}$ is the OCT resistance value at power-up.
3. ΔT is the variation of temperature with respect to the temperature at power-up.
4. ΔV is the variation of voltage with respect to the $V_{CCIO}$ at power-up.
5. dR/dT is the percentage change of $R_{SCAL}$ with temperature.
6. dR/dV is the percentage change of $R_{SCAL}$ with voltage.

**Table 90. OCT Variation after Power-Up Calibration for Arria V GZ Devices**

Valid for a $V_{CCIO}$ range of ±5% and a temperature range of 0° to 85°C.

| Symbol | Description | $V_{CCIO}$ (V) | Typical | Unit |
|---|---|---|---|---|
| dR/dV | OCT variation with voltage without re-calibration | 3.0 | 0.0297 | %/mV |
| | | 2.5 | 0.0344 | |
| | | 1.8 | 0.0499 | |
| | | 1.5 | 0.0744 | |
| | | 1.2 | 0.1241 | |
| dR/dT | OCT variation with temperature without re-calibration | 3.0 | 0.189 | %/°C |
| | | 2.5 | 0.208 | |
| | | 1.8 | 0.266 | |
| | | 1.5 | 0.273 | |
| | | 1.2 | 0.317 | |

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### 2.1.1.4.6. Pin Capacitance

**Table 91. Pin Capacitance for Arria V GZ Devices**

| Symbol | Description | Maximum | Unit |
|---|---|---|---|
| $C_{IOTB}$ | Input capacitance on the top and bottom I/O pins | 6 | pF |
| $C_{IOLR}$ | Input capacitance on the left and right I/O pins | 6 | pF |
| $C_{OUTFB}$ | Input capacitance on dual-purpose clock output and feedback pins | 6 | pF |

### 2.1.1.4.7. Hot Socketing

**Table 92. Hot Socketing Specifications for Arria V GZ Devices**

| Symbol | Description | Maximum |
|---|---|---|
| $I_{IOPIN\ (DC)}$ | DC current per I/O pin | 300 µA |
| $I_{IOPIN\ (AC)}$ | AC current per I/O pin | 8 mA (127) |
| $I_{XCVR\text{-}TX\ (DC)}$ | DC current per transceiver transmitter pin | 100 mA |
| $I_{XCVR\text{-}RX\ (DC)}$ | DC current per transceiver receiver pin | 50 mA |

(127) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}|$ = C dv/dt, in which C is the I/O pin capacitance and dv/dt is the slew rate.

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### 2.1.1.4.8. Internal Weak Pull-Up Resistor

**Table 93. Internal Weak Pull-Up Resistor for Arria V GZ Devices**

All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins. The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 kΩ .

| Symbol | Description | $V_{CCIO}$ Conditions (V) (128) | Value (129) | Unit |
|---|---|---|---|---|
| $R_{PU}$ | Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option. | 3.0 ±5% | 25 | k Ω |
| | | 2.5 ±5% | 25 | k Ω |
| | | 1.8 ±5% | 25 | k Ω |
| | | 1.5 ±5% | 25 | kΩ |
| | | 1.35 ±5% | 25 | k Ω |
| | | 1.25 ±5% | 25 | k Ω |
| | | 1.2 ±5% | 25 | k Ω |

## 2.1.1.5. I/O Standard Specifications

The $V_{OL}$ and $V_{OH}$ values are valid at the corresponding $I_{OH}$ and $I_{OL}$, respectively.

**Table 94. Single-Ended I/O Standards for Arria V GZ Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{IL}$ (V) | | $V_{IH}$ (V) | | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{OL}$ (mA) | $I_{OH}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Max | Max | Min | | |
| LVTTL | 2.85 | 3 | 3.15 | –0.3 | 0.8 | 1.7 | 3.6 | 0.4 | 2.4 | 2 | –2 |
| LVCMOS | 2.85 | 3 | 3.15 | –0.3 | 0.8 | 1.7 | 3.6 | 0.2 | $V_{CCIO}$ – 0.2 | 0.1 | –0.1 |
| 2.5 V | 2.375 | 2.5 | 2.625 | –0.3 | 0.7 | 1.7 | 3.6 | 0.4 | 2 | 1 | –1 |

*continued...*

(128) The pin pull-up resistance values may be lower if an external source drives the pin higher than $V_{CCIO}$.

(129) These specifications are valid with a ±10% tolerance to cover changes over PVT.

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| I/O Standard | $V_{CCIO}$ (V) | | | $V_{IL}$ (V) | | $V_{IH}$ (V) | | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{OL}$ (mA) | $I_{OH}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Max | Max | Min | | |
| 1.8 V | 1.71 | 1.8 | 1.89 | –0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.45 | $V_{CCIO}$ – 0.45 | 2 | –2 |
| 1.5 V | 1.425 | 1.5 | 1.575 | –0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 2 | –2 |
| 1.2 V | 1.14 | 1.2 | 1.26 | –0.3 | 0.35 × $V_{CCIO}$ | 0.65 × $V_{CCIO}$ | $V_{CCIO}$ + 0.3 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 2 | –2 |

**Table 95. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Arria V GZ Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{REF}$ (V) | | | $V_{TT}$ (V) | | |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| SSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 | $V_{REF}$ – 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | 0.49 × $V_{CCIO}$ | 0.5 × VCCIO | 0.51 × $V_{CCIO}$ |
| SSTL-135 Class I, II | 1.283 | 1.35 | 1.418 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ |
| SSTL-125 Class I, II | 1.19 | 1.25 | 1.26 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | 0.49 × $V_{CCIO}$ | 0.5 × VCCIO | 0.51 × $V_{CCIO}$ |
| SSTL-12 Class I, II | 1.14 | 1.20 | 1.26 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | 0.49 × $V_{CCIO}$ | 0.5 × VCCIO | 0.51 × $V_{CCIO}$ |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.85 | 0.9 | 0.95 | — | $V_{CCIO}$/2 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.68 | 0.75 | 0.9 | — | $V_{CCIO}$/2 | — |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.47 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.53 × $V_{CCIO}$ | — | $V_{CCIO}$/2 | — |
| HSUL-12 | 1.14 | 1.2 | 1.3 | 0.49 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.51 × $V_{CCIO}$ | — | — | — |

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## Table 96. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Arria V GZ Devices

| I/O Standard | $V_{IL(DC)}$ (V) | | $V_{IH(DC)}$ (V) | | $V_{IL(AC)}$ (V) | $V_{IH(AC)}$ (V) | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{ol}$ (mA) | $I_{oh}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Max | Min | Max | Min | | |
| SSTL-2 Class I | –0.3 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.31 | $V_{REF}$ + 0.31 | $V_{TT}$ – 0.608 | $V_{TT}$ + 0.608 | 8.1 | –8.1 |
| SSTL-2 Class II | –0.3 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.31 | $V_{REF}$ + 0.31 | $V_{TT}$ – 0.81 | $V_{TT}$ + 0.81 | 16.2 | –16.2 |
| SSTL-18 Class I | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.25 | $V_{REF}$ + 0.25 | $V_{TT}$ – 0.603 | $V_{TT}$ + 0.603 | 6.7 | –6.7 |
| SSTL-18 Class II | –0.3 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCIO}$ + 0.3 | $V_{REF}$ – 0.25 | $V_{REF}$ + 0.25 | 0.28 | $V_{CCIO}$ – 0.28 | 13.4 | –13.4 |
| SSTL-15 Class I | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.175 | $V_{REF}$ + 0.175 | 0.2 × $V_{CCIO}$ | 0.8 × $V_{CCIO}$ | 8 | –8 |
| SSTL-15 Class II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.175 | $V_{REF}$ + 0.175 | 0.2 × $V_{CCIO}$ | 0.8 × $V_{CCIO}$ | 16 | –16 |
| SSTL-135 Class I, II | — | $V_{REF}$ – 0.09 | $V_{REF}$ + 0.09 | — | $V_{REF}$ – 0.16 | $V_{REF}$ + 0.16 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | — | — |
| SSTL-125 Class I, II | — | $V_{REF}$ – 0.85 | $V_{REF}$ + 0.85 | — | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | — | — |
| SSTL-12 Class I, II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | — | — |
| HSTL-18 Class I | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ – 0.4 | 8 | –8 |
| HSTL-18 Class II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ – 0.4 | 16 | –16 |
| HSTL-15 Class I | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ – 0.4 | 8 | –8 |
| HSTL-15 Class II | — | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 0.4 | $V_{CCIO}$ – 0.4 | 16 | –16 |
| HSTL-12 Class I | –0.15 | $V_{REF}$ – 0.08 | $V_{REF}$ + 0.08 | $V_{CCIO}$ + 0.15 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 8 | –8 |
| HSTL-12 Class II | –0.15 | $V_{REF}$ – 0.08 | $V_{REF}$ + 0.08 | $V_{CCIO}$ + 0.15 | $V_{REF}$ – 0.15 | $V_{REF}$ + 0.15 | 0.25 × $V_{CCIO}$ | 0.75 × $V_{CCIO}$ | 16 | –16 |
| HSUL-12 | — | $V_{REF}$ – 0.13 | $V_{REF}$ + 0.13 | — | $V_{REF}$ – 0.22 | $V_{REF}$ + 0.22 | 0.1 × $V_{CCIO}$ | 0.9 × $V_{CCIO}$ | — | — |

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### Table 97. Differential SSTL I/O Standards for Arria V GZ Devices

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{SWING(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{SWING(AC)}$ (V) | |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 0.3 | $V_{CCIO}$ + 0.6 | $V_{CCIO}/2$ – 0.2 | — | $V_{CCIO}/2$ + 0.2 | 0.62 | $V_{CCIO}$ + 0.6 |
| SSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.25 | $V_{CCIO}$ + 0.6 | $V_{CCIO}/2$ – 0.175 | — | $V_{CCIO}/2$ + 0.175 | 0.5 | $V_{CCIO}$ + 0.6 |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | (130) | $V_{CCIO}/2$ – 0.15 | — | $V_{CCIO}/2$ + 0.15 | 0.35 | — |
| SSTL-135 Class I, II | 1.283 | 1.35 | 1.45 | 0.2 | (130) | $V_{CCIO}/2$ – 0.15 | $V_{CCIO}/2$ | $V_{CCIO}/2$ + 0.15 | $2(V_{IH(AC)} - V_{REF})$ | $2(V_{IL(AC)} - V_{REF})$ |
| SSTL-125 Class I, II | 1.19 | 1.25 | 1.31 | 0.18 | (130) | $V_{CCIO}/2$ – 0.15 | $V_{CCIO}/2$ | $V_{CCIO}/2$ + 0.15 | $2(V_{IH(AC)} - V_{REF})$ | — |
| SSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.18 | — | $V_{REF}$ –0.15 | $V_{CCIO}/2$ | $V_{REF}$ + 0.15 | –0.30 | 0.30 |

### Table 98. Differential HSTL and HSUL I/O Standards for Arria V GZ Devices

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{DIF(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{CM(DC)}$ (V) | | | $V_{DIF(AC)}$ (V) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Typ | Max | Min | Max |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.2 | — | 0.78 | — | 1.12 | 0.78 | — | 1.12 | 0.4 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | — | 0.68 | — | 0.9 | 0.68 | — | 0.9 | 0.4 | — |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.16 | $V_{CCIO}$ + 0.3 | — | 0.5 × $V_{CCIO}$ | — | 0.4 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.6 × $V_{CCIO}$ | 0.3 | $V_{CCIO}$ + 0.48 |
| HSUL-12 | 1.14 | 1.2 | 1.3 | 0.26 | 0.26 | 0.5 × $V_{CCIO}$ – 0.12 | 0.5 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ + 0.12 | 0.4 × $V_{CCIO}$ | 0.5 × $V_{CCIO}$ | 0.6 × $V_{CCIO}$ | 0.44 | 0.44 |

(130) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

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## Table 99. Differential I/O Standard Specifications for Arria V GZ Devices

| I/O Standard | $V_{CCIO}$ (V) (131) | | | $V_{ID}$ (mV) (132) | | | $V_{ICM(DC)}$ (V) | | | $V_{OD}$ (V) (133) | | | $V_{OCM}$ (V) (133) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Condition | Max | Min | Condition | Max | Min | Typ | Max | Min | Typ | Max |
| PCML | Transmitter, receiver, and input reference clock pins of the high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to the "Transceiver Performance Specifications" section. | | | | | | | | | | | | | | |
| 2.5 V LVDS (134) | 2.375 | 2.5 | 2.625 | 100 | $V_{CM}$ = 1.25 V | — | 0.05 | $D_{MAX}$ ≤ 700 Mbps | 1.8 | 0.247 | — | 0.6 | 1.125 | 1.25 | 1.375 |
| | | | | | | — | 1.05 | $D_{MAX}$ > 700 Mbps | 1.55 | 0.247 | — | 0.6 | 1.125 | 1.25 | 1.375 |
| BLVDS (135) | 2.375 | 2.5 | 2.625 | 100 | — | — | — | — | — | — | — | — | — | — | — |
| RSDS (HIO) (136) | 2.375 | 2.5 | 2.625 | 100 | $V_{CM}$ = 1.25 V | — | 0.3 | — | 1.4 | 0.1 | 0.2 | 0.6 | 0.5 | 1.2 | 1.4 |

*continued...*

(131) Differential inputs are powered by VCCPD which requires 2.5 V.

(132) The minimum VID value is applicable over the entire common mode range, VCM.

(133) RL range: 90 ≤ RL ≤ 110 Ω.

(134) For optimized LVDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.6 V for data rates above 700 Mbps, and 0 V to 1.85 V for data rates below 700 Mbps.

(135) There are no fixed $V_{ICM}$, $V_{OD}$, and $V_{OCM}$ specifications for BLVDS. They depend on the system topology.

(136) For optimized RSDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.45 V.

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| I/O Standard | $V_{CCIO}$ (V) (131) | | | $V_{ID}$ (mV) (132) | | | $V_{ICM(DC)}$ (V) | | | $V_{OD}$ (V) (133) | | | $V_{OCM}$ (V) (133) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Condition | Max | Min | Condition | Max | Min | Typ | Max | Min | Typ | Max |
| Mini-LVDS (HIO) (137) | 2.375 | 2.5 | 2.625 | 200 | — | 600 | 0.4 | — | 1.325 | 0.25 | — | 0.6 | 1 | 1.2 | 1.4 |
| LVPECL (138), (139) | — | — | — | 300 | — | — | 0.6 | $D_{MAX}$ ≤ 700 Mbps | 1.8 | — | — | — | — | — | — |
| | — | — | — | 300 | — | — | 1 | $D_{MAX}$ > 700 Mbps | 1.6 | — | — | — | — | — | — |

**Related Information**

Glossary on page 169

(131) Differential inputs are powered by VCCPD which requires 2.5 V.

(132) The minimum VID value is applicable over the entire common mode range, VCM.

(133) RL range: 90 ≤ RL ≤ 110 Ω.

(137) For optimized Mini-LVDS receiver performance, the receiver voltage input range must be between 0.3 V to 1.425 V.

(138) LVPECL is only supported on dedicated clock input pins.

(139) For optimized LVPECL receiver performance, the receiver voltage input range must be between 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.

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# 2.2. Switching Characteristics

## 2.2.1. Transceiver Performance Specifications

### 2.2.1.1. Reference Clock

**Table 100. Reference Clock Specifications for Arria V GZ Devices**

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Intel Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

| Symbol/Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| **Reference Clock** | | | | | | | | |
| Supported I/O Standards | Dedicated reference clock pin | 1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL | | | | | | |
| | RX reference clock pin | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS | | | | | | |
| Input Reference Clock Frequency (CMU PLL) (140) | — | 40 | — | 710 | 40 | — | 710 | MHz |
| Input Reference Clock Frequency (ATX PLL)(140) | — | 100 | — | 710 | 100 | — | 710 | MHz |
| Rise time | Measure at ±60 mV of differential signal (141) | — | — | 400 | — | — | 400 | ps |
| Fall time | Measure at ±60 mV of differential signal (141) | — | — | 400 | — | — | 400 | |
| Duty cycle | — | 45 | — | 55 | 45 | — | 55 | % |
| Spread-spectrum modulating clock frequency | PCI Express (PCIe) | 30 | — | 33 | 30 | — | 33 | kHz |
| Spread-spectrum downspread | PCIe | — | 0 to –0.5 | — | — | 0 to –0.5 | — | % |

*continued...*

(140) The input reference clock frequency options depend on the data rate and the device speed grade.

(141) REFCLK performance requires to meet transmitter REFCLK phase noise specification.

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| Symbol/Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| On-chip termination resistors | — | — | 100 | — | — | 100 | — | Ω |
| Absolute $V_{MAX}$ | Dedicated reference clock pin | — | — | 1.6 | — | — | 1.6 | V |
| | RX reference clock pin | — | — | 1.2 | — | — | 1.2 | |
| Absolute $V_{MIN}$ | — | –0.4 | — | — | –0.4 | — | — | V |
| Peak-to-peak differential input voltage | — | 200 | — | 1600 | 200 | — | 1600 | mV |
| $V_{ICM}$ (AC coupled) | Dedicated reference clock pin | 1000/900/850 (142) | | | 1000/900/850 (142) | | | mV |
| | RX reference clock pin | 1.0/0.9/0.85 (143) | | | 1.0/0.9/0.85(143) | | | mV |
| $V_{ICM}$ (DC coupled) | HCSL I/O standard for PCIe reference clock | 250 | — | 550 | 250 | — | 550 | mV |
| Transmitter REFCLK Phase Noise (622 MHz) (144) | 100 Hz | — | — | -70 | — | — | -70 | dBc/Hz |
| | 1 kHz | — | — | -90 | — | — | -90 | dBc/Hz |
| | 10 kHz | — | — | -100 | — | — | -100 | dBc/Hz |
| | 100 kHz | — | — | -110 | — | — | -110 | dBc/Hz |
| | ≥1 MHz | — | — | -120 | — | — | -120 | dBc/Hz |
| Transmitter REFCLK Phase Jitter (100 MHz) (145) | 10 kHz to 1.5 MHz (PCIe) | — | — | 3 | — | — | 3 | ps (rms) |
| $R_{REF}$ | — | — | 1800 ±1% | — | — | 1800 ±1% | — | Ω |

(142) The reference clock common mode voltage is equal to the $V_{CCR_GXB}$ power supply level.

(143) This supply follows VCCR_GXB

(144) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).

(145) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula:
REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.

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### Related Information

Arria V Device Overview
For more information about device ordering codes.

## 2.2.1.2. Transceiver Clocks

### Table 101. Transceiver Clocks Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Intel Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

| Symbol/Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| `fixedclk` clock frequency | PCIe Receiver Detect | — | 100 or 125 | — | — | 100 or 125 | — | MHz |
| Reconfiguration clock (`mgmt_clk_clk`) frequency | — | 100 | — | 125 | 100 | — | 125 | MHz |

### Related Information

Arria V Device Overview
For more information about device ordering codes.

## 2.2.1.3. Receiver

### Table 102. Receiver Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Intel Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

| Symbol/Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Supported I/O Standards | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS | | | | | | | |
| Data rate (Standard PCS) (146), (147) | — | 600 | — | 9900 | 600 | — | 8800 | Mbps |

*continued...*

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| Symbol/Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Data rate (10G PCS) (146), (147) | — | 600 | — | 12500 | 600 | — | 10312.5 | Mbps |
| Absolute $V_{MAX}$ for a receiver pin (148) | — | — | — | 1.2 | — | — | 1.2 | V |
| Absolute $V_{MIN}$ for a receiver pin | — | –0.4 | — | — | –0.4 | — | — | V |
| Maximum peak-to-peak differential input voltage $V_{ID}$ (diff p-p) before device configuration | — | — | — | 1.6 | — | — | 1.6 | V |
| Maximum peak-to-peak differential input voltage $V_{ID}$ (diff p-p) after device configuration (149) | $V_{CCR_GXB}$ = 1.0 V ($V_{ICM}$ = 0.75 V) | — | — | 1.8 | — | — | 1.8 | V |
| | $V_{CCR_GXB}$ = 0.85 V ($V_{ICM}$ = 0.6 V) | — | — | 2.4 | — | — | 2.4 | V |
| Minimum differential eye opening at receiver serial input pins (150)(151) | — | 85 | — | — | 85 | — | — | mV |
| Differential on-chip termination resistors | 85–Ω setting | — | 85 ± 30% | — | — | 85 ± 30% | — | Ω |
| | 100–Ω setting | — | 100 ± 30% | — | — | 100 ± 30% | — | Ω |
| | 120–Ω setting | — | 120 ± 30% | — | — | 120 ± 30% | — | Ω |

*continued...*

(146) The line data rate may be limited by PCS-FPGA interface speed grade.

(147) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

(148) The device cannot tolerate prolonged operation at this absolute maximum.

(149) The maximum peak to peak differential input voltage $V_{ID}$ after device configuration is equal to 4 × (absolute $V_{MAX}$ for receiver pin - $V_{ICM}$).

(150) The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(151) Minimum eye opening of 85 mV is only for the unstressed input eye condition.

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| Symbol/Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| | 150−Ω setting | — | 150 ± 30% | — | — | 150 ± 30% | — | Ω |
| $V_{ICM}$ (AC and DC coupled) | $V_{CCR_GXB}$ = 0.85 V full bandwidth | — | 600 | — | — | 600 | — | mV |
| | $V_{CCR_GXB}$ = 0.85 V half bandwidth | — | 600 | — | — | 600 | — | mV |
| | $V_{CCR_GXB}$ = 1.0 V full bandwidth | — | 700 | — | — | 700 | — | mV |
| | $V_{CCR_GXB}$ = 1.0 V half bandwidth | — | 700 | — | — | 700 | — | mV |
| $t_{LTR}$ (152) | — | — | — | 10 | — | — | 10 | µs |
| $t_{LTD}$ (153) | — | 4 | — | — | 4 | — | — | µs |
| $t_{LTD_manual}$ (154) | — | 4 | — | — | 4 | — | — | µs |
| $t_{LTR_LTD_manual}$ (155) | — | 15 | — | — | 15 | — | — | µs |
| Programmable equalization (AC Gain) | Full bandwidth (6.25 GHz) Half bandwidth (3.125 GHz) | — | — | 16 | — | — | 16 | dB |
| Programmable DC gain | DC gain setting = 0 | — | 0 | — | — | 0 | — | dB |
| | DC gain setting = 1 | — | 2 | — | — | 2 | — | dB |

*continued...*

(152) $t_{LTR}$ is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

(153) $t_{LTD}$ is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high.

(154) $t_{LTD_manual}$ is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high when the CDR is functioning in the manual mode.

(155) $t_{LTR_LTD_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedtoref` signal goes high when the CDR is functioning in the manual mode.

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| Symbol/Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| | DC gain setting = 2 | — | 4 | — | — | 4 | — | dB |
| | DC gain setting = 3 | — | 6 | — | — | 6 | — | dB |
| | DC gain setting = 4 | — | 8 | — | — | 8 | — | dB |

**Related Information**

Arria V Device Overview
For more information about device ordering codes.

## 2.2.1.4. Transmitter

### Table 103. Transmitter Specifications for Arria V GZ Devices

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Intel Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

| Symbol/Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Supported I/O Standards | 1.4-V and 1.5-V PCML | | | | | | | |
| Data rate (Standard PCS) | — | 600 | — | 9900 | 600 | — | 8800 | Mbps |
| Data rate (10G PCS) | — | 600 | — | 12500 | 600 | — | 10312.5 | Mbps |
| Differential on-chip termination resistors | 85-Ω setting | — | 85 ± 20% | — | — | 85 ± 20% | — | Ω |
| | 100-Ω setting | — | 100 ± 20% | — | — | 100 ± 20% | — | Ω |
| | 120-Ω setting | — | 120 ± 20% | — | — | 120 ± 20% | — | Ω |
| | 150-Ω setting | — | 150 ± 20% | — | — | 150 ± 20% | — | Ω |
| $V_{OCM}$ (AC coupled) | 0.65-V setting | — | 650 | — | — | 650 | — | mV |
| $V_{OCM}$ (DC coupled) | — | — | 650 | — | — | 650 | — | mV |

*continued...*

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| Symbol/Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Intra-differential pair skew | Tx $V_{CM}$ = 0.5 V and slew rate of 15 ps | — | — | 15 | — | — | 15 | ps |
| Intra-transceiver block transmitter channel-to-channel skew | x6 PMA bonded mode | — | — | 120 | — | — | 120 | ps |
| Inter-transceiver block transmitter channel-to-channel skew | xN PMA bonded mode | — | — | 500 | — | — | 500 | ps |

**Related Information**

Arria V Device Overview
For more information about device ordering codes.

## 2.2.1.5. CMU PLL

**Table 104. CMU PLL Specifications for Arria V GZ Devices**

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Intel Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

| Symbol/Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Supported data range | — | 600 | — | 12500 | 600 | — | 10312.5 | Mbps |
| $t_{pll_powerdown}$ (156) | — | 1 | — | — | 1 | — | — | µs |
| $t_{pll_lock}$ (157) | — | | — | 10 | — | — | 10 | µs |

**Related Information**

Arria V Device Overview
For more information about device ordering codes.

(156) $t_{pll_powerdown}$ is the PLL powerdown minimum pulse width.

(157) $t_{pll_lock}$ is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.

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### 2.2.1.6. ATX PLL

**Table 105. ATX PLL Specifications for Arria V GZ Devices**

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Intel Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

| Symbol/Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Supported data rate range | VCO post-divider L = 2 | 8000 | — | 12500 | 8000 | — | 10312.5 | Mbps |
| | L = 4 | 4000 | — | 6600 | 4000 | — | 6600 | Mbps |
| | L = 8 (158) | 2000 | — | 3300 | 2000 | — | 3300 | Mbps |
| $t_{pll_powerdown}$ (159) | — | 1 | — | — | 1 | — | — | µs |
| $t_{pll_lock}$ (160) | — | — | — | 10 | — | — | 10 | µs |

**Related Information**

- Arria V Device Overview
  For more information about device ordering codes.
- Transceiver Clocking in Arria V Devices
  For more information about clocking ATX PLLs.
- Dynamic Reconfiguration in Arria V Devices
  For more information about reconfiguring ATX PLLs.

(158) This clock can be further divided by central or local clock dividers making it possible to use ATX PLL for data rates < 1 Gbps. For more information about ATX PLLs, refer to the Transceiver Clocking in Arria V Devices chapter and the Dynamic Reconfiguration in Arria V Devices chapter.

(159) $t_{pll_powerdown}$ is the PLL powerdown minimum pulse width.

(160) $t_{pll_lock}$ is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.

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### 2.2.1.7. Fractional PLL

**Table 106. Fractional PLL Specifications for Arria V GZ Devices**

Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Intel Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Arria V Device Overview*.

| Symbol/Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Supported data range | — | 600 | — | 3250/ 3125(161) | 600 | — | 3250/ 3125 (161) | Mbps |
| $t_{pll_powerdown}$(162) | — | 1 | — | — | 1 | — | — | µs |
| $t_{pll_lock}$ (163) | — | — | — | 10 | | — | 10 | µs |

**Related Information**

Arria V Device Overview
For more information about device ordering codes.

(161) When you use fPLL as a TXPLL of the transceiver.

(162) $t_{pll_powerdown}$ is the PLL powerdown minimum pulse width.

(163) $t_{pll_lock}$ is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.

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### 2.2.1.8. Clock Network Data Rate

**Table 107. Clock Network Maximum Data Rate Transmitter Specifications**

Valid data rates below the maximum specified in this table depend on the reference clock frequency and the PLL counter settings. Check the Parameter Editor message during the Arria V Transceiver Native PHY Intel FPGA IP core instantiation.

| Clock Network | ATX PLL | | | CMU PLL (164) | | | fPLL | | |
|---|---|---|---|---|---|---|---|---|---|
| | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span |
| x1 (165) | 12.5 | — | 6 | 12.5 | — | 6 | 3.125 | — | 3 |
| x6 (165) | — | 12.5 | 6 | — | 12.5 | 6 | — | 3.125 | 6 |
| x6 PLL Feedback (166) | — | 12.5 | Side-wide | — | 12.5 | Side-wide | — | — | — |
| xN (PCIe) | — | 8.0 | 8 | — | 5.0 | 8 | — | — | — |
| xN (Arria V Transceiver Native PHY Intel FPGA IP core) | 8.0 | 8.0 | Up to 13 channels above and below PLL | 7.99 | 7.99 | Up to 13 channels above and below PLL | 3.125 | 3.125 | Up to 13 channels above and below PLL |
| | — | 8.01 to 9.8304 | Up to 7 channels above and below PLL | | | | | | |

(164) ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.

(165) Channel span is within a transceiver bank.

(166) Side-wide channel bonding is allowed up to the maximum supported by the Arria V Transceiver Native PHY Intel FPGA IP core.

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### 2.2.1.9. Standard PCS Data Rate

**Table 108. Standard PCS Approximate Maximum Date Rate (Gbps) for Arria V GZ Devices**

The maximum data rate is also constrained by the transceiver speed grade. Refer to the "Commercial and Industrial Speed Grade Offering for Arria V GZ Devices" table for the transceiver speed grade.

| Mode (167) | Transceiver Speed Grade | PMA Width | 20 | 20 | 16 | 16 | 10 | 10 | 8 | 8 |
|---|---|---|---|---|---|---|---|---|---|---|
| | | PCS/Core Width | 40 | 20 | 32 | 16 | 20 | 10 | 16 | 8 |
| FIFO | 2 | C3, I3L core speed grade | 9.9 | 9 | 7.84 | 7.2 | 5.3 | 4.7 | 4.24 | 3.76 |
| | 3 | C4, I4 core speed grade | 8.8 | 8.2 | 7.2 | 6.56 | 4.8 | 4.3 | 3.84 | 3.44 |
| Register | 2 | C3, I3L core speed grade | 9.9 | 9 | 7.92 | 7.2 | 4.9 | 4.,5 | 3.92 | 3.6 |
| | 3 | C4, I4 core speed grade | 8.8 | 8.2 | 7.04 | 6.56 | 4.4 | 4.1 | 3.52 | 3.28 |

**Related Information**

Operating Conditions on page 100

(167) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

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### 2.2.1.10. 10G PCS Data Rate

**Table 109. 10G PCS Approximate Maximum Data Rate (Gbps) for Arria V GZ Devices**

| Mode (168) | Transceiver Speed Grade | PMA Width | 64 | 40 | 40 | 40 | 32 | 32 |
|---|---|---|---|---|---|---|---|---|
| | | PCS Width | 64 | 66/67 | 50 | 40 | 64/66/67 | 32 |
| FIFO | 2 | C3, I3L core speed grade | 12.5 | 12.5 | 10.69 | 12.5 | 10.88 | 10.88 |
| | 3 | C4, I4 core speed grade | 10.3125 | 10.3125 | 10.69 | 10.3125 | 9.92 | 9.92 |
| Register | 2 | C3, I3L core speed grade | 12.5 | 12.5 | 10.69 | 12.5 | 10.88 | 10.88 |
| | 3 | C4, I4 core speed grade | 10.3125 | 10.3125 | 10.69 | 10.3125 | 9.92 | 9.92 |

### 2.2.1.11. Typical VOD Settings

**Table 110. Typical $V_{OD}$ Setting for Arria V GZ Channel, TX Termination = 100 Ω**

The tolerance is +/-20% for all VOD settings except for settings 2 and below.

| Symbol | $V_{OD}$ Setting | $V_{OD}$ Value (mV) | $V_{OD}$ Setting | $V_{OD}$ Value (mV) |
|---|---|---|---|---|
| $V_{OD}$ **differential peak to peak typical** | 0 (169) | 0 | 32 | 640 |
| | 1(169) | 20 | 33 | 660 |
| | 2(169) | 40 | 34 | 680 |
| | 3(169) | 60 | 35 | 700 |
| | 4(169) | 80 | 36 | 720 |
| | 5(169) | 100 | 37 | 740 |
| | 6 | 120 | 38 | 760 |
| | 7 | 140 | 39 | 780 |
| | 8 | 160 | 40 | 800 |

*continued...*

(168) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

(169) If TX termination resistance = 100 Ω,this VOD setting is illegal.

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| Symbol | $V_{OD}$ Setting | $V_{OD}$ Value (mV) | $V_{OD}$ Setting | $V_{OD}$ Value (mV) |
|---|---|---|---|---|
| | 9 | 180 | 41 | 820 |
| | 10 | 200 | 42 | 840 |
| | 11 | 220 | 43 | 860 |
| | 12 | 240 | 44 | 880 |
| | 13 | 260 | 45 | 900 |
| | 14 | 280 | 46 | 920 |
| $V_{OD}$ **differential peak to peak typical** | 15 | 300 | 47 | 940 |
| | 16 | 320 | 48 | 960 |
| | 17 | 340 | 49 | 980 |
| | 18 | 360 | 50 | 1000 |
| | 19 | 380 | 51 | 1020 |
| | 20 | 400 | 52 | 1040 |
| | 21 | 420 | 53 | 1060 |
| | 22 | 440 | 54 | 1080 |
| | 23 | 460 | 55 | 1100 |
| | 24 | 480 | 56 | 1120 |
| | 25 | 500 | 57 | 1140 |
| | 26 | 520 | 58 | 1160 |
| | 27 | 540 | 59 | 1180 |
| | 28 | 560 | 60 | 1200 |
| | 29 | 580 | 61 | 1220 |
| | 30 | 600 | 62 | 1240 |
| | 31 | 620 | 63 | 1260 |

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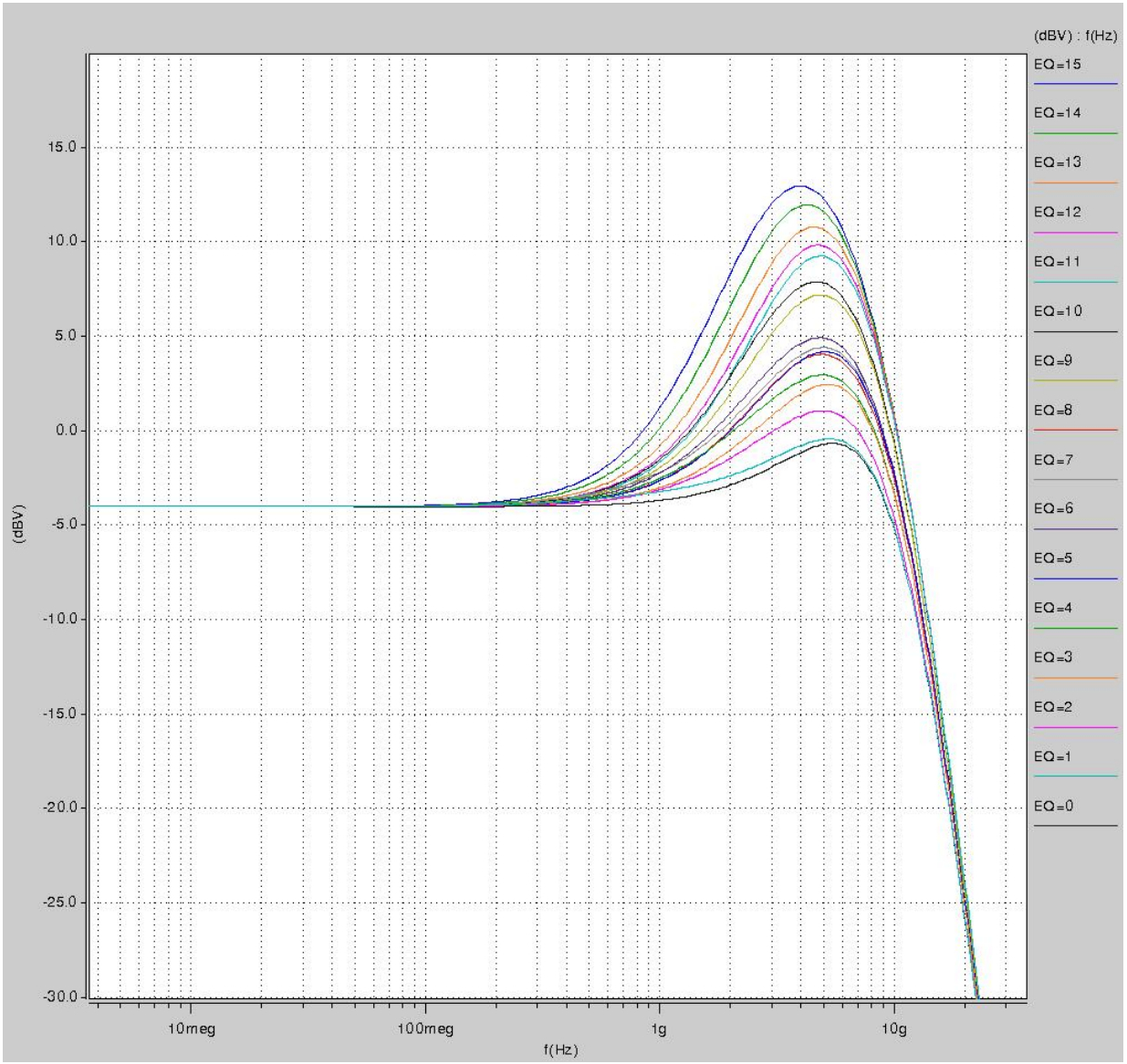
**Figure 24. AC Gain Curves for Arria V GZ Channels (full bandwidth)**



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## 2.2.2. Core Performance Specifications

### 2.2.2.1. Clock Tree Specifications

**Table 111. Clock Tree Performance for Arria V GZ Devices**

| Symbol | Performance | | Unit |
|---|---|---|---|
| | C3, I3L | C4, I4 | |
| Global and Regional Clock | 650 | 580 | MHz |
| Periphery Clock | 500 | 500 | MHz |

### 2.2.2.2. PLL Specifications

**Table 112. PLL Specifications for Arria V GZ Devices**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{IN}$ (170) | Input clock frequency (C3, I3L speed grade) | 5 | — | 800 | MHz |
| | Input clock frequency (C4, I4 speed grade) | 5 | — | 650 | MHz |
| $f_{INPFD}$ | Input frequency to the PFD | 5 | — | 325 | MHz |
| $f_{FINPFD}$ | Fractional Input clock frequency to the PFD | 50 | — | 160 | MHz |
| $f_{VCO}$ (171) | PLL VCO operating range (C3, I3L speed grade) | 600 | — | 1600 | MHz |
| | PLL VCO operating range (C4, I4 speed grade) | 600 | — | 1300 | MHz |
| $t_{EINDUTY}$ | Input clock or external feedback clock input duty cycle | 40 | — | 60 | % |

*continued...*

(170) This specification is limited in the Intel Quartus Prime software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(171) The VCO frequency reported by the Intel Quartus Prime software in the **PLL Usage Summary** section of the compilation report takes into consideration the VCO post divider value. Therefore, if the VCO post divider value is 2, the frequency reported can be lower than the $f_{VCO}$ specification.

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| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{OUT}$ (172) | Output frequency for an internal global or regional clock (C3, I3L speed grade) | — | — | 650 | MHz |
| | Output frequency for an internal global or regional clock (C4, I4 speed grade) | — | — | 580 | MHz |
| $f_{OUT_EXT}$ (172) | Output frequency for an external clock output (C3, I3L speed grade) | — | — | 667 | MHz |
| | Output frequency for an external clock output (C4, I4 speed grade) | — | — | 533 | MHz |
| $t_{OUTDUTY}$ | Duty cycle for a dedicated external clock output (when set to 50%) | 45 | 50 | 55 | % |
| $t_{FCOMP}$ | External feedback clock compensation time | — | — | 10 | ns |
| $f_{DYCONFIGCLK}$ | Dynamic configuration clock for `mgmt_clk` and `scanclk` | — | — | 100 | MHz |
| $t_{LOCK}$ | Time required to lock from the end-of-device configuration or deassertion of `areset` | — | — | 1 | ms |
| $t_{DLOCK}$ | Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) | — | — | 1 | ms |
| $f_{CLBW}$ | PLL closed-loop low bandwidth | — | 0.3 | — | MHz |
| | PLL closed-loop medium bandwidth | — | 1.5 | — | MHz |
| | PLL closed-loop high bandwidth (173) | — | 4 | — | MHz |
| $t_{PLL_PSERR}$ | Accuracy of PLL phase shift | — | — | ±50 | ps |
| $t_{ARESET}$ | Minimum pulse width on the `areset` signal | 10 | — | — | ns |
| $t_{INCCJ}$ (174), (175) | Input clock cycle-to-cycle jitter ($f_{REF}$ ≥ 100 MHz) | — | — | 0.15 | UI (p-p) |

*continued...*

(172) This specification is limited by the lower of the two: I/O $f_{MAX}$ or $f_{OUT}$ of the PLL.

(173) High bandwidth PLL settings are not supported in external feedback mode.

(174) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

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| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| | Input clock cycle-to-cycle jitter ($f_{REF}$ < 100 MHz) | -750 | — | +750 | ps (p-p) |
| $t_{OUTPJ_DC}$ (176) | Period Jitter for dedicated clock output in integer PLL ($f_{OUT}$ ≥ 100 MHz) | — | — | 175 | ps (p-p) |
| | Period Jitter for dedicated clock output in integer PLL ($f_{OUT}$ < 100 Mhz) | — | — | 17.5 | mUI (p-p) |
| $t_{FOUTPJ_DC}$ (176) | Period Jitter for dedicated clock output in fractional PLL ($f_{OUT}$ ≥ 100 MHz) | — | — | 250(179), 175(177) | ps (p-p) |
| | Period Jitter for dedicated clock output in fractional PLL ($f_{OUT}$ < 100 MHz) | — | — | 25(179), 17.5 (177) | mUI (p-p) |
| $t_{OUTCCJ_DC}$ (176) | Cycle-to-cycle Jitter for a dedicated clock output in integer PLL ($f_{OUT}$ ≥ 100 MHz) | — | — | 175 | ps (p-p) |
| | Cycle-to-cycle Jitter for a dedicated clock output in integer PLL ($f_{OUT}$ < 100 MHz) | — | — | 17.5 | mUI (p-p) |
| $t_{FOUTCCJ_DC}$ (176) | Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{OUT}$ ≥ 100 MHz) | — | — | 250(179), 175 (177) | ps (p-p) |
| | Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{OUT}$ < 100 MHz) | — | — | 25(179), 17.5 (177) | mUI (p-p) |
| $t_{OUTPJ_IO}$, (176), (178) | Period Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT}$ ≥ 100 MHz) | — | — | 600 | ps (p-p) |
| | Period Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT}$ < 100 MHz) | — | — | 60 | mUI (p-p) |

***continued...***

(175) The $f_{REF}$ is $f_{IN}/N$ specification applies when N = 1.

(176) Peak-to-peak jitter with a probability level of $10^{-12}$ (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in the *Worst-Case DCD on Arria V GZ I/O Pins* table.

(177) This specification only covered fractional PLL for low bandwidth. The $f_{VCO}$ for fractional value range 0.20–0.80 must be ≥ 1200 MHz.

(178) The external memory interface clock output jitter specifications use a different measurement method, which is available in the *Memory Output Clock Jitter Specification for Arria V GZ Devices* table.

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| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{FOUTPJ_IO}$ (176), (178), (179) | Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} \geq 100$ MHz) | — | — | 600 | ps (p-p) |
| | Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} < 100$ MHz) | — | — | 60 | mUI (p-p) |
| $t_{OUTCCJ_IO}$ (176), (178) | Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} \geq 100$ MHz) | — | — | 600 | ps (p-p) |
| | Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{OUT} < 100$ MHz) | — | — | 60 | mUI (p-p) |
| $t_{FOUTCCJ_IO}$ (176), (178), (179) | Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} \geq 100$ MHz) | — | — | 600 | ps (p-p) |
| | Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{OUT} < 100$ MHz) | — | — | 60 | mUI (p-p) |
| $t_{CASC_OUTPJ_DC}$ (176), (180) | Period Jitter for a dedicated clock output in cascaded PLLs ($f_{OUT} \geq 100$ MHz) | — | — | 175 | ps (p-p) |
| | Period Jitter for a dedicated clock output in cascaded PLLS ($f_{OUT} < 100$ MHz) | — | — | 17.5 | mUI (p-p) |
| $dK_{BIT}$ | Bit number of Delta Sigma Modulator (DSM) | 8 | 24 | 32 | Bits |
| $k_{VALUE}$ | Numerator of Fraction | 128 | 8388608 | 2147483648 | — |
| $f_{RES}$ | Resolution of VCO frequency ($f_{INPFD}$ = 100 MHz) | 390625 | 5.96 | 0.023 | Hz |

**Related Information**

- Duty Cycle Distortion (DCD) Specifications on page 150
- DLL Range Specifications on page 148

(179) This specification only covered fractional PLL for low bandwidth. The $f_{VCO}$ for fractional value range 0.05–0.95 must be ≥ 1000 MHz.

(180) The cascaded PLL specification is only applicable with the following condition:
a. Upstream PLL: 0.59Mhz ≤ Upstream PLL BW < 1 MHz
b. Downstream PLL: Downstream PLL BW > 2 MHz

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### 2.2.2.3. DSP Block Specifications

**Table 113. DSP Block Performance Specifications for Arria V GZ Devices**

| Mode | Performance | | | Unit |
|---|---|---|---|---|
| | C3, I3L | C4 | I4 | |
| **Modes using One DSP Block** | | | | |
| Three 9 × 9 | 480 | 420 | | MHz |
| One 18 × 18 | 480 | 420 | 400 | MHz |
| Two partial 18 × 18 (or 16 × 16) | 480 | 420 | 400 | MHz |
| One 27 × 27 | 400 | 350 | | MHz |
| One 36 × 18 | 400 | 350 | | MHz |
| One sum of two 18 × 18 (One sum of two 16 × 16) | 400 | 350 | | MHz |
| One sum of square | 400 | 350 | | MHz |
| One 18 × 18 plus 36 (a × b) + c | 400 | 350 | | MHz |
| **Modes using Two DSP Blocks** | | | | |
| Three 18 × 18 | 400 | 350 | | MHz |
| One sum of four 18 × 18 | 380 | 300 | | MHz |
| One sum of two 27 × 27 | 380 | 300 | 290 | MHz |
| One sum of two 36 × 18 | 380 | 300 | | MHz |
| One complex 18 × 18 | 400 | 350 | | MHz |
| One 36 × 36 | 380 | 300 | | MHz |
| **Modes using Three DSP Blocks** | | | | |
| One complex 18 × 25 | 340 | 275 | 265 | MHz |
| **Modes using Four DSP Blocks** | | | | |
| One complex 27 × 27 | 350 | 310 | | MHz |

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### 2.2.2.4. Memory Block Specifications

#### Table 114. Memory Block Performance Specifications for Arria V GZ Devices

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50%** output duty cycle. Use the Intel Quartus Prime software to report timing for this and other memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in $F_{MAX}$.

| Memory | Mode | Resources Used | | Performance | | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | ALUTs | Memory | C3 | C4 | I3L | I4 | |
| MLAB | Single port, all supported widths | 0 | 1 | 400 | 315 | 400 | 315 | MHz |
| | Simple dual-port, x32/x64 depth | 0 | 1 | 400 | 315 | 400 | 315 | MHz |
| | Simple dual-port, x16 depth (181) | 0 | 1 | 533 | 400 | 533 | 400 | MHz |
| | ROM, all supported widths | 0 | 1 | 500 | 450 | 500 | 450 | MHz |
| M20K Block | Single-port, all supported widths | 0 | 1 | 650 | 550 | 500 | 450 | MHz |
| | Simple dual-port, all supported widths | 0 | 1 | 650 | 550 | 500 | 450 | MHz |
| | Simple dual-port with the read-during-write option set to **Old Data**, all supported widths | 0 | 1 | 455 | 400 | 455 | 400 | MHz |
| | Simple dual-port with ECC enabled, 512 × 32 | 0 | 1 | 400 | 350 | 400 | 350 | MHz |
| | Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32 | 0 | 1 | 500 | 450 | 500 | 450 | MHz |
| | True dual port, all supported widths | 0 | 1 | 650 | 550 | 500 | 450 | MHz |
| | ROM, all supported widths | 0 | 1 | 650 | 550 | 500 | 450 | MHz |

(181) The $F_{MAX}$ specification is only achievable with Fitter options, **MLAB Implementation In 16-Bit Deep Mode** enabled.

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### 2.2.2.5. Temperature Sensing Diode Specifications

**Table 115. Internal Temperature Sensing Diode Specification for Arria V GZ Devices**

| Temperature Range | Accuracy | Offset Calibrated Option | Sampling Rate | Conversion Time(182) | Resolution | Minimum Resolution with no Missing Codes |
|---|---|---|---|---|---|---|
| –40°C to 100°C | ±8°C | No | 1 MHz, 500 kHz | < 100 ms | 8 bits | 8 bits |

**Table 116. External Temperature Sensing Diode Specifications for Arria V GZ Devices**

| Description | Min | Typ | Max | Unit |
|---|---|---|---|---|
| $I_{bias}$, diode source current | 8 | — | 200 | µA |
| $V_{bias,}$ voltage across diode | 0.3 | — | 0.9 | V |
| Series resistance | — | — | < 1 | Ω |
| Diode ideality factor | 1.006 | 1.008 | 1.010 | — |

**Related Information**

Intel FPGA Temperature Sensor IP Core User Guide
Provides more information about the temperature sensing operation.

## 2.2.3. Periphery Performance

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.

*Note:* The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

### 2.2.3.1. High-Speed I/O Specification

(182) For more details about the temperature sensing operations, refer to the *Intel FPGA Temperature Sensor IP Core User Guide*.

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### 2.2.3.1.1. High-Speed Clock Specifications

### Table 117. High-Speed Clock Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

For LVDS applications, you must use the PLLs in integer PLL mode.

Arria V GZ devices support the following output standards using true LVDS output buffer types on all I/O banks.

- True RSDS output standard with data rates of up to 230 Mbps
- True mini-LVDS output standard with data rates of up to 340 Mbps

| Symbol | Conditions | C3, I3L | | | C4, I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSCLK_in}$ (input clock frequency) True Differential I/O Standards (183) | Clock boost factor W = 1 to 40 (184) | 5 | — | 625 | 5 | — | 525 | MHz |
| $f_{HSCLK_in}$ (input clock frequency) Single Ended I/O Standards | Clock boost factor W = 1 to 40 (184) | 5 | — | 625 | 5 | — | 525 | MHz |
| $f_{HSCLK_in}$ (input clock frequency) Single Ended I/O Standards | Clock boost factor W = 1 to 40 (184) | 5 | — | 420 | 5 | — | 420 | MHz |
| $f_{HSCLK_OUT}$ (output clock frequency) | — | 5 | — | 625 (185) | 5 | — | 525 (185) | MHz |

(183) This only applies to DPA and soft-CDR modes.

(184) Clock Boost Factor (W) is the ratio between the input data rate to the input clock rate.

(185) This is achieved by using the LVDS clock network.

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### 2.2.3.1.2. Transmitter High-Speed I/O Specifications

**Table 118. Transmitter High-Speed I/O Specifications for Arria V GZ Devices**

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

| Symbol | Conditions | C3, I3L | | | C4, I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| True Differential I/O Standards - $f_{HSDR}$ (data rate) | SERDES factor J = 3 to 10 (186), (187) | (188) | — | 1250 | (188) | — | 1050 | Mbps |
| | SERDES factor J ≥ 4<br>LVDS TX with DPA (189), (190), (191), (192) | (188) | — | 1600 | (188) | — | 1250 | Mbps |
| | SERDES factor J = 2, uses DDR Registers | (188) | — | (193) | (188) | — | (193) | Mbps |
| | SERDES factor J = 1, uses SDR Register | (188) | — | (193) | (188) | — | (193) | Mbps |

*continued...*

(186) If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.

(187) The $F_{MAX}$ specification is based on the fast clock used for serial data. The interface $F_{MAX}$ is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

(188) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

(189) Arria V GZ RX LVDS will need DPA. For Arria V GZ TX LVDS, the receiver side component must have DPA.

(190) Requires package skew compensation with PCB trace length.

(191) Do not mix single-ended I/O buffer within LVDS I/O bank.

(192) Chip-to-chip communication only with a maximum load of 5 pF.

(193) The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (fOUT) provided you can close the design timing and the signal integrity simulation is clean.

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| Symbol | Conditions | C3, I3L | | | C4, I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Emulated Differential I/O Standards with Three External Output Resistor Networks - $f_{HSDR}$ (data rate) (194) | SERDES factor J = 4 to 10 (195) | (188) | — | 840 | (188) | — | 840 | Mbps |
| $t_{x\ Jitter}$ - True Differential I/O Standards | Total Jitter for Data Rate 600 Mbps - 1.25 Gbps | — | — | 160 | — | — | 160 | ps |
| | Total Jitter for Data Rate < 600 Mbps | — | — | 0.1 | — | — | 0.1 | UI |
| $t_{x\ Jitter}$ - Emulated Differential I/O Standards with Three External Output Resistor Network | Total Jitter for Data Rate 600 Mbps - 1.25 Gbps | — | — | 300 | — | — | 325 | ps |
| | Total Jitter for Data Rate < 600 Mbps | — | — | 0.2 | — | — | 0.25 | UI |
| $t_{DUTY}$ | Transmitter output clock duty cycle for both True and Emulated Differential I/O Standards | 45 | 50 | 55 | 45 | 50 | 55 | % |
| $t_{RISE}$ & $t_{FALL}$ | True Differential I/O Standards | — | — | 200 | — | — | 200 | ps |
| | Emulated Differential I/O Standards with three external output resistor networks | — | — | 250 | — | — | 300 | ps |
| TCCS | True Differential I/O Standards | — | — | 150 | — | — | 150 | ps |
| | Emulated Differential I/O Standards | — | — | 300 | — | — | 300 | ps |

(194) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine leftover timing margin.

(195) When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.

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### 2.2.3.1.3. Receiver High-Speed I/O Specifications

**Table 119. Receiver High-Speed I/O Specifications for Arria V GZ Devices**

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

| Symbol | Conditions | C3, I3L | | | C4, I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| True Differential I/O Standards - $f_{HSDRDPA}$ (data rate) | SERDES factor J = 3 to 10 (196), (197), (198), (199), (200), (201) | 150 | — | 1250 | 150 | — | 1050 | Mbps |
| | SERDES factor J ≥ 4 LVDS RX with DPA (197), (199), (200), (201) | 150 | — | 1600 | 150 | — | 1250 | Mbps |
| | SERDES factor J = 2, uses DDR Registers | (202) | — | (203) | (202) | — | (203) | Mbps |
| | SERDES factor J = 1, uses SDR Register | (202) | — | (203) | (202) | — | (203) | Mbps |

*continued...*

(196) The $F_{MAX}$ specification is based on the fast clock used for serial data. The interface $F_{MAX}$ is also dependent on the parallel clock domain which is design dependent and requires timing analysis.

(197) Arria V GZ RX LVDS will need DPA. For Arria V GZ TX LVDS, the receiver side component must have DPA.

(198) Arria V GZ LVDS serialization and de-serialization factor needs to be x4 and above.

(199) Requires package skew compensation with PCB trace length.

(200) Do not mix single-ended I/O buffer within LVDS I/O bank.

(201) Chip-to-chip communication only with a maximum load of 5 pF.

(202) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

(203) The maximum ideal data rate is the SERDES factor (J) x the PLL maximum output frequency (fOUT) provided you can close the design timing and the signal integrity simulation is clean.

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| Symbol | Conditions | C3, I3L | | | C4, I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| $f_{HSDR}$ (data rate) | SERDES factor J = 3 to 10 | (202) | — | (204) | (202) | — | (204) | Mbps |
| | SERDES factor J = 2, uses DDR Registers | (202) | — | (203) | (202) | — | (203) | Mbps |
| | SERDES factor J = 1, uses SDR Register | (202) | — | (203) | (202) | — | (203) | Mbps |

### 2.2.3.1.4. DPA Mode High-Speed I/O Specifications

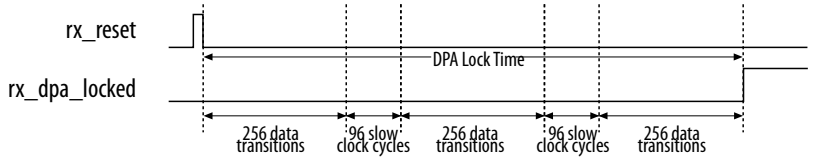
**Table 120. High-Speed I/O Specifications for Arria V GZ Devices**

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

| Symbol | Conditions | C3, I3L | | | C4, I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| DPA run length | — | — | — | 10000 | — | — | 10000 | UI |

**Figure 25. DPA Lock Time Specification with DPA PLL Calibration Enabled**




(204) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

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### Table 121. DPA Lock Time Specifications for Arria V GZ Devices

The DPA lock time is for one channel.

One data transition is defined as a 0-to-1 or 1-to-0 transition.

The DPA lock time stated in this table applies to both commercial and industrial grade.

| Standard | Training Pattern | Number of Data Transitions in One Repetition of the Training Pattern | Number of Repetitions per 256 Data Transitions (205) | Maximum |
|---|---|---|---|---|
| SPI-4 | 00000000001111111111 | 2 | 128 | 640 data transitions |
| Parallel Rapid I/O | 00001111 | 2 | 128 | 640 data transitions |
| | 10010000 | 4 | 64 | 640 data transitions |
| Miscellaneous | 10101010 | 8 | 32 | 640 data transitions |
| | 01010101 | 8 | 32 | 640 data transitions |

## 2.2.3.1.5. Soft CDR Mode High-Speed I/O Specifications

### Table 122. High-Speed I/O Specifications for Arria V GZ Devices

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

| Symbol | Conditions | C3, I3L | | | C4, I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Soft-CDR ppm tolerance | — | — | — | 300 | — | — | 300 | ± ppm |

(205) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

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**Figure 26. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate ≥ 1.25 Gbps**

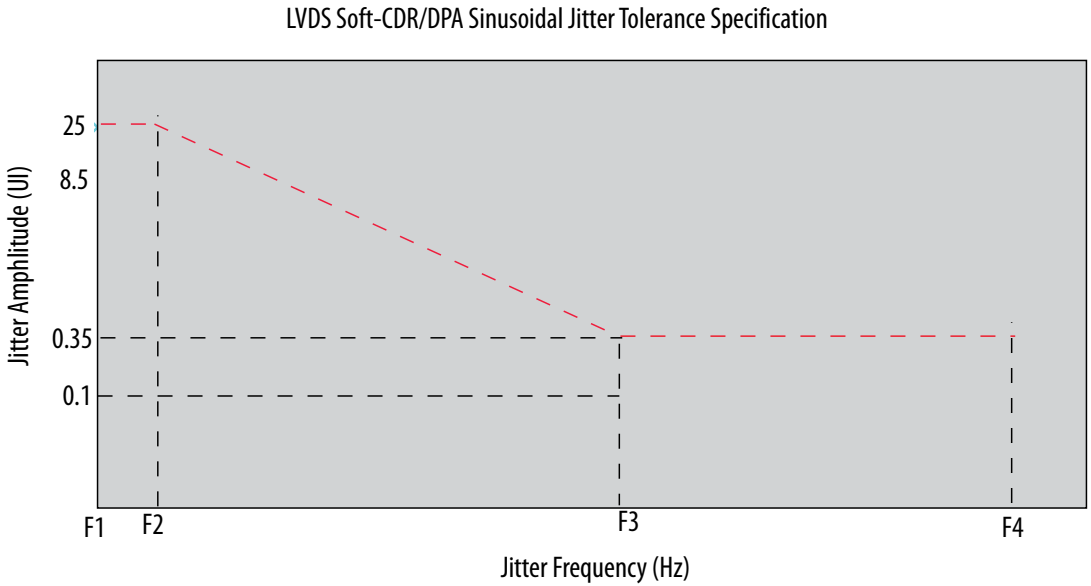


**Table 123. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate ≥ 1.25 Gbps**

| Jitter Frequency (Hz) | | Sinusoidal Jitter (UI) |
|---|---|---|
| F1 | 10,000 | 25.000 |
| F2 | 17,565 | 25.000 |
| F3 | 1,493,000 | 0.350 |
| F4 | 50,000,000 | 0.350 |

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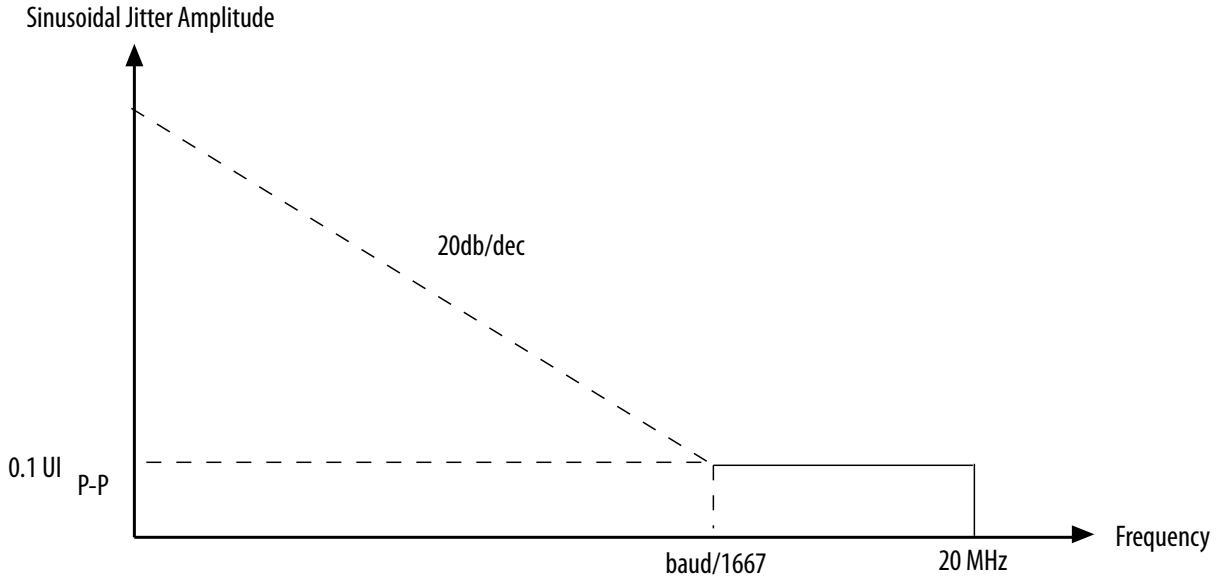
**Figure 27. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate < 1.25 Gbps**




### 2.2.3.1.6. Non DPA Mode High-Speed I/O Specifications

**Table 124. High-Speed I/O Specifications for Arria V GZ Devices**

When J = 3 to 10, use the serializer/deserializer (SERDES) block.

When J = 1 or 2, bypass the SERDES block.

| Symbol | Conditions | C3, I3L | | | C4, I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Sampling Window | — | — | — | 300 | — | — | 300 | ps |

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### 2.2.3.2. DLL Range Specifications

#### Table 125. DLL Range Specifications for Arria V GZ Devices

Arria V GZ devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

| Parameter | C3, I3L | C4, I4 | Unit |
|---|---|---|---|
| DLL operating frequency range | 300 – 890 | 300 – 890 | MHz |

### 2.2.3.3. DQS Logic Block Specifications

#### Table 126. DQS Phase Offset Delay Per Setting for Arria V GZ Devices

The typical value equals the average of the minimum and maximum values.

The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a –3 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is [625 ps + (10 × 11 ps) ± 20 ps] = 735 ps ± 20 ps.

| Speed Grade | Min | Max | Unit |
|---|---|---|---|
| C3, I3L | 8 | 15 | ps |
| C4, I4 | 8 | 16 | ps |

#### Table 127. DQS Phase Shift Error Specification for DLL-Delayed Clock ($t_{DQS_PSERR}$) for Arria V GZ Devices

This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a –3 speed grade is ±84 ps or ±42 ps.

| Number of DQS Delay Buffers | C3, I3L | C4, I4 | Unit |
|---|---|---|---|
| 1 | 30 | 32 | ps |
| 2 | 60 | 64 | ps |
| 3 | 90 | 96 | ps |
| 4 | 120 | 128 | ps |

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## 2.2.3.4. Memory Output Clock Jitter Specifications

### Table 128. Memory Output Clock Jitter Specification for Arria V GZ Devices

The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Intel recommends using PHY clock networks whenever possible.

The clock jitter specification applies to the memory output clock pins clocked by an integer PLL.

The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) -12, equivalent to 14 sigma.

| Clock Network | Parameter | Symbol | C3, I3L | | C4, I4 | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| Regional | Clock period jitter | $t_{JIT(per)}$ | –55 | 55 | –55 | 55 | ps |
| | Cycle-to-cycle period jitter | $t_{JIT(cc)}$ | –110 | 110 | –110 | 110 | ps |
| | Duty cycle jitter | $t_{JIT(duty)}$ | –82.5 | 82.5 | –82.5 | 82.5 | ps |
| Global | Clock period jitter | $t_{JIT(per)}$ | –82.5 | 82.5 | –82.5 | 82.5 | ps |
| | Cycle-to-cycle period jitter | $t_{JIT(cc)}$ | –165 | 165 | –165 | 165 | ps |
| | Duty cycle jitter | $t_{JIT(duty)}$ | –90 | 90 | –90 | 90 | ps |
| PHY Clock | Clock period jitter | $t_{JIT(per)}$ | –30 | 30 | –35 | 35 | ps |
| | Cycle-to-cycle period jitter | $t_{JIT(cc)}$ | –60 | 60 | –70 | 70 | ps |
| | Duty cycle jitter | $t_{JIT(duty)}$ | –45 | 45 | –56 | 56 | ps |

## 2.2.3.5. OCT Calibration Block Specifications

### Table 129. OCT Calibration Block Specifications for Arria V GZ Devices

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| OCTUSRCLK | Clock required by the OCT calibration blocks | — | — | 20 | MHz |
| $T_{OCTCAL}$ | Number of OCTUSRCLK clock cycles required for OCT $R_S/R_T$ calibration | — | 1000 | — | Cycles |
| $T_{OCTSHIFT}$ | Number of OCTUSRCLK clock cycles required for the OCT code to shift out | — | 32 | — | Cycles |
| $T_{RS_RT}$ | Time required between the `dyn_term_ctrl` and `oe` signal transitions in a bidirectional I/O buffer to dynamically switch between OCT $R_S$ and $R_T$ (See the figure below.) | — | 2.5 | — | ns |

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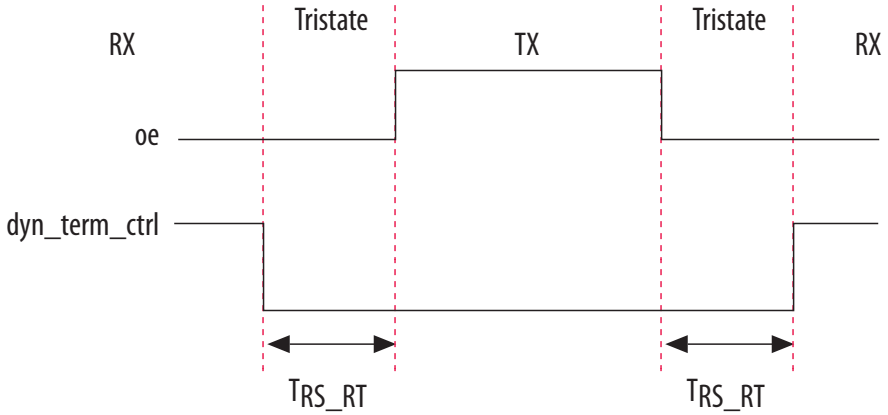
**Figure 28. Timing Diagram for oe and dyn_term_ctrl Signals**




## 2.2.3.6. Duty Cycle Distortion (DCD) Specifications

**Table 130. Worst-Case DCD on Arria V GZ I/O Pins**

The DCD numbers do not cover the core clock network.

| Symbol | C3, I3L | | C4, I4 | | Unit |
|---|---|---|---|---|---|
| | Min | Max | Min | Max | |
| Output Duty Cycle | 45 | 55 | 45 | 55 | % |

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# 2.3. Configuration Specification

## 2.3.1. POR Specifications

### Table 131. Fast and Standard POR Delay Specification for Arria V GZ Devices

Select the POR delay based on the MSEL setting as described in the "Configuration Schemes for Arria V Devices" table in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

| POR Delay | Minimum (ms) | Maximum (ms) |
|---|---|---|
| Fast | 4 | 12 (206) |
| Standard | 100 | 300 |

**Related Information**

Configuration, Design Security, and Remote System Upgrades in Arria V Devices

## 2.3.2. JTAG Configuration Specifications

### Table 132. JTAG Timing Parameters and Values for Arria V GZ Devices

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JCP}$ | TCK clock period | 30 | — | ns |
| $t_{JCP}$ | TCK clock period | 167 (207) | — | ns |
| $t_{JCH}$ | TCK clock high time | 14 | — | ns |
| $t_{JCL}$ | TCK clock low time | 14 | — | ns |
| $t_{JPSU\ (TDI)}$ | TDI JTAG port setup time | 2 | — | ns |
| $t_{JPSU\ (TMS)}$ | TMS JTAG port setup time | 3 | — | ns |
| $t_{JPH}$ | JTAG port hold time | 5 | — | ns |

***continued...***

(206) The maximum pulse width of the fast POR delay is 12 ms, providing enough time for the Arria V Hard IP for PCI Express Intel FPGA IP to initialize after the POR trip.

(207) The minimum TCK clock period is 167 ns if VCCBAT is within the range 1.2V-1.5V when you perform the volatile key programming.

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| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JPCO}$ | JTAG port clock to output | — | 11 (208) | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output | — | 14 (208) | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | — | 14 (208) | ns |

## 2.3.3. Fast Passive Parallel (FPP) Configuration Timing

### 2.3.3.1. DCLK-to-DATA[] Ratio (r) for FPP Configuration

FPP configuration requires a different DCLK-to-DATA[] ratio when you turn on encryption or the compression feature.

**Table 133. DCLK-to-DATA[] Ratio for Arria V GZ Devices**

Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is r times the data rate in bytes per second (Bps), or words per second (Wps). For example, in FPP ×16 when the DCLK-to-DATA[] ratio is 2, the DCLK frequency must be 2 times the data rate in Wps. Arria V GZ devices use the additional clock cycles to decrypt and decompress the configuration data.

| Configuration Scheme | Decompression | Design Security | DCLK-to-DATA[] Ratio |
|---|---|---|---|
| FPP ×8 | Disabled | Disabled | 1 |
| | Disabled | Enabled | 1 |
| | Enabled | Disabled | 2 |
| | Enabled | Enabled | 2 |
| FPP ×16 | Disabled | Disabled | 1 |
| | Disabled | Enabled | 2 |
| | Enabled | Disabled | 4 |
| | Enabled | Enabled | 4 |
| FPP ×32 | Disabled | Disabled | 1 |

*continued...*

(208) A 1-ns adder is required for each $V_{CCIO}$ voltage step down from 3.0 V. For example, $t_{JPCO}$ = 12 ns if $V_{CCIO}$ of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

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| Configuration Scheme | Decompression | Design Security | DCLK-to-DATA[] Ratio |
|---|---|---|---|
| | Disabled | Enabled | 4 |
| | Enabled | Disabled | 8 |
| | Enabled | Enabled | 8 |

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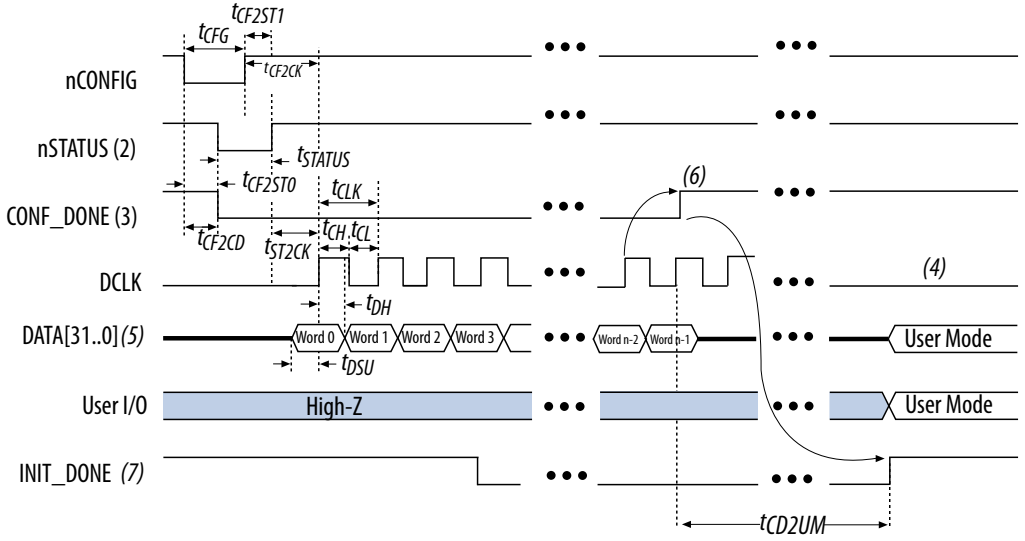
### 2.3.3.2. FPP Configuration Timing when DCLK to DATA[] = 1

**Figure 29. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is 1**

Timing waveform for FPP configuration when using a MAX® II or MAX V device as an external host.




Notes:

1. The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
2. After power-up, the Arria V GZ device holds nSTATUS low for the time of the POR delay.
3. After power-up, before and during configuration, CONF_DONE is low.
4. Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
5. For FPP ×16, use DATA[15..0]. For FPP ×8, use DATA[7..0]. DATA[31..0] are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.
6. To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF_DONE is released high when the Arria V GZ device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
7. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

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*Note:* When you enable the decompression or design security feature, the DCLK-to-DATA[] ratio varies for FPP ×8, FPP ×16, and FPP ×32. For the respective DCLK-to-DATA[] ratio, refer to the *DCLK-to-DATA[] Ratio for Arria V GZ Devices* table.

**Table 134. FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is 1**

Use these timing parameters when the decompression and design security features are disabled.

| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{CF2CD}$ | nCONFIG low to CONF_DONE low | — | 600 | ns |
| $t_{CF2ST0}$ | nCONFIG low to nSTATUS low | — | 600 | ns |
| $t_{CFG}$ | nCONFIG low pulse width | 2 | — | µs |
| $t_{STATUS}$ | nSTATUS low pulse width | 268 | 1,506 (209) | µs |
| $t_{CF2ST1}$ | nCONFIG high to nSTATUS high | — | 1,506 (210) | µs |
| $t_{CF2CK}$ (211) | nCONFIG high to first rising edge on DCLK | 1,506 | — | µs |
| $t_{ST2CK}$ (211) | nSTATUS high to first rising edge of DCLK | 2 | — | µs |
| $t_{DSU}$ | DATA[] setup time before rising edge on DCLK | 5.5 | — | ns |
| $t_{DH}$ | DATA[] hold time after rising edge on DCLK | 0 | — | ns |
| $t_{CH}$ | DCLK high time | 0.45 × 1/$f_{MAX}$ | — | s |
| $t_{CL}$ | DCLK low time | 0.45 × 1/$f_{MAX}$ | — | s |
| $t_{CLK}$ | DCLK period | 1/$f_{MAX}$ | — | s |
| $f_{MAX}$ | DCLK frequency (FPP ×8/×16) | — | 125 | MHz |
| | DCLK frequency (FPP ×32) | — | 100 | MHz |

*continued...*

(209) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(210) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

(211) If nSTATUS is monitored, follow the $t_{ST2CK}$ specification. If nSTATUS is not monitored, follow the $t_{CF2CK}$ specification.

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| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{CD2UM}$ | CONF_DONE high to user mode (212) | 175 | 437 | µs |
| $t_{CD2CU}$ | CONF_DONE high to CLKUSR enabled | 4 × maximum DCLK period | — | — |
| $t_{CD2UMC}$ | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU}$ + (8576 × CLKUSR period) (213) | — | — |

### Related Information

- DCLK-to-DATA[] Ratio (r) for FPP Configuration on page 152
- Configuration, Design Security, and Remote System Upgrades in Arria V Devices

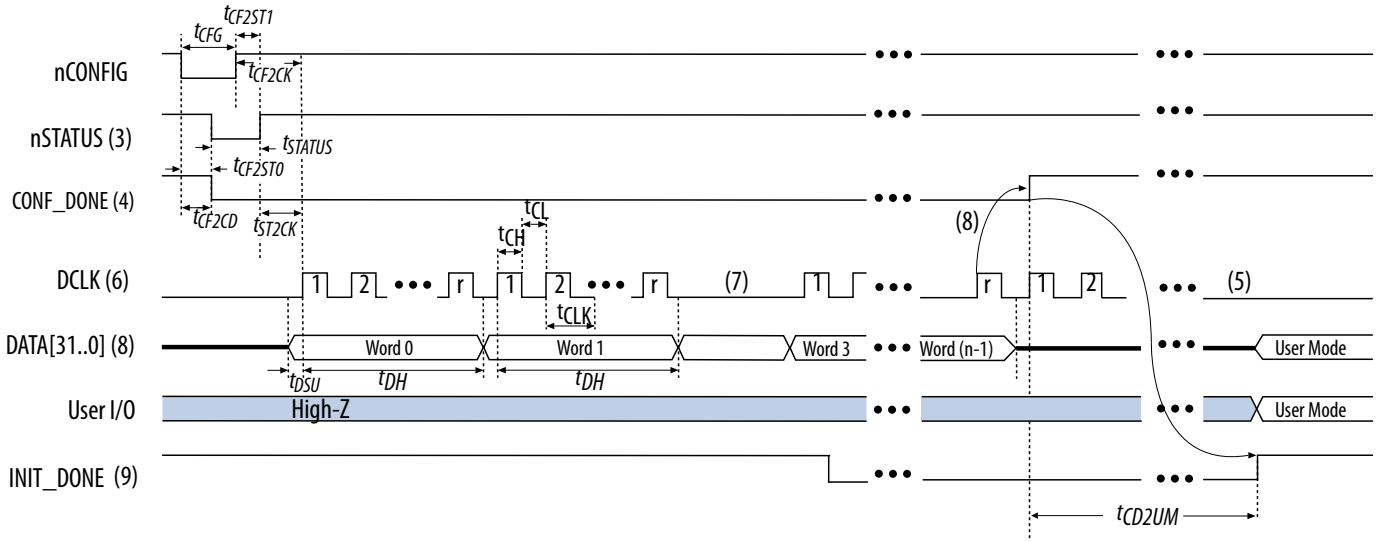
(212) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

(213) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the *Initialization* section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

### 2.3.3.3. FPP Configuration Timing when DCLK to DATA[] > 1

**Figure 30. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1 ,**

Timing when using a MAX II device, MAX V device, or microprocessor as an external host.




Notes:

1. To find out the DCLK-to-DATA[] ratio for your system, refer to the "DCLK-to-DATA[] Ratio for Arria V GZ Devices" table.
2. The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
3. After power-up, the Arria V GZ device holds nSTATUS low for the time as specified by the POR delay.
4. After power-up, before and during configuration, CONF_DONE is low.
5. Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
6. “r” denotes the DCLK-to-DATA[] ratio. For the DCLK-to-DATA[] ratio based on the decompression and the design security feature enable settings, refer to the "DCLK-to-DATA[] Ratio for Arria V GZ Devices" table.
7. If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA[31..0] pins prior to sending the first DCLK rising edge.
8. To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF_DONE is released high after the Arria V GZ device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
9. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

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### Table 135. FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is >1

Use these timing parameters when you use the decompression and design security features.

| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{CF2CD}$ | nCONFIG low to CONF_DONE low | — | 600 | ns |
| $t_{CF2ST0}$ | nCONFIG low to nSTATUS low | — | 600 | ns |
| $t_{CFG}$ | nCONFIG low pulse width | 2 | — | µs |
| $t_{STATUS}$ | nSTATUS low pulse width | 268 | 1,506 (214) | µs |
| $t_{CF2ST1}$ | nCONFIG high to nSTATUS high | — | 1,506 (215) | µs |
| $t_{CF2CK}$ (216) | nCONFIG high to first rising edge on DCLK | 1,506 | — | µs |
| $t_{ST2CK}$ (216) | nSTATUS high to first rising edge of DCLK | 2 | — | µs |
| $t_{DSU}$ | DATA[] setup time before rising edge on DCLK | 5.5 | — | ns |
| $t_{DH}$ | DATA[] hold time after rising edge on DCLK | $N-1/f_{DCLK}$ (217) | — | s |
| $t_{CH}$ | DCLK high time | $0.45 \times 1/f_{MAX}$ | — | s |
| $t_{CL}$ | DCLK low time | $0.45 \times 1/f_{MAX}$ | — | s |
| $t_{CLK}$ | DCLK period | $1/f_{MAX}$ | — | s |
| $f_{MAX}$ | DCLK frequency (FPP ×8/×16) | — | 125 | MHz |
| | DCLK frequency (FPP ×32) | — | 100 | MHz |
| $t_R$ | Input rise time | — | 40 | ns |
| $t_F$ | Input fall time | — | 40 | ns |

*continued...*

(214) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(215) You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.

(216) If nSTATUS is monitored, follow the $t_{ST2CK}$ specification. If nSTATUS is not monitored, follow the $t_{CF2CK}$ specification.

(217) N is the DCLK-to-DATA ratio and $f_{DCLK}$ is the DCLK frequency the system is operating.

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| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{CD2UM}$ | CONF_DONE high to user mode (218) | 175 | 437 | µs |
| $t_{CD2CU}$ | CONF_DONE high to CLKUSR enabled | 4 × maximum DCLK period | — | — |
| $t_{CD2UMC}$ | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU}$ + (8576 × CLKUSR period) (219) | — | — |

### Related Information

- DCLK-to-DATA[] Ratio (r) for FPP Configuration on page 152
- Configuration, Design Security, and Remote System Upgrades in Arria V Devices

(218) The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.

(219) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the *Initialization* section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

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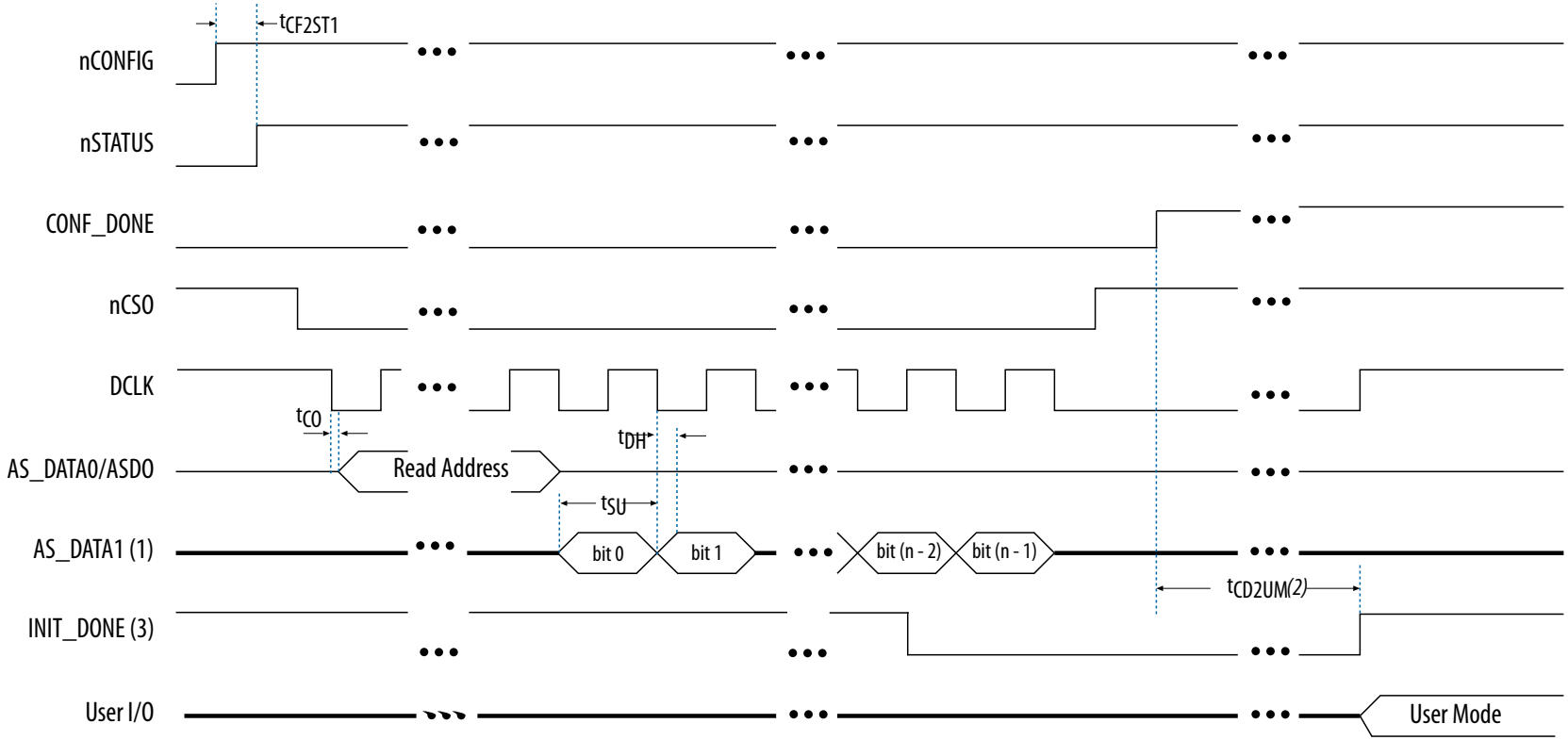
## 2.3.4. Active Serial Configuration Timing

**Figure 31. AS Configuration Timing**

Timing waveform for the active serial (AS) x1 mode and AS x4 mode configuration timing.




Notes:
1. If you are using AS ×4 mode, this signal represents the AS_DATA[3..0] and EPCQ sends in 4-bits of data for each DCLK cycle.
2. The initialization clock can be from internal oscillator or CLKUSR pin.
3. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

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## Table 136. AS Timing Parameters for AS x1 and AS x4 Configurations in Arria V GZ Devices

The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

$t_{CF2CD}$, $t_{CF2ST0}$, $t_{CFG}$, $t_{STATUS}$, and $t_{CF2ST1}$ timing parameters are identical to the timing parameters for PS mode listed in the "PS Timing Parameters for Arria V GZ Devices" table.

| Symbol | Parameter | Condition | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| $t_{CO}$ (220) | DCLK falling edge to AS_DATA0/ASDO output | — | — | 4 | ns |
| $t_{SU}$ (221) | Data setup time before falling edge on DCLK | — | 1.5 | — | ns |
| $t_{DH}$ (221) | Data hold time after falling edge on DCLK | –3 speed grade | 3.7 | — | ns |
| | | –4 speed grade | 3.9 | — | ns |
| $t_{CD2UM}$ | CONF_DONE high to user mode (222) | — | 175 | 437 | µs |
| $t_{CD2CU}$ | CONF_DONE high to CLKUSR enabled | — | 4 × maximum DCLK period | — | — |
| $t_{CD2UMC}$ | CONF_DONE high to user mode with CLKUSR option on | — | $t_{CD2CU}$ + (8576 × CLKUSR period) | — | — |

(220) Load capacitance for DCLK = 6 pF and AS_DATA/ASDO = 8 pF. Intel recommends obtaining the $t_{CO}$ for a given link (including receiver, transmission lines, connectors, and termination resistors) through IBIS or HSPICE simulation.

(221) To evaluate the data setup ($t_{SU}$) and data hold time ($t_{DH}$) slack on your board in order to ensure you are meeting the $t_{SU}$ and $t_{DH}$ requirement, Intel recommends following the guideline in the "Evaluating Data Setup and Hold Timing Slack" chapter in *AN822: Intel FPGA Configuration Device Migration Guideline*.

(222) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on this pin, refer to the "Initialization" section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

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### Table 137. DCLK Frequency Specification in the AS Configuration Scheme

This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.

The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

| Minimum | Typical | Maximum | Unit |
|---|---|---|---|
| 5.3 | 7.9 | 12.5 | MHz |
| 10.6 | 15.7 | 25.0 | MHz |
| 21.3 | 31.4 | 50.0 | MHz |
| 42.6 | 62.9 | 100.0 | MHz |

#### Related Information

- Passive Serial Configuration Timing on page 163
- Evaluating Data Setup and Hold Timing Slack chapter, AN822: Intel FPGA Configuration Device Migration Guideline
- Configuration, Design Security, and Remote System Upgrades in Arria V Devices

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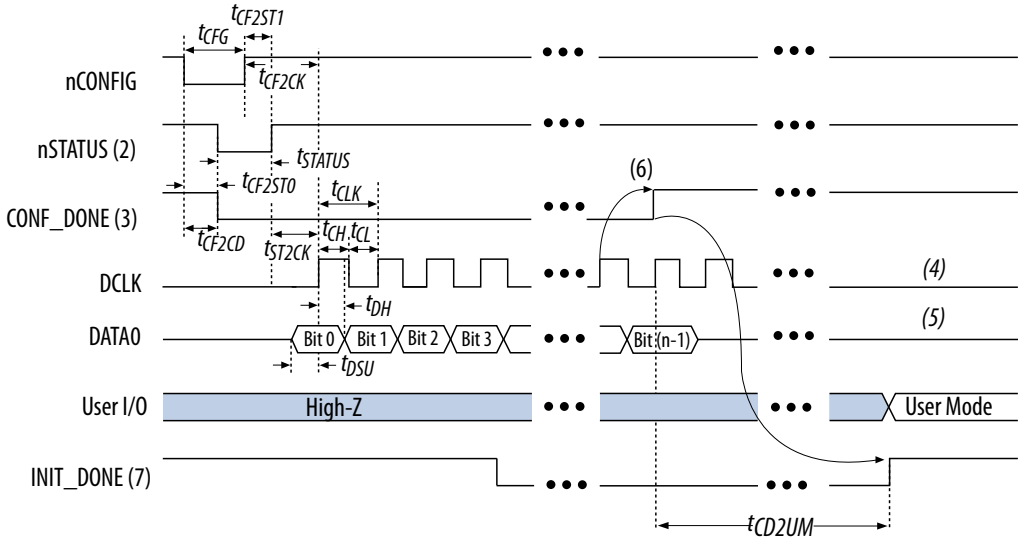
## 2.3.5. Passive Serial Configuration Timing

### Figure 32. PS Configuration Timing Waveform

Timing waveform for a passive serial (PS) configuration when using a MAX II device, MAX V device, or microprocessor as an external host.




Notes:

1. The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
2. After power-up, the Arria V GZ device holds nSTATUS low for the time of the POR delay.
3. After power-up, before and during configuration, CONF_DONE is low.
4. Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
5. DATA0 is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the Device and Pins Option.
6. To ensure a successful configuration, send the entire configuration data to the Arria V GZ device. CONF_DONE is released high after the Arria V GZ device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
7. After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

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### Table 138. PS Timing Parameters for Arria V GZ Devices

| Symbol | Parameter | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $t_{CF2CD}$ | nCONFIG low to CONF_DONE low | — | 600 | ns |
| $t_{CF2ST0}$ | nCONFIG low to nSTATUS low | — | 600 | ns |
| $t_{CFG}$ | nCONFIG low pulse width | 2 | — | µs |
| $t_{STATUS}$ | nSTATUS low pulse width | 268 | 1,506 (223) | µs |
| $t_{CF2ST1}$ | nCONFIG high to nSTATUS high | — | 1,506 (224) | µs |
| $t_{CF2CK}$ (225) | nCONFIG high to first rising edge on DCLK | 1,506 | — | µs |
| $t_{ST2CK}$ (225) | nSTATUS high to first rising edge of DCLK | 2 | — | µs |
| $t_{DSU}$ | DATA[] setup time before rising edge on DCLK | 5.5 | — | ns |
| $t_{DH}$ | DATA[] hold time after rising edge on DCLK | 0 | — | ns |
| $t_{CH}$ | DCLK high time | 0.45 × 1/$f_{MAX}$ | — | s |
| $t_{CL}$ | DCLK low time | 0.45 × 1/$f_{MAX}$ | — | s |
| $t_{CLK}$ | DCLK period | 1/$f_{MAX}$ | — | s |
| $f_{MAX}$ | DCLK frequency | — | 125 | MHz |
| $t_{CD2UM}$ | CONF_DONE high to user mode (226) | 175 | 437 | µs |
| $t_{CD2CU}$ | CONF_DONE high to CLKUSR enabled | 4 × maximum DCLK period | — | — |
| $t_{CD2UMC}$ | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU}$ + (8576 × CLKUSR period) (227) | — | — |

(223) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(224) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

(225) If nSTATUS is monitored, follow the $t_{ST2CK}$ specification. If nSTATUS is not monitored, follow the $t_{CF2CK}$ specification.

(226) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

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**Related Information**

Configuration, Design Security, and Remote System Upgrades in Arria V Devices

## 2.3.6. Initialization

**Table 139. Initialization Clock Source Option and the Maximum Frequency for Arria V GZ Devices**

| Initialization Clock Source | Configuration Schemes | Maximum Frequency (MHz) | Minimum Number of Clock Cycles |
|---|---|---|---|
| Internal Oscillator | AS, PS, FPP | 12.5 | 8576 |
| CLKUSR (228) | PS, FPP | 125 | |
| | AS | 100 | |
| DCLK | PS, FPP | 125 | |

## 2.3.7. Configuration Files

Use the following table to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal file (`.hex`) or tabular text file (`.ttf`) format, have different file sizes.

For the different types of configuration file and file sizes, refer to the Intel Quartus Prime software. However, for a specific version of the Intel Quartus Prime software, any design targeted for the same device has the same uncompressed configuration file size.

(227) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the *Initialization* section of the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

(228) To enable CLKUSR as the initialization clock source, turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Intel Quartus Prime software from the **General** panel of the **Device and Pin Options** dialog box.

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### Table 140. Uncompressed .rbf Sizes for Arria V GZ Devices

| Variant | Member Code | Configuration .rbf Size (bits) | IOCSR .rbf Size (bits) (229) |
|---|---|---|---|
| Arria V GZ | E1 | 137,598,880 | 562,208 |
| | E3 | 137,598,880 | 562,208 |
| | E5 | 213,798,880 | 561,760 |
| | E7 | 213,798,880 | 561,760 |

### Table 141. Minimum Configuration Time Estimation for Arria V GZ Devices

| Variant | Member Code | Active Serial (230) | | | Fast Passive Parallel (231) | | |
|---|---|---|---|---|---|---|---|
| | | Width | DCLK (MHz) | Min Config Time (ms) | Width | DCLK (MHz) | Min Config Time (ms) |
| Arria V GZ | E1 | 4 | 100 | 344 | 32 | 100 | 43 |
| | E3 | 4 | 100 | 344 | 32 | 100 | 43 |
| | E5 | 4 | 100 | 534 | 32 | 100 | 67 |
| | E7 | 4 | 100 | 534 | 32 | 100 | 67 |

(229) The IOCSR **.rbf** size is specifically for the Configuration via Protocol (CvP) feature.

(230) DCLK frequency of 100 MHz using external CLKUSR.

(231) Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

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## 2.3.8. Remote System Upgrades Circuitry Timing Specification

**Table 142. Remote System Upgrade Circuitry Timing Specifications**

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| $t_{RU_nCONFIG}$ (232) | 250 | — | ns |
| $t_{RU_nRSTIMER}$ (233) | 250 | — | ns |

**Related Information**

- Configuration, Design Security, and Remote System Upgrades in Arria V Devices
  For more information about the reconfiguration input for the Remote Update Intel FPGA IP core, refer to the *User Watchdog Timer* section.
- Configuration, Design Security, and Remote System Upgrades in Arria V Devices
  For more information about the `reset_timer` input for the Remote Update Intel FPGA IP core, refer to the *Remote System Upgrade State Machine* section.

## 2.3.9. User Watchdog Internal Oscillator Frequency Specification

**Table 143. User Watchdog Internal Oscillator Frequency Specifications**

| Minimum | Typical | Maximum | Unit |
|---|---|---|---|
| 5.3 | 7.9 | 12.5 | MHz |

## 2.4. I/O Timing

Intel offers two ways to determine I/O timing—the Excel-based I/O Timing and the Intel Quartus Prime Timing Analyzer.

(232) This is equivalent to strobing the reconfiguration input of the Remote Update Intel FPGA IP core high for the minimum timing specification. For more information, refer to the *Remote System Upgrade State Machine* section in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

(233) This is equivalent to strobing the reset_timer input of the Remote Update Intel FPGA IP core high for the minimum timing specification. For more information, refer to the *User Watchdog Timer* section in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

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Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis.

The Intel Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

**Related Information**

Arria V Devices Documentation page
For the Excel-based I/O Timing spreadsheet.

## 2.4.1. Programmable IOE Delay

**Table 144. IOE Programmable Delay for Arria V GZ Devices**

| Parameter (234) | Available Settings | Min Offset (235) | Fast Model | | Slow Model | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | C3 | C4 | I3L | I4 | |
| D1 | 64 | 0 | 0.464 | 0.493 | 0.924 | 1.011 | 0.921 | 1.006 | ns |
| D2 | 32 | 0 | 0.230 | 0.244 | 0.459 | 0.503 | 0.456 | 0.500 | ns |
| D3 | 8 | 0 | 1.587 | 1.699 | 2.992 | 3.192 | 3.047 | 3.257 | ns |
| D4 | 64 | 0 | 0.464 | 0.492 | 0.924 | 1.011 | 0.920 | 1.006 | ns |
| D5 | 64 | 0 | 0.464 | 0.493 | 0.924 | 1.011 | 0.921 | 1.006 | ns |
| D6 | 32 | 0 | 0.229 | 0.244 | 0.458 | 0.503 | 0.456 | 0.499 | ns |

(234) You can set this value in the Intel Quartus Prime software by selecting **D1**, **D2**, **D3**, **D4**, **D5**, and **D6** in the **Assignment Name** column of **Assignment Editor**.

(235) Minimum offset does not include the intrinsic delay.

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## 2.4.2. Programmable Output Buffer Delay

### Table 145. Programmable Output Buffer Delay for Arria V GZ Devices

You can set the programmable output buffer delay in the Intel Quartus Prime software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

| Symbol | Parameter | Typical | Unit |
|---|---|---|---|
| $D_{OUTBUF}$ | Rising and/or falling edge delay | 0 (default) | ps |
| | | 50 | ps |
| | | 100 | ps |
| | | 150 | ps |

## 2.5. Glossary

### Table 146. Glossary

| Term | Definition |
|---|---|
| Differential I/O Standards | Receiver Input Waveforms |

*continued...*

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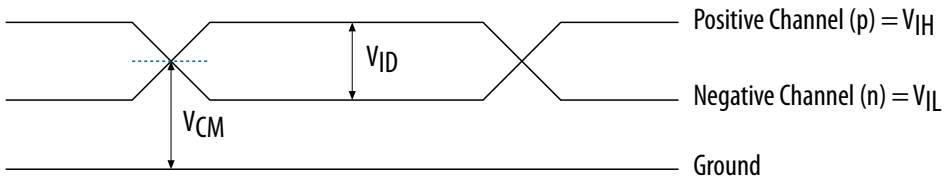
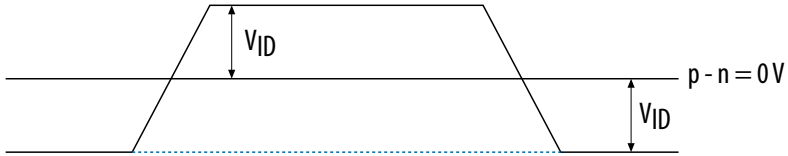
| Term | Definition |
|---|---|
| | **Single-Ended Waveform**<br>  <br>**Differential Waveform**<br>  <br>Transmitter Output Waveforms |

*continued...*

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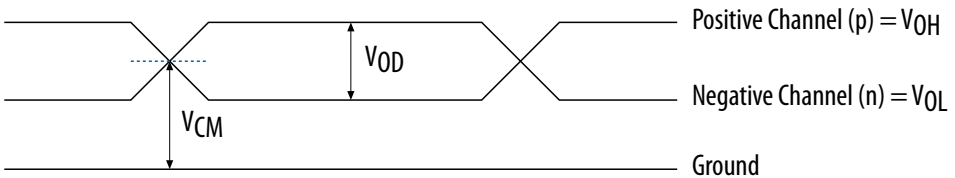
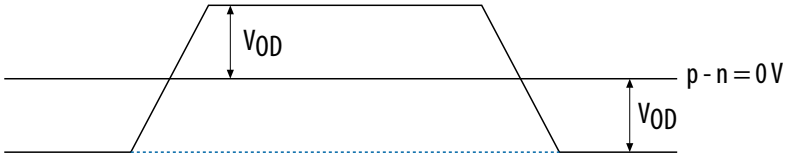
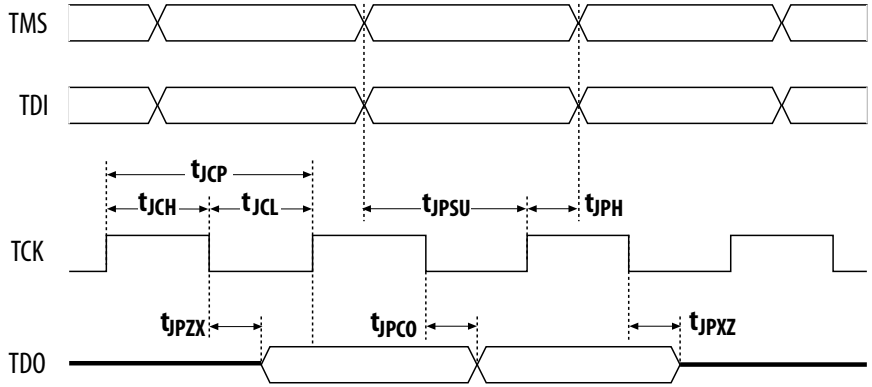
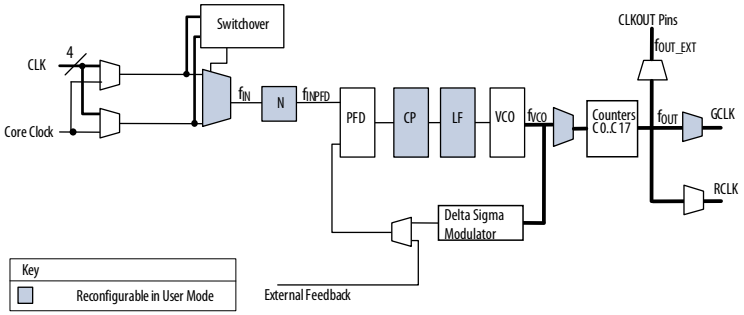
| Term | Definition |
|---|---|
| | **Single-Ended Waveform**<br>  <br><br>**Differential Waveform**<br>  <br> |
| $f_{HSCLK}$ | Left and right PLL input clock frequency. |
| $f_{HSDR}$ | High-speed I/O block—Maximum and minimum LVDS data transfer rate ($f_{HSDR}$ = 1/TUI), non-DPA. |
| $f_{HSDRDPA}$ | High-speed I/O block—Maximum and minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA. |
| J | High-speed I/O block—Deserialization factor (width of parallel data bus). |
| JTAG Timing Specifications | JTAG Timing Specifications: |

***continued...***

| Term | Definition |
|---|---|
| |  |
| PLL Specifications | Diagram of PLL Specifications<br>  <br>Note:<br>1. Core Clock can only be fed by dedicated clock input pins or PLL outputs. |
| $R_L$ | Receiver differential input discrete resistor (external to the Arria V GZ device). |
| SW (sampling window) | Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown: |

*continued...*

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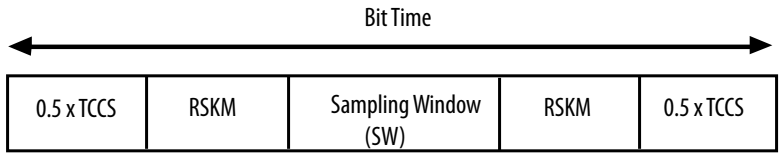
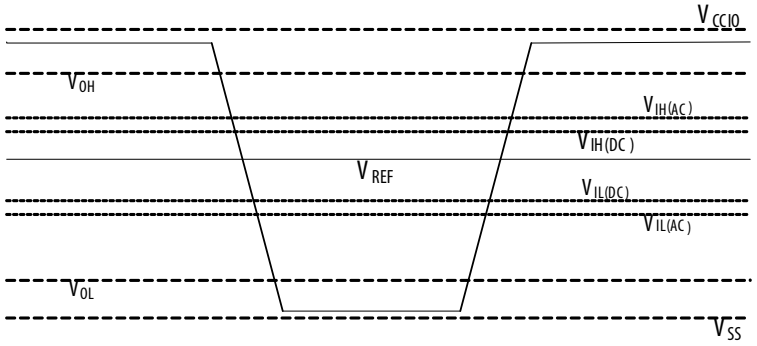
| Term | Definition |
|---|---|
| |  |
| Single-ended voltage referenced I/O standard | The JEDEC standard for SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.<br>The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing:<br>Single-Ended Voltage Referenced I/O Standard<br>  |
| $t_C$ | High-speed receiver and transmitter input and output clock period. |
| TCCS (channel-to-channel-skew) | The timing difference between the fastest and slowest output edges, including $t_{CO}$ variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table). |
| $t_{DUTY}$ | High-speed I/O block—Duty cycle on the high-speed transmitter output clock. |
| $t_{FALL}$ | Signal high-to-low transition time (80-20%) |
| $t_{INCCJ}$ | Cycle-to-cycle jitter tolerance on the PLL clock input. |
| $t_{OUTPJ_IO}$ | Period jitter on the general purpose I/O driven by a PLL. |
| $t_{OUTPJ_DC}$ | Period jitter on the dedicated clock output driven by a PLL. |
| $t_{RISE}$ | Signal low-to-high transition time (20-80%) |

***continued...***

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| Term | Definition |
|---|---|
| Timing Unit Interval (TUI) | The timing budget allowed for skew, propagation delays, and the data sampling window.<br>(TUI = 1/(receiver input clock frequency multiplication factor) = $t_C$/w) |
| $V_{CM(DC)}$ | DC common mode input voltage. |
| $V_{ICM}$ | Input common mode voltage—The common mode of the differential signal at the receiver. |
| $V_{ID}$ | Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver. |
| $V_{DIF(AC)}$ | AC differential input voltage—Minimum AC input differential voltage required for switching. |
| $V_{DIF(DC)}$ | DC differential input voltage— Minimum DC input differential voltage required for switching. |
| $V_{IH}$ | Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high. |
| $V_{IH(AC)}$ | High-level AC input voltage |
| $V_{IH(DC)}$ | High-level DC input voltage |
| $V_{IL}$ | Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low. |
| $V_{IL(AC)}$ | Low-level AC input voltage |
| $V_{IL(DC)}$ | Low-level DC input voltage |
| $V_{OCM}$ | Output common mode voltage—The common mode of the differential signal at the transmitter. |
| $V_{OD}$ | Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter. |
| $V_{SWING}$ | Differential input voltage |
| $V_X$ | Input differential cross point voltage |
| $V_{OX}$ | Output differential cross point voltage |
| W | High-speed I/O block—clock boost factor |

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## 2.6. Arria V GZ Device Datasheet Revision History

| Document Version | Changes |
|---|---|
| 2019.04.26 | Added a note for Conversion Time in the *Internal Temperature Sensing Diode Specification for Arria V GZ Devices* table. |
| 2019.01.25 | • Added *Arria V GZ Devices Overshoot Duration* diagram.<br>• Changed "VCO post-scale counter K value" to "VCO post divider value" in the $f_{VCO}$ note in the *PLL Specifications for Arria V GZ Devices* table.<br>• Updated the *AS Timing Parameters for AS ×1 and ×4 Configurations in Arria V GZ Devices* table.<br>— Updated $t_{DH}$ specifications. These specifications are applicable to the commercial and industrial grade devices.<br>— Added note to $t_{CO}$, $t_{SU}$, and $t_{DH}$.<br>• Changed instances of *Quartus II* to *Intel Quartus Prime*.<br>• Removed PowerPlay text from tool name.<br>• Renamed IP cores as per Intel rebranding. |

| Date | Version | Changes |
|---|---|---|
| February 2017 | 2017.02.10 | • Changed the minimum value for $t_{CD2UMC}$ in the "FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is 1" table.<br>• Changed the minimum value for $t_{CD2UMC}$ in the "FPP Timing Parameters for Arria V GZ Devices When the DCLK-to-DATA[] Ratio is >1" table.<br>• Changed the minimum value for $t_{CD2UMC}$ in the "AS Timing Parameters for AS x1 and AS x4 Configurations in Arria V GZ Devices" table.<br>• Changed the minimum value for $t_{CD2UMC}$ in the "PS Timing Parameters for Arria V GZ Devices" table.<br>• Changed the minimum number of clock cycles value in the "Initialization Clock Source Option and the Maximum Frequency for Arria V GZ Devices" table. |
| June 2016 | 2016.06.20 | • Changed column heading from "Value" to "Maximum" in the "Pin Capacitance for Arria V GZ Devices" table.<br>• Changed the minimum supported data rate range values from "1000" to "2000" in the "ATX PLL Specifications for Arria V GZ Devices" table.<br>• Added the supported data rates for the following output standards using true LVDS output buffer types in the "High-Speed Clock Specifications for Arria V GZ Devices" table:<br>— True RSDS output standard: data rates of up to 230 Mbps<br>— True mini-LVDS output standard: data rates of up to 340 Mbps |
| December 2015 | 2015.12.16 | • Removed the CDR ppm tolerance specification from the "Receiver Specifications for Arria V GZ Devices" table.<br>• Removed transmitter rise and fall time specifications from the "Transmitter Specifications for Arria V GZ Devices" table.<br>• Changed the .rbf sizes in the "Uncompressed .rbf Sizes for Arria V GZ Devices" table.<br>• Added a footnote to the "Transmitter High-Speed I/O Specifications for Arria V GZ Devices" table. |

***continued...***

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| Date | Version | Changes |
|---|---|---|
| June 2015 | 2015.06.16 | • Changed the conditions for the reference clock rise and fall time and added a note to the condition in the "Reference Clock Specifications for Arria V GZ Devices" table.<br>• Added a note to the "Minimum differential eye opening at receiver serial input pins" specification in the "Receiver Specifications for Arria V GZ Devices" table. |
| January 2015 | 2015.01.30 | • Added 240-Ω to the "OCT Calibration Accuracy Specifications for Arria V GZ Devices" table.<br>• Changed the CDR PPM tolerance spec in the "Receiver Specifications for Arria V GZ Devices" table.<br>• Added additional max data rate for fPLL in the "Fractional PLL Specifications for Arria V GZ Devices" table. |
| July 2014 | 3.8 | • Updated Table 21.<br>• Updated Table 22 $V_{OCM}$ (DC Coupled) condition.<br>• Updated the DCLK note to Figure 6, Figure 7, and Figure 9.<br>• Added note to Table 5 and Table 6.<br>• Added the DCLK specification to Table 50.<br>• Added note to Table 51.<br>• Updated the list of parameters in Table 53. |
| February 2014 | 3.7 | Updated Table 28. |
| December 2013 | 3.6 | • Updated Table 2, Table 13, Table 18, Table 19, Table 22, Table 30, Table 33, Table 37, Table 38, Table 45, Table 46, Table 47, Table 56, Table 49.<br>• Updated “PLL Specifications”. |
| August 2013 | 3.5 | Updated Table 28. |
| August 2013 | 3.4 | • Removed Preliminary tags for Table 2, Table 4, Table 5, Table 14, Table 27, Table 28, Table 29, Table 31, Table 32, Table 43, Table 45, Table 46, Table 47, Table 48, Table 49, Table 50, and Table 54.<br>• Updated Table 2 and Table 28. |
| June 2013 | 3.3 | Updated Table 23, Table 28, Table 51, and Table 55. |
| May 2013 | 3.2 | • Added Table 23.<br>• Updated Table 5, Table 22, Table 26, and Table 57.<br>• Updated Figure 6, Figure 7, Figure 8, and Figure 9. |
| March 2013 | 3.1 | • Updated Table 2, Table 6, Table 7, Table 8, Table 19, Table 22, Table 26, Table 29, Table 52.<br>• Updated “Maximum Allowed Overshoot and Undershoot Voltage”. |
| December 2012 | 3.0 | Initial release. |

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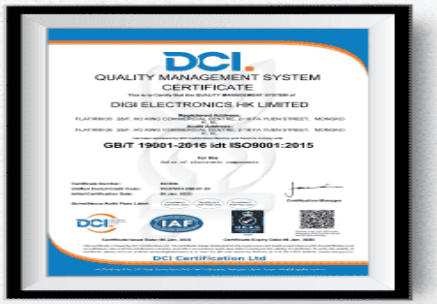

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