5M240ZT100C4N Datasheet

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DiGi Electronics Part Number	5M240ZT100C4N-DG
Manufacturer	Intel
Manufacturer Product Number	5M240ZT100C4N
Description	IC CPLD 192MC 7.5NS 100TQFP
Detailed Description	Embedded, Integrated Circuits (ICs)

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RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
5M240ZT100C4N	Intel
Series:	Product Status:
MAX® V	Active
DiGi-Electronics Programmable:	Programmable Type:
Verified	In System Programmable
Delay Time tpd(1) Max:	Voltage Supply - Internal:
7.5 ns	1.71V ~ 1.89V
Number of Logic Elements/Blocks:	Number of Macrocells:
240	192
Number of I/O:	Operating Temperature:
79	0°C ~ 85°C (TJ)
Mounting Type:	Package / Case:
Surface Mount	100-TQFP
Supplier Device Package:	Base Product Number:
100-TQFP (14x14)	5M240Z

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
RoHS Compliant	3 (168 Hours)
REACH Status:	ECCN:
REACH Unaffected	3A991D
HTSUS:	
8542.39.0001	

Section I. MAX V Device Core

This section provides a complete overview of all features relating to the MAX® V device family.

This section includes the following chapters:

1. MAX V Device Family Overview

MV51001-1.2

The MAX® V family of low cost and low power CPLDs offer more density and I/Os per footprint versus other CPLDs. Ranging in density from 40 to 2,210 logic elements (LEs) (32 to 1,700 equivalent macrocells) and up to 271 I/Os, MAX V devices provide programmable solutions for applications such as I/O expansion, bus and protocol bridging, power monitoring and control, FPGA configuration, and analog IC interface.

MAX V devices feature on-chip flash storage, internal oscillator, and memory functionality. With up to 50% lower total power versus other CPLDs and requiring as few as one power supply, MAX V CPLDs can help you meet your low power design requirement.

This chapter contains the following sections:

Feature Summary

The following list summarizes the MAX V device family features:

- Low-cost, low-power, and non-volatile CPLD architecture
- Instant-on (0.5 ms or less) configuration time
- Standby current as low as 25 µA and fast power-down/reset operation
- Fast propagation delay and clock-to-output times
- Internal oscillator
- Emulated RSDS output support with a data rate of up to 200 Mbps
- Emulated LVDS output support with a data rate of up to 304 Mbps
- Four global clocks with two clocks available per logic array block (LAB)
- User flash memory block up to 8 Kbits for non-volatile storage with up to 1000 read/write cycles
- Single 1.8-V external supply for device core
- MultiVolt I/O interface supporting 3.3-V, 2.5-V, 1.8-V, 1.5-V, and 1.2-V logic levels
- Bus-friendly architecture including programmable slew rate, drive strength, bus-hold, and programmable pull-up resistors
- Schmitt triggers enabling noise tolerant inputs (programmable per pin)

- I/Os are fully compliant with the PCI-SIG® PCI Local Bus Specification, revision 2.2 for 3.3-V operation
- Hot-socket compliant
- Built-in JTAG BST circuitry compliant with IEEE Std. 1149.1-1990

Table 1–1 lists the MAX V family features.

Table 1–1. MAX V Family Features

Feature	5M40Z	5M80Z	5M160Z	5M240Z	5M570Z	5M1270Z	5M2210Z
LEs	40	80	160	240	570	1,270	2,210
Typical Equivalent Macrocells	32	64	128	192	440	980	1,700
User Flash Memory Size (bits)	8,192	8,192	8,192	8,192	8,192	8,192	8,192
Global Clocks	4	4	4	4	4	4	4
Internal Oscillator	1	1	1	1	1	1	1
Maximum User I/O pins	54	79	79	114	159	271	271
t_{PD1} (ns) *(1)*	7.5	7.5	7.5	7.5	9.0	6.2	7.0
f_{CNT} (MHz) *(2)*	152	152	152	152	152	304	304
t_{SU} (ns)	2.3	2.3	2.3	2.3	2.2	1.2	1.2
t_{CO} (ns)	6.5	6.5	6.5	6.5	6.7	4.6	4.6

Notes to Table 1–1:

(1) t_{PD1} represents a pin-to-pin delay for the worst case I/O placement with a full diagonal path across the device and combinational logic implemented in a single LUT and LAB that is adjacent to the output pin.

(2) The maximum global clock frequency, f_{CNT}, is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay will run faster than this number.

MAX V devices accept 1.8 V on their VCCINT pins. The 1.8-V V_{CCINT} external supply powers the device core directly. MAX V devices operate internally at 1.8 V. The supported MultiVolt I/O interface voltage levels (V_{CCIO}) are 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V.

MAX V devices are available in two speed grades: –4 and –5, with –4 being the fastest. For commercial applications, speed grades –C4 and –C5 are available. For industrial and automotive applications, speed grade –I5 and –A5 are available, respectively. These speed grades represent the overall relative performance, not any specific timing parameter.

For propagation delay timing numbers within each speed grade and density, refer to the *DC and Switching Characteristics for MAX V Devices* chapter.

MAX V devices are available in space-saving FineLine BGA (FBGA), Micro FineLine BGA (MBGA), plastic enhanced quad flat pack (EQFP), and thin quad flat pack (TQFP) packages (refer to Table 1–2 and Table 1–3). MAX V devices support vertical migration within the same package (for example, you can migrate between the 5M570Z, 5M1270Z, and 5M2210Z devices in the 256-pin FineLine BGA package). Vertical migration means that you can migrate to devices whose dedicated pins and JTAG pins are the same and power pins are subsets or supersets for a given package across device densities. The largest density in any package has the highest number of power pins; you must lay out for the largest planned density in a package to provide

the necessary power pins for migration. For I/O pin migration across densities, cross reference the available I/O pins using the device pin-outs for all planned densities of a given package type to identify which I/O pins can be migrated. The Quartus® II software can automatically cross-reference and place all pins for you when given a device migration list.

Table 1–2. MAX V Packages and User I/O Pins ***(Note 1)***

Device	64-Pin MBGA	64-Pin EQFP	68-Pin MBGA	100-Pin TQFP	100-Pin MBGA	144-Pin TQFP	256-Pin FBGA	324-Pin FBGA
5M40Z	30	54	—	—	—	—	—	—
5M80Z	30	54	52	79	—	—	—	—
5M160Z	—	54	52	79	79	—	—	—
5M240Z	—	—	52	79	79	114	—	—
5M570Z	—	—	—	74	74	114	159	—
5M1270Z	—	—	—	—	—	114	211	271
5M2210Z	—	—	—	—	—	—	203	271

Note to Table 1–2:

(1) Device packages under the same arrow sign have vertical migration capability.

Table 1–3. MAX V Package Sizes

Package	64-Pin MBGA	64-Pin EQFP	68-Pin MBGA	100-Pin TQFP	100-Pin MBGA	144-Pin TQFP	256-Pin FBGA	324-Pin FBGA
Pitch (mm)	0.5	0.4	0.5	0.5	0.5	0.5	1	1
Area (mm^2)	20.25	81	25	256	36	484	289	361
Length × width (mm × mm)	4.5 × 4.5	9 × 9	5 × 5	16 × 16	6 × 6	22 × 22	17 × 17	19 × 19

Integrated Software Platform

The Quartus II software provides an integrated environment for HDL and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, and programming of MAX V devices.

For more information about the Quartus II software features, refer to the *Quartus II Handbook*.

You can debug your MAX V designs using In-System Sources and Probes Editor in the Quartus II software. This feature allows you to easily control any internal signal and provides you with a completely dynamic debugging environment.

For more information about the In-System Sources and Probes Editor, refer to the *Design Debugging Using In-System Sources and Probes* chapter of the *Quartus II Handbook*.

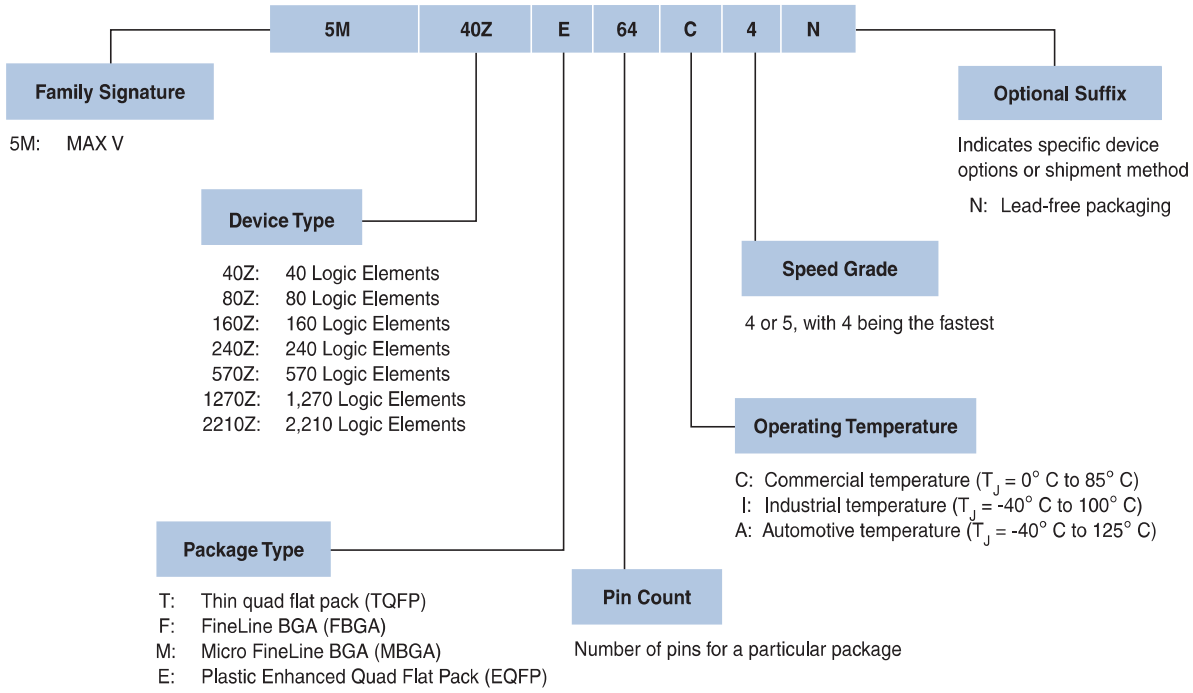
Device Pin-Outs

For more information, refer to the MAX V Device Pin-Out Files page.

Ordering Information

Figure 1–1 shows the ordering codes for MAX V devices.

Figure 1–1. MAX V Device Packaging Ordering Information



Document Revision History

Table 1–4 lists the revision history for this chapter.

Table 1–4. Document Revision History

Date	Version	Changes
May 2011	1.2	■ Updated Figure 1–1. ■ Updated Table 1–3.
January 2011	1.1	Updated "Feature Summary" section.
December 2010	1.0	Initial release.

2. MAX V Architecture

MV51002-1.0

This chapter describes the architecture of the MAX® V device and contains the following sections:

Functional Description

MAX V devices contain a two-dimensional row- and column-based architecture to implement custom logic. Row and column interconnects provide signal interconnects between the logic array blocks (LABs).

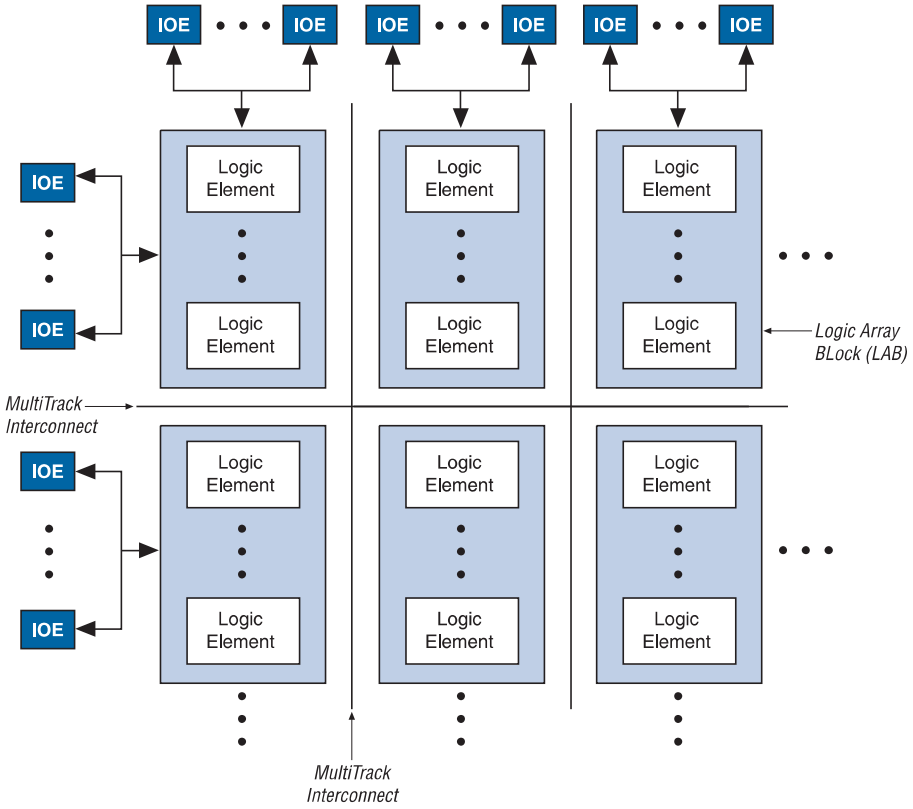
Each LAB in the logic array contains 10 logic elements (LEs). An LE is a small unit of logic that provides efficient implementation of user logic functions. LABs are grouped into rows and columns across the device. The MultiTrack interconnect provides fast granular timing delays between LABs. The fast routing between LEs provides minimum timing delay for added levels of logic versus globally routed interconnect structures.

The I/O elements (IOEs) located after the LAB rows and columns around the periphery of the MAX V device feeds the I/O pins. Each IOE contains a bidirectional I/O buffer with several advanced features. I/O pins support Schmitt trigger inputs and various single-ended standards, such as 33-MHz, 32-bit PCI™, and LVTTL.

MAX V devices provide a global clock network. The global clock network consists of four global clock lines that drive throughout the entire device, providing clocks for all resources within the device. You can also use the global clock lines for control signals such as clear, preset, or output enable.

Figure 2–1 shows a functional block diagram of the MAX V device.

Figure 2–1. Device Block Diagram



Each MAX V device contains a flash memory block within its floorplan. This block is located on the left side of the 5M40Z, 5M80Z, 5M160Z, and 5M240Z devices. On the 5M240Z (T144 package), 5M570Z, 5M1270Z, and 5M2210Z devices, the flash memory block is located on the bottom-left area of the device. The majority of this flash memory storage is partitioned as the dedicated configuration flash memory (CFM) block. The CFM block provides the non-volatile storage for all of the SRAM configuration information. The CFM automatically downloads and configures the logic and I/O at power-up, providing instant-on operation.

For more information about configuration upon power-up, refer to the *Hot Socketing and Power-On Reset for MAX V Devices* chapter.

A portion of the flash memory within the MAX V device is partitioned into a small block for user data. This user flash memory (UFM) block provides 8,192 bits of general-purpose user storage. The UFM provides programmable port connections to the logic array for reading and writing. There are three LAB rows adjacent to this block, with column numbers varying by device.

Table 2–1 lists the number of LAB rows and columns in each device, as well as the number of LAB rows and columns adjacent to the flash memory area. The long LAB rows are full LAB rows that extend from one side of row I/O blocks to the other. The short LAB rows are adjacent to the UFM block; their length is shown as width in LAB columns.

Table 2–1. Device Resources for MAX V Devices

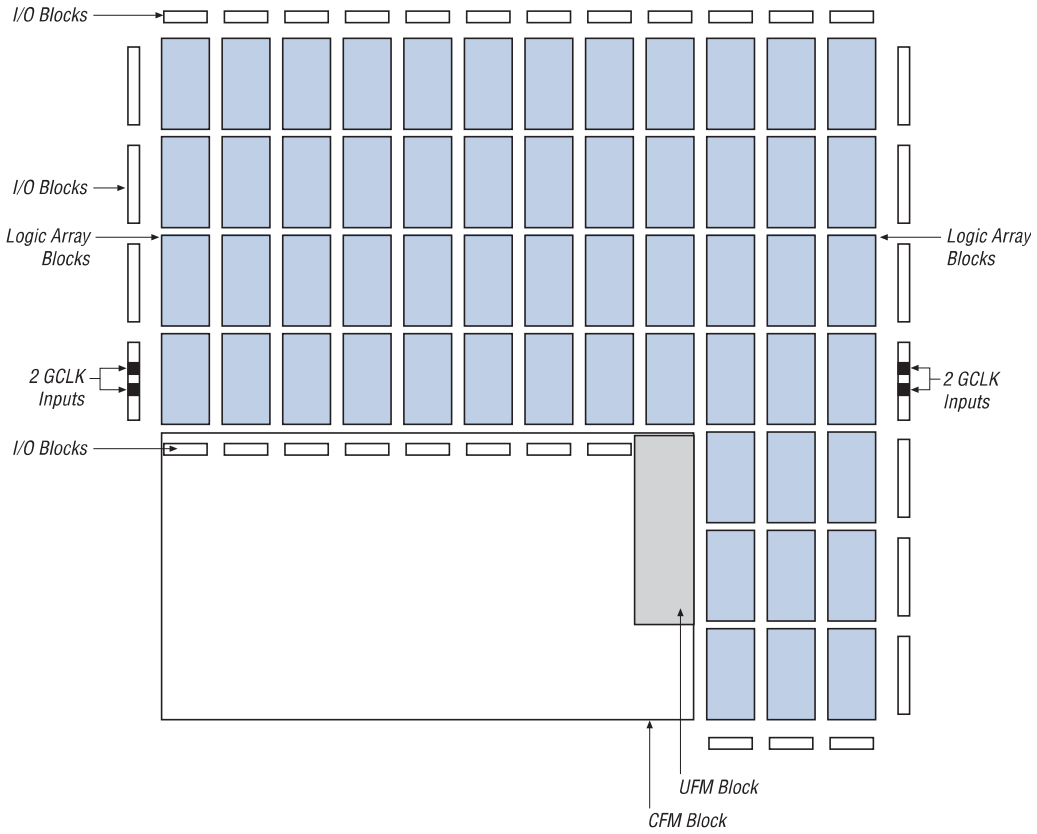
Device	UFM Blocks	LAB Columns	LAB Rows		Total LABs
			Long LAB Rows	Short LAB Rows (Width) *(1)*	
5M40Z	1	6	4	—	24
5M80Z	1	6	4	—	24
5M160Z	1	6	4	—	24
5M240Z *(2)*	1	6	4	—	24
5M240Z *(3)*	1	12	4	3 (3)	57
5M570Z	1	12	4	3 (3)	57
5M1270Z *(4)*	1	16	7	3 (5)	127
5M1270Z *(5)*	1	20	10	3 (7)	221
5M2210Z	1	20	10	3 (7)	221

Notes to Table 2–1:

(1) The width is the number of LAB columns in length.
(2) Not applicable to T144 package of the 5M240Z device.
(3) Only applicable to T144 package of the 5M240Z device.
(4) Not applicable to F324 package of the 5M1270Z device.
(5) Only applicable to F324 package of the 5M1270Z device.

Figure 2–2 shows a floorplan of a MAX V device.

Figure 2–2. Device Floorplan for MAX V Devices ***(Note 1)***



Note to Figure 2–2:

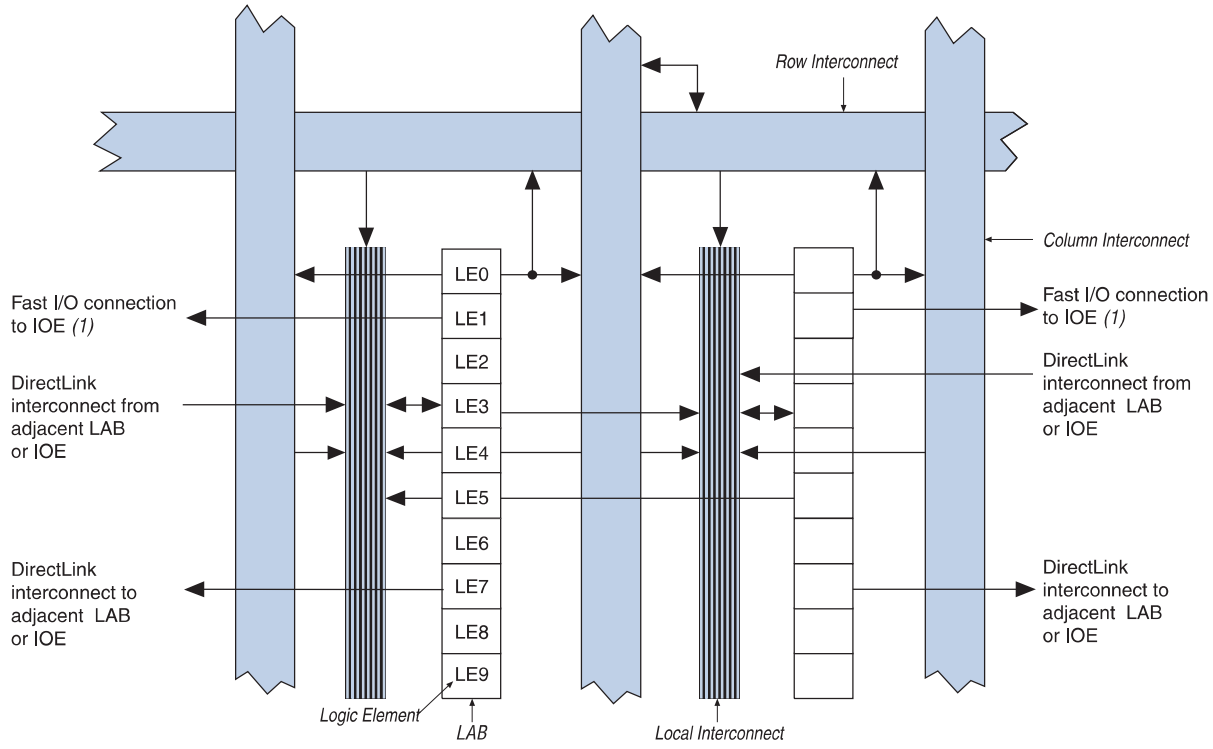
(1) The device shown is a 5M570Z device. 5M1270Z and 5M2210Z devices have a similar floorplan with more LABs. For 5M40Z, 5M80Z, 5M160Z, and 5M240Z devices, the CFM and UFM blocks are located on the left side of the device.

Logic Array Blocks

Each LAB consists of 10 LEs, LE carry chains, LAB control signals, a local interconnect, a look-up table (LUT) chain, and register chain connection lines. There are 26 possible unique inputs into an LAB, with an additional 10 local feedback input lines fed by LE outputs in the same LAB. The local interconnect transfers signals between LEs in the same LAB. LUT chain connections transfer the LUT output from one LE to the

adjacent LE for fast sequential LUT connections within the same LAB. Register chain connections transfer the output of one LE's register to the adjacent LE's register within an LAB. The Quartus® II software places associated logic within an LAB or adjacent LABs, allowing the use of local, LUT chain, and register chain connections for performance and area efficiency. Figure 2–3 shows the MAX V LAB.

Figure 2–3. LAB Structure for MAX V Devices



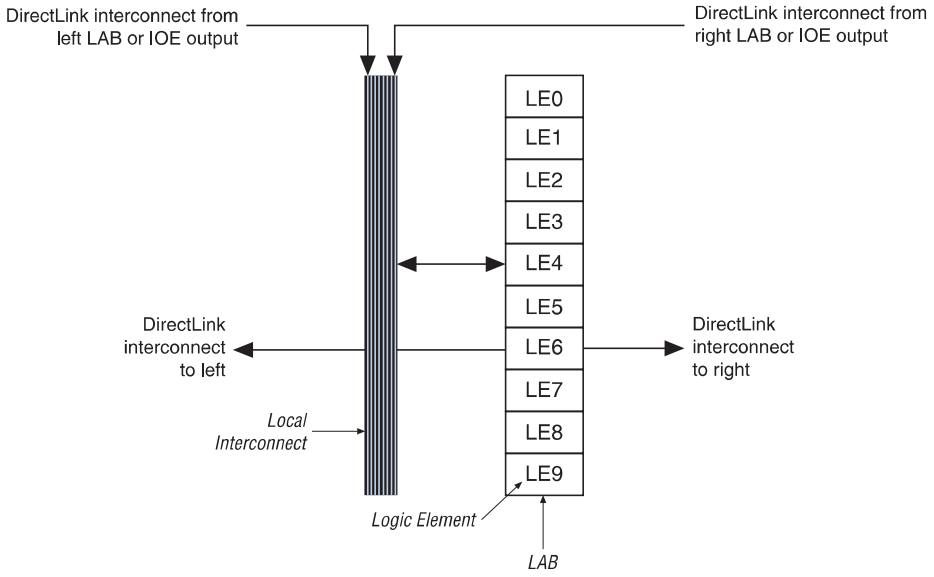
Note to Figure 2–3:

(1) Only from LABs adjacent to IOEs.

LAB Interconnects

Column and row interconnects and LE outputs within the same LAB drive the LAB local interconnect. Adjacent LABs, from the left and right, can also drive an LAB's local interconnect through the DirectLink connection. The DirectLink connection feature minimizes the use of row and column interconnects, providing higher performance and flexibility. Each LE can drive 30 other LEs through fast local and DirectLink interconnects. Figure 2–4 shows the DirectLink connection.

Figure 2–4. DirectLink Connection



LAB Control Signals

Each LAB contains dedicated logic for driving control signals to its LEs. The control signals include two clocks, two clock enables, two asynchronous clears, a synchronous clear, an asynchronous preset/load, a synchronous load, and add/subtract control signals, providing a maximum of 10 control signals at a time. Synchronous load and clear signals are generally used when implementing counters but they can also be used with other functions.

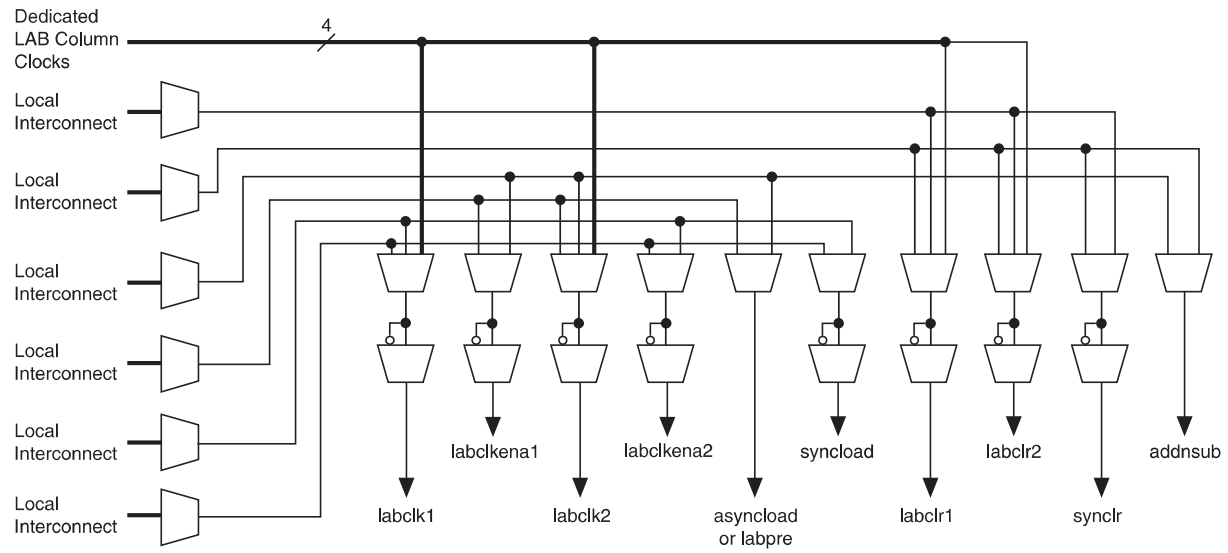
Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked. For example, any LE in a particular LAB using the `labclk1` signal also uses `labclkena1`. If the LAB uses both the rising and falling edges of a clock, it also uses both LAB-wide clock signals. Deasserting the clock enable signal turns off the LAB-wide clock.

Each LAB can use two asynchronous clear signals and an asynchronous load/preset signal. By default, the Quartus II software uses a `NOT` gate push-back technique to achieve preset. If you disable the `NOT` gate push-back option or assign a given register to power-up high using the Quartus II software, the preset is then achieved using the asynchronous load signal with asynchronous load data input tied high.

With the LAB-wide `addnsub` control signal, a single LE can implement a one-bit adder and subtractor. This signal saves LE resources and improves performance for logic functions such as correlators and signed multipliers that alternate between addition and subtraction depending on data.

The LAB column clocks `[3..0]`, driven by the global clock network, and LAB local interconnect generate the LAB-wide control signals. The MultiTrack interconnect structure drives the LAB local interconnect for non-global control signal generation. The MultiTrack interconnect's inherent low skew allows clock and control signal distribution in addition to data signals. Figure 2–5 shows the LAB control signal generation circuit.

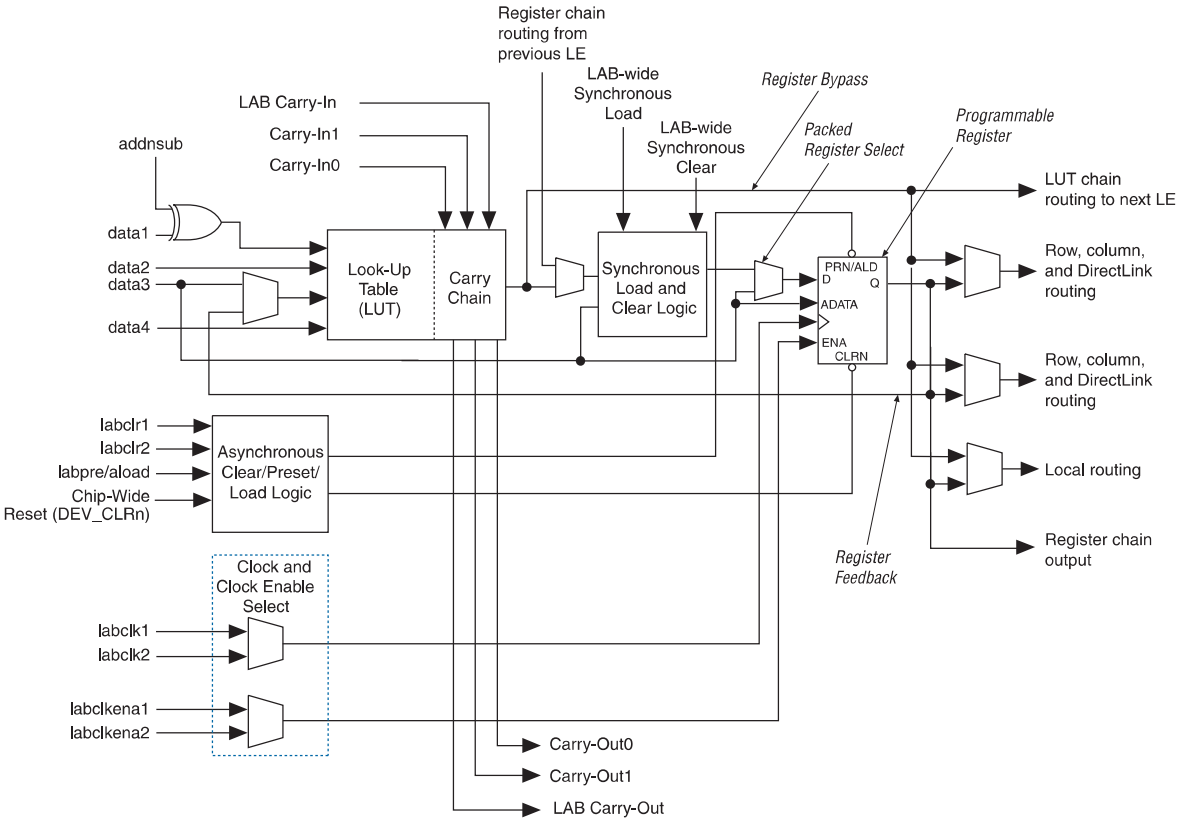
Figure 2–5. LAB-Wide Control Signals



Logic Elements

The smallest unit of logic in the MAX V architecture, the LE, is compact and provides advanced features with efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can implement any function of four variables. In addition, each LE contains a programmable register and carry chain with carry-select capability. A single LE also supports dynamic single-bit addition or subtraction mode that is selected by an LAB-wide control signal. Each LE drives all types of interconnects: local, row, column, LUT chain, register chain, and DirectLink interconnects as shown in Figure 2–6.

Figure 2–6. LE for MAX V Devices



You can configure each LE's programmable register for D, T, JK, or SR operation. Each register has data, true asynchronous load data, clock, clock enable, clear, and asynchronous load/preset inputs. Global signals, general purpose I/O (GPIO) pins, or any LE can drive the register's clock and clear control signals. Either GPIO pins or LEs can drive the clock enable, preset, asynchronous load, and asynchronous data. The asynchronous load data input comes from the `data3` input of the LE. For combinational functions, the LUT output bypasses the register and drives directly to the LE outputs.

Each LE has three outputs that drive the local, row, and column routing resources. The LUT or register output can drive these three outputs independently. Two LE outputs drive either a column or row and DirectLink routing connections while one output drives the local interconnect resources. This configuration allows the LUT to drive one output while the register drives another output. This register packing feature

improves device utilization because the device can use the register and the LUT for unrelated functions. Another special packing mode allows the register output to feed back into the LUT of the same LE so that the register is packed with its own fan-out LUT. This mode provides another mechanism for improved fitting. The LE can also drive out registered and unregistered versions of the LUT output.

LUT Chain and Register Chain

In addition to the three general routing outputs, the LEs within a LAB have LUT chain and register chain outputs. LUT chain connections allow LUTs within the same LAB to cascade together for wide input functions. Register chain outputs allow registers within the same LAB to cascade together. The register chain output allows a LAB to use LUTs for a single combinational function and the registers for an unrelated shift register implementation. These resources speed up connections between LABs while saving local interconnect resources. For more information about LUT chain and register chain connections, refer to "MultiTrack Interconnect" on page 2–14.

addnsub Signal

The LE's dynamic adder/subtractor feature saves logic resources by using one set of LEs to implement both an adder and a subtractor. This feature is controlled by the LAB-wide control signal `addnsub`. The `addnsub` signal sets the LAB to perform either A + B or A – B. The LUT computes addition; subtraction is computed by adding the two's complement of the intended subtractor. The LAB-wide signal converts to two's complement by inverting the B bits within the LAB and setting carry-in to 1, which adds one to the LSB. The LSB of an adder/subtractor must be placed in the first LE of the LAB, where the LAB-wide `addnsub` signal automatically sets the carry-in to 1. The Quartus II Compiler automatically places and uses the adder/subtractor feature when using adder/subtractor parameterized functions.

LE Operating Modes

The MAX V LE can operate in one of the following modes:

- "Normal Mode"
- "Dynamic Arithmetic Mode"

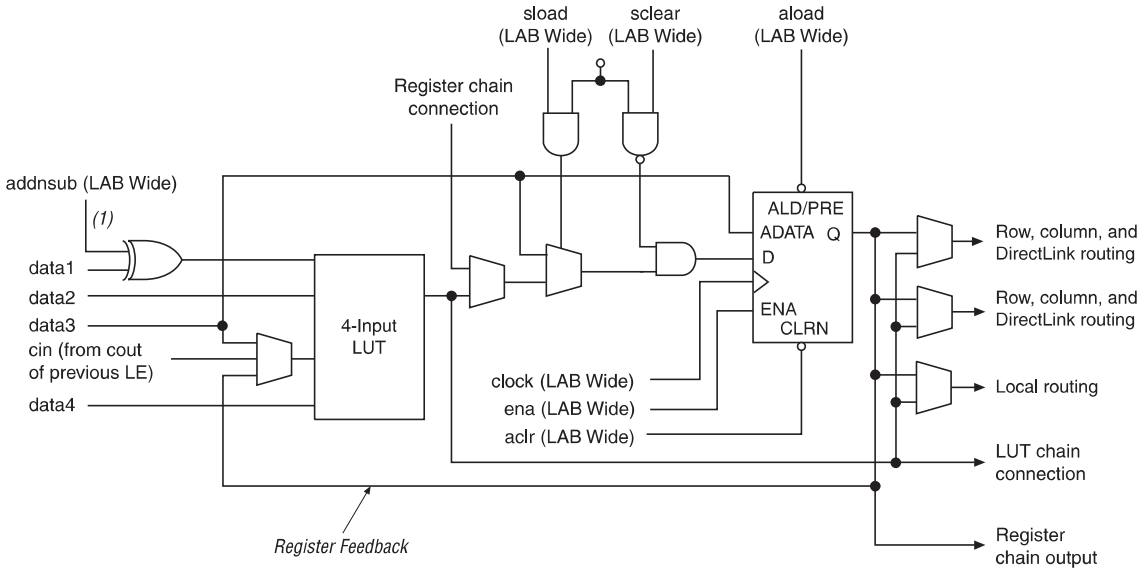
Each mode uses LE resources differently. In each mode, eight available inputs to the LE, the four data inputs from the LAB local interconnect, `carry-in0` and `carry-in1` from the previous LE, the LAB carry-in from the previous carry-chain LAB, and the register chain connection are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset/load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes. The `addnsub` control signal is allowed in arithmetic mode.

The Quartus II software, along with parameterized functions such as the library of parameterized modules (LPM) functions, automatically chooses the appropriate mode for common functions such as counters, adders, subtractors, and arithmetic functions.

Normal Mode

The normal mode is suitable for general logic applications and combinational functions. In normal mode, four data inputs from the LAB local interconnect are inputs to a four-input LUT as shown in Figure 2–7. The Quartus II Compiler automatically selects the carry-in or the `data3` signal as one of the inputs to the LUT. Each LE can use LUT chain connections to drive its combinational output directly to the next LE in the LAB. Asynchronous load data for the register comes from the `data3` input of the LE. LEs in normal mode support packed registers.

Figure 2–7. LE in Normal Mode



Note to Figure 2–7:

(1) This signal is only allowed in normal mode if the LE is after an adder/subtractor chain.

Dynamic Arithmetic Mode

The dynamic arithmetic mode is ideal for implementing adders, counters, accumulators, wide parity functions, and comparators. A LE in dynamic arithmetic mode uses four 2-input LUTs configurable as a dynamic adder/subtractor. The first two 2-input LUTs compute two summations based on a possible carry-in of 1 or 0; the other two LUTs generate carry outputs for the two chains of the carry-select circuitry. As shown in Figure 2–8, the LAB carry-in signal selects either the `carry-in0` or `carry-in1` chain. The selected chain's logic level in turn determines which parallel sum is generated as a combinational or registered output. For example, when implementing an adder, the sum output is the selection of two possible calculated sums:

```
data1 + data2 + carry-in0
```

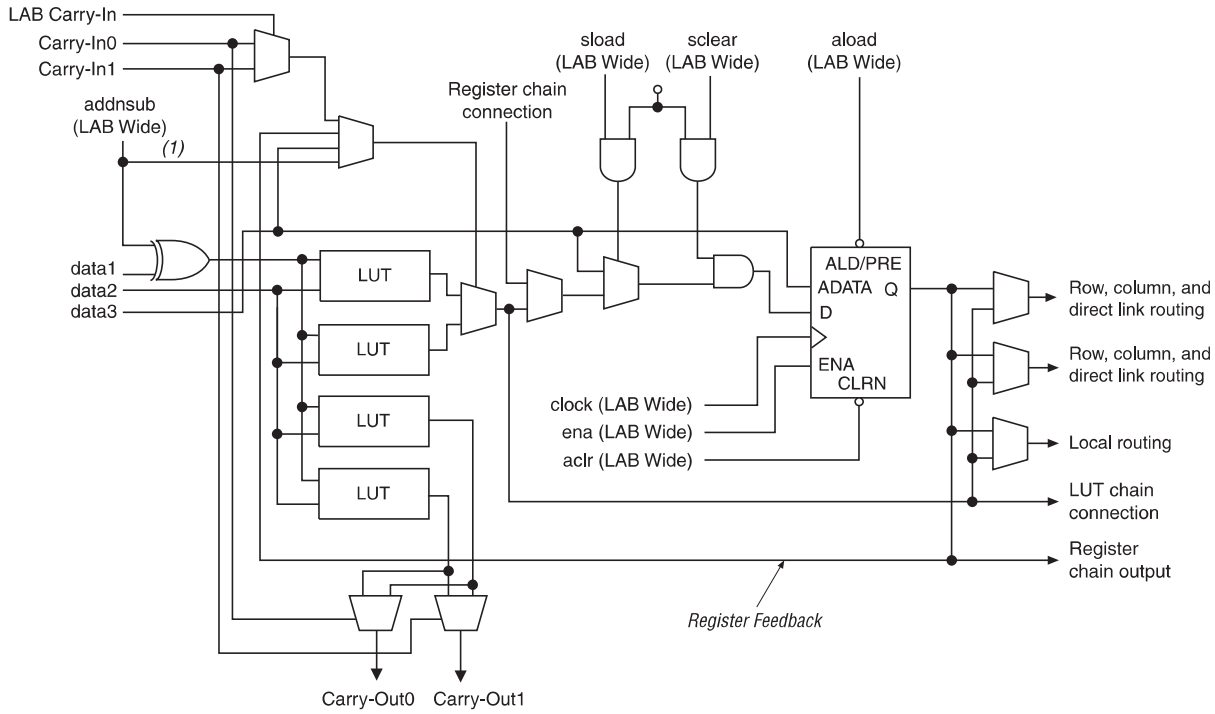
or

```
data1 + data2 + carry-in1
```

The other two LUTs use the `data1` and `data2` signals to generate two possible carry-out signals: one for a carry of 1 and the other for a carry of 0. The `carry-in0` signal acts as the carry-select for the `carry-out0` output and `carry-in1` acts as the carry-select for the `carry-out1` output. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The dynamic arithmetic mode also offers clock enable, counter enable, synchronous up/down control, synchronous clear, synchronous load, and dynamic adder/subtractor options. The LAB local interconnect data inputs generate the counter enable and synchronous up/down control signals. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. The Quartus II software automatically places any registers that are not used by the counter into other LABs. The `addnsub` LAB-wide signal controls whether the LE acts as an adder or subtractor.

Figure 2–8. LE in Dynamic Arithmetic Mode



Note to Figure 2–8:

(1) The `addnsub` signal is tied to the carry input for the first LE of a carry chain only.

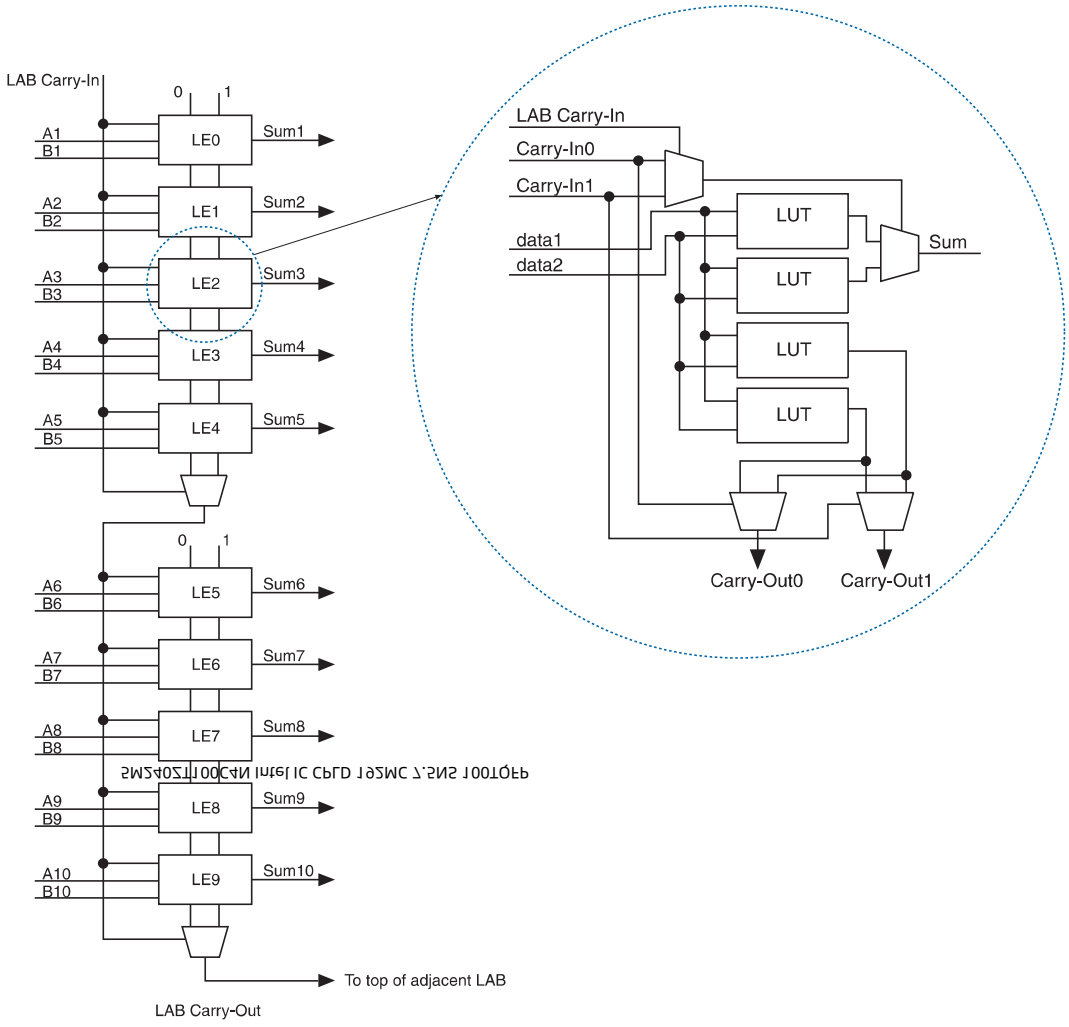
Carry-Select Chain

The carry-select chain provides a very fast carry-select function between LEs in dynamic arithmetic mode. The carry-select chain uses the redundant carry calculation to increase the speed of carry functions. The LE is configured to calculate outputs for a possible carry-in of 0 and carry-in of 1 in parallel. The `carry-in0` and `carry-in1` signals from a lower-order bit feed forward into the higher-order bit via the parallel carry chain and feed into both the LUT and the next portion of the carry chain. Carry-select chains can begin in any LE within an LAB.

The speed advantage of the carry-select chain is in the parallel pre-computation of carry chains. Because the LAB carry-in selects the precomputed carry chain, not every LE is in the critical path. Only the propagation delays between LAB carry-in generation (LE5 and LE10) are now part of the critical path. This feature allows the MAX V architecture to implement high-speed counters, adders, multipliers, parity functions, and comparators of arbitrary width.

Figure 2–9 shows the carry-select circuitry in an LAB for a 10-bit full adder. One portion of the LUT generates the sum of two bits using the input signals and the appropriate carry-in bit; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT generates carry-out bits. An LAB-wide carry-in bit selects which chain is used for the addition of given inputs. The carry-in signal for each chain, carry-in0 or carry-in1, selects the carry-out to carry forward to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is fed to local, row, or column interconnects.

Figure 2–9. Carry-Select Chain



The Quartus II software automatically creates carry chain logic during design processing, or you can create it manually during design entry. Parameterized functions such as LPM functions automatically take advantage of carry chains for the appropriate functions. The Quartus II software creates carry chains longer than 10 LEs by linking adjacent LABs within the same row together automatically. A carry chain can extend horizontally up to one full LAB row, but does not extend between LAB rows.

Clear and Preset Logic Control

LAB-wide signals control the logic for the register's clear and preset signals. The LE directly supports an asynchronous clear and preset function. The register preset is achieved through the asynchronous load of a logic high. MAX V devices support simultaneous preset/asynchronous load and clear signals. An asynchronous clear signal takes precedence if both signals are asserted simultaneously. Each LAB supports up to two clears and one preset signal.

In addition to the clear and preset ports, MAX V devices provide a chip-wide reset pin (DEV_CLRn) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This chip-wide reset overrides all other control signals and uses its own dedicated routing resources without using any of the four global resources. Driving this signal low before or during power-up prevents user mode from releasing clears within the design. This allows you to control when clear is released on a device that has just been powered-up. If not set for its chip-wide reset function, the DEV_CLRn pin is a regular I/O pin.

By default, all registers in MAX V devices are set to power-up low. However, this power-up state can be set to high on individual registers during design entry using the Quartus II software.

LE RAM

The Quartus II memory compiler can configure the unused LEs as LE RAM.

MAX V devices support the following memory types:

- FIFO synchronous R/W
- FIFO asynchronous R/W
- 1 port SRAM
- 2 port SRAM
- 3 port SRAM
- shift registers

For more information about memory, refer to the *Internal Memory (RAM and ROM) User Guide*.

MultiTrack Interconnect

In the MAX V architecture, connections between LEs, the UFM, and device I/O pins are provided by the MultiTrack interconnect structure. The MultiTrack interconnect consists of continuous, performance-optimized routing lines used for inter- and intra-design block connectivity. The Quartus II Compiler automatically places critical design paths on faster interconnects to improve design performance.

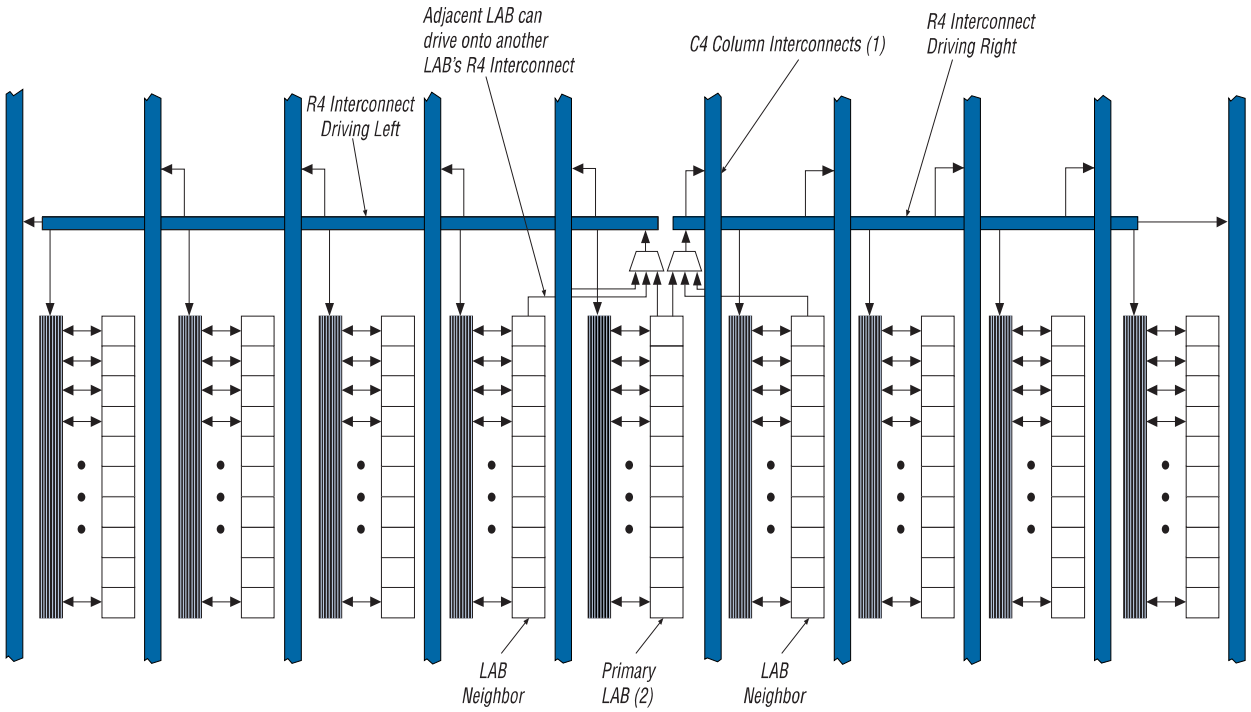
The MultiTrack interconnect consists of row and column interconnects that span fixed distances. A routing structure with fixed length resources for all devices allows predictable and short delays between logic levels instead of large delays associated with global or long routing lines. Dedicated row interconnects route signals to and from LABs within the same row. These row resources include:

- DirectLink interconnects between LABs
- R4 interconnects traversing four LABs to the right or left

The DirectLink interconnect allows an LAB to drive into the local interconnect of its left and right neighbors. The DirectLink interconnect provides fast communication between adjacent LABs and blocks without using row interconnect resources.

The R4 interconnects span four LABs and are used for fast row connections in a four-LAB region. Every LAB has its own set of R4 interconnects to drive either left or right. Figure 2–10 shows R4 interconnect connections from an LAB. R4 interconnects can drive and be driven by row IOEs. For LAB interfacing, a primary LAB or horizontal LAB neighbor can drive a given R4 interconnect. For R4 interconnects that drive to the right, the primary LAB and right neighbor can drive on to the interconnect. For R4 interconnects that drive to the left, the primary LAB and its left neighbor can drive on to the interconnect. R4 interconnects can drive other R4 interconnects to extend the range of LABs they can drive. R4 interconnects can also drive C4 interconnects for connections from one row to another.

Figure 2–10. R4 Interconnect Connections



Notes to Figure 2–10:

(1) C4 interconnects can drive R4 interconnects.

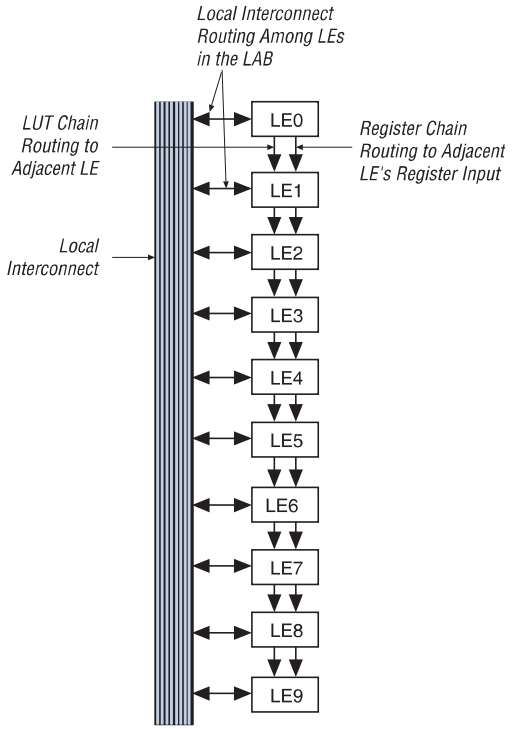
(2) This pattern is repeated for every LAB in the LAB row.

The column interconnect operates similarly to the row interconnect. Each column of LABs is served by a dedicated column interconnect, which vertically routes signals to and from LABs and row and column IOEs. These column resources include:

- LUT chain interconnects within an LAB
- Register chain interconnects within an LAB
- C4 interconnects traversing a distance of four LABs in an up and down direction

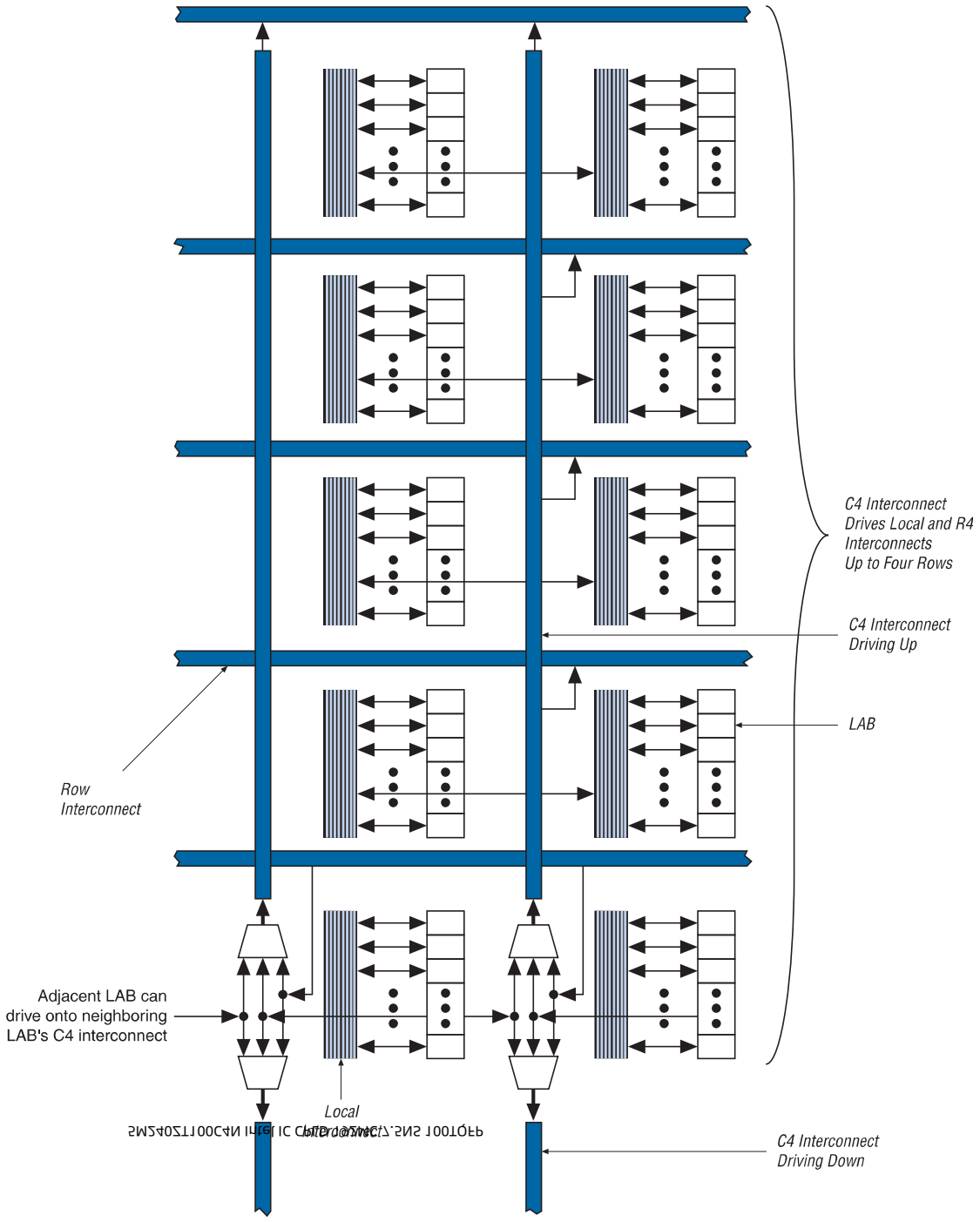
MAX V devices include an enhanced interconnect structure within LABs for routing LE output to LE input connections faster using LUT chain connections and register chain connections. The LUT chain connection allows the combinational output of an LE to directly drive the fast input of the LE right below it, bypassing the local interconnect. These resources can be used as a high-speed connection for wide fan-in functions from `LE 1` to `LE 10` in the same LAB. The register chain connection allows the register output of one LE to connect directly to the register input of the next LE in the LAB for fast shift registers. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. Figure 2–11 shows the LUT chain and register chain interconnects.

Figure 2–11. LUT Chain and Register Chain Interconnects



The C4 interconnects span four LABs up or down from a source LAB. Every LAB has its own set of C4 interconnects to drive either up or down. Figure 2–12 shows the C4 interconnect connections from an LAB in a column. The C4 interconnects can drive and be driven by column and row IOEs. For LAB interconnection, a primary LAB or its vertical LAB neighbor can drive a given C4 interconnect. C4 interconnects can drive each other to extend their range as well as drive row interconnects for column-to-column connections.

Figure 2–12. C4 Interconnect Connections ***(Note 1)***



Note to Figure 2–12:

(1) Each C4 interconnect can drive either up or down four rows.

The UFM block communicates with the logic array similar to LAB-to-LAB interfaces. The UFM block connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. This block also has DirectLink interconnects for fast connections to and from a neighboring LAB. For more information about the UFM interface to the logic array, refer too "User Flash Memory Block" on page 2–21.

Table 2–2 lists the MAX V device routing scheme.

Table 2–2. Routing Scheme for MAX V Devices

Source	Destination										
	LUT Chain	Register Chain	Local (1)	DirectLink (1)	R4 (1)	C4 (1)	LE	UFM Block	Column IOE	Row IOE	Fast I/O (1)
LUT Chain	—	—	—	—	—	—	✓	—	—	—	—
Register Chain	—	—	—	—	—	—	✓	—	—	—	—
Local Interconnect	—	—	—	—	—	—	✓	✓	✓	✓	—
DirectLink Interconnect	—	—	✓	—	—	—	—	—	—	—	—
R4 Interconnect	—	—	✓	—	✓	✓	—	—	—	—	—
C4 Interconnect	—	—	✓	—	✓	✓	—	—	—	—	—
LE	✓	✓	✓	✓	✓	✓	—	—	✓	✓	✓
UFM Block	—	—	✓	✓	✓	✓	—	—	—	—	—
Column IOE	—	—	—	—	—	✓	—	—	—	—	—
Row IOE	—	—	—	✓	✓	✓	—	—	—	—	—

Note to Table 2–2:

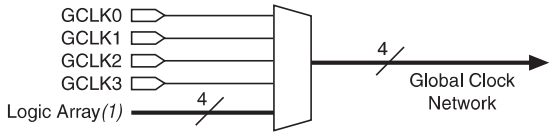
(1) These categories are interconnects.

Global Signals

Each MAX V device has four dual-purpose dedicated clock pins (GCLK[3..0], two pins on the left side and two pins on the right side) that drive the global clock network for clocking, as shown in Figure 2–13. These four pins can also be used as GPIOs if they are not used to drive the global clock network.

The four global clock lines in the global clock network drive throughout the entire device. The global clock network can provide clocks for all resources within the device including LEs, LAB local interconnect, IOEs, and the UFM block. The global clock lines can also be used for global control signals, such as clock enables, synchronous or asynchronous clears, presets, output enables, or protocol control signals such as TRDY and IRDY for the PCI I/O standard. Internal logic can drive the global clock network for internally-generated global clocks and control signals. Figure 2–13 shows the various sources that drive the global clock network.

Figure 2–13. Global Clock Generation

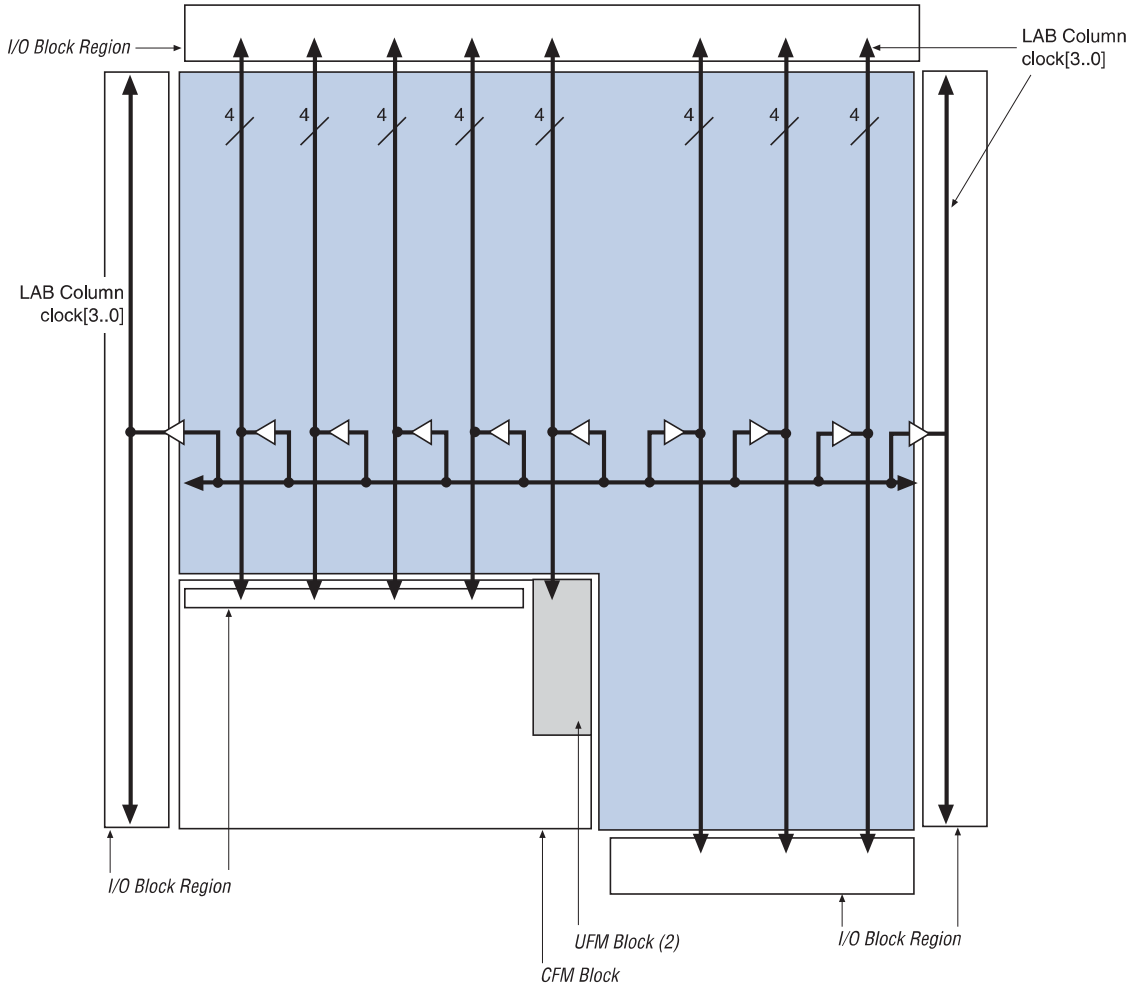


Note to Figure 2–13:

(1) Any I/O pin can use a MultiTrack interconnect to route as a logic array-generated global clock signal.

The global clock network drives to individual LAB column signals, LAB column clocks [3..0], that span an entire LAB column from the top to the bottom of the device. Unused global clocks or control signals in an LAB column are turned off at the LAB column clock buffers shown in Figure 2–14. The LAB column clocks [3..0] are multiplexed down to two LAB clock signals and one LAB clear signal. Other control signal types route from the global clock network into the LAB local interconnect. For more information, refer to "LAB Control Signals" on page 2–6.

Figure 2–14. Global Clock Network ***(Note 1)***



Notes to Figure 2–14:

(1) LAB column clocks in I/O block regions provide high fan-out output enable signals.

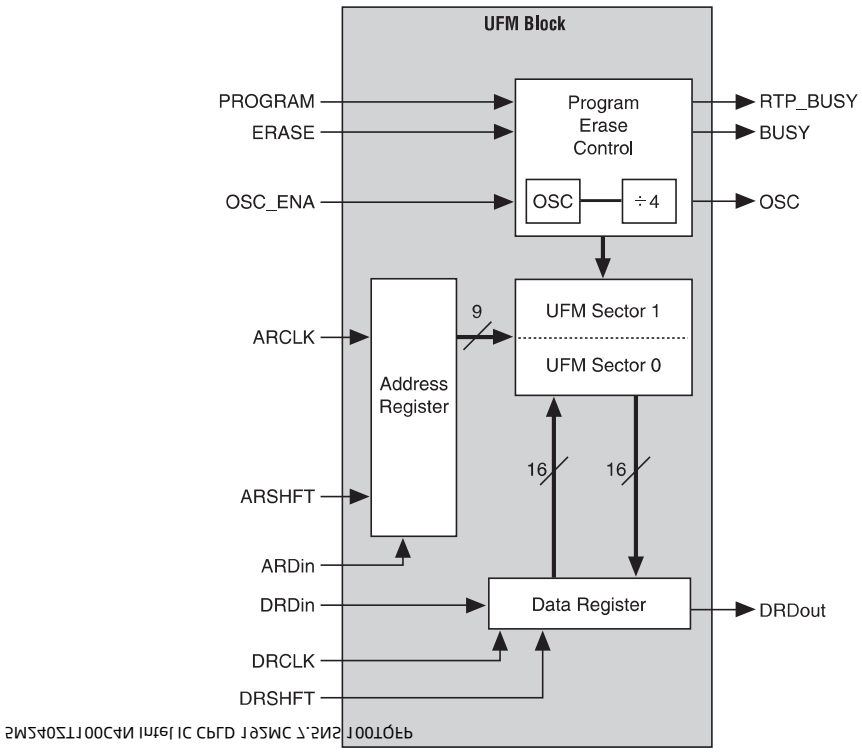
(2) LAB column clocks drive to the UFM block.

User Flash Memory Block

MAX V devices feature a single UFM block, which can be used like a serial EEPROM for storing non-volatile information up to 8,192 bits. The UFM block connects to the logic array through the MultiTrack interconnect, allowing any LE to interface to the UFM block. Figure 2–15 shows the UFM block and interface signals. The logic array is used to create customer interface or protocol logic to interface the UFM block data outside of the device. The UFM block offers the following features:

- Non-volatile storage up to 16-bit wide and 8,192 total bits
- Two sectors for partitioned sector erase
- Built-in internal oscillator that optionally drives logic array
- Program, erase, and busy signals
- Auto-increment addressing
- Serial interface to logic array with programmable interface

Figure 2–15. UFM Block and Interface Signals



UFM Storage

Each device stores up to 8,192 bits of data in the UFM block. Table 2–3 lists the data size, sector, and address sizes for the UFM block.

Table 2–3. UFM Array Size

Device	Total Bits	Sectors	Address Bits	Data Width
5M40Z	8,192	2 (4,096 bits per sector)	9	16
5M80Z	8,192	2 (4,096 bits per sector)	9	16
5M160Z	8,192	2 (4,096 bits per sector)	9	16
5M240Z	8,192	2 (4,096 bits per sector)	9	16
5M570Z	8,192	2 (4,096 bits per sector)	9	16
5M1270Z	8,192	2 (4,096 bits per sector)	9	16
5M2210Z	8,192	2 (4,096 bits per sector)	9	16

There are 512 locations with 9-bit addressing ranging from 000h to 1FFh. The sector 0 address space is 000h to 0FFh and the sector 1 address space is from 100h to 1FFh. The data width is up to 16 bits of data. The Quartus II software automatically creates logic to accommodate smaller read or program data widths. Erasure of the UFM involves individual sector erasing (that is, one erase of sector 0 and one erase of sector 1 is required to erase the entire UFM block). Because sector erase is required before a program or write operation, having two sectors enables a sector size of data to be left untouched while the other sector is erased and programmed with new data.

Internal Oscillator

As shown in Figure 2–15, the dedicated circuitry within the UFM block contains an oscillator. The dedicated circuitry uses this oscillator internally for its read and program operations. This oscillator's divide by 4 output can drive out of the UFM block as a logic interface clock source or for general-purpose logic clocking. The typical OSC output signal frequency ranges from 3.9 to 5.3 MHz, and its exact frequency of operation is not programmable.

The UFM internal oscillator can be instantiated using the MegaWizard™ Plug-In Manager. You can also use the MAX II/MAX V Oscillator megafunction to instantiate the UFM oscillator without using the UFM memory block.

Program, Erase, and Busy Signals

The UFM block's dedicated circuitry automatically generates the necessary internal program and erase algorithm after the PROGRAM or ERASE input signals have been asserted. The PROGRAM or ERASE signal must be asserted until the busy signal deasserts, indicating the UFM internal program or erase operation has completed. The UFM block also supports JTAG as the interface for programming and reading.

For more information about programming and erasing the UFM block, refer to the *User Flash Memory in MAX V Devices* chapter.

Auto-Increment Addressing

The UFM block supports standard read or stream read operations. The stream read is supported with an auto-increment address feature. Deasserting the ARSHIFT signal while clocking the ARCLK signal increments the address register value to read consecutive locations from the UFM array.

Serial Interface

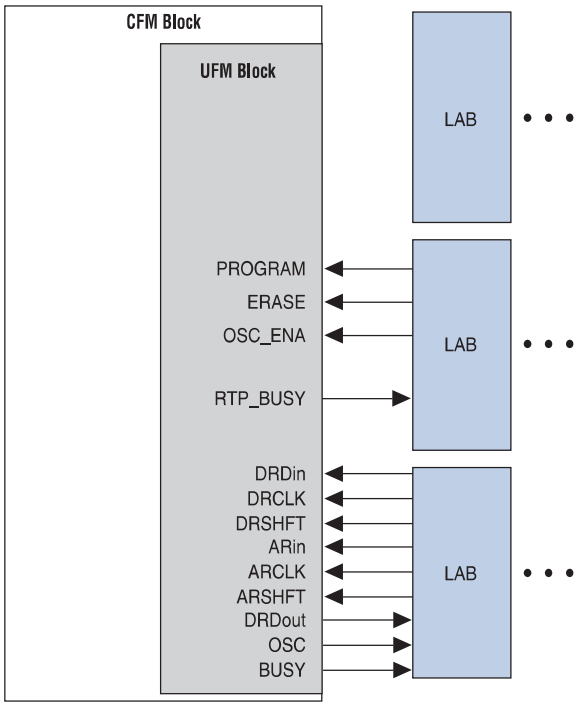
The UFM block supports a serial interface with serial address and data signals. The internal shift registers within the UFM block for address and data are 9 bits and 16 bits wide, respectively. The Quartus II software automatically generates interface logic in LEs for a parallel address and data interface to the UFM block. Other standard protocol interfaces such as SPI are also automatically generated in LE logic by the Quartus II software.

For more information about the UFM interface signals and the Quartus II LE-based alternate interfaces, refer to the *User Flash Memory in MAX V Devices* chapter.

UFM Block to Logic Array Interface

The UFM block is a small partition of the flash memory that contains the CFM block, as shown in Figure 2–1 and Figure 2–2. The UFM block for the 5M40Z, 5M80Z, 5M160Z, and 5M240Z devices is located on the left side of the device adjacent to the left most LAB column. The UFM blocks for the 5M570Z, 5M1270Z, and 5M2210Z devices are located at the bottom left of the device. The UFM input and output signals interface to all types of interconnects (R4 interconnect, C4 interconnect, and DirectLink interconnect to/from adjacent LAB rows). The UFM signals can also be driven from global clocks, `GCLK[3..0]`. The interface regions for the 5M40Z, 5M80Z, 5M160Z, and 5M240Z devices are shown in Figure 2–16. The interface regions for 5M570Z, 5M1270Z, and 5M2210Z devices are shown in Figure 2–17.

Figure 2–16. 5M40Z, 5M80Z, 5M160Z, and 5M240Z UFM Block LAB Row Interface *(Note 1)*, *(2)*

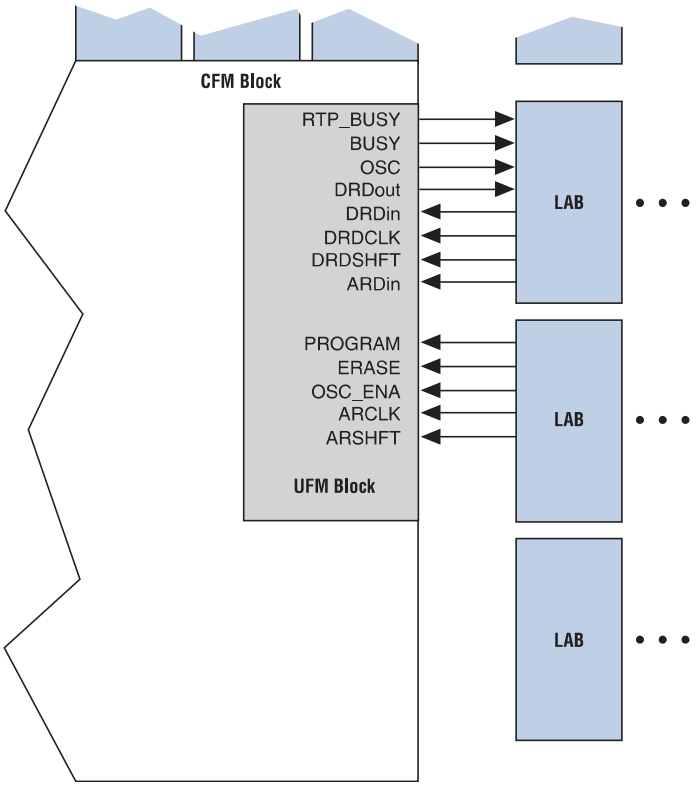


Notes to Figure 2–16:

(1) The UFM block inputs and outputs can drive to and from all types of interconnects, not only DirectLink interconnects from adjacent row LABs.

(2) Not applicable to the T144 package of the 5M240Z device.

Figure 2–17. 5M240Z, 5M570Z, 5M1270Z, and 5M2210Z UFM Block LAB Row Interface ***(Note 1)***



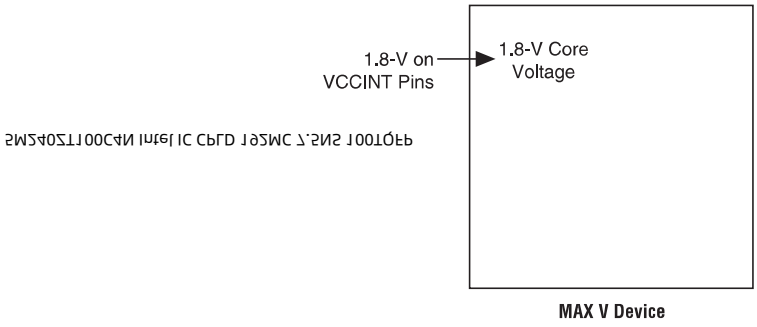
Note to Figure 2–17:

(1) Only applicable to the T144 package of the 5M240Z device.

Core Voltage

The MAX V architecture supports a 1.8-V core voltage on the V_{CCINT} supply. You must use a 1.8-V V_{CC} external supply to power the VCCINT pins.

Figure 2–18. Core Voltage Feature in MAX V Devices



I/O Structure

IOEs support many features, including:

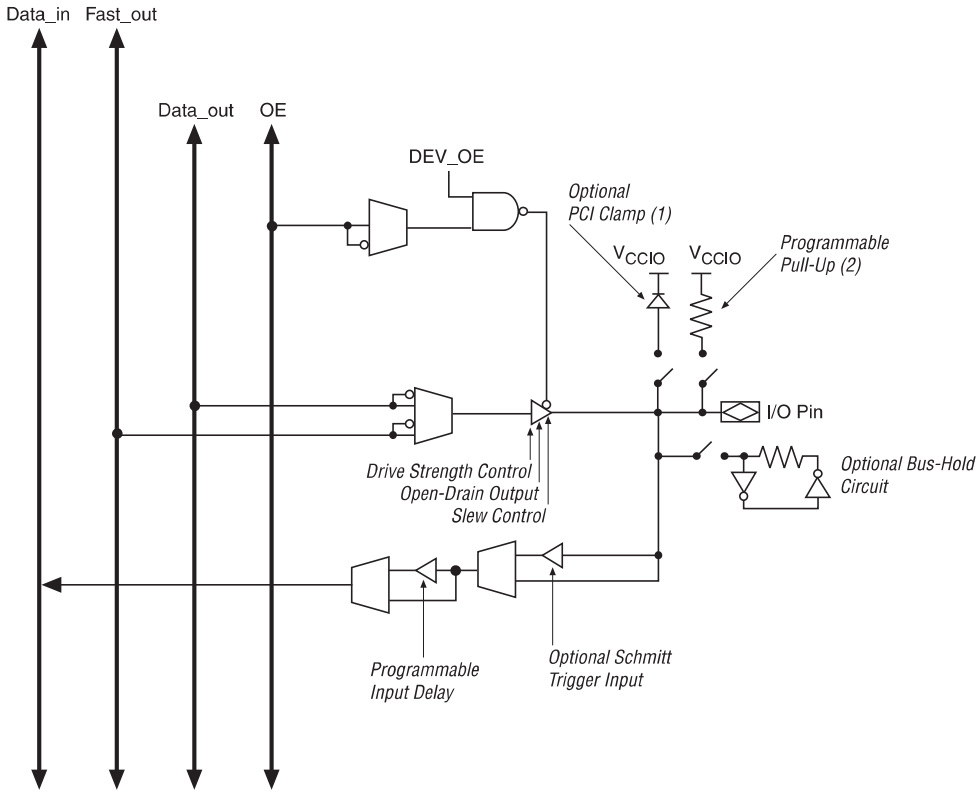
- LVTTL, LVCMOS, LVDS, and RSDS I/O standards
- 3.3-V, 32-bit, 33-MHz PCI compliance
- JTAG boundary-scan test (BST) support
- Programmable drive strength control
- Weak pull-up resistors during power-up and in system programming
- Slew-rate control
- Tri-state buffers with individual output enable control
- Bus-hold circuitry
- Programmable pull-up resistors in user mode
- Unique output enable per pin
- Open-drain outputs
- Schmitt trigger inputs
- Fast I/O connection
- Programmable input delay

MAX V device IOEs contain a bidirectional I/O buffer. Figure 2–19 shows the MAX V IOE structure. Registers from adjacent LABs can drive to or be driven from the IOE's bidirectional I/O buffers. The Quartus II software automatically attempts to place registers in the adjacent LAB with fast I/O connection to achieve the fastest possible clock-to-output and registered output enable timing. When the fast input registers option is enabled, the Quartus II software automatically routes the register to guarantee zero hold time. You can set timing assignments in the Quartus II software to achieve desired I/O timing.

Fast I/O Connection

A dedicated fast I/O connection from the adjacent LAB to the IOEs within an I/O block provides faster output delays for clock-to-output and t_{PD} propagation delays. This connection exists for data output signals, not output enable signals or input signals. Figure 2–20, Figure 2–21, and Figure 2–22 illustrate the fast I/O connection.

Figure 2–19. IOE Structure for MAX V Devices



Notes to Figure 2–19:

(1) Available only in I/O bank 3 of 5M1270Z and 5M2210Z devices.

(2) The programmable pull-up resistor is active during power-up, in-system programming (ISP), and if the device is unprogrammed.

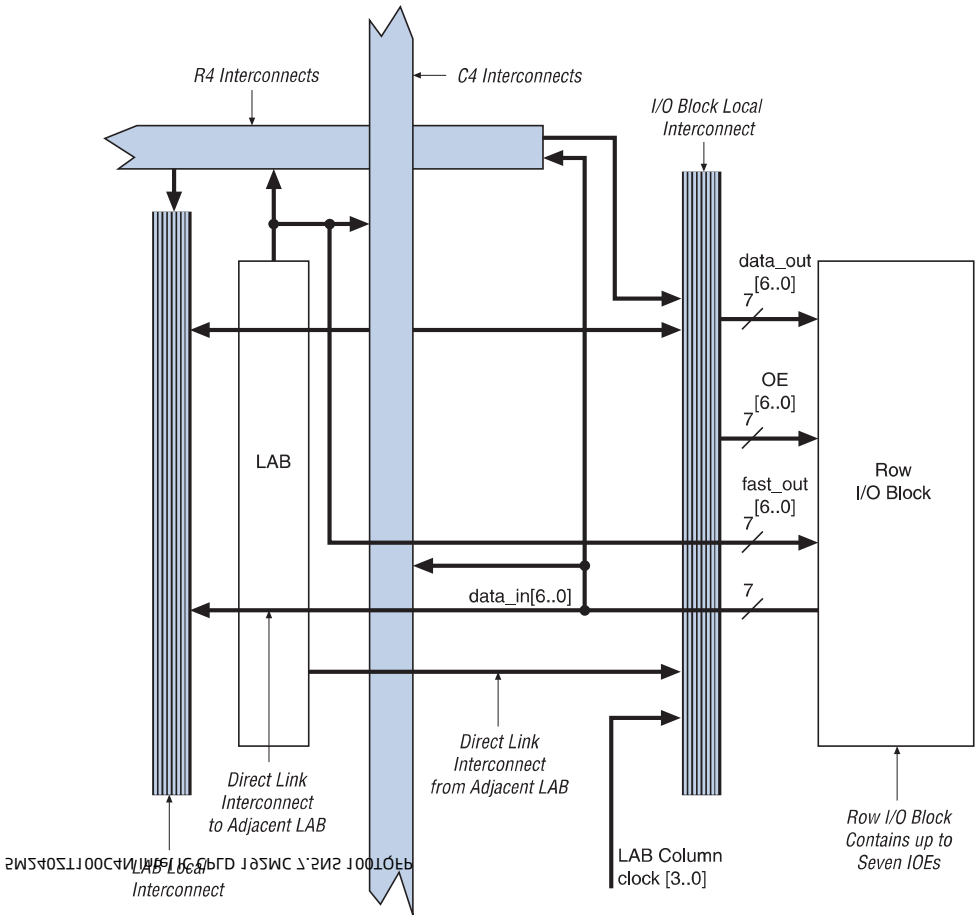
I/O Blocks

The IOEs are located in I/O blocks around the periphery of the MAX V device. There are up to seven IOEs per row I/O block and up to four IOEs per column I/O block. Each column or row I/O block interfaces with its adjacent LAB and MultiTrack interconnect to distribute signals throughout the device. The row I/O blocks drive row, column, or DirectLink interconnects. The column I/O blocks drive column interconnects.

☞ 5M40Z, 5M80Z, 5M160Z, and 5M240Z devices have a maximum of five IOEs per row I/O block.

Figure 2–20 shows how a row I/O block connects to the logic array.

Figure 2–20. Row I/O Block Connection to the Interconnect ***(Note 1)***

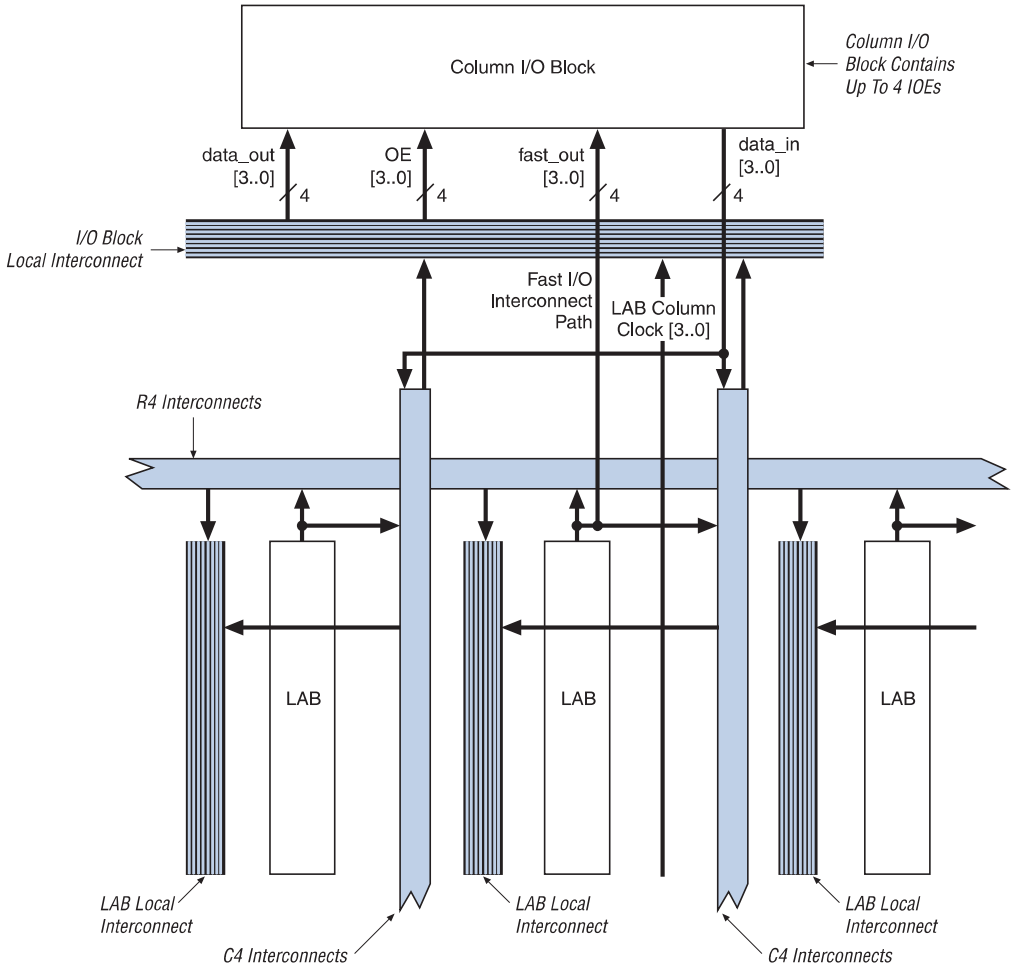


Note to Figure 2–20:

(1) Each of the seven IOEs in the row I/O block can have one `data_out` or `fast_out` output, one `OE` output, and one `data_in` input.

Figure 2–21 shows how a column I/O block connects to the logic array.

Figure 2–21. Column I/O Block Connection to the Interconnect ***(Note 1)***



Note to Figure 2–21:

(1) Each of the four IOEs in the column I/O block can have one `data_out` or `fast_out` output, one `OE` output, and one `data_in` input.

I/O Standards and Banks

Table 2–4 lists the I/O standards supported by MAX V devices.

Table 2–4. MAX V I/O Standards (Part 1 of 2)

I/O Standard	Type	Output Supply Voltage (V_{CCIO}) (V)
3.3-V LVTTL/LVCMOS	Single-ended	3.3
2.5-V LVTTL/LVCMOS	Single-ended	2.5
1.8-V LVTTL/LVCMOS	Single-ended	1.8
1.5-V LVCMOS	Single-ended	1.5
1.2-V LVCMOS	Single-ended	1.2

Table 2–4. MAX V I/O Standards (Part 2 of 2)

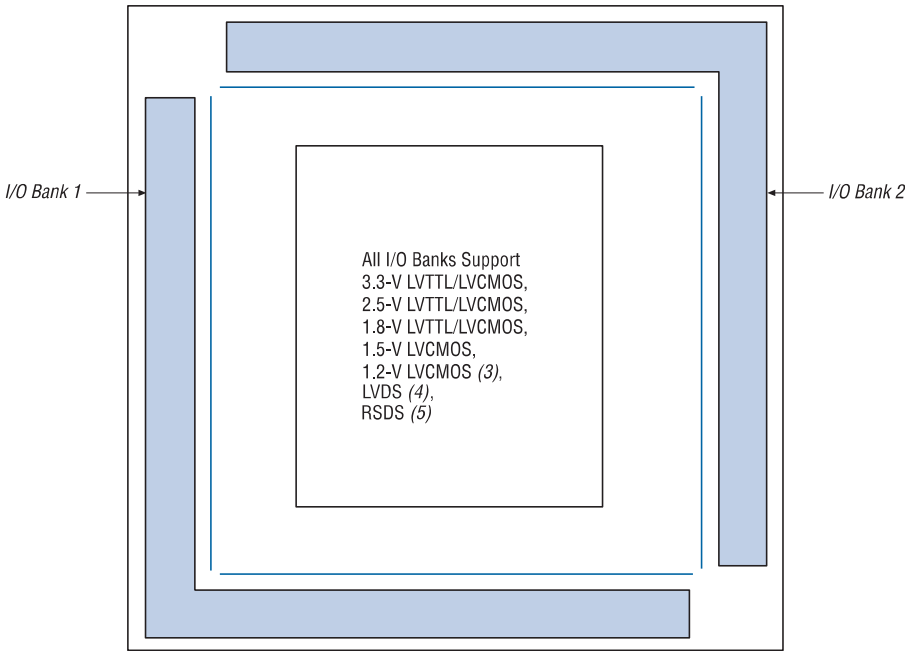
I/O Standard	Type	Output Supply Voltage (V_{CCIO}) (V)
3.3-V PCI *(1)*	Single-ended	3.3
LVDS *(2)*	Differential	2.5
RSDS *(3)*	Differential	2.5

Notes to Table 2–4:

(1) The 3.3-V PCI compliant I/O is supported in Bank 3 of the 5M1270Z and 5M2210Z devices.
(2) MAX V devices only support emulated LVDS output using a three resistor network (LVDS_E_3R).
(3) MAX V devices only support emulated RSDS output using a three resistor network (RSDS_E_3R).

The 5M40Z, 5M80Z, 5M160Z, 5M240Z, and 5M570Z devices support two I/O banks, as shown in Figure 2–22. Each of these banks support all the LVTTL, LVCMOS, LVDS, and RSDS standards shown in Table 2–4. PCI compliant I/O is not supported in these devices and banks.

Figure 2–22. I/O Banks for 5M40Z, 5M80Z, 5M160Z, 5M240Z, and 5M570Z Devices *(Note 1)*, *(2)*

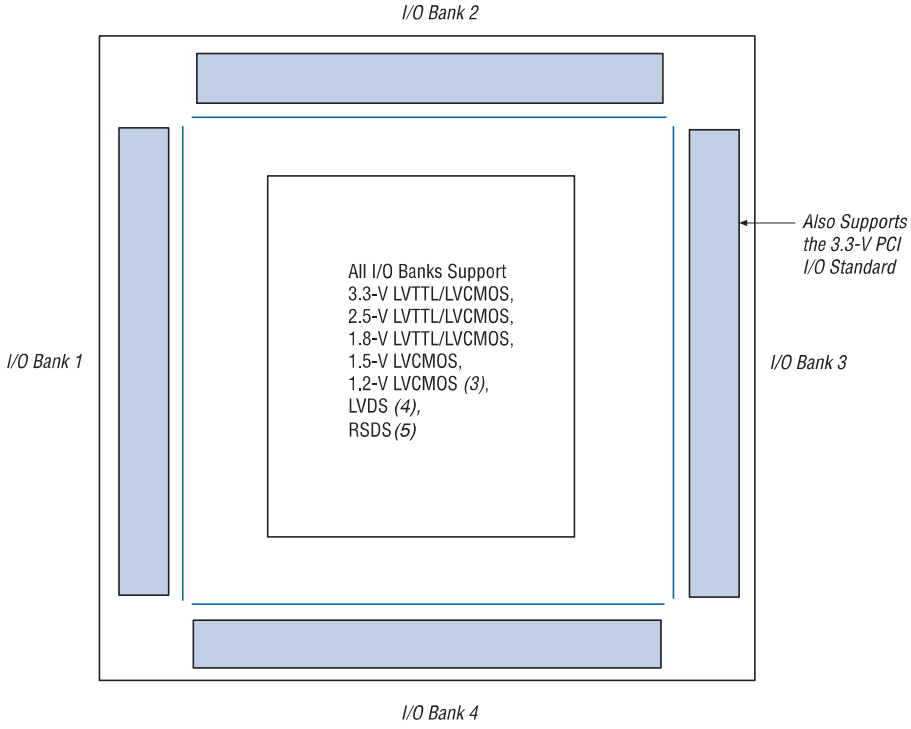


Notes to Figure 2–22:

(1) Figure 2–22 is a top view of the silicon die.
(2) Figure 2–22 is a graphical representation only. Refer to the pin list and the Quartus II software for exact pin locations.
(3) This I/O standard is not supported in Bank 1.
(4) Emulated LVDS output using a three resistor network (LVDS_E_3R).
(5) Emulated RSDS output using a three resistor network (RSDS_E_3R).

The 5M1270Z and 5M2210Z devices support four I/O banks, as shown in Figure 2–23. Each of these banks support all of the LVTTL, LVCMOS, LVDS, and RSDS standards shown in Table 2–4. PCI compliant I/O is supported in Bank 3. Bank 3 supports the PCI clamping diode on inputs and PCI drive compliance on outputs. You must use Bank 3 for designs requiring PCI compliant I/O pins. The Quartus II software automatically places I/O pins in this bank if assigned with the PCI I/O standard.

Figure 2–23. I/O Banks for 5M1270Z and 5M2210Z Devices *(Note 1), (2)*



Notes to Figure 2–23:

(1) Figure 2–23 is a top view of the silicon die.
(2) Figure 2–23 is a graphical representation only. Refer to the pin list and the Quartus II software for exact pin locations.
(3) This I/O standard is not supported in Bank 1.
(4) Emulated LVDS output using a three resistor network (LVDS_E_3R).
(5) Emulated RSDS output using a three resistor network (RSDS_E_3R).

Each I/O bank has dedicated V_{CCIO} pins that determine the voltage standard support in that bank. A single device can support 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V interfaces; each individual bank can support a different standard. Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. For example, when V_{CCIO} is 3.3 V, Bank 3 can support LVTTL, LVCMOS, and 3.3-V PCI. V_{CCIO} powers both the input and output buffers in MAX V devices.

The JTAG pins for MAX V devices are dedicated pins that cannot be used as regular I/O pins. The pins TMS, TDI, TDO, and TCK support all the I/O standards shown in Table 2–4 on page 2–29 except for PCI and 1.2-V LVCMOS. These pins reside in Bank 1 for all MAX V devices and their I/O standard support is controlled by the V_{CCIO} setting for Bank 1.

PCI Compliance

The MAX V 5M1270Z and 5M2210Z devices are compliant with PCI applications as well as all 3.3-V electrical specifications in the *PCI Local Bus Specification Revision 2.2*. These devices are also large enough to support PCI intellectual property (IP) cores. Table 2–5 shows the MAX V device speed grades that meet the PCI timing specifications.

Table 2–5. 3.3-V PCI Electrical Specifications and PCI Timing Support for MAX V Devices

Device	33-MHz PCI
5M1270Z	All Speed Grades
5M2210Z	All Speed Grades

LVDS and RSDS Channels

The MAX V device supports emulated LVDS and RSDS outputs on both row and column I/O banks. You can configure the rows and columns as emulated LVDS or RSDS output buffers that use two single-ended output buffers with three external resistor networks.

Table 2–6. LVDS and RSDS Channels supported in MAX V Devices *(Note 1)*

Device	64 MBGA	64 EQFP	68 MBGA	100 TQFP	100 MBGA	144 TQFP	256 FBGA	324 FBGA
5M40Z	10 eTx	20 eTx	—	—	—	—	—	—
5M80Z	10 eTx	20 eTx	20 eTx	33 eTx	—	—	—	—
5M160Z	—	20 eTx	20 eTx	33 eTx	33 eTx	—	—	—
5M240Z	—	—	20 eTx	33 eTx	33 eTx	49 eTx	—	—
5M570Z	—	—	—	28 eTx	28 eTx	49 eTx	75 eTx	—
5M1270Z	—	—	—	—	—	42 eTx	90 eTx	115 eTx
5M2210Z	—	—	—	—	—	—	83 eTx	115 eTx

Note to Table 2–6:

(1) eTx = emulated LVDS output buffers (LVDS_E_3R) or emulated RSDS output buffers (RSDS_E_3R).

Schmitt Trigger

The input buffer for each MAX V device I/O pin has an optional Schmitt trigger setting for the 3.3-V and 2.5-V standards. The Schmitt trigger allows input buffers to respond to slow input edge rates with a fast output edge rate. Most importantly, Schmitt triggers provide hysteresis on the input buffer, preventing slow-rising noisy input signals from ringing or oscillating on the input signal driven into the logic array. This provides system noise tolerance on MAX V inputs, but adds a small, nominal input delay.

The JTAG input pins (TMS, TCK, and TDI) have Schmitt trigger buffers that are always enabled.

The TCK input is susceptible to high pulse glitches when the input signal fall time is greater than 200 ns for all I/O standards.

Output Enable Signals

Each MAX V IOE output buffer supports output enable signals for tri-state control. The output enable signal can originate from the GCLK[3..0] global signals or from the MultiTrack interconnect. The MultiTrack interconnect routes output enable signals and allows for a unique output enable for each output or bidirectional pin.

MAX V devices also provide a chip-wide output enable pin (DEV_OE) to control the output enable for every output pin in the design. An option set before compilation in the Quartus II software controls this pin. This chip-wide output enable uses its own routing resources and does not use any of the four global resources. If this option is turned on, all outputs on the chip operate normally when DEV_OE is asserted. When the pin is deasserted, all outputs are tri-stated. If this option is turned off, the DEV_OE pin is disabled when the device operates in user mode and is available as a user I/O pin.

Programmable Drive Strength

The output buffer for each MAX V device I/O pin has two levels of programmable drive strength control for each of the LVTTL and LVCMOS I/O standards. Programmable drive strength provides system noise reduction control for high performance I/O designs. Although a separate slew-rate control feature exists, using the lower drive strength setting provides signal slew-rate control to reduce system noise and signal overshoot without the large delay adder associated with the slew-rate control feature. Table 2–7 lists the possible settings for the I/O standards with drive strength control. The Quartus II software uses the maximum current strength as the default setting. The PCI I/O standard is always set at 20 mA with no alternate setting.

Table 2–7. Programmable Drive Strength ***(Note 1)***

I/O Standard	IOH/IOL Current Strength Setting (mA)
3.3-V LVTTL	16
	8
3.3-V LVCMOS	8
	4
2.5-V LVTTL/LVCMOS	14
	7
1.8-V LVTTL/LVCMOS	6
	3
1.5-V LVCMOS	4
	2
1.2-V LVCMOS	3

Note to Table 2–7:

(1) The I_{OH} current strength numbers shown are for a condition of a $V_{OUT} = V_{OH}$ minimum, where the V_{OH} minimum is specified by the I/O standard. The I_{OL} current strength numbers shown are for a condition of a $V_{OUT} = V_{OL}$ maximum, where the V_{OL} maximum is specified by the I/O standard. For 2.5-V LVTTL/LVCMOS, the I_{OH} condition is V_{OUT} = 1.7 V and the I_{OL} condition is V_{OUT} = 0.7 V.

The programmable drive strength feature can be used simultaneously with the slew-rate control feature.

Slew-Rate Control

The output buffer for each MAX V device I/O pin has a programmable output slew-rate control that can be configured for low noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal output delay to rising and falling edges. The lower the voltage standard (for example, 1.8-V LVTTL) the larger the output delay when slow slew is enabled. Each I/O pin has an individual slew-rate control, allowing you to specify the slew rate on a pin-by-pin basis. The slew-rate control affects both the rising and falling edges. If no slew-rate control is specified, the Quartus II software defaults to a fast slew rate.

The slew-rate control feature can be used simultaneously with the programmable drive strength feature.

Open-Drain Output

MAX V devices provide an optional open-drain (equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (for example, interrupt and write enable signals) that can be asserted by any of several devices. This output can also provide an additional wired-OR plane.

Programmable Ground Pins

Each unused I/O pin on MAX V devices can be used as an additional ground pin. This programmable ground feature does not require the use of the associated LEs in the device. In the Quartus II software, unused pins can be set as programmable GND on a global default basis or they can be individually assigned. Unused pins also have the option of being set as tri-stated input pins.

Bus-Hold

Each MAX V device I/O pin provides an optional bus-hold feature. The bus-hold circuitry can hold the signal on an I/O pin at its last-driven state. Because the bus-hold feature holds the last-driven state of the pin until the next input signal is present, an external pull-up or pull-down resistor is not necessary to hold a signal level when the bus is tri-stated.

The bus-hold circuitry also pulls un-driven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. You can select this feature individually for each I/O pin. The bus-hold output will drive no higher than V_{CCIO} to prevent overdriving signals. If the bus-hold feature is enabled, the device cannot use the programmable pull-up option.

The bus-hold circuitry is only active after the device has fully initialized. The bus-hold circuit captures the value on the pin present at the moment user mode is entered.

Programmable Pull-Up Resistor

Each MAX V device I/O pin provides an optional programmable pull-up resistor during user mode. If you enable this feature for an I/O pin, the pull-up resistor holds the output to the V_{CCIO} level of the output pin's bank.

☞ The programmable pull-up resistor feature should not be used at the same time as the bus-hold feature on a given I/O pin.

☞ The programmable pull-up resistor is active during power-up, ISP, and if the device is unprogrammed.

Programmable Input Delay

The MAX V IOE includes a programmable input delay that is activated to ensure zero hold times. A path where a pin directly drives a register, with minimal routing between the two, may require the delay to ensure zero hold time. However, a path where a pin drives a register through long routing or through combinational logic may not require the delay to achieve a zero hold time. The Quartus II software uses this delay to ensure zero hold times when needed.

MultiVolt I/O Interface

The MAX V architecture supports the MultiVolt I/O interface feature, which allows MAX V devices in all packages to interface with systems of different supply voltages. The devices have one set of VCC pins for internal operation (V_{CCINT}), and up to four sets for input buffers and I/O output driver buffers (V_{CCIO}), depending on the number of I/O banks available in the devices where each set of VCCIO pins powers one I/O bank. The 5M40Z, 5M80Z, 5M160Z, 5M240Z, and 5M570Z devices each have two I/O banks while the 5M1270Z and 5M2210Z devices each have four I/O banks.

Connect VCCIO pins to either a 1.2-, 1.5-, 1.8-, 2.5-, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (that is, when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems. Table 2–8 summarizes MAX V MultiVolt I/O support.

Table 2–8. MultiVolt I/O Support in MAX V Devices (Part 1 of 2) ***(Note 1)***

VCCIO (V)	Input Signal						Output Signal					
	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
1.2	✓	—	—	—	—	—	✓	—	—	—	—	—
1.5	—	✓	✓	✓	✓	—	✓	✓	—	—	—	—
1.8	—	✓	✓	✓	✓	—	✓ (2)	✓ (2)	✓	—	—	—
2.5	—	—	—	✓	✓	—	✓ (3)	✓ (3)	✓ (3)	✓	—	—

Table 2–8. MultiVolt I/O Support in MAX V Devices (Part 2 of 2) *(Note 1)*

VCCIO (V)	Input Signal						Output Signal					
	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
3.3	—	—	—	✓ (4)	✓	✓ (5)	✓ (6)	✓ (6)	✓ (6)	✓ (6)	✓	✓ (7)

Notes to Table 2–8:

(1) To drive inputs higher than V_{CCIO} but less than 4.0 V including the overshoot, disable the I/O clamp diode. However, to drive 5.0-V signals to the device, enable the I/O clamp diode to prevent V_I from rising above 4.0 V. Use an external diode if the I/O pin does not support the clamp diode.

(2) When V_{CCIO} = 1.8 V, a MAX V device can drive a 1.2-V or 1.5-V device with 1.8-V tolerant inputs.

(3) When V_{CCIO} = 2.5 V, a MAX V device can drive a 1.2-V, 1.5-V, or 1.8-V device with 2.5-V tolerant inputs.

(4) When V_{CCIO} = 3.3 V and a 2.5-V input signal feeds an input pin, the VCCIO supply current will be slightly larger than expected.

(5) MAX V devices can be 5.0-V tolerant with the use of an external resistor and the internal I/O clamp diode on the 5M1270Z and 5M2210Z devices. Use an external clamp diode if the internal clamp diode is not available.

(6) When V_{CCIO} = 3.3 V, a MAX V device can drive a 1.2-V, 1.5-V, 1.8-V, or 2.5-V device with 3.3-V tolerant inputs.

(7) When V_{CCIO} = 3.3 V, a MAX V device can drive a device with 5.0-V TTL inputs but not 5.0-V CMOS inputs. For 5.0-V CMOS, open-drain setting with internal I/O clamp diode (available only on 5M1270Z and 5M2210Z devices) and external resistor is required. Use an external clamp diode if the internal clamp diode is not available.

Document Revision History

Table 2–9 lists the revision history for this chapter.

Table 2–9. Document Revision History

Date	Version	Changes
December 2010	1.0	Initial release.

3. DC and Switching Characteristics for MAX V Devices

MV51003-1.2

This chapter covers the electrical and switching characteristics for MAX® V devices. Electrical characteristics include operating conditions and power consumptions. This chapter also describes the timing model and specifications.

You must consider the recommended DC and switching conditions described in this chapter to maintain the highest possible performance and reliability of the MAX V devices.

This chapter contains the following sections:

Operating Conditions

Table 3–1 through Table 3–15 on page 3–9 list information about absolute maximum ratings, recommended operating conditions, DC electrical characteristics, and other specifications for MAX V devices.

Absolute Maximum Ratings

Table 3–1 lists the absolute maximum ratings for the MAX V device family.

Table 3–1. Absolute Maximum Ratings for MAX V Devices *(Note 1)*, *(2)*

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Internal supply voltage	With respect to ground	–0.5	2.4	V
V_{CCIO}	I/O supply voltage	—	–0.5	4.6	V
V_I	DC input voltage	—	–0.5	4.6	V
I_{OUT}	DC output current, per pin	—	–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	°C
T_{AMB}	Ambient temperature	Under bias *(3)*	–65	135	°C
T_J	Junction temperature	TQFP and BGA packages under bias	—	135	°C

Notes to Table 3–1:

(1) For more information, refer to the *Operating Requirements for Altera Devices Data Sheet*.

(2) Conditions beyond those listed in Table 3–1 may cause permanent damage to a device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse affects on the device.

(3) For more information about "under bias" conditions, refer to Table 3–2.

Recommended Operating Conditions

Table 3–2 lists recommended operating conditions for the MAX V device family.

Table 3–2. Recommended Operating Conditions for MAX V Devices

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT} *(1)*	1.8-V supply voltage for internal logic and in-system programming (ISP)	MAX V devices	1.71	1.89	V
V_{CCIO} *(1)*	Supply voltage for I/O buffers, 3.3-V operation	—	3.00	3.60	V
	Supply voltage for I/O buffers, 2.5-V operation	—	2.375	2.625	V
	Supply voltage for I/O buffers, 1.8-V operation	—	1.71	1.89	V
	Supply voltage for I/O buffers, 1.5-V operation	—	1.425	1.575	V
	Supply voltage for I/O buffers, 1.2-V operation	—	1.14	1.26	V
V_I	Input voltage	*(2)*, *(3)*, *(4)*	–0.5	4.0	V
V_O	Output voltage	—	0	V_{CCIO}	V
T_J	Operating junction temperature	Commercial range	0	85	°C
		Industrial range	–40	100	°C
		Extended range *(5)*	–40	125	°C

Notes to Table 3–2:

(1) MAX V device ISP and/or user flash memory (UFM) programming using JTAG or logic array is not guaranteed outside the recommended operating conditions (for example, if brown-out occurs in the system during a potential write/program sequence to the UFM, Altera recommends that you read back the UFM contents and verify it against the intended write data).

(2) The minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

(3) During transitions, the inputs may overshoot to the voltages shown below based on the input duty cycle. The DC case is equivalent to 100% duty cycle. For more information about 5.0-V tolerance, refer to the *Using MAX V Devices in Multi-Voltage Systems* chapter.

V_{IN}	Max. Duty Cycle
4.0 V	100% (DC)
4.1 V	90%
4.2 V	50%
4.3 V	30%
4.4 V	17%
4.5 V	10%

(4) All pins, including the clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.

(5) For the extended temperature range of 100 to 125°C, MAX V UFM programming (erase/write) is only supported using the JTAG interface. UFM programming using the logic array interface is not guaranteed in this range.

Programming/Erasure Specifications

Table 3–3 lists the programming/erasure specifications for the MAX V device family.

Table 3–3. Programming/Erasure Specifications for MAX V Devices

Parameter	Block	Minimum	Typical	Maximum	Unit
Erase and reprogram cycles	UFM	—	—	1000 *(1)*	Cycles
	Configuration flash memory (CFM)	—	—	100	Cycles

Note to Table 3–3:

(1) This value applies to the commercial grade devices. For the industrial grade devices, the value is 100 cycles.

DC Electrical Characteristics

Table 3–4 lists DC electrical characteristics for the MAX V device family.

Table 3–4. DC Electrical Characteristics for MAX V Devices *(Note 1)* (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_I	Input pin leakage current	$V_I = V_{CCIO}$ max to 0 V *(2)*	–10	—	10	µA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIO}$ max to 0 V *(2)*	–10	—	10	µA
$I_{CCSTANDBY}$	V_{CCINT} supply current (standby) *(3)*	5M40Z, 5M80Z, 5M160Z, and 5M240Z (Commercial grade) *(4)*, *(5)*	—	25	90	µA
		5M240Z (Commercial grade) *(6)*	—	27	96	µA
		5M40Z, 5M80Z, 5M160Z, and 5M240Z (Industrial grade) *(5)*, *(7)*	—	25	139	µA
		5M240Z (Industrial grade) *(6)*	—	27	152	µA
		5M570Z (Commercial grade) *(4)*	—	27	96	µA
		5M570Z (Industrial grade) *(7)*	—	27	152	µA
		5M1270Z and 5M2210Z	—	2	—	mA
$V_{SCHMITT}$ *(8)*	Hysteresis for Schmitt trigger input *(9)*	V_{CCIO} = 3.3 V	—	400	—	mV
		V_{CCIO} = 2.5 V	—	190	—	mV
$I_{CCPOWERUP}$	V_{CCINT} supply current during power-up *(10)*	MAX V devices	—	—	40	mA
R_{PULLUP}	Value of I/O pin pull-up resistor during user mode and ISP	V_{CCIO} = 3.3 V *(11)*	5	—	25	kΩ
		V_{CCIO} = 2.5 V *(11)*	10	—	40	kΩ
		V_{CCIO} = 1.8 V *(11)*	25	—	60	kΩ
		V_{CCIO} = 1.5 V *(11)*	45	—	95	kΩ
		V_{CCIO} = 1.2 V *(11)*	80	—	130	kΩ

Table 3–4. DC Electrical Characteristics for MAX V Devices *(Note 1)* (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_{PULLUP}	I/O pin pull-up resistor current when I/O is unprogrammed	—	—	—	300	µA
C_{IO}	Input capacitance for user I/O pin	—	—	—	8	pF
C_{GCLK}	Input capacitance for dual-purpose GCLK/user I/O pin	—	—	—	8	pF

Notes to Table 3–4:

(1) Typical values are for T_A = 25°C, V_{CCINT} = 1.8 V and V_{CCIO} = 1.2, 1.5, 1.8, 2.5, or 3.3 V.

(2) This value is specified for normal device operation. The value may vary during power-up. This applies to all V_{CCIO} settings (3.3, 2.5, 1.8, 1.5, and 1.2 V).

(3) V_I = ground, no load, and no toggling inputs.

(4) Commercial temperature ranges from 0°C to 85°C with the maximum current at 85°C.

(5) Not applicable to the T144 package of the 5M240Z device.

(6) Only applicable to the T144 package of the 5M240Z device.

(7) Industrial temperature ranges from –40°C to 100°C with the maximum current at 100°C.

(8) This value applies to commercial and industrial range devices. For extended temperature range devices, the $V_{SCHMITT}$ typical value is 300 mV for V_{CCIO} = 3.3 V and 120 mV for V_{CCIO} = 2.5 V.

(9) The TCK input is susceptible to high pulse glitches when the input signal fall time is greater than 200 ns for all I/O standards.

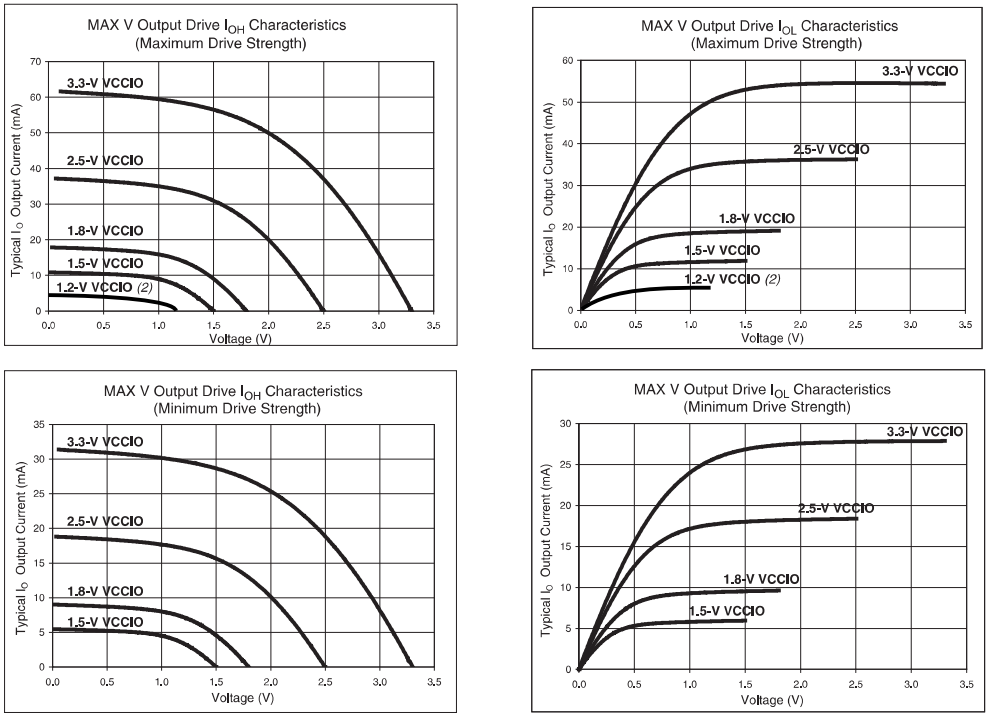
(10) This is a peak current value with a maximum duration of t_{CONFIG} time.

(11) Pin pull-up resistance values will lower if an external source drives the pin higher than V_{CCIO}.

Output Drive Characteristics

Figure 3–1 shows the typical drive strength characteristics of MAX V devices.

Figure 3–1. Output Drive Characteristics of MAX V Devices ***(Note 1)***



Notes to Figure 3–1:

(1) The DC output current per pin is subject to the absolute maximum rating of Table 3–1 on page 3–1.

(2) 1.2-V V_{CCIO} is only applicable to the maximum drive strength.

I/O Standard Specifications

Table 3–5 through Table 3–13 on page 3–8 list the I/O standard specifications for the MAX V device family.

Table 3–5. 3.3-V LVTTL Specifications for MAX V Devices

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	3.0	3.6	V
V_{IH}	High-level input voltage	—	1.7	4.0	V
V_{IL}	Low-level input voltage	—	–0.5	0.8	V
V_{OH}	High-level output voltage	IOH = –4 mA *(1)*	2.4	—	V
V_{OL}	Low-level output voltage	IOL = 4 mA *(1)*	—	0.45	V

Note to Table 3–5:

(1) This specification is supported across all the programmable drive strength settings available for this I/O standard, as shown in the *MAX V Device Architecture* chapter.

Table 3–6. 3.3-V LVCMOS Specifications for MAX V Devices

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	3.0	3.6	V
V_{IH}	High-level input voltage	—	1.7	4.0	V
V_{IL}	Low-level input voltage	—	–0.5	0.8	V
V_{OH}	High-level output voltage	V_{CCIO} = 3.0, IOH = –0.1 mA *(1)*	V_{CCIO} – 0.2	—	V
V_{OL}	Low-level output voltage	V_{CCIO} = 3.0, IOL = 0.1 mA *(1)*	—	0.2	V

Note to Table 3–6:

(1) This specification is supported across all the programmable drive strength settings available for this I/O standard, as shown in the *MAX V Device Architecture* chapter.

Table 3–7. 2.5-V I/O Specifications for MAX V Devices

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	2.375	2.625	V
V_{IH}	High-level input voltage	—	1.7	4.0	V
V_{IL}	Low-level input voltage	—	–0.5	0.7	V
V_{OH}	High-level output voltage	IOH = –0.1 mA *(1)*	2.1	—	V
		IOH = –1 mA *(1)*	2.0	—	V
		IOH = –2 mA *(1)*	1.7	—	V
V_{OL}	Low-level output voltage	IOL = 0.1 mA *(1)*	—	0.2	V
		IOL = 1 mA *(1)*	—	0.4	V
		IOL = 2 mA *(1)*	—	0.7	V

Note to Table 3–7:

(1) This specification is supported across all the programmable drive strength settings available for this I/O standard, as shown in the *MAX V Device Architecture* chapter.

Table 3–8. 1.8-V I/O Specifications for MAX V Devices

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	1.71	1.89	V
V_{IH}	High-level input voltage	—	0.65 × V_{CCIO}	2.25 *(2)*	V
V_{IL}	Low-level input voltage	—	–0.3	0.35 × V_{CCIO}	V
V_{OH}	High-level output voltage	IOH = –2 mA *(1)*	V_{CCIO} – 0.45	—	V
V_{OL}	Low-level output voltage	IOL = 2 mA *(1)*	—	0.45	V

Notes to Table 3–8:

(1) This specification is supported across all the programmable drive strength settings available for this I/O standard, as shown in the *MAX V Device Architecture* chapter.

(2) This maximum V_{IH} reflects the JEDEC specification. The MAX V input buffer can tolerate a V_{IH} maximum of 4.0, as specified by the V_I parameter in Table 3–2 on page 3–2.

Table 3–9. 1.5-V I/O Specifications for MAX V Devices

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	1.425	1.575	V
V_{IH}	High-level input voltage	—	0.65 × V_{CCIO}	V_{CCIO} + 0.3 *(2)*	V
V_{IL}	Low-level input voltage	—	–0.3	0.35 × V_{CCIO}	V
V_{OH}	High-level output voltage	IOH = –2 mA *(1)*	0.75 × V_{CCIO}	—	V
V_{OL}	Low-level output voltage	IOL = 2 mA *(1)*	—	0.25 × V_{CCIO}	V

Notes to Table 3–9:

(1) This specification is supported across all the programmable drive strength settings available for this I/O standard, as shown in the *MAX V Device Architecture* chapter.

(2) This maximum V_{IH} reflects the JEDEC specification. The MAX V input buffer can tolerate a V_{IH} maximum of 4.0, as specified by the V_I parameter in Table 3–2 on page 3–2.

Table 3–10. 1.2-V I/O Specifications for MAX V Devices

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	1.14	1.26	V
V_{IH}	High-level input voltage	—	0.8 × V_{CCIO}	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage	—	–0.3	0.25 × V_{CCIO}	V
V_{OH}	High-level output voltage	IOH = –2 mA *(1)*	0.75 × V_{CCIO}	—	V
V_{OL}	Low-level output voltage	IOL = 2 mA *(1)*	—	0.25 × V_{CCIO}	V

Note to Table 3–10:

(1) This specification is supported across all the programmable drive strength settings available for this I/O standard, as shown in the *MAX V Device Architecture* chapter.

Table 3–11. 3.3-V PCI Specifications for MAX V Devices *(Note 1)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	3.0	3.3	3.6	V
V_{IH}	High-level input voltage	—	0.5 × V_{CCIO}	—	V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage	—	–0.5	—	0.3 × V_{CCIO}	V
V_{OH}	High-level output voltage	IOH = –500 µA	0.9 × V_{CCIO}	—	—	V
V_{OL}	Low-level output voltage	IOL = 1.5 mA	—	—	0.1 × V_{CCIO}	V

Note to Table 3–11:

(1) 3.3-V PCI I/O standard is only supported in Bank 3 of the 5M1270Z and 5M2210Z devices.

Table 3–12. LVDS Specifications for MAX V Devices *(Note 1)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	2.375	2.5	2.625	V
V_{OD}	Differential output voltage swing	—	247	—	600	mV
V_{OS}	Output offset voltage	—	1.125	1.25	1.375	V

Note to Table 3–12:

(1) Supports emulated LVDS output using a three-resistor network (LVDS_E_3R).

Table 3–13. RSDS Specifications for MAX V Devices *(Note 1)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	2.375	2.5	2.625	V
V_{OD}	Differential output voltage swing	—	247	—	600	mV
V_{OS}	Output offset voltage	—	1.125	1.25	1.375	V

Note to Table 3–13:

(1) Supports emulated RSDS output using a three-resistor network (RSDS_E_3R).

Bus Hold Specifications

Table 3–14 lists the bus hold specifications for the MAX V device family.

Table 3–14. Bus Hold Specifications for MAX V Devices

Parameter	Conditions	V_{CCIO} Level										Unit
		1.2 V		1.5 V		1.8 V		2.5 V		3.3 V		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	$V_{IN} > V_{IL}$ (maximum)	10	—	20	—	30	—	50	—	70	—	µA
High sustaining current	$V_{IN} < V_{IH}$ (minimum)	–10	—	–20	—	–30	—	–50	—	–70	—	µA
Low overdrive current	$0 V < V_{IN} < V_{CCIO}$	—	130	—	160	—	200	—	300	—	500	µA
High overdrive current	$0 V < V_{IN} < V_{CCIO}$	—	–130	—	–160	—	–200	—	–300	—	–500	µA

Power-Up Timing

Table 3–15 lists the power-up timing characteristics for the MAX V device family.

Table 3–15. Power-Up Timing for MAX V Devices

Symbol	Parameter	Device	Temperature Range	Min	Typ	Max	Unit
t_{CONFIG}	The amount of time from when minimum V_{CCINT} is reached until the device enters user mode *(1)*	5M40Z	Commercial and industrial	—	—	200	µs
			Extended	—	—	300	µs
		5M80Z	Commercial and industrial	—	—	200	µs
			Extended	—	—	300	µs
		5M160Z	Commercial and industrial	—	—	200	µs
			Extended	—	—	300	µs
		5M240Z *(2)*	Commercial and industrial	—	—	200	µs
			Extended	—	—	300	µs
		5M240Z *(3)*	Commercial and industrial	—	—	300	µs
			Extended	—	—	400	µs
		5M570Z	Commercial and industrial	—	—	300	µs
			Extended	—	—	400	µs
		5M1270Z *(4)*	Commercial and industrial	—	—	300	µs
			Extended	—	—	400	µs
		5M1270Z *(5)*	Commercial and industrial	—	—	450	µs
			Extended	—	—	500	µs
		5M2210Z	Commercial and industrial	—	—	450	µs
			Extended	—	—	500	µs

Notes to Table 3–15:

(1) For more information about power-on reset (POR) trigger voltage, refer to the *Hot Socketing and Power-On Reset in MAX V Devices* chapter.
(2) Not applicable to the T144 package of the 5M240Z device.
(3) Only applicable to the T144 package of the 5M240Z device.
(4) Not applicable to the F324 package of the 5M1270Z device.
(5) Only applicable to the F324 package of the 5M1270Z device.

Power Consumption

You can use the Altera® PowerPlay Early Power Estimator and PowerPlay Power Analyzer to estimate the device power.

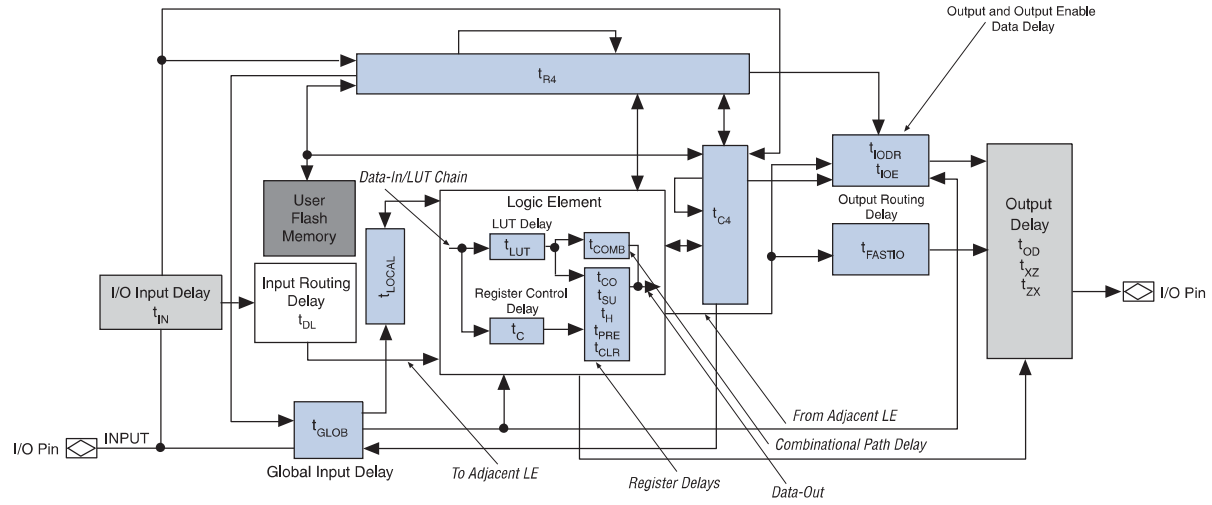
For more information about these power analysis tools, refer to the *PowerPlay Early Power Estimator for Altera CPLDs User Guide* and the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

Timing Model and Specifications

MAX V devices timing can be analyzed with the Altera Quartus® II software, a variety of industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 3–2.

MAX V devices have predictable internal delays that allow you to determine the worst-case timing of any design. The software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for device-wide performance evaluation.

Figure 3–2. Timing Model for MAX V Devices



You can derive the timing characteristics of any signal path from the timing model and parameters of a particular device. You can calculate external timing parameters, which represent pin-to-pin timing delays, as the sum of the internal parameters.

For more information, refer to *AN629: Understanding Timing in Altera CPLDs*.

Preliminary and Final Timing

This section describes the performance, internal, external, and UFM timing specifications. All specifications are representative of the worst-case supply voltage and junction temperature conditions.

Timing models can have either preliminary or final status. The Quartus II software issues an informational message during the design compilation if the timing models are preliminary. Table 3–16 lists the status of the MAX V device timing models.

Preliminary status means the timing model is subject to change. Initially, timing numbers are created using simulation results, process data, and other known parameters. These tests are used to make the preliminary numbers as close to the actual timing parameters as possible.

Final timing numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under the worst-case voltage and junction temperature conditions.

Table 3–16. Timing Model Status for MAX V Devices

Device	Final
5M40Z	✓
5M80Z	✓
5M160Z	✓
5M240Z	✓
5M570Z	✓
5M1270Z	✓
5M2210Z	✓

Performance

Table 3–17 lists the MAX V device performance for some common designs. All performance values were obtained with the Quartus II software compilation of megafunctions.

Table 3–17. Device Performance for MAX V Devices (Part 1 of 2)

Resource Used	Design Size and Function	Resources Used			Performance				Unit
					5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z		5M1270Z/ 5M2210Z		
		Mode	LEs	UFM Blocks	C4	C5, I5	C4	C5, I5	
LE	16-bit counter *(1)*	—	16	0	184.1	118.3	247.5	201.1	MHz
	64-bit counter *(1)*	—	64	0	83.2	80.5	154.8	125.8	MHz
	16-to-1 multiplexer	—	11	0	17.4	20.4	8.0	9.3	ns
	32-to-1 multiplexer	—	24	0	12.5	25.3	9.0	11.4	ns
	16-bit XOR function	—	5	0	9.0	16.1	6.6	8.2	ns
	16-bit decoder with single address line	—	5	0	9.2	16.1	6.6	8.2	ns

Table 3–17. Device Performance for MAX V Devices (Part 2 of 2)

Resource Used	Design Size and Function	Resources Used			Performance				Unit
					5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z		5M1270Z/ 5M2210Z		
		Mode	LEs	UFM Blocks	C4	C5, I5	C4	C5, I5	
UFM	512 × 16	None	3	1	10.0	10.0	10.0	10.0	MHz
	512 × 16	SPI *(2)*	37	1	9.7	9.7	8.0	8.0	MHz
	512 × 8	Parallel *(3)*	73	1	*(4)*	*(4)*	*(4)*	*(4)*	MHz
	512 × 16	I^2C *(3)*	142	1	100 *(5)*	100 *(5)*	100 *(5)*	100 *(5)*	kHz

Notes to Table 3–17:

(1) This design is a binary loadable up counter.
(2) This design is configured for read-only operation in Extended mode. Read and write ability increases the number of logic elements (LEs) used.
(3) This design is configured for read-only operation. Read and write ability increases the number of LEs used.
(4) This design is asynchronous.
(5) The I^2C megafunction is verified in hardware up to 100-kHz serial clock line rate.

Internal Timing Parameters

Internal timing parameters are specified on a speed grade basis independent of device density. Table 3–18 through Table 3–25 on page 3–19 list the MAX V device internal timing microparameters for LEs, input/output elements (IOEs), UFM blocks, and MultiTrack interconnects.

For more information about each internal timing microparameters symbol, refer to *AN629: Understanding Timing in Altera CPLDs*.

Table 3–18. LE Internal Timing Microparameters for MAX V Devices (Part 1 of 2)

Symbol	Parameter	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{LUT}	LE combinational look-up table (LUT) delay	—	1,215	—	2,247	—	742	—	914	ps
t_{COMB}	Combinational path delay	—	243	—	309	—	192	—	236	ps
t_{CLR}	LE register clear delay	401	—	545	—	309	—	381	—	ps
t_{PRE}	LE register preset delay	401	—	545	—	309	—	381	—	ps
t_{SU}	LE register setup time before clock	260	—	321	—	271	—	333	—	ps
t_H	LE register hold time after clock	0	—	0	—	0	—	0	—	ps
t_{CO}	LE register clock-to-output delay	—	380	—	494	—	305	—	376	ps

Table 3–18. LE Internal Timing Microparameters for MAX V Devices (Part 2 of 2)

Symbol	Parameter	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{CLKHL}	Minimum clock high or low time	253	—	339	—	216	—	266	—	ps
t_{C}	Register control delay	—	1,356	—	1,741	—	1,114	—	1,372	ps

Table 3–19. IOE Internal Timing Microparameters for MAX V Devices

Symbol	Parameter	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{FASTIO}	Data output delay from adjacent LE to I/O block	—	170	—	428	—	207	—	254	ps
t_{IN}	I/O input pad and buffer delay	—	907	—	986	—	920	—	1,132	ps
t_{GLOB} *(1)*	I/O input pad and buffer delay used as global signal pin	—	2,261	—	3,322	—	1,974	—	2,430	ps
t_{IOE}	Internally generated output enable delay	—	530	—	1,410	—	374	—	460	ps
t_{DL}	Input routing delay	—	318	—	509	—	291	—	358	ps
t_{OD} *(2)*	Output delay buffer and pad delay	—	1,319	—	1,543	—	1,383	—	1,702	ps
t_{XZ} *(3)*	Output buffer disable delay	—	1,045	—	1,276	—	982	—	1,209	ps
t_{ZX} *(4)*	Output buffer enable delay	—	1,160	—	1,353	—	1,303	—	1,604	ps

Notes to Table 3–19:

(1) Delay numbers for t_{GLOB} differ for each device density and speed grade. The delay numbers for t_{GLOB}, shown in Table 3–19, are based on a 5M240Z device target.

(2) For more information about delay adders associated with different I/O standards, drive strengths, and slew rates, refer to Table 3–34 on page 3–24 and Table 3–35 on page 3–25.

(3) For more information about t_{XZ} delay adders associated with different I/O standards, drive strengths, and slew rates, refer to Table 3–22 on page 3–15 and Table 3–23 on page 3–15.

(4) For more information about t_{ZX} delay adders associated with different I/O standards, drive strengths, and slew rates, refer to Table 3–20 on page 3–14 and Table 3–21 on page 3–14.

Table 3–20 through Table 3–23 list the adder delays for t_{ZX} and t_{XZ} microparameters when using an I/O standard other than 3.3-V LVTTL with 16 mA drive strength.

Table 3–20. t_{ZX} IOE Microparameter Adders for Fast Slew Rate for MAX V Devices

Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	16 mA	—	0	—	0	—	0	—	0	ps
	8 mA	—	72	—	74	—	101	—	125	ps
3.3-V LVCMOS	8 mA	—	0	—	0	—	0	—	0	ps
	4 mA	—	72	—	74	—	101	—	125	ps
2.5-V LVTTL / LVCMOS	14 mA	—	126	—	127	—	155	—	191	ps
	7 mA	—	196	—	197	—	545	—	671	ps
1.8-V LVTTL / LVCMOS	6 mA	—	608	—	610	—	721	—	888	ps
	3 mA	—	681	—	685	—	2012	—	2477	ps
1.5-V LVCMOS	4 mA	—	1162	—	1157	—	1590	—	1957	ps
	2 mA	—	1245	—	1244	—	3269	—	4024	ps
1.2-V LVCMOS	3 mA	—	1889	—	1856	—	2860	—	3520	ps
3.3-V PCI	20 mA	—	72	—	74	—	–18	—	–22	ps
LVDS	—	—	126	—	127	—	155	—	191	ps
RSDS	—	—	126	—	127	—	155	—	191	ps

Table 3–21. t_{ZX} IOE Microparameter Adders for Slow Slew Rate for MAX V Devices

Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	16 mA	—	5,951	—	6,063	—	6,012	—	5,743	ps
	8 mA	—	6,534	—	6,662	—	8,785	—	8,516	ps
3.3-V LVCMOS	8 mA	—	5,951	—	6,063	—	6,012	—	5,743	ps
	4 mA	—	6,534	—	6,662	—	8,785	—	8,516	ps
2.5-V LVTTL / LVCMOS	14 mA	—	9,110	—	9,237	—	10,072	—	9,803	ps
	7 mA	—	9,830	—	9,977	—	12,945	—	12,676	ps
1.8-V LVTTL / LVCMOS	6 mA	—	21,800	—	21,787	—	21,185	—	20,916	ps
	3 mA	—	23,020	—	23,037	—	24,597	—	24,328	ps
1.5-V LVCMOS	4 mA	—	39,120	—	39,067	—	34,517	—	34,248	ps
	2 mA	—	40,670	—	40,617	—	39,717	—	39,448	ps
1.2-V LVCMOS	3 mA	—	69,505	—	70,461	—	55,800	—	55,531	ps
3.3-V PCI	20 mA	—	6,534	—	6,662	—	35	—	44	ps

Table 3–22. t_{XZ} IOE Microparameter Adders for Fast Slew Rate for MAX V Devices

Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	16 mA	—	0	—	0	—	0	—	0	ps
	8 mA	—	–69	—	–69	—	–74	—	–91	ps
3.3-V LVCMOS	8 mA	—	0	—	0	—	0	—	0	ps
	4 mA	—	–69	—	–69	—	–74	—	–91	ps
2.5-V LVTTL / LVCMOS	14 mA	—	–7	—	–10	—	–46	—	–56	ps
	7 mA	—	–66	—	–69	—	–82	—	–101	ps
1.8-V LVTTL / LVCMOS	6 mA	—	45	—	37	—	–7	—	–8	ps
	3 mA	—	34	—	25	—	119	—	147	ps
1.5-V LVCMOS	4 mA	—	166	—	155	—	339	—	418	ps
	2 mA	—	190	—	179	—	464	—	571	ps
1.2-V LVCMOS	3 mA	—	300	—	283	—	817	—	1,006	ps
3.3-V PCI	20 mA	—	–69	—	–69	—	80	—	99	ps
LVDS	—	—	–7	—	–10	—	–46	—	–56	ps
RSDS	—	—	–7	—	–10	—	–46	—	–56	ps

Table 3–23. t_{XZ} IOE Microparameter Adders for Slow Slew Rate for MAX V Devices

Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	16 mA	—	171	—	174	—	73	—	–132	ps
	8 mA	—	112	—	116	—	758	—	553	ps
3.3-V LVCMOS	8 mA	—	171	—	174	—	73	—	–132	ps
	4 mA	—	112	—	116	—	758	—	553	ps
2.5-V LVTTL / LVCMOS	14 mA	—	213	—	213	—	32	—	–173	ps
	7 mA	—	166	—	166	—	714	—	509	ps
1.8-V LVTTL / LVCMOS	6 mA	—	441	—	438	—	96	—	–109	ps
	3 mA	—	496	—	494	—	963	—	758	ps
1.5-V LVCMOS	4 mA	—	765	—	755	—	238	—	33	ps
	2 mA	—	903	—	897	—	1,319	—	1,114	ps
1.2-V LVCMOS	3 mA	—	1,159	—	1,130	—	400	—	195	ps
3.3-V PCI	20 mA	—	112	—	116	—	303	—	373	ps

☞ The default slew rate setting for MAX V devices in the Quartus II design software is "fast".

Table 3–24. UFM Block Internal Timing Microparameters for MAX V Devices (Part 1 of 2)

Symbol	Parameter	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACLK}	Address register clock period	100	—	100	—	100	—	100	—	ns
t_{ASU}	Address register shift signal setup to address register clock	20	—	20	—	20	—	20	—	ns
t_{AH}	Address register shift signal hold to address register clock	20	—	20	—	20	—	20	—	ns
t_{ADS}	Address register data in setup to address register clock	20	—	20	—	20	—	20	—	ns
t_{ADH}	Address register data in hold from address register clock	20	—	20	—	20	—	20	—	ns
t_{DCLK}	Data register clock period	100	—	100	—	100	—	100	—	ns
t_{DSS}	Data register shift signal setup to data register clock	60	—	60	—	60	—	60	—	ns
t_{DSH}	Data register shift signal hold from data register clock	20	—	20	—	20	—	20	—	ns
t_{DDS}	Data register data in setup to data register clock	20	—	20	—	20	—	20	—	ns
t_{DDH}	Data register data in hold from data register clock	20	—	20	—	20	—	20	—	ns
t_{DP}	Program signal to data clock hold time	0	—	0	—	0	—	0	—	ns
t_{PB}	Maximum delay between program rising edge to UFM busy signal rising edge	—	960	—	960	—	960	—	960	ns
t_{BP}	Minimum delay allowed from UFM busy signal going low to program signal going low	20	—	20	—	20	—	20	—	ns
t_{PPMX}	Maximum length of busy pulse during a program	—	100	—	100	—	100	—	100	µs

Table 3–24. UFM Block Internal Timing Microparameters for MAX V Devices (Part 2 of 2)

Symbol	Parameter	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{AE}	Minimum erase signal to address clock hold time	0	—	0	—	0	—	0	—	ns
t_{EB}	Maximum delay between the erase rising edge to the UFM busy signal rising edge	—	960	—	960	—	960	—	960	ns
t_{BE}	Minimum delay allowed from the UFM busy signal going low to erase signal going low	20	—	20	—	20	—	20	—	ns
t_{EPMX}	Maximum length of busy pulse during an erase	—	500	—	500	—	500	—	500	ms
t_{DCO}	Delay from data register clock to data register output	—	5	—	5	—	5	—	5	ns
t_{OE}	Delay from OSC_ENA signal reaching UFM to rising clock of OSC leaving the UFM	180	—	180	—	180	—	180	—	ns
t_{RA}	Maximum read access time	—	65	—	65	—	65	—	65	ns
t_{OSCS}	Maximum delay between the OSC_ENA rising edge to the erase/program signal rising edge	250	—	250	—	250	—	250	—	ns
t_{OSCH}	Minimum delay allowed from the erase/program signal going low to OSC_ENA signal going low	250	—	250	—	250	—	250	—	ns

Figure 3–3 through Figure 3–5 show the read, program, and erase waveforms for UFM block timing parameters listed in Table 3–24.

Figure 3–3. UFM Read Waveform

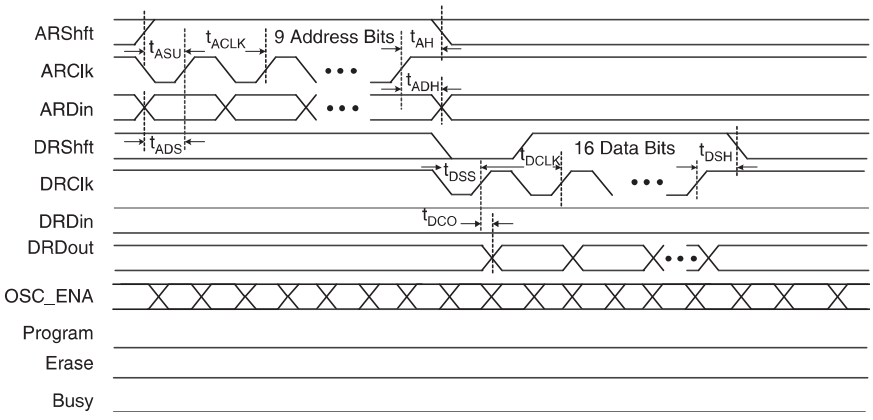


Figure 3–4. UFM Program Waveform

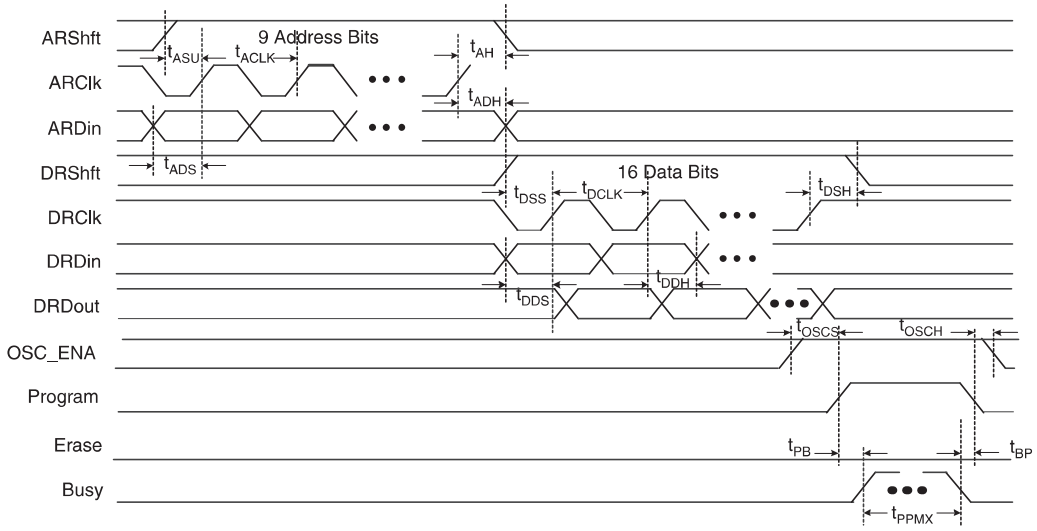


Figure 3–5. UFM Erase Waveform

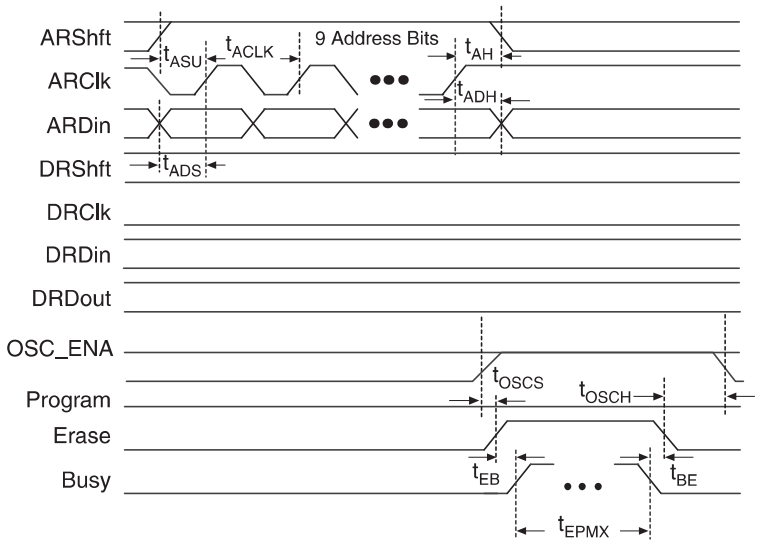


Table 3–25. Routing Delay Internal Timing Microparameters for MAX V Devices

Routing	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
	C4		C5, I5		C4		C5, I5		
	Min	Max	Min	Max	Min	Max	Min	Max	
t_{C4}	—	860	—	1,973	—	561	—	690	ps
t_{R4}	—	655	—	1,479	—	445	—	548	ps
t_{LOCAL}	—	1,143	—	2,947	—	731	—	899	ps

External Timing Parameters

External timing parameters are specified by device density and speed grade. All external I/O timing parameters shown are for the 3.3-V LVTTL I/O standard with the maximum drive strength and fast slew rate. For external I/O timing using standards other than LVTTL or for different drive strengths, use the I/O standard input and output delay adders in Table 3–32 on page 3–23 through Table 3–36 on page 3–25.

For more information about each external timing parameters symbol, refer to *AN 628: Understanding Timing in Altera CPLDs*.

Table 3–26 lists the external I/O timing parameters for the 5M40Z, 5M80Z, 5M160Z, and 5M240Z devices.

Table 3–26. Global Clock External I/O Timing Parameters for the 5M40Z, 5M80Z, 5M160Z, and 5M240Z Devices *(Note 1)*, *(2)*

Symbol	Parameter	Condition	C4		C5, I5		Unit
			Min	Max	Min	Max	
t_{PD1}	Worst case pin-to-pin delay through one LUT	10 pF	—	7.9	—	14.0	ns
t_{PD2}	Best case pin-to-pin delay through one LUT	10 pF	—	5.8	—	8.5	ns
t_{SU}	Global clock setup time	—	2.4	—	4.6	—	ns
t_{H}	Global clock hold time	—	0	—	0	—	ns
t_{CO}	Global clock to output delay	10 pF	2.0	6.6	2.0	8.6	ns
t_{CH}	Global clock high time	—	253	—	339	—	ps
t_{CL}	Global clock low time	—	253	—	339	—	ps
t_{CNT}	Minimum global clock period for 16-bit counter	—	5.4	—	8.4	—	ns
f_{CNT}	Maximum global clock frequency for 16-bit counter	—	—	184.1	—	118.3	MHz

Notes to Table 3–26:

(1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

(2) Not applicable to the T144 package of the 5M240Z device.

Table 3–27 lists the external I/O timing parameters for the T144 package of the 5M240Z device.

Table 3–27. Global Clock External I/O Timing Parameters for the 5M240Z Device *(Note 1)*, *(2)*

Symbol	Parameter	Condition	C4		C5, I5		Unit
			Min	Max	Min	Max	
t_{PD1}	Worst case pin-to-pin delay through one LUT	10 pF	—	9.5	—	17.7	ns
t_{PD2}	Best case pin-to-pin delay through one LUT	10 pF	—	5.7	—	8.5	ns
t_{SU}	Global clock setup time	—	2.2	—	4.4	—	ns
t_{H}	Global clock hold time	—	0	—	0	—	ns
t_{CO}	Global clock to output delay	10 pF	2.0	6.7	2.0	8.7	ns
t_{CH}	Global clock high time	—	253	—	339	—	ps
t_{CL}	Global clock low time	—	253	—	339	—	ps
t_{CNT}	Minimum global clock period for 16-bit counter	—	5.4	—	8.4	—	ns
f_{CNT}	Maximum global clock frequency for 16-bit counter	—	—	184.1	—	118.3	MHz

Notes to Table 3–27:

(1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

(2) Only applicable to the T144 package of the 5M240Z device.

Table 3–28 lists the external I/O timing parameters for the 5M570Z device.

Table 3–28. Global Clock External I/O Timing Parameters for the 5M570Z Device *(Note 1)*

Symbol	Parameter	Condition	C4		C5, I5		Unit
			Min	Max	Min	Max	
t_{PD1}	Worst case pin-to-pin delay through one LUT	10 pF	—	9.5	—	17.7	ns
t_{PD2}	Best case pin-to-pin delay through one LUT	10 pF	—	5.7	—	8.5	ns
t_{SU}	Global clock setup time	—	2.2	—	4.4	—	ns
t_{H}	Global clock hold time	—	0	—	0	—	ns
t_{CO}	Global clock to output delay	10 pF	2.0	6.7	2.0	8.7	ns
t_{CH}	Global clock high time	—	253	—	339	—	ps
t_{CL}	Global clock low time	—	253	—	339	—	ps
t_{CNT}	Minimum global clock period for 16-bit counter	—	5.4	—	8.4	—	ns
f_{CNT}	Maximum global clock frequency for 16-bit counter	—	—	184.1	—	118.3	MHz

Note to Table 3–28:

(1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

Table 3–29 lists the external I/O timing parameters for the 5M1270Z device.

Table 3–29. Global Clock External I/O Timing Parameters for the 5M1270Z Device *(Note 1)*, *(2)*

Symbol	Parameter	Condition	C4		C5, I5		Unit
			Min	Max	Min	Max	
t_{PD1}	Worst case pin-to-pin delay through one LUT	10 pF	—	8.1	—	10.0	ns
t_{PD2}	Best case pin-to-pin delay through one LUT	10 pF	—	4.8	—	5.9	ns
t_{SU}	Global clock setup time	—	1.5	—	1.9	—	ns
t_{H}	Global clock hold time	—	0	—	0	—	ns
t_{CO}	Global clock to output delay	10 pF	2.0	5.9	2.0	7.3	ns
t_{CH}	Global clock high time	—	216	—	266	—	ps
t_{CL}	Global clock low time	—	216	—	266	—	ps
t_{CNT}	Minimum global clock period for 16-bit counter	—	4.0	—	5.0	—	ns
f_{CNT}	Maximum global clock frequency for 16-bit counter	—	—	247.5	—	201.1	MHz

Notes to Table 3–29:

(1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

(2) Not applicable to the F324 package of the 5M1270Z device.

Table 3–30 lists the external I/O timing parameters for the F324 package of the 5M1270Z device.

Table 3–30. Global Clock External I/O Timing Parameters for the 5M1270Z Device *(Note 1)*, *(2)*

Symbol	Parameter	Condition	C4		C5, I5		Unit
			Min	Max	Min	Max	
t_{PD1}	Worst case pin-to-pin delay through one LUT	10 pF	—	9.1	—	11.2	ns
t_{PD2}	Best case pin-to-pin delay through one LUT	10 pF	—	4.8	—	5.9	ns
t_{SU}	Global clock setup time	—	1.5	—	1.9	—	ns
t_{H}	Global clock hold time	—	0	—	0	—	ns
t_{CO}	Global clock to output delay	10 pF	2.0	6.0	2.0	7.4	ns
t_{CH}	Global clock high time	—	216	—	266	—	ps
t_{CL}	Global clock low time	—	216	—	266	—	ps
t_{CNT}	Minimum global clock period for 16-bit counter	—	4.0	—	5.0	—	ns
f_{CNT}	Maximum global clock frequency for 16-bit counter	—	—	247.5	—	201.1	MHz

Notes to Table 3–30:

(1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

(2) Only applicable to the F324 package of the 5M1270Z device.

Table 3–31 lists the external I/O timing parameters for the 5M2210Z device.

Table 3–31. Global Clock External I/O Timing Parameters for the 5M2210Z Device *(Note 1)*

Symbol	Parameter	Condition	C4		C5, I5		Unit
			Min	Max	Min	Max	
t_{PD1}	Worst case pin-to-pin delay through one LUT	10 pF	—	9.1	—	11.2	ns
t_{PD2}	Best case pin-to-pin delay through one LUT	10 pF	—	4.8	—	5.9	ns
t_{SU}	Global clock setup time	—	1.5	—	1.9	—	ns
t_{H}	Global clock hold time	—	0	—	0	—	ns
t_{CO}	Global clock to output delay	10 pF	2.0	6.0	2.0	7.4	ns
t_{CH}	Global clock high time	—	216	—	266	—	ps
t_{CL}	Global clock low time	—	216	—	266	—	ps
t_{CNT}	Minimum global clock period for 16-bit counter	—	4.0	—	5.0	—	ns
f_{CNT}	Maximum global clock frequency for 16-bit counter	—	—	247.5	—	201.1	MHz

Note to Table 3–31:

(1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

External Timing I/O Delay Adders

The I/O delay timing parameters for the I/O standard input and output adders and the input delays are specified by speed grade, independent of device density.

Table 3–32 through Table 3–36 on page 3–25 list the adder delays associated with I/O pins for all packages. If you select an I/O standard other than 3.3-V LVTTL, add the input delay adder to the external t_{SU} timing parameters listed in Table 3–26 on page 3–20 through Table 3–31. If you select an I/O standard other than 3.3-V LVTTL with 16 mA drive strength and fast slew rate, add the output delay adder to the external t_{CO} and t_{PD} listed in Table 3–26 on page 3–20 through Table 3–31.

Table 3–32. External Timing Input Delay Adders for MAX V Devices

I/O Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	Without Schmitt Trigger	—	0	—	0	—	0	—	0	ps
	With Schmitt Trigger	—	387	—	442	—	480	—	591	ps
3.3-V LVCMOS	Without Schmitt Trigger	—	0	—	0	—	0	—	0	ps
	With Schmitt Trigger	—	387	—	442	—	480	—	591	ps
2.5-V LVTTL / LVCMOS	Without Schmitt Trigger	—	42	—	42	—	246	—	303	ps
	With Schmitt Trigger	—	429	—	483	—	787	—	968	ps
1.8-V LVTTL / LVCMOS	Without Schmitt Trigger	—	378	—	368	—	695	—	855	ps
1.5-V LVCMOS	Without Schmitt Trigger	—	681	—	658	—	1,334	—	1,642	ps
1.2-V LVCMOS	Without Schmitt Trigger	—	1,055	—	1,010	—	2,324	—	2,860	ps
3.3-V PCI	Without Schmitt Trigger	—	0	—	0	—	0	—	0	ps

Table 3–33. External Timing Input Delay t_{GLOB} Adders for GCLK Pins for MAX V Devices (Part 1 of 2)

I/O Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	Without Schmitt Trigger	—	0	—	0	—	0	—	0	ps
	With Schmitt Trigger	—	387	—	442	—	400	—	493	ps

Table 3–33. External Timing Input Delay t_{GLOB} Adders for GCLK Pins for MAX V Devices (Part 2 of 2)

I/O Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVCMOS	Without Schmitt Trigger	—	0	—	0	—	0	—	0	ps
	With Schmitt Trigger	—	387	—	442	—	400	—	493	ps
2.5-V LVTTL / LVCMOS	Without Schmitt Trigger	—	242	—	242	—	287	—	353	ps
	With Schmitt Trigger	—	429	—	483	—	550	—	677	ps
1.8-V LVTTL / LVCMOS	Without Schmitt Trigger	—	378	—	368	—	459	—	565	ps
1.5-V LVCMOS	Without Schmitt Trigger	—	681	—	658	—	1,111	—	1,368	ps
1.2-V LVCMOS	Without Schmitt Trigger	—	1,055	—	1,010	—	2,067	—	2,544	ps
3.3-V PCI	Without Schmitt Trigger	—	0	—	0	—	7	—	9	ps

Table 3–34. External Timing Output Delay and t_{OD} Adders for Fast Slew Rate for MAX V Devices

I/O Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	16 mA	—	0	—	0	—	0	—	0	ps
	8 mA	—	39	—	58	—	84	—	104	ps
3.3-V LVCMOS	8 mA	—	0	—	0	—	0	—	0	ps
	4 mA	—	39	—	58	—	84	—	104	ps
2.5-V LVTTL / LVCMOS	14 mA	—	122	—	129	—	158	—	195	ps
	7 mA	—	196	—	188	—	251	—	309	ps
1.8-V LVTTL / LVCMOS	6 mA	—	624	—	624	—	738	—	909	ps
	3 mA	—	686	—	694	—	850	—	1,046	ps
1.5-V LVCMOS	4 mA	—	1,188	—	1,184	—	1,376	—	1,694	ps
	2 mA	—	1,279	—	1,280	—	1,517	—	1,867	ps
1.2-V LVCMOS	3 mA	—	1,911	—	1,883	—	2,206	—	2,715	ps
3.3-V PCI	20 mA	—	39	—	58	—	4	—	5	ps
LVDS	—	—	122	—	129	—	158	—	195	ps
RSDS	—	—	122	—	129	—	158	—	195	ps

Table 3–35. External Timing Output Delay and t_{OD} Adders for Slow Slew Rate for MAX V Devices

I/O Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
		C4		C5, I5		C4		C5, I5		
		Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	16 mA	—	5,913	—	6,043	—	6,612	—	6,293	ps
	8 mA	—	6,488	—	6,645	—	7,313	—	6,994	ps
3.3-V LVCMOS	8 mA	—	5,913	—	6,043	—	6,612	—	6,293	ps
	4 mA	—	6,488	—	6,645	—	7,313	—	6,994	ps
2.5-V LVTTL / LVCMOS	14 mA	—	9,088	—	9,222	—	10,021	—	9,702	ps
	7 mA	—	9,808	—	9,962	—	10,881	—	10,562	ps
1.8-V LVTTL / LVCMOS	6 mA	—	21,758	—	21,782	—	21,134	—	20,815	ps
	3 mA	—	23,028	—	23,032	—	22,399	—	22,080	ps
1.5-V LVCMOS	4 mA	—	39,068	—	39,032	—	34,499	—	34,180	ps
	2 mA	—	40,578	—	40,542	—	36,281	—	35,962	ps
1.2-V LVCMOS	3 mA	—	69,332	—	70,257	—	55,796	—	55,477	ps
3.3-V PCI	20 mA	—	6,488	—	6,645	—	339	—	418	ps

Table 3–36. IOE Programmable Delays for MAX V Devices

Parameter	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z				5M1270Z/ 5M2210Z				Unit
	C4		C5, I5		C4		C5, I5		
	Min	Max	Min	Max	Min	Max	Min	Max	
Input Delay from Pin to Internal Cells = 1	—	1,858	—	2,214	—	1,592	—	1,960	ps
Input Delay from Pin to Internal Cells = 0	—	569	—	616	—	115	—	142	ps

Maximum Input and Output Clock Rates

Table 3–37 and Table 3–38 list the maximum input and output clock rates for standard I/O pins in MAX V devices.

Table 3–37. Maximum Input Clock Rate for I/Os for MAX V Devices

I/O Standard		5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z/5M1270Z/ 5M2210Z	Unit
		C4, C5, I5	
3.3-V LVTTL	Without Schmitt Trigger	304	MHz
	With Schmitt Trigger	304	MHz
3.3-V LVCMOS	Without Schmitt Trigger	304	MHz
	With Schmitt Trigger	304	MHz
2.5-V LVTTL	Without Schmitt Trigger	304	MHz
	With Schmitt Trigger	304	MHz
2.5-V LVCMOS	Without Schmitt Trigger	304	MHz
	With Schmitt Trigger	304	MHz
1.8-V LVTTL	Without Schmitt Trigger	200	MHz
1.8-V LVCMOS	Without Schmitt Trigger	200	MHz
1.5-V LVCMOS	Without Schmitt Trigger	150	MHz
1.2-V LVCMOS	Without Schmitt Trigger	120	MHz
3.3-V PCI	Without Schmitt Trigger	304	MHz

Table 3–38. Maximum Output Clock Rate for I/Os for MAX V Devices

I/O Standard	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z/5M1270Z/ 5M2210Z	Unit
	C4, C5, I5	
3.3-V LVTTL	304	MHz
3.3-V LVCMOS	304	MHz
2.5-V LVTTL	304	MHz
2.5-V LVCMOS	304	MHz
1.8-V LVTTL	200	MHz
1.8-V LVCMOS	200	MHz
1.5-V LVCMOS	150	MHz
1.2-V LVCMOS	120	MHz
3.3-V PCI	304	MHz
LVDS	304	MHz
RSDS	200	MHz

LVDS and RSDS Output Timing Specifications

Table 3–39 lists the emulated LVDS output timing specifications for MAX V devices.

Table 3–39. Emulated LVDS Output Timing Specifications for MAX V Devices

Parameter	Mode	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z/5M1270Z/ 5M2210Z		Unit
		C4, C5, I5		
		Min	Max	
Data rate *(1)*, *(2)*	×10	—	304	Mbps
	×9	—	304	Mbps
	×8	—	304	Mbps
	×7	—	304	Mbps
	×6	—	304	Mbps
	×5	—	304	Mbps
	×4	—	304	Mbps
	×3	—	304	Mbps
	×2	—	304	Mbps
	×1	—	304	Mbps
t_{DUTY}	—	45	55	%
Total jitter *(3)*	—	—	0.2	UI
t_{RISE}	—	—	450	ps
t_{FALL}	—	—	450	ps

Notes to Table 3–39:

(1) The performance of the LVDS_E_3R transmitter system is limited by the lower of the two—the maximum data rate supported by LVDS_E_3R I/O buffer or 2x (F_{MAX} of the ALTLVDS_TX instance). The actual performance of your LVDS_E_3R transmitter system must be attained through the Quartus II timing analysis of the complete design.

(2) For the input clock pin to achieve 304 Mbps, use I/O standard with V_{CCIO} of 2.5 V and above.

(3) This specification is based on external clean clock source.

Table 3–40 lists the emulated RSDS output timing specifications for MAX V devices.

Table 3–40. Emulated RSDS Output Timing Specifications for MAX V Devices

Parameter	Mode	5M40Z/ 5M80Z/ 5M160Z/ 5M240Z/ 5M570Z/5M1270Z/ 5M2210Z		Unit
		C4, C5, I5		
		Min	Max	
Data rate *(1)*	×10	—	200	Mbps
	×9	—	200	Mbps
	×8	—	200	Mbps
	×7	—	200	Mbps
	×6	—	200	Mbps
	×5	—	200	Mbps
	×4	—	200	Mbps
	×3	—	200	Mbps
	×2	—	200	Mbps
	×1	—	200	Mbps
t_{DUTY}	—	45	55	%
Total jitter *(2)*	—	—	0.2	UI
t_{RISE}	—	—	450	ps
t_{FALL}	—	—	450	ps

Notes to Table 3–40:

(1) For the input clock pin to achieve 200 Mbps, use I/O standard with V_{CCIO} of 1.8 V and above.

(2) This specification is based on external clean clock source.

JTAG Timing Specifications

Figure 3–6 shows the timing waveform for the JTAG signals for the MAX V device family.

Figure 3–6. JTAG Timing Waveform for MAX V Devices

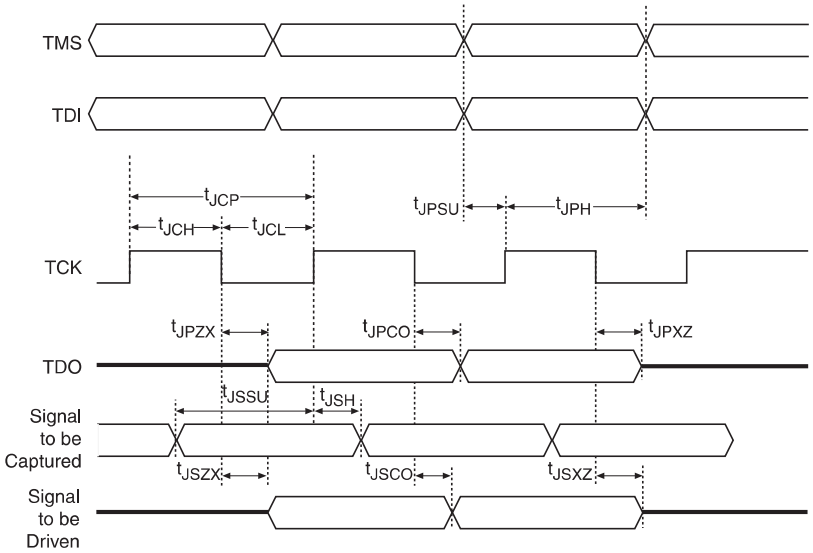


Table 3–41 lists the JTAG timing parameters and values for the MAX V device family.

Table 3–41. JTAG Timing Parameters for MAX V Devices (Part 1 of 2)

Symbol	Parameter	Min	Max	Unit
t_{JCP} *(1)*	TCK clock period for V_{CCIO1} = 3.3 V	55.5	—	ns
	TCK clock period for V_{CCIO1} = 2.5 V	62.5	—	ns
	TCK clock period for V_{CCIO1} = 1.8 V	100	—	ns
	TCK clock period for V_{CCIO1} = 1.5 V	143	—	ns
t_{JCH}	TCK clock high time	20	—	ns
t_{JCL}	TCK clock low time	20	—	ns
t_{JPSU}	JTAG port setup time *(2)*	8	—	ns
t_{JPH}	JTAG port hold time	10	—	ns
t_{JPCO}	JTAG port clock to output *(2)*	—	15	ns
t_{JPZX}	JTAG port high impedance to valid output *(2)*	—	15	ns
t_{JPXZ}	JTAG port valid output to high impedance *(2)*	—	15	ns
t_{JSSU}	Capture register setup time	8	—	ns
t_{JSH}	Capture register hold time	10	—	ns
t_{JSCO}	Update register clock to output	—	25	ns
t_{JSZX}	Update register high impedance to valid output	—	25	ns

Table 3–41. JTAG Timing Parameters for MAX V Devices (Part 2 of 2)

Symbol	Parameter	Min	Max	Unit
t_{JSXZ}	Update register valid output to high impedance	—	25	ns

Notes to Table 3–41:

(1) Minimum clock period specified for 10 pF load on the TDO pin. Larger loads on TDO degrades the maximum TCK frequency.

(2) This specification is shown for 3.3-V LVTTL/LVCMOS and 2.5-V LVTTL/LVCMOS operation of the JTAG pins. For 1.8-V LVTTL/LVCMOS and 1.5-V LVCMOS operation, the t_{JPSU} minimum is 6 ns and t_{JPCO}, t_{JPZX}, and t_{JPXZ} are maximum values at 35 ns.

Document Revision History

Table 3–42 lists the revision history for this chapter.

Table 3–42. Document Revision History

Date	Version	Changes
May 2011	1.2	Updated Table 3–2, Table 3–15, Table 3–16, and Table 3–33.
January 2011	1.1	Updated Table 3–37, Table 3–38, Table 3–39, and Table 3–40.
December 2010	1.0	Initial release.

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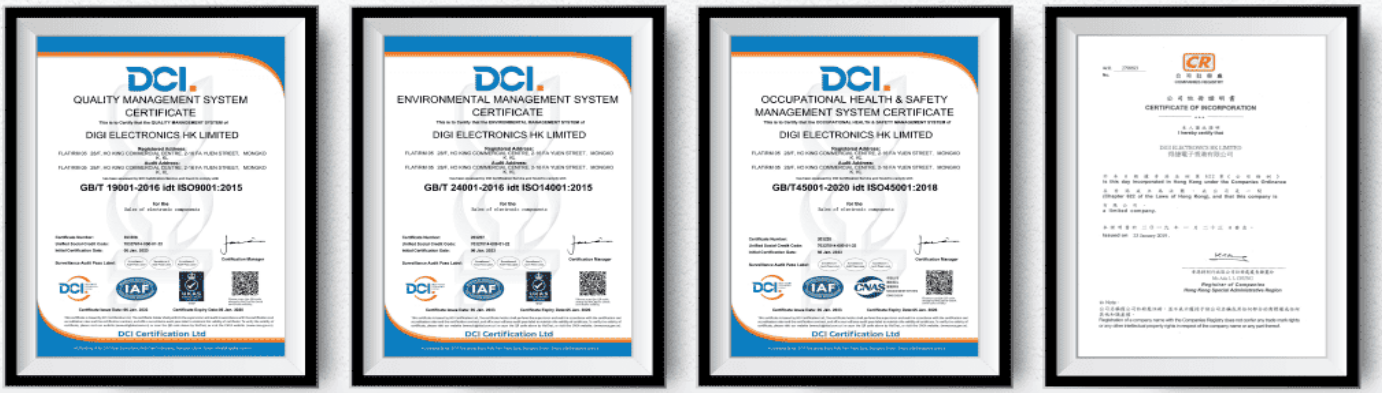

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