

BSC0302LSATMA1 Datasheet



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DiGi Electronics Part Number	BSC0302LSATMA1-DG
Manufacturer	Infineon Technologies
Manufacturer Product Number	BSC0302LSATMA1
Description	MOSFET N-CH 120V 12A/99A TDSON
Detailed Description	N-Channel 120 V 12A (Ta), 99A (Tc) 156W (Tc) Surface Mount PG-TDSON-8-7

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Manufacturer Product Number:

BSC0302LSATMA1

Series:

OptiMOS™ 2

FET Type:

N-Channel

Drain to Source Voltage (Vdss):

120 V

Drive Voltage (Max Rds On, Min Rds On):

4.5V, 10V

Vgs(th) (Max) @ Id:

2.4V @ 112µA

Vgs (Max):

±20V

FET Feature:

-

Operating Temperature:

-55°C ~ 150°C (Tj)

Supplier Device Package:

PG-TDSON-8-7

Base Product Number:

BSC0302

Manufacturer:

Infineon Technologies

Product Status:

Active

Technology:

MOSFET (Metal Oxide)

Current - Continuous Drain (Id) @ 25°C:

12A (Ta), 99A (Tc)

Rds On (Max) @ Id, Vgs:

8mOhm @ 50A, 10V

Gate Charge (Qg) (Max) @ Vgs:

79 nC @ 10 V

Input Capacitance (Ciss) (Max) @ Vds:

7400 pF @ 60 V

Power Dissipation (Max):

156W (Tc)

Mounting Type:

Surface Mount

Package / Case:

8-PowerTDFN

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8541.29.0095

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

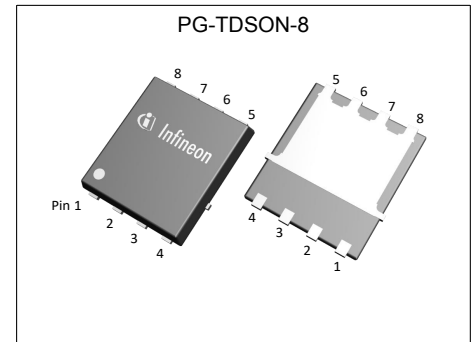
EAR99

MOSFET

OptiMOS™ 3 Power-Transistor, 120 V

Features

- N-channel, logic level
- 100% avalanche tested
- Excellent gate charge x RDS(on) product (FOM)
- Very low on-resistance RDS(on)
- 150 °C operating temperature
- Pb-free lead plating; RoHS compliant
- Ideal for high-frequency switching and synchronous rectification
- Halogen-free according to IEC61249-2-21

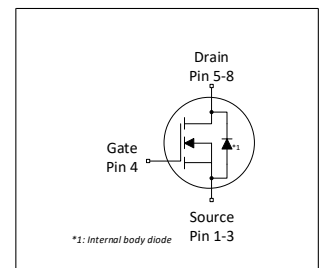


Product validation

Qualified according to JEDEC Standard

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	120	V
$R_{DS(on),max}$	8.0	m Ω
I_D	99	A
Q_{oss}	79	nC
$Q_G(0V..10V)$	79	nC



RoHS

Type / Ordering Code	Package	Marking	Related Links
BSC0302LS	PG-TDSON-8	0302LS	-



OptiMOS™ 3 Power-Transistor, 120 V

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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	99	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=4.5\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=45\text{ °C/W}^{(1)}$
Pulsed drain current ⁽²⁾	$I_{D,pulse}$	-	-	394	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse ⁽³⁾	E_{AS}	-	-	377	mJ	$I_D=50\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	156	W	$T_C=25\text{ °C}$
Operating and storage temperature	T_j , T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	0.45	0.8	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	18	°C/W	-
Thermal resistance, junction - ambient, minimal footprint	R_{thJA}	-	-	62	°C/W	-
Thermal resistance, junction - ambient, 6 cm ² cooling area ⁽²⁾	R_{thJA}	-	-	45	°C/W	-

¹⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

²⁾ See Diagram 3 for more detailed information

³⁾ See Diagram 13 for more detailed information

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3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	120	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	1.2	1.85	2.4	V	$V_{DS}=V_{GS}$, $I_D=112\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.01 1	1 100	μA	$V_{DS}=120\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=120\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	1	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	6.5 7.8	8.0 9.5	m Ω	$V_{GS}=10\text{ V}$, $I_D=50\text{ A}$ $V_{GS}=4.5\text{ V}$, $I_D=25\text{ A}$
Gate resistance	R_G	-	0.85	-	Ω	-
Transconductance	g_{fs}	60	120	-	S	$ V_{DS} \geq 2 I_D R_{DS(on)max}$, $I_D=50\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance ¹⁾	C_{iss}	-	5600	7400	pF	$V_{GS}=0\text{ V}$, $V_{DS}=60\text{ V}$, $f=1\text{ MHz}$
Output capacitance ¹⁾	C_{oss}	-	590	770	pF	$V_{GS}=0\text{ V}$, $V_{DS}=60\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance ¹⁾	C_{rss}	-	28	42	pF	$V_{GS}=0\text{ V}$, $V_{DS}=60\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	11	-	ns	$V_{DD}=60\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=25\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	9	-	ns	$V_{DD}=60\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=25\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	37	-	ns	$V_{DD}=60\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=25\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Fall time	t_f	-	13	-	ns	$V_{DD}=60\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=25\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$

Table 6 Gate charge characteristics²⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	17.5	-	nC	$V_{DD}=60\text{ V}$, $I_D=25\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	Q_{gd}	-	12.9	-	nC	$V_{DD}=60\text{ V}$, $I_D=25\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	Q_{sw}	-	20.1	-	nC	$V_{DD}=60\text{ V}$, $I_D=25\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total	Q_g	-	79	-	nC	$V_{DD}=60\text{ V}$, $I_D=25\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	3.1	-	V	$V_{DD}=60\text{ V}$, $I_D=25\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge	Q_{oss}	-	79	-	nC	$V_{DD}=60\text{ V}$, $V_{GS}=0\text{ V}$

¹⁾ Defined by design. Not subject to production test.

²⁾ See "Gate charge waveforms" for parameter definition

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Table 7 Reverse diode

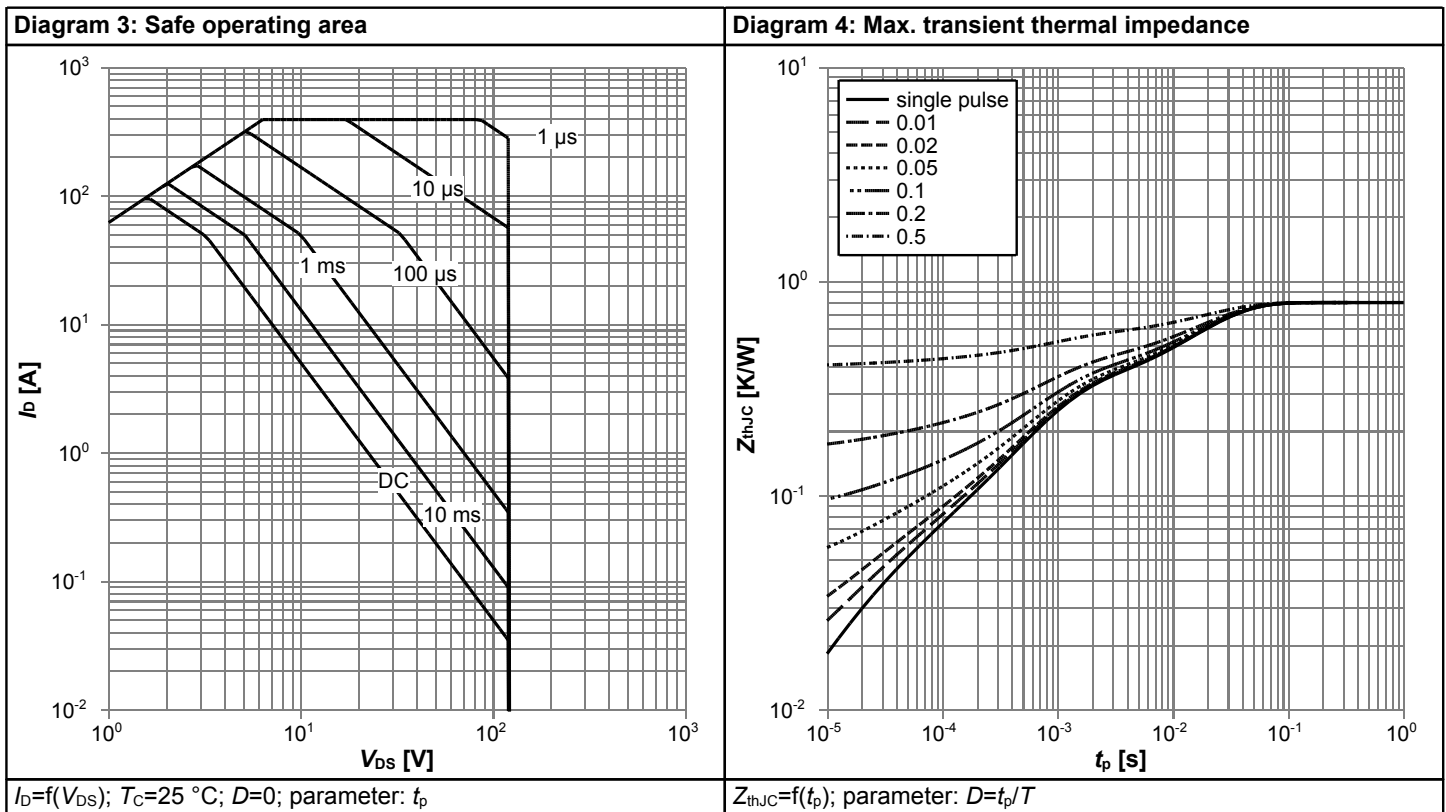
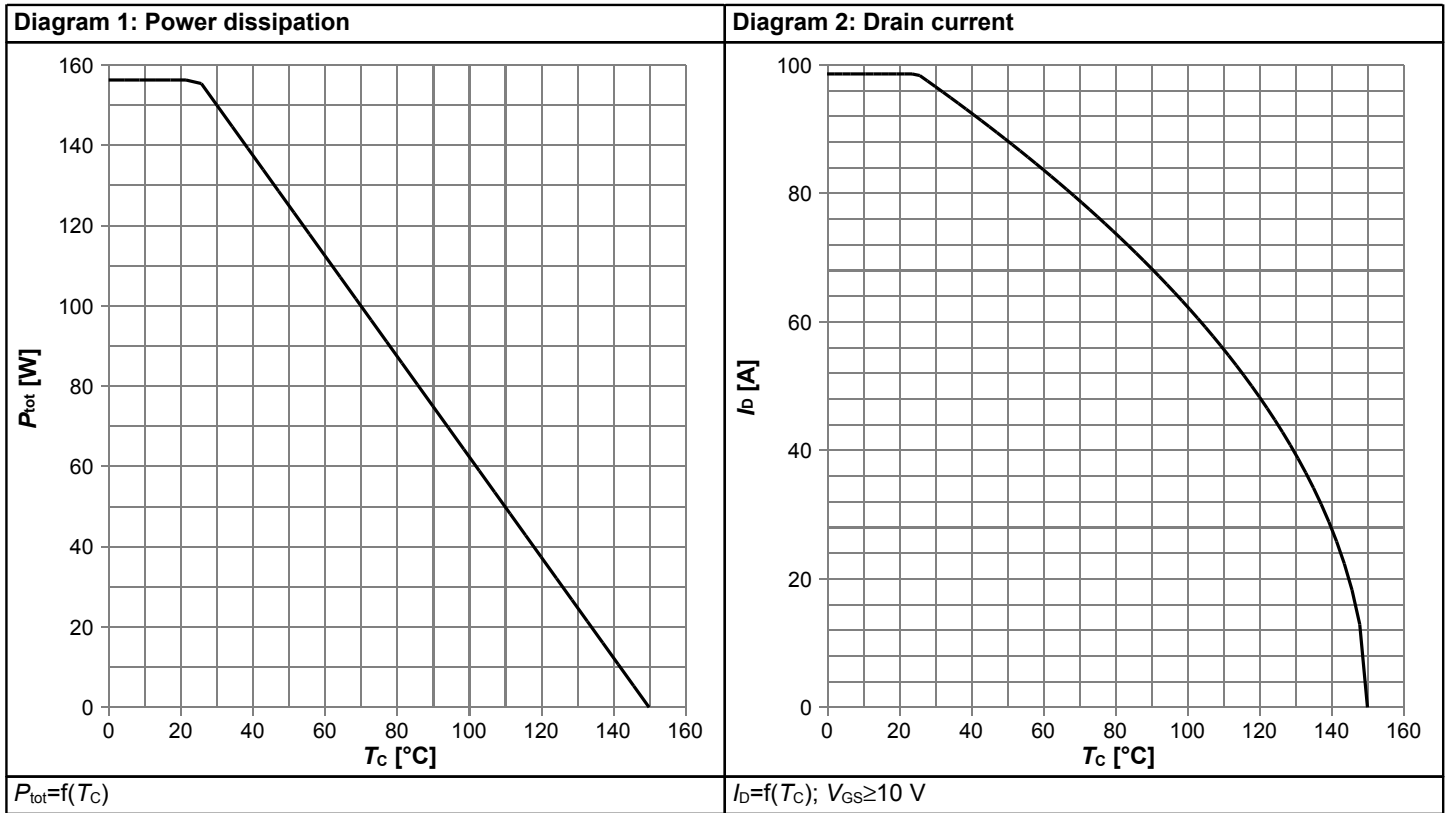
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	109	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	394	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.88	1.2	V	$V_{GS}=0\text{ V}, I_F=50\text{ A}, T_j=25\text{ °C}$
Reverse recovery time	t_{rr}	-	107	-	ns	$V_R=60\text{ V}, I_F=25\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}	-	220	-	nC	$V_R=60\text{ V}, I_F=25\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$



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4 Electrical characteristics diagrams

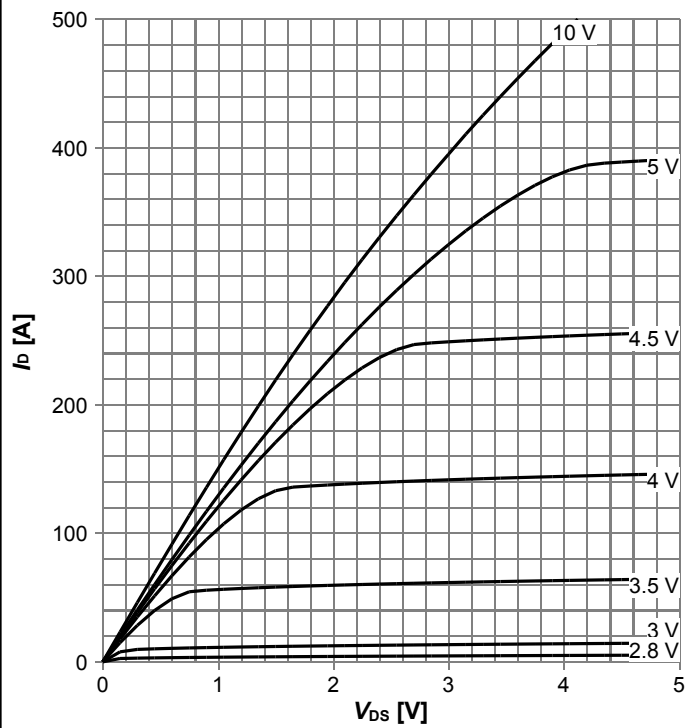




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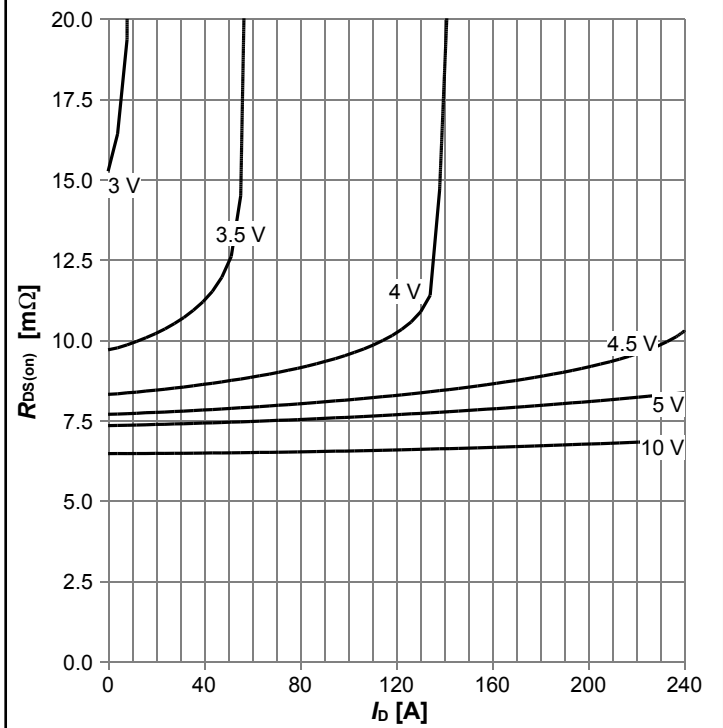
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Diagram 5: Typ. output characteristics



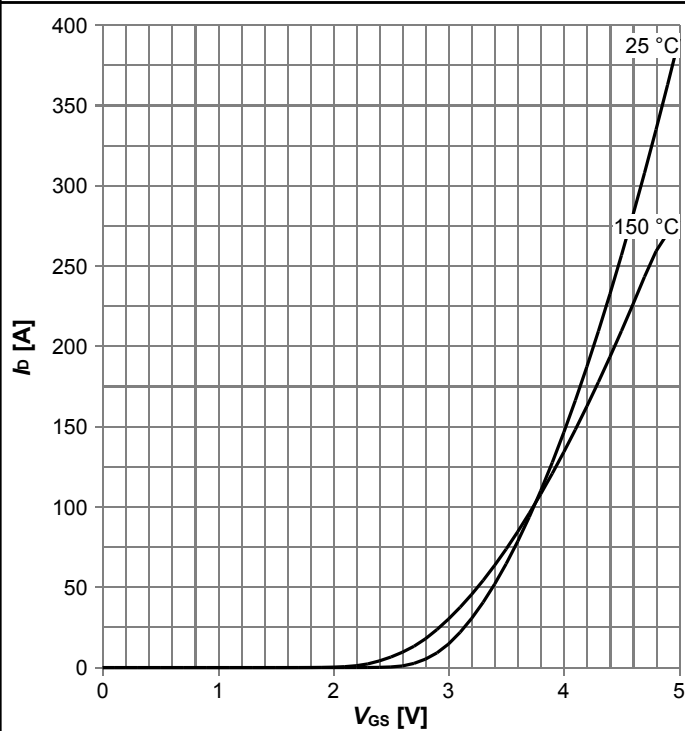
$I_D = f(V_{DS})$, $T_j = 25\text{ °C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



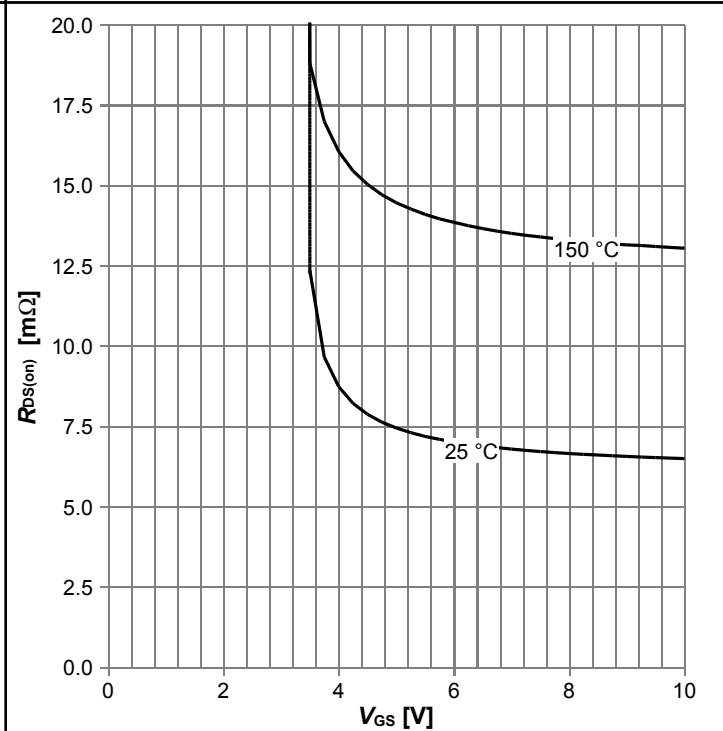
$R_{DS(on)} = f(I_D)$, $T_j = 25\text{ °C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



$I_D = f(V_{GS})$, $|V_{DS}| > 2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



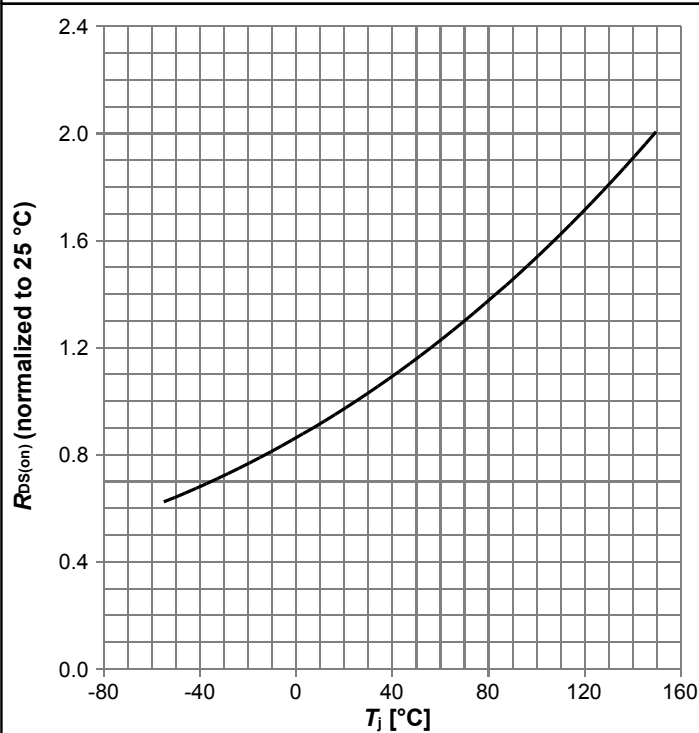
$R_{DS(on)} = f(V_{GS})$, $I_D = 50\text{ A}$; parameter: T_j



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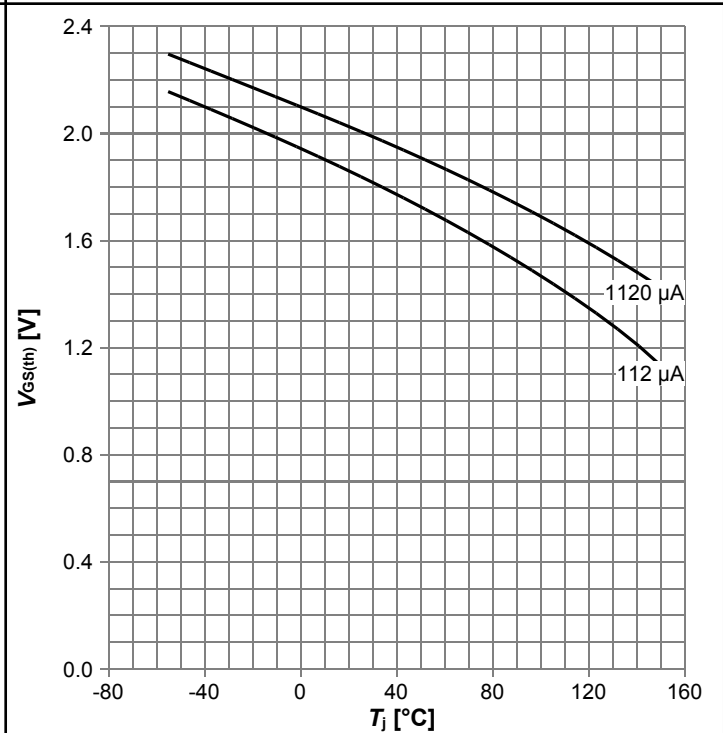
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Diagram 9: Normalized drain-source on resistance



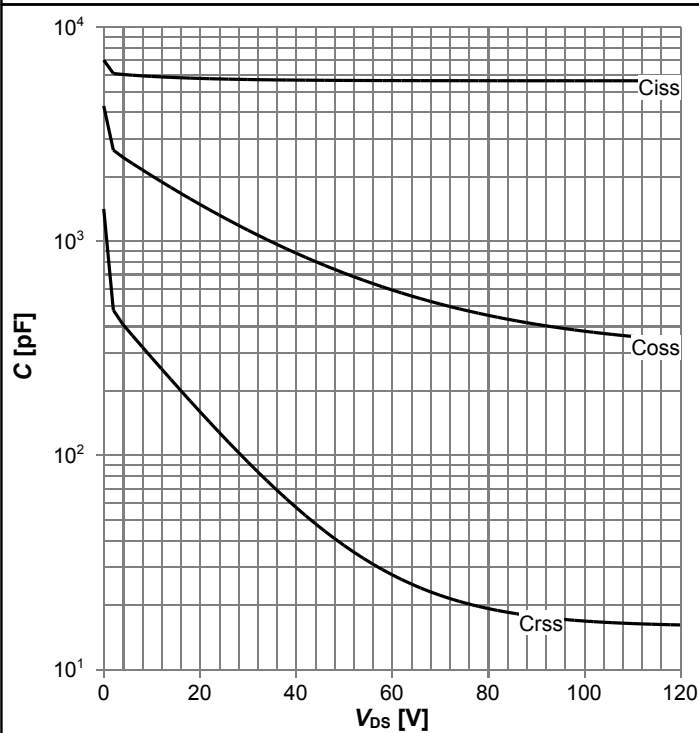
$R_{DS(on)}=f(T_j)$, $I_D=50$ A, $V_{GS}=10$ V

Diagram 10: Typ. gate threshold voltage



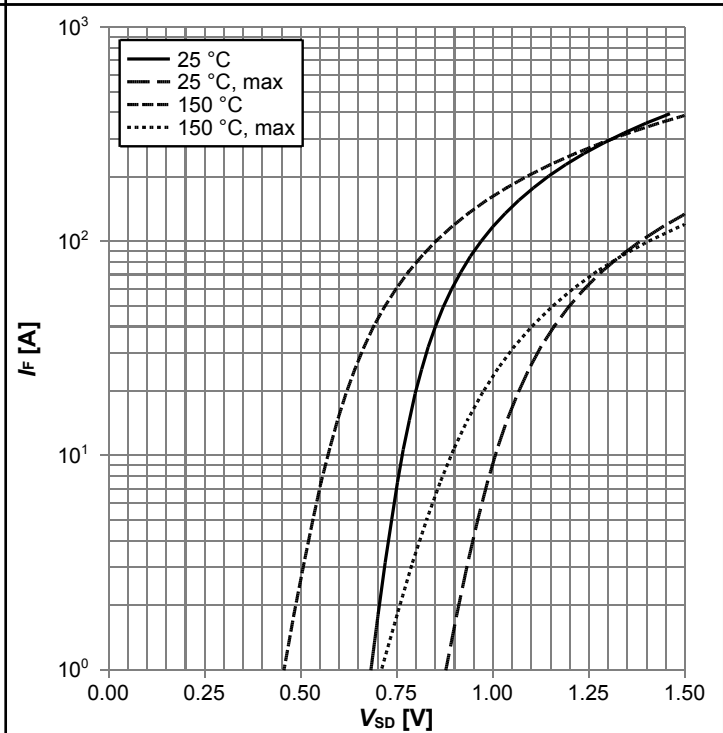
$V_{GS(th)}=f(T_j)$, $V_{GS}=V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz

Diagram 12: Forward characteristics of reverse diode



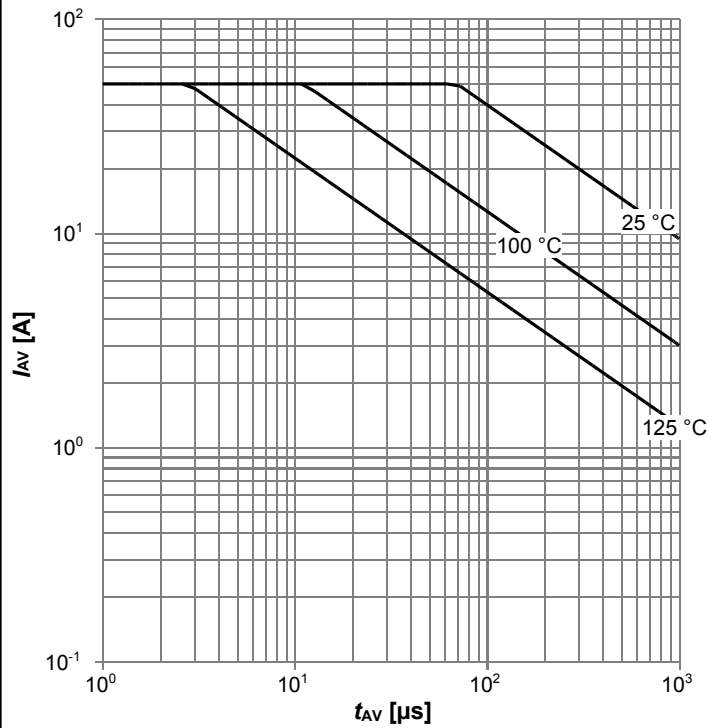
$I_F=f(V_{SD})$; parameter: T_j



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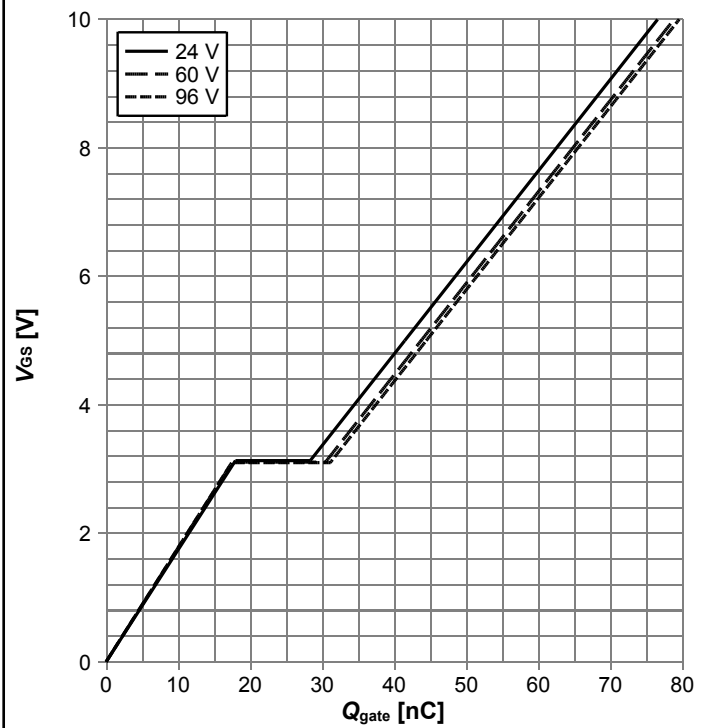
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Diagram 13: Avalanche characteristics



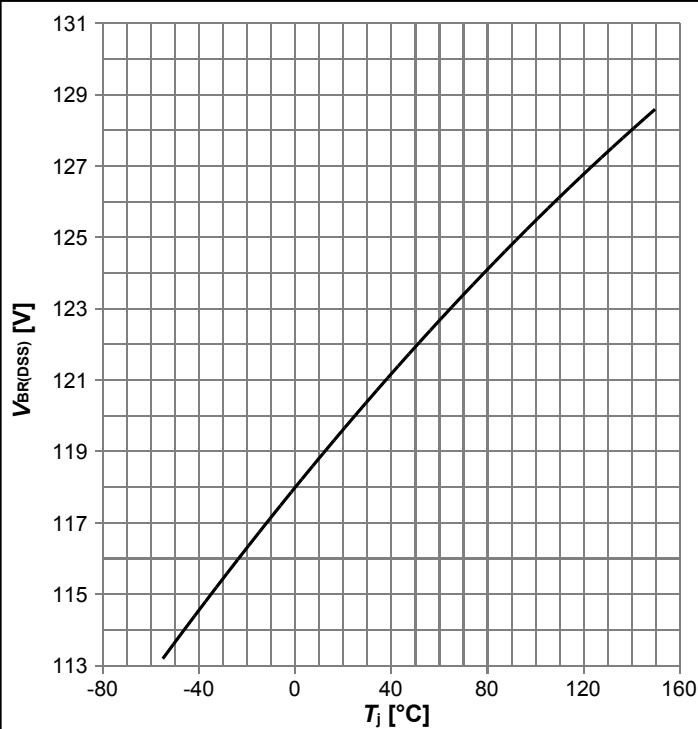
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



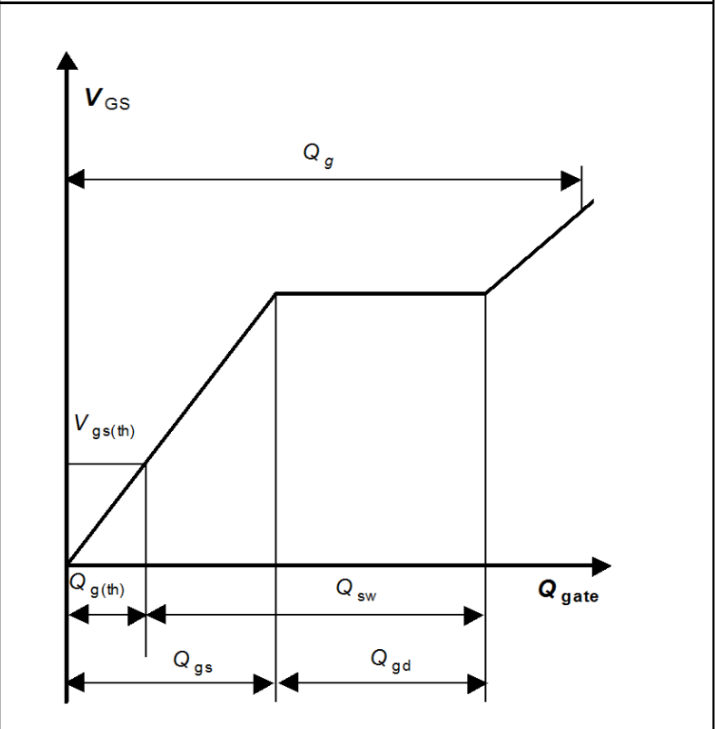
$V_{GS}=f(Q_{gate}), I_D=25 A$ pulsed, $T_j=25 \text{ °C}$; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

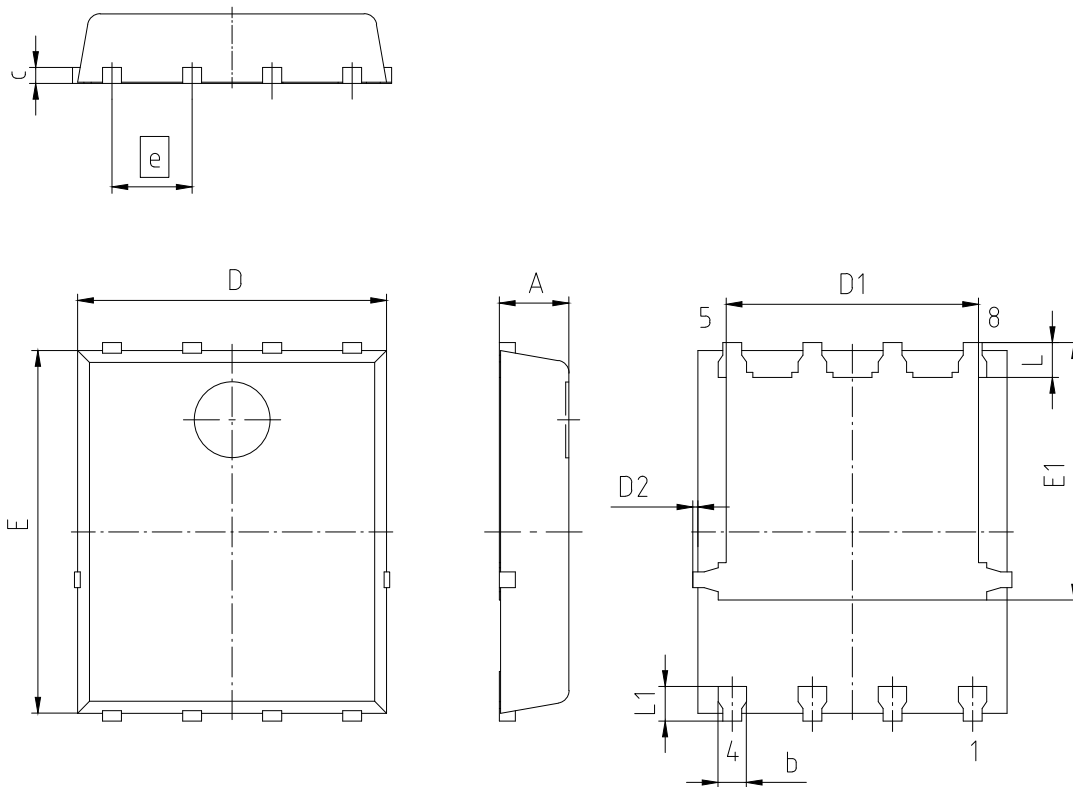
Diagram Gate charge waveforms



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5 Package Outlines



PACKAGE - GROUP NUMBER:		PG-TDSON-8-U08	
DIMENSIONS	MILLIMETERS		
	MIN.	MAX.	
A	0.90	1.20	
b	0.34	0.54	
c	0.15	0.35	
D	4.80	5.35	
D1	3.90	4.40	
D2	0.00	0.22	
E	5.70	6.10	
E1	4.05	4.25	
e	1.27		
L	0.45	0.65	
L1	0.45	0.65	

- 1) EXCLUDING MOLD FLASH
- 2) REMOVAL ON MOLD GATE
INTRUSION 0.1 MM
PROTRUSION 0.1 MM
- 3) ALL METAL SURFACES ARE PLATED,
EXCEPT AREA OF CUT

Figure 1 Outline PG-TDSON-8, dimensions in mm

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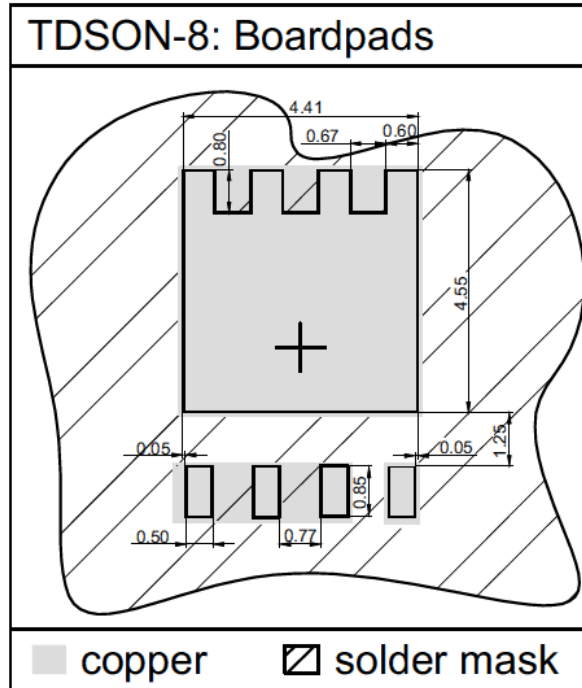


Figure 2 Outline Footprint (TDSO8-8)



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Revision History

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Revision: 2022-09-21, Rev. 2.2

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2019-12-02	Release of final version
2.1	2022-08-09	Update "Features", qualification, footnotes and fix bug.
2.2	2022-09-21	Update outline drawing

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