

BSC094N06LS5ATMA1 Datasheet



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DiGi Electronics Part Number	BSC094N06LS5ATMA1-DG
Manufacturer	Infineon Technologies
Manufacturer Product Number	BSC094N06LS5ATMA1
Description	MOSFET N-CHANNEL 60V 47A 8TDSO8
Detailed Description	N-Channel 60 V 47A (Tc) 36W (Tc) Surface Mount PG-TDSO8-8-6



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Purchase and inquiry

Manufacturer Product Number:

BSC094N06LS5ATMA1

Series:

OptiMOS™

FET Type:

N-Channel

Drain to Source Voltage (Vdss):

60 V

Drive Voltage (Max Rds On, Min Rds On):

4.5V, 10V

Vgs(th) (Max) @ Id:

2.3V @ 14µA

Vgs (Max):

±20V

FET Feature:

-

Operating Temperature:

-55°C ~ 150°C (Tj)

Supplier Device Package:

PG-TDSON-8-6

Base Product Number:

BSC094

Manufacturer:

Infineon Technologies

Product Status:

Active

Technology:

MOSFET (Metal Oxide)

Current - Continuous Drain (Id) @ 25°C:

47A (Tc)

Rds On (Max) @ Id, Vgs:

9.4mOhm @ 24A, 10V

Gate Charge (Qg) (Max) @ Vgs:

9.4 nC @ 4.5 V

Input Capacitance (Ciss) (Max) @ Vds:

1300 pF @ 30 V

Power Dissipation (Max):

36W (Tc)

Mounting Type:

Surface Mount

Package / Case:

8-PowerTDFN

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8541.29.0095

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

MOSFET

OptiMOS™ Power-Transistor, 60 V

Features

- Optimized for high performance SMPS, e.g. sync. rec.
- 100% avalanche tested
- Superior thermal resistance
- N-channel, logic level
- Qualified according to JEDEC¹⁾ for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

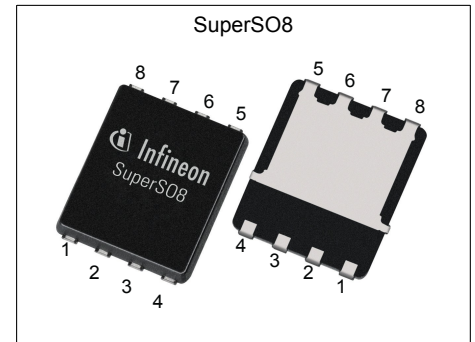
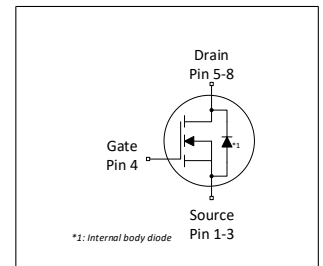


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	60	V
$R_{DS(on),max}$	9.4	m Ω
I_D	47	A
Q_{OSS}	13	nC
$Q_G(0V..4.5V)$	7	nC



RoHS

Type / Ordering Code	Package	Marking	Related Links
BSC094N06LS5	PG-TDSON-8	094N06LS	-

¹⁾ J-STD20 and JESD22



OptiMOS™ Power-Transistor, 60 V

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OptiMOS™ Power-Transistor, 60 V

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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	47	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=50\text{K/W}^{(1)}$
		-	-	30		
		-	-	11		
Pulsed drain current ⁽²⁾	$I_{D,pulse}$	-	-	188	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse ⁽³⁾	E_{AS}	-	-	13	mJ	$I_D=30\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	36	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{thJA}=50\text{ K/W}^{(1)}$
		-	-	2.1		
Operating and storage temperature	T_j , T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	2.1	3.5	K/W	-
Device on PCB, 6 cm ² cooling area ⁽¹⁾	R_{thJA}	-	-	50	K/W	-

¹⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

²⁾ See Diagram 3 for more detailed information

³⁾ See Diagram 13 for more detailed information

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3 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	1.1	1.7	2.3	V	$V_{DS}=V_{GS}$, $I_D=14\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	μA	$V_{DS}=60\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ }^\circ\text{C}$ $V_{DS}=60\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ }^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	7.7 11	9.4 13.4	$\text{m}\Omega$	$V_{GS}=10\text{ V}$, $I_D=24\text{ A}$ $V_{GS}=4.5\text{ V}$, $I_D=12\text{ A}$
Gate resistance ¹⁾	R_G	-	1.1	1.65	Ω	-
Transconductance	g_{fs}	22	45	-	S	$ V_{DS} >2 I_D R_{DS(on)max}$, $I_D=24\text{ A}$

Table 5 Dynamic characteristics¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	970	1300	pF	$V_{GS}=0\text{ V}$, $V_{DS}=30\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}	-	210	280	pF	$V_{GS}=0\text{ V}$, $V_{DS}=30\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance	C_{rss}	-	12	21	pF	$V_{GS}=0\text{ V}$, $V_{DS}=30\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	4	-	ns	$V_{DD}=30\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=24\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	3	-	ns	$V_{DD}=30\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=24\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	14	-	ns	$V_{DD}=30\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=24\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Fall time	t_f	-	3	-	ns	$V_{DD}=30\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=24\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$

Table 6 Gate charge characteristics²⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	3	-	nC	$V_{DD}=30\text{ V}$, $I_D=24\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	2	-	nC	$V_{DD}=30\text{ V}$, $I_D=24\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate to drain charge ¹⁾	Q_{gd}	-	2	3.5	nC	$V_{DD}=30\text{ V}$, $I_D=24\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Switching charge	Q_{sw}	-	4	-	nC	$V_{DD}=30\text{ V}$, $I_D=24\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total ¹⁾	Q_g	-	7	9.4	nC	$V_{DD}=30\text{ V}$, $I_D=24\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	3.1	-	V	$V_{DD}=30\text{ V}$, $I_D=24\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	12	-	nC	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge ¹⁾	Q_{oss}	-	13	18	nC	$V_{DD}=30\text{ V}$, $V_{GS}=0\text{ V}$

¹⁾ Defined by design. Not subject to production test.

²⁾ See "Gate charge waveforms" for parameter definition

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Table 7 Reverse diode

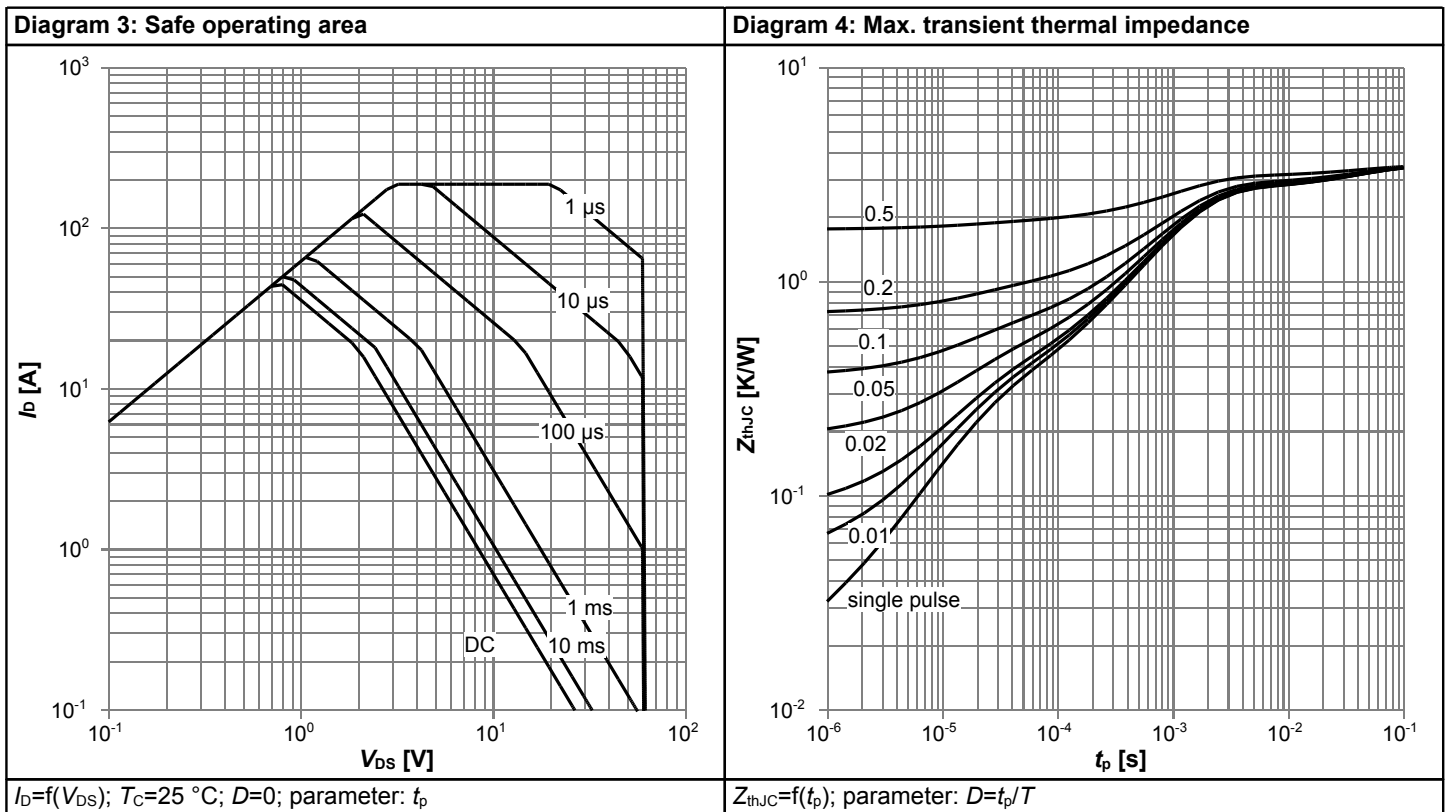
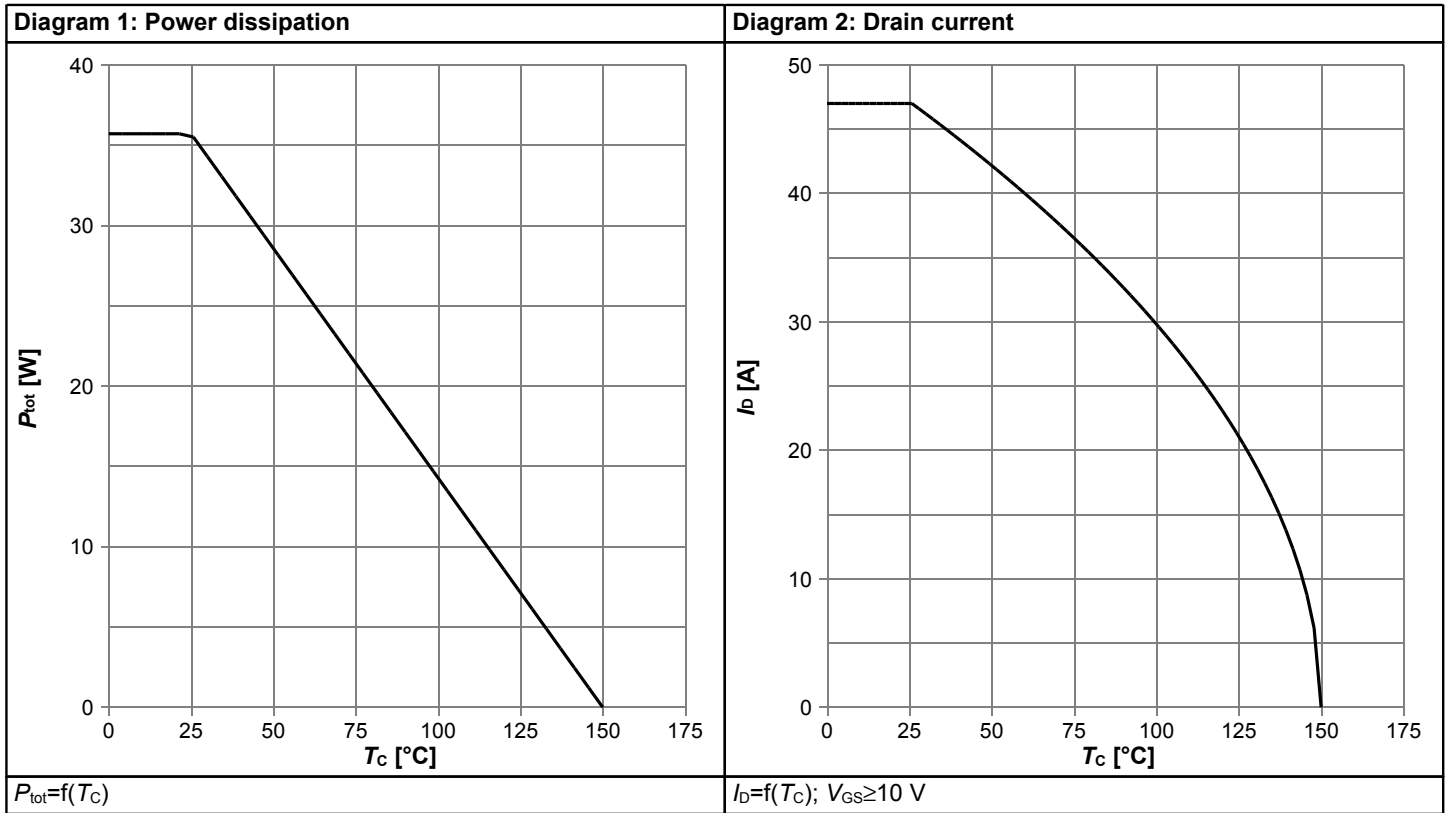
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	30	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	188	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.9	1.2	V	$V_{GS}=0\text{ V}, I_F=24\text{ A}, T_j=25\text{ °C}$
Reverse recovery time ¹⁾	t_{rr}	-	18	36	ns	$V_R=30\text{ V}, I_F=24\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁾	Q_{rr}	-	6	12	nC	$V_R=30\text{ V}, I_F=24\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$

¹⁾ Defined by design. Not subject to production test.



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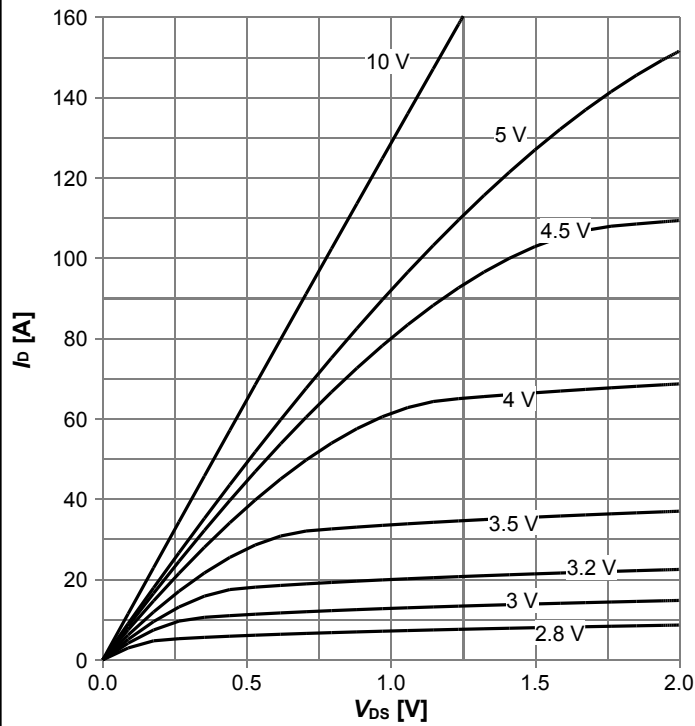
4 Electrical characteristics diagrams





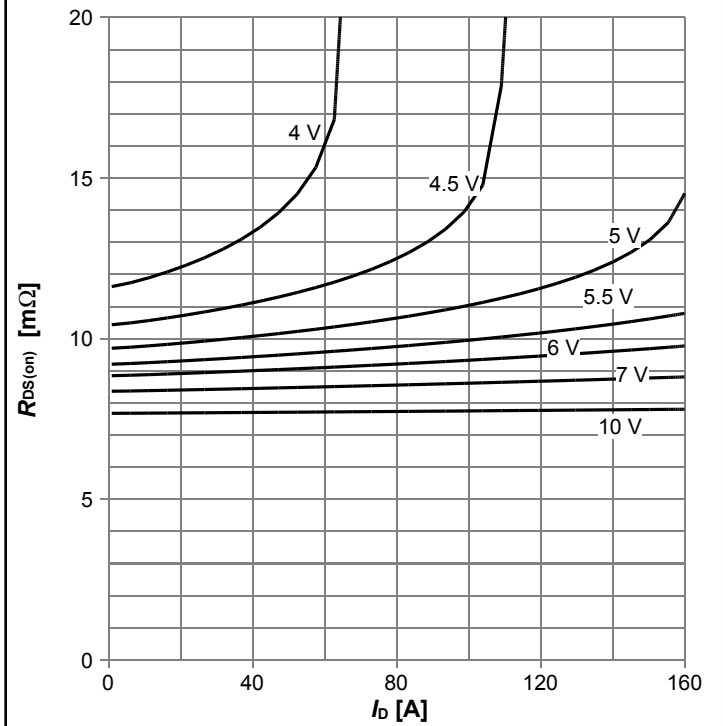
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Diagram 5: Typ. output characteristics



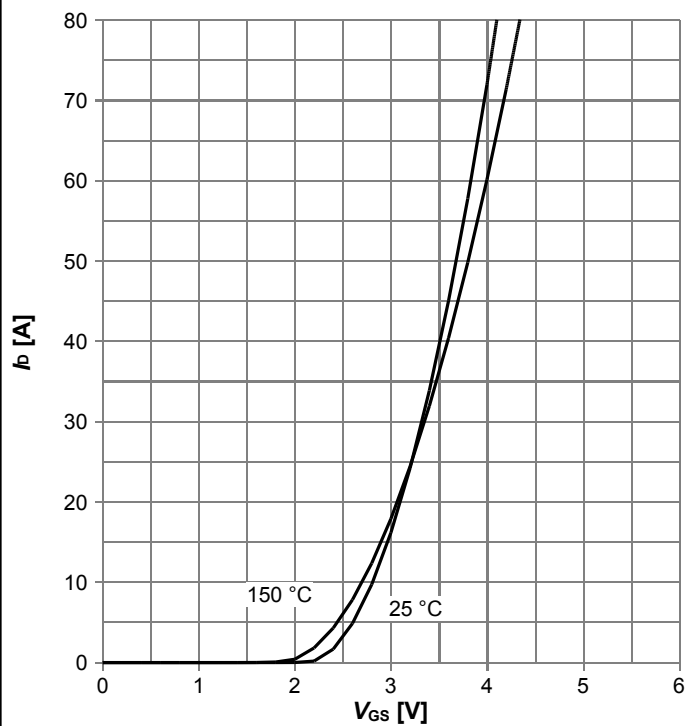
$I_D=f(V_{DS}); T_j=25\text{ °C}; \text{parameter: } V_{GS}$

Diagram 6: Typ. drain-source on resistance



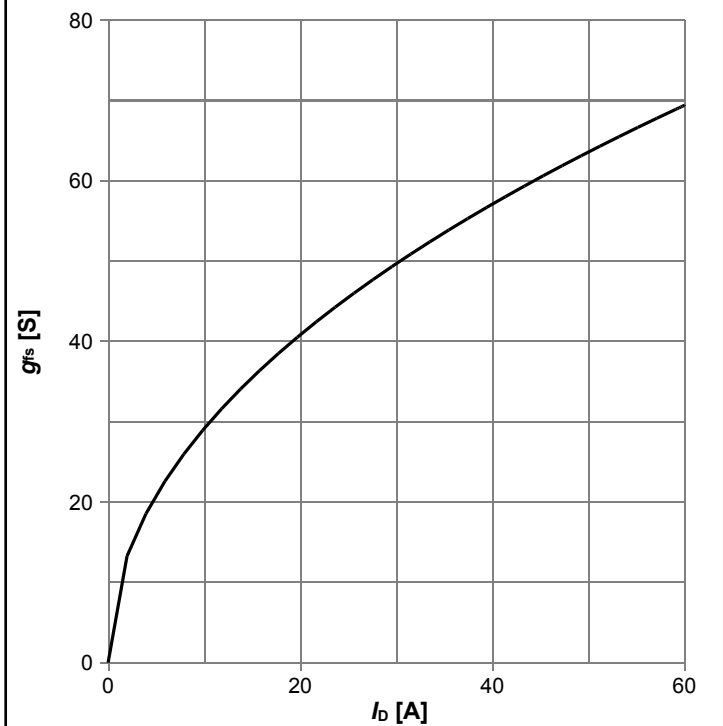
$R_{DS(on)}=f(I_D); T_j=25\text{ °C}; \text{parameter: } V_{GS}$

Diagram 7: Typ. transfer characteristics



$I_D=f(V_{GS}); |V_{DS}|>2|I_D|R_{DS(on)max}; \text{parameter: } T_j$

Diagram 8: Typ. forward transconductance

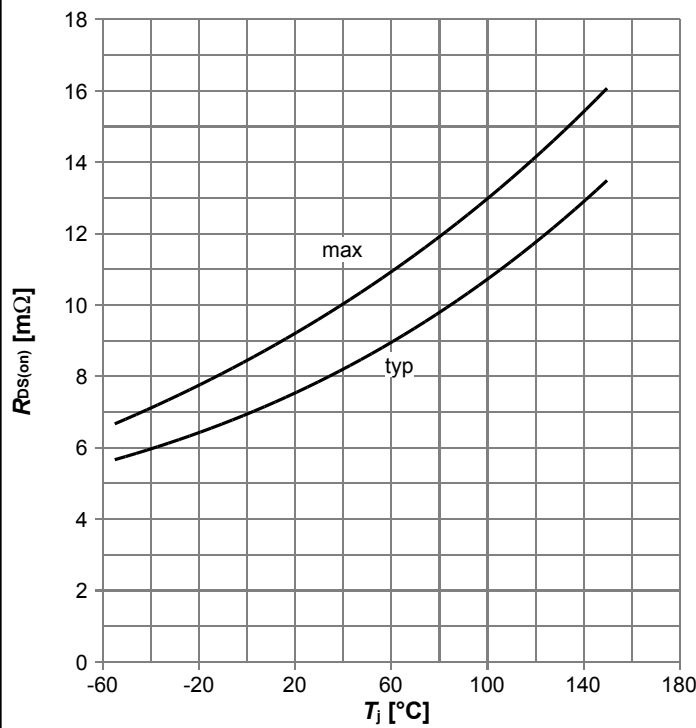


$g_{fs}=f(I_D); T_j=25\text{ °C}$



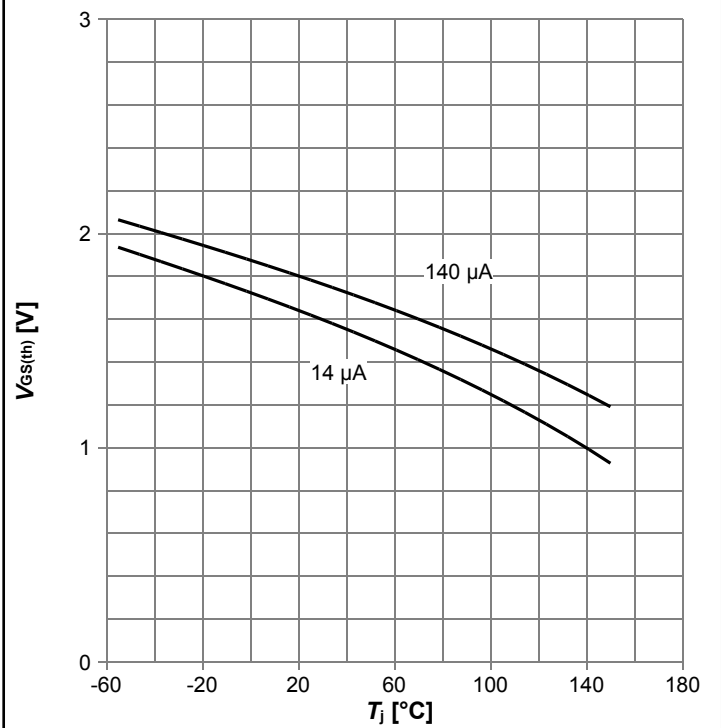
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Diagram 9: Drain-source on-state resistance



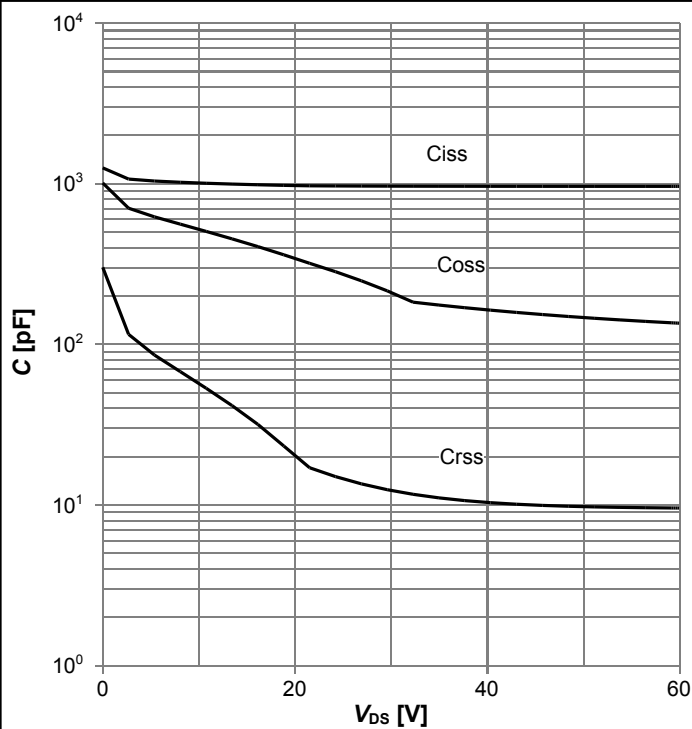
$R_{DS(on)}=f(T_j)$; $I_D=24$ A; $V_{GS}=10$ V

Diagram 10: Typ. gate threshold voltage



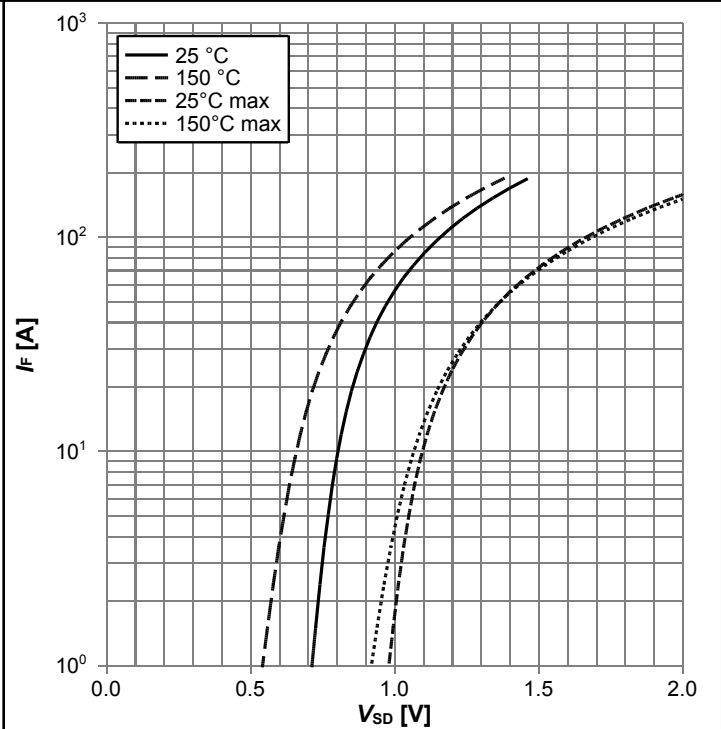
$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$

Diagram 11: Typ. capacitances



$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz

Diagram 12: Forward characteristics of reverse diode

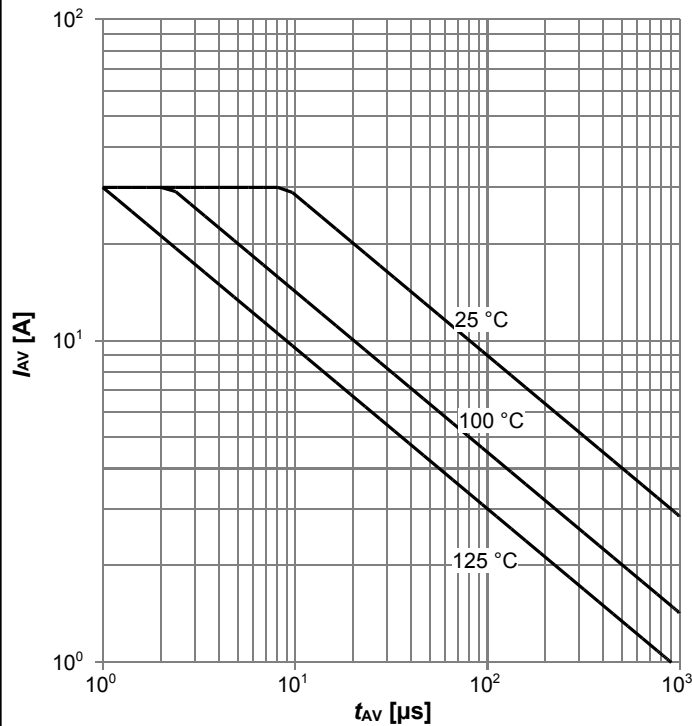


$I_F=f(V_{SD})$; parameter: T_j



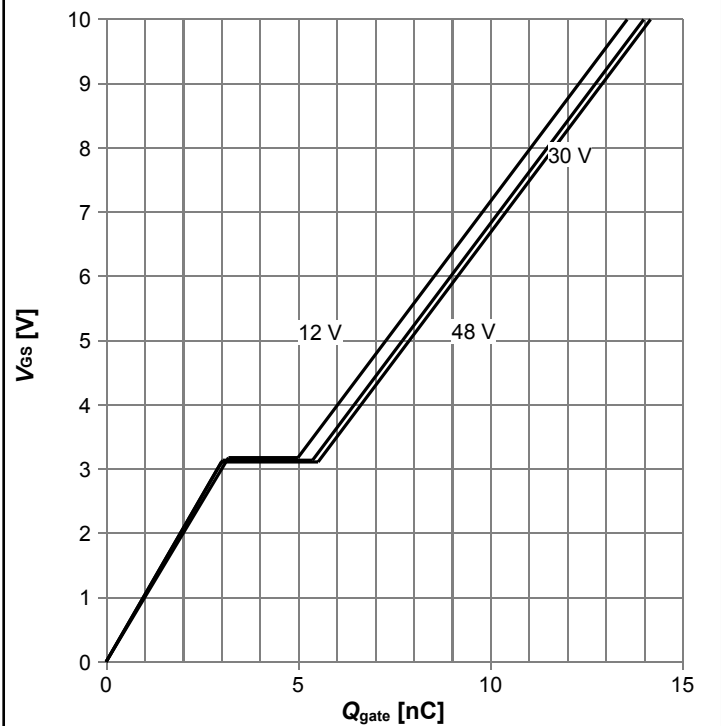
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Diagram 13: Avalanche characteristics



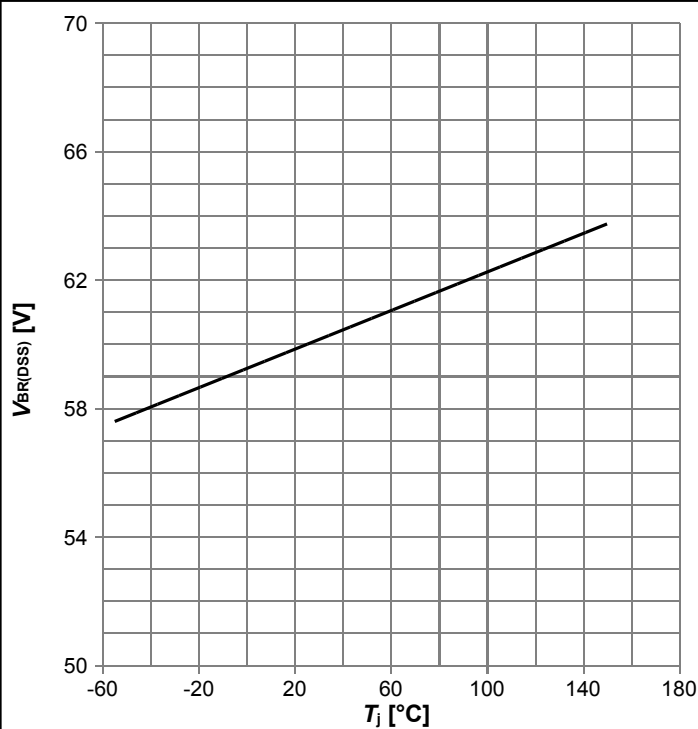
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



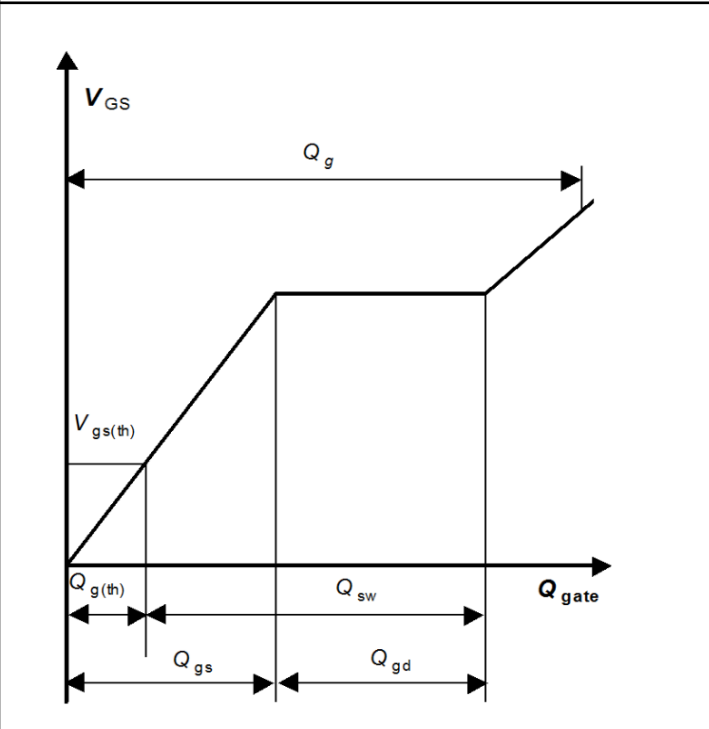
$V_{GS}=f(Q_{gate}); I_D=24 \text{ A pulsed}$; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

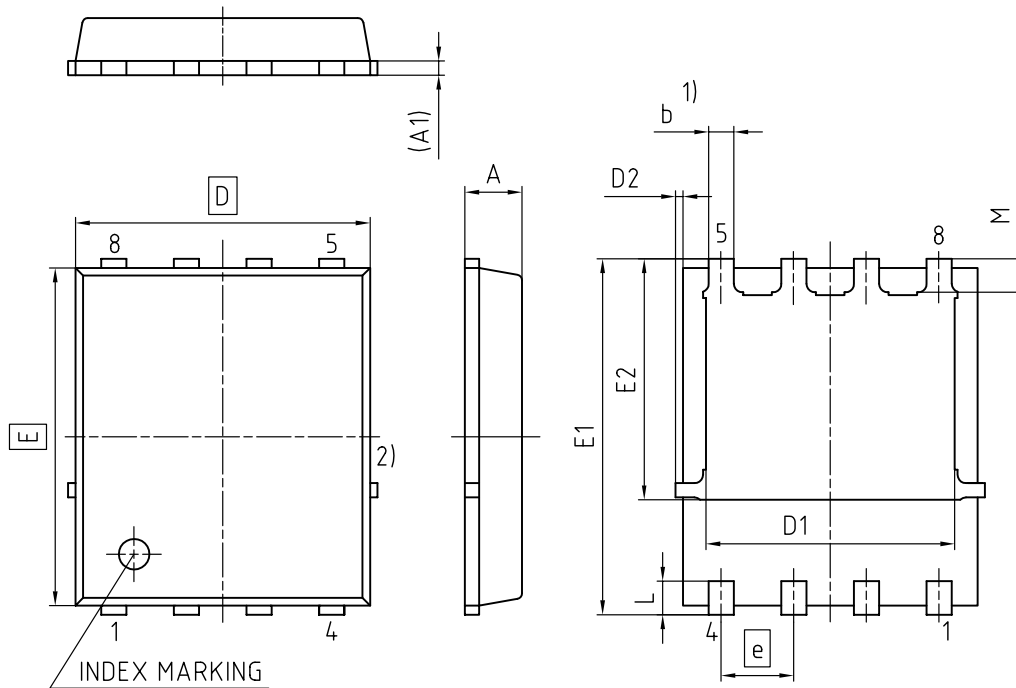
Diagram Gate charge waveforms



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5 Package Outlines



- 1) EXCLUDING MOLD FLASH
 2) REMOVAL ON MOLD GATE
 INTRUSION 0.1 MM
 PROTRUSION 0.1 MM
 LEAD LENGTH UP TO ANTI FLASH LINE
 ALL METAL SURFACES ARE PLATED, EXCEPT AREA OF CUT

DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.20
A1	0.15	0.35
b	0.34	0.54
D	4.80	5.35
D1	3.90	4.40
D2	0.03	0.23
E	5.70	6.10
E1	5.90	6.42
E2	3.88	4.31
e	1.27	
L	0.45	0.71
M	0.45	0.69

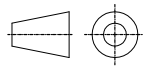
DOCUMENT NO. Z8B00003332
REVISION 07
SCALE 10:1 0 1 2 3mm
EUROPEAN PROJECTION 
ISSUE DATE 06.06.2019

Figure 1 Outline PG-TDSON-8, dimensions in mm

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PG-TDSO-8: Recommended Boardpads & Apertures

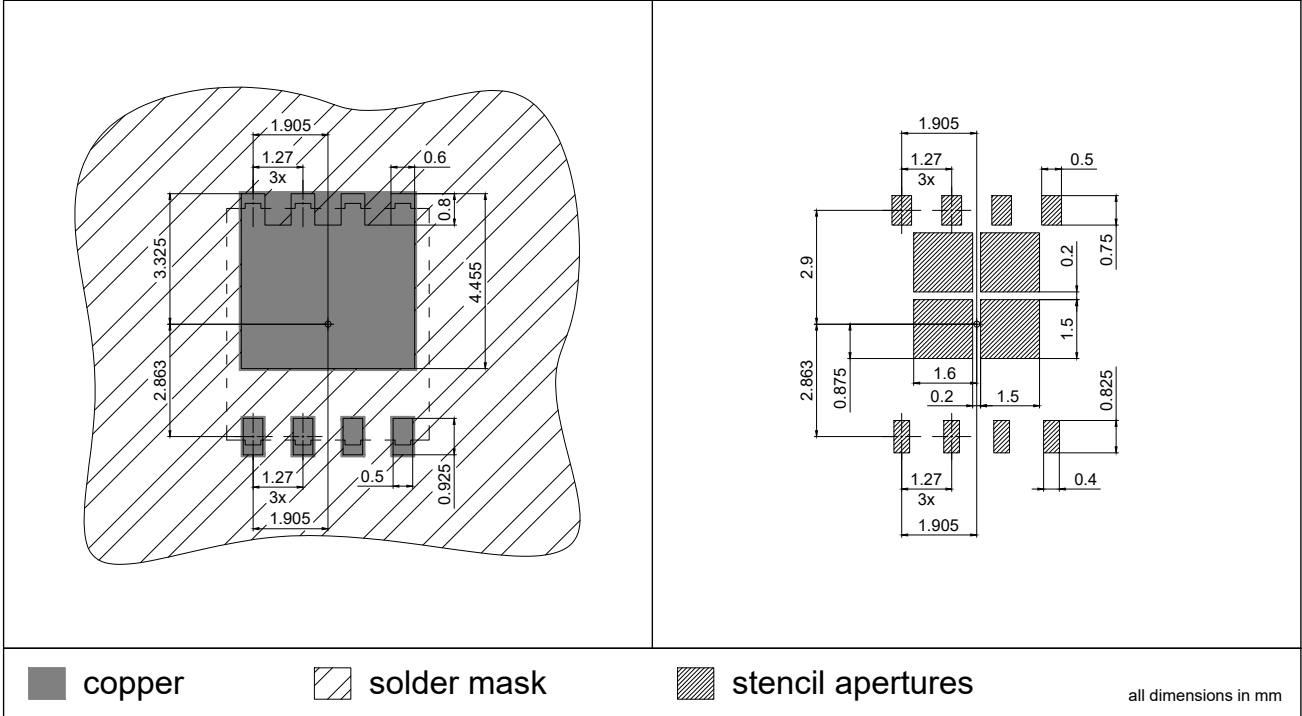
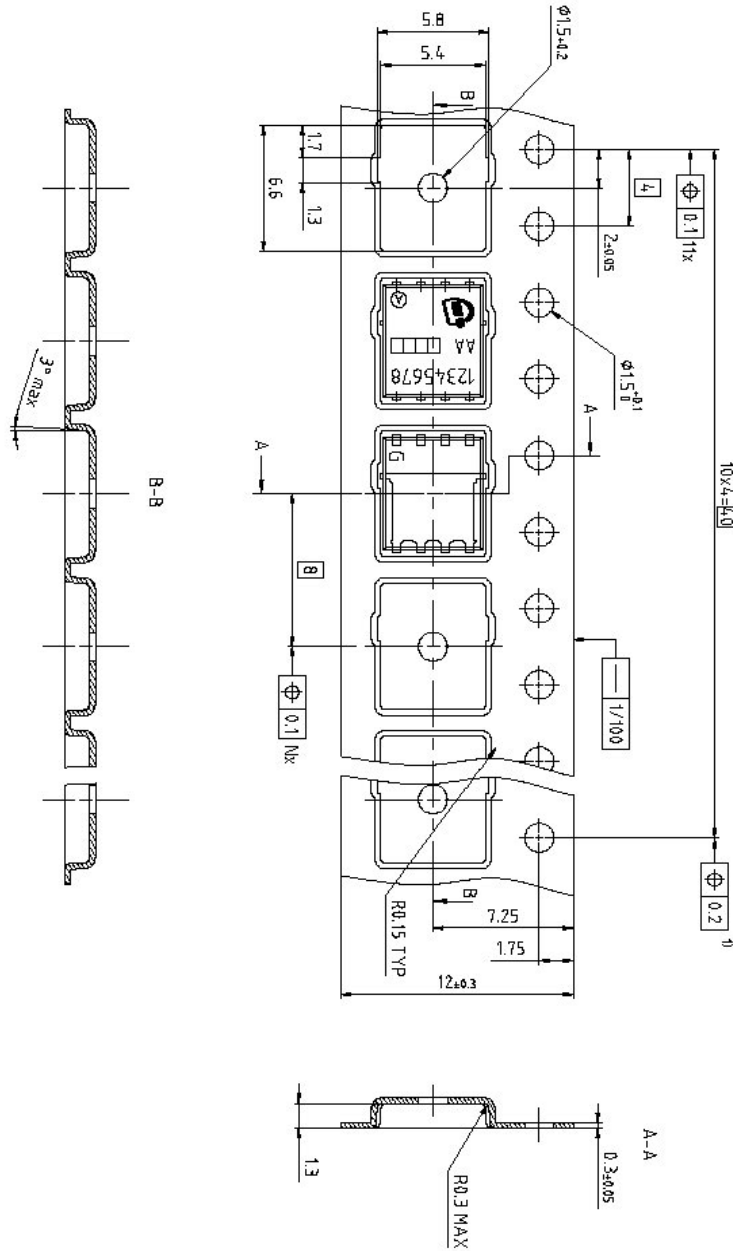


Figure 2 Outline Boardpads (TDSO-8), dimensions in mm

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Dimension in mm

Figure 3 Outline Tape (TDSON-8)



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Revision History

BSC094N06LS5

Revision: 2023-01-13, Rev. 2.2

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2016-09-23	Release of final version
2.1	2020-05-15	Update package drawings
2.2	2023-01-13	Update Marking

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