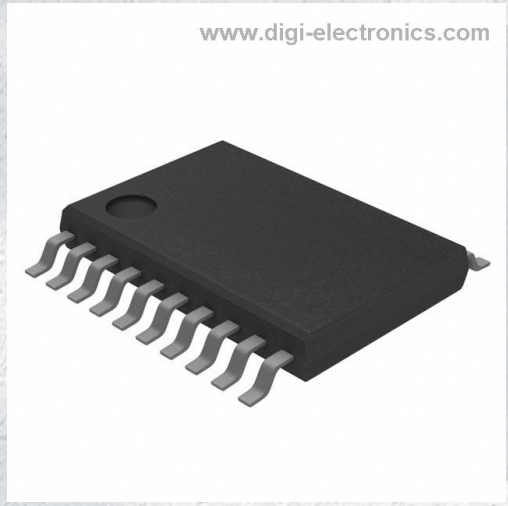
# CY25404ZXI217 Datasheet




| | |
|---|---|
| DiGi Electronics Part Number | CY25404ZXI217-DG |
| Manufacturer | Cypress Semiconductor Corp |
| Manufacturer Product Number | CY25404ZXI217 |
| Description | CLOCKS |
| Detailed Description | IC |

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## Purchase and inquiry

| Manufacturer Product Number: | Manufacturer: |
| --- | --- |
| CY25404ZXI217 | Cypress Semiconductor Corp |
| Series: | Product Status: |
| * | Active |
| DiGi-Electronics Programmable: | Base Product Number: |
| Not Verified | CY25404 |

# CY25404

# Quad PLL Programmable Clock Generator with Spread Spectrum

## Features

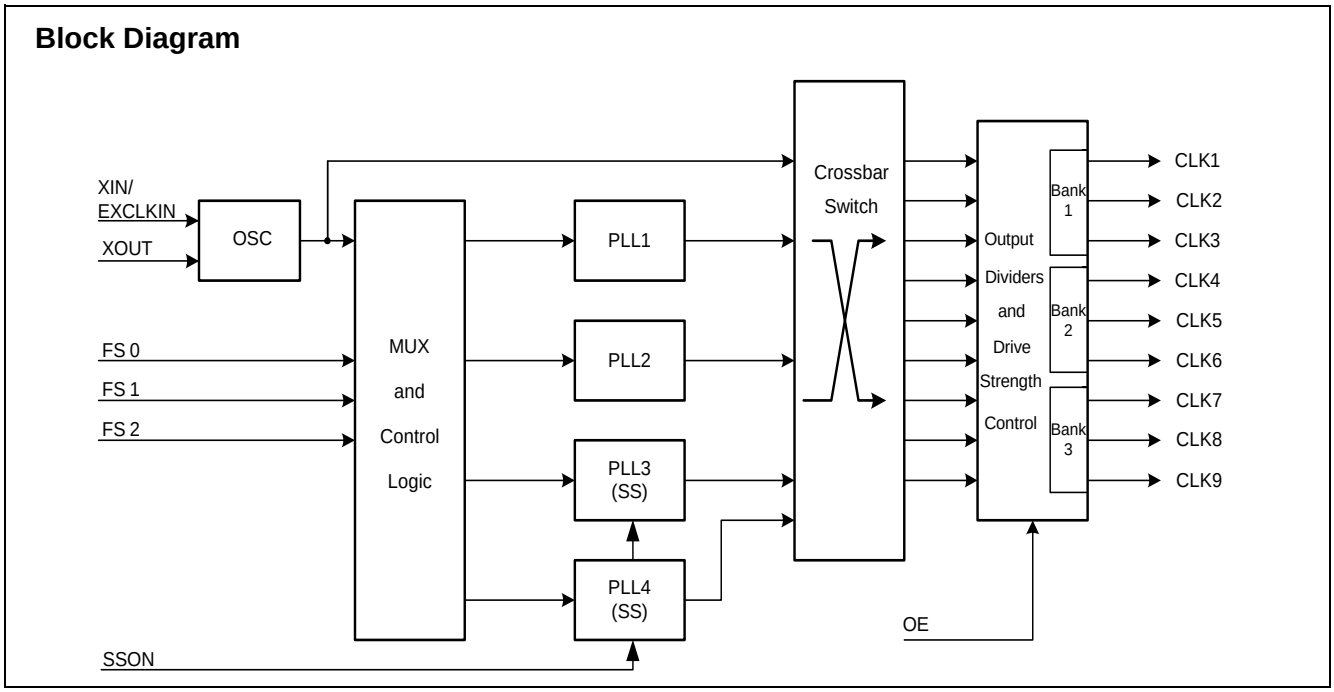
- Four fully-integrated phase-locked loops (PLLs)
- Input frequency range
  - External crystal: 8 to 48 MHz
  - External reference: 8 to 166 MHz clock
- Wide operating output frequency range
  - 3 to 166 MHz
- Programmable spread spectrum with center and down spread option and lexmark and linear modulation profiles
- Selectable $V_{DD}$ supply voltage options:
  - 2.5 V, 3.0 V, and 3.3 V
- Selectable output clock voltages, independent of $V_{DD}$ supply:
  - 1.8 V, 2.5 V, 3.0 V, and 3.3 V
- Frequency select feature with option to select eight different frequencies over nine clock outputs
- Output enable, and SS ON/OFF controls
- Low jitter, high accuracy outputs
- Ability to synthesize nonstandard frequencies with Fractional-N capability
- Up to nine clock outputs with programmable drive strength
- Glitch-free outputs while frequency switching
- 20-pin TSSOP package
- Commercial and Industrial temperature ranges
- One-time programmability
  For programming support, contact Cypress technical support or send an email to clocks@cypress.com

## Benefits

- Multiple high-performance PLLs allow synthesis of unrelated frequencies
- Nonvolatile programming for personalization of PLL frequencies, spread spectrum characteristics, drive strength, crystal load capacitance, and output frequencies
- Application specific programmable electromagnetic interference (EMI) reduction using spread spectrum for clocks
- Programmable PLLs for system frequency margin tests
- Meets critical timing requirements in complex system designs
- Suitability for PC, consumer, portable, and networking applications
- Capable of zero parts per million (PPM) frequency synthesis error
- Uninterrupted system operation during clock frequency switch
- Application compatibility in standard and low-power systems

For a complete list of related documentation, click here.

## Block Diagram



## Contents

**Figure 1. Pin Diagram - CY25404 20 LD TSSOP**

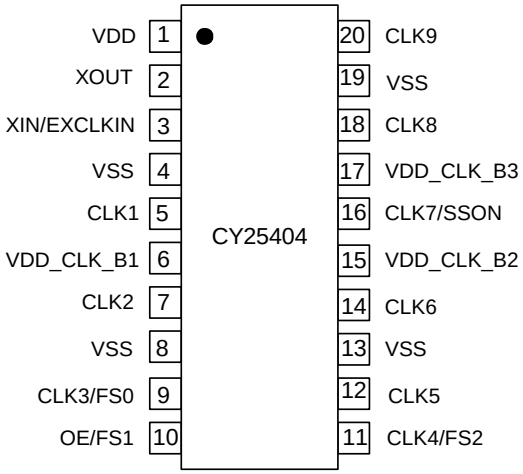



**Table 1. Pin Definition - CY25404 ($V_{DD}$ = 2.5 V, 3.0 V or 3.3 V Supply)**

| Pin Number | Name | IO | Description |
|---|---|---|---|
| 1 | $V_{DD}$ | Power | Power supply: 2.5 V/3.0 V/3.3 V |
| 2 | XOUT | Output | Crystal output |
| 3 | XIN/EXCLKIN | Input | Crystal input or 1.8 V external clock input |
| 4 | $V_{SS}$ | Power | Power supply ground |
| 5 | CLK1 | Output | Programmable clock output with spread spectrum. Output voltage depends on $V_{DD\_CLK\_B1}$ voltage |
| 6 | $V_{DD\_CLK\_B1}$ | Power | Power supply for Bank1, (CLK1, CLK2, CLK3) outputs: 1.8 V/2.5 V/3.0 V/3.3 V |
| 7 | CLK2 | Output | Programmable clock output with spread spectrum. Output voltage depends on $V_{DD\_CLK\_B1}$ voltage |
| 8 | $V_{SS}$ | Power | Power supply ground |
| 9 | CLK3/FS0 | Output/Input | Multifunction programmable pin: Programmable clock output with no spread spectrum or frequency select input pin. Output voltage of CLK3 depends on $V_{DD\_CLK\_B1}$ voltage |
| 10 | OE/FS1 | Input | Multifunction programmable pin: High-true output enable or frequency select pin |
| 11 | CLK4/FS2 | Output/Input | Multifunction programmable pin: Programmable clock output with no spread spectrum or frequency select input pin. Output voltage of CLK4 depends on $V_{DD\_CLK\_B2}$ voltage |
| 12 | CLK5 | Output | Programmable clock output with no spread spectrum. Output voltage depends on $V_{DD\_CLK\_B2}$ voltage |
| 13 | $V_{SS}$ | Power | Power supply ground |
| 14 | CLK6 | Output | Programmable clock output with spread spectrum. Output voltage depends on $V_{DD\_CLK\_B2}$ voltage |
| 15 | $V_{DD\_CLK\_B2}$ | Power | Power supply for Bank2, (CLK4, CLK5, CLK6) outputs: 1.8 V/2.5 V/3.0 V/3.3 V |
| 16 | CLK7/SSON | Output/Input | Multifunction programmable pin. Programmable clock output with spread spectrum or spread spectrum On/OFF control input pin. Output voltage of CLK7 depends on $V_{DD\_CLK\_B3}$ voltage |
| 17 | $V_{DD\_CLK\_B3}$ | Power | Power supply for Bank3, (CLK7, CLK8, CLK9) outputs: 1.8 V/2.5 V/3.0 V/3.3 V |
| 18 | CLK8 | Output | Programmable clock output with spread spectrum. Output voltage depends on $V_{DD\_CLK\_B3}$ voltage |
| 19 | $V_{SS}$ | Power | Power supply ground |
| 20 | CLK9 | Output | Programmable clock output with spread spectrum. Output voltage depends on $V_{DD\_CLK\_B3}$ voltage |

## General Description

### Four Configurable PLLs

The CY25404 has four programmable PLLs that can be used to generate output frequencies ranging from 3 to 166 MHz. The advantage of having four PLLs is that a single device generates up to four independent frequencies from a single crystal.

### Input Reference Clocks

The input to the CY25404 can be either a crystal or a clock signal. The input frequency range for crystals is 8 MHz to 48 MHz, while that for clock signals is 8 MHz to 166 MHz. The required voltage level for the input reference clock (EXCLKIN) is shown in the DC and AC Electrical Specification tables.

### $V_{DD}$ Power Supply Options

This device has programmable power supply option and it can be programmed to operate at any voltage 2.5 V, 3.0 V, or 3.3 V.

### Output Bank Settings

There are nine clock outputs grouped in three output driver banks. The Bank 1, Bank 2, and Bank 3 correspond to (CLK1, CLK2, CLK3), (CLK4, CLK5, CLK6), and (CLK7, CLK8, CLK9) respectively. Separate power supplies are used for each of these banks and they can be any of 1.8 V, 2.5 V, 3.0 V, or 3.3 V. These voltages are independent of $V_{DD}$ power supply used, giving user multiple choice of output clock voltage levels.

### Output Source Selection

These devices have programmable input sources for each of its nine clock outputs (CLK1–9). There are five available clock sources for these outputs. These clock sources are: XIN/EXCLKIN, PLL1, PLL2, PLL3, or PLL4. Output clock source selection is done using four out of five crossbar switch. Thus, any one of these five available clock sources can be arbitrarily selected for the clock outputs. This gives user a flexibility to have up to four independent clock outputs.

### Spread Spectrum Control

Two of the four PLLs (PLL3 and PLL4) have spread spectrum capability for EMI reduction in the system. The device uses a Cypress proprietary PLL and spread spectrum clock (SSC) technology to synthesize and modulate the frequency of the PLL. The spread spectrum feature can be turned on or off using a multifunction control pin (CLK7/SSON). It can be programmed to either center spread range from ±0.125% to ±2.50% or down spread range from –0.25% to –5.0% with Lexmark or Linear profile.

### Frequency Select

There are three multifunction frequency select pins (FS0, FS1 and FS2) that provide an option to select eight different sets of frequencies among each of the four PLLs. Each output has programmable output divider options.

### Glitch-Free Frequency Switch

When the frequency select pin (FS) is used to switch frequency, the outputs are glitch-free provided frequency is switched using output dividers. This feature enables uninterrupted system operation while clock frequency is being switched.

### Output Enable Mode

There is a multifunction programmable pin 10, OE/FS1 that can be programmed to operate as output enable (OE) mode. OE is a high-true input and individual clock outputs can be programmed to be sensitive to this OE pin. If activated it shuts off the output drivers, resulting in minimum power consumption for the device.

### Output Drive Strength

The DC drive strength of the individual clock output can be programmed for different values. Table 2 shows the typical rise and fall times for different drive strength settings.

**Table 2. Output Drive Strength**

| Output Drive Strength | Rise/Fall Time (ns) (Typical Value) |
|---|---|
| Low | 6.8 |
| Mid Low | 3.4 |
| Mid High | 2.0 |
| High | 1.0 |

### Generic Configuration and Custom Frequency

There is a generic set of output frequencies available from the factory that can be used for the device evaluation purposes. The device, CY25404 can be custom programmed to any desired frequencies and listed features. For customer specific programming, contact your local Cypress field application engineer (FAE) or sales representative.

### Output Driver Supply and Multi-Function Input Restriction

There are three programmable Output/Input function pins for CLK3/FS0, CLK4/FS2, and CLK7/SSON. These are configurable as clock output or select input or spread spectrum ON/OFF control input pin.

- When configured as Output, the driver supply voltage is defined by $V_{DD\_CLK\_Bx}$ and can be individually used with 1.8 V, 2.5 V, 3.0 V, or 3.3 V power supply apart from the $V_{DD}$ supply.
- When configured as Input, the input threshold level is defined by $V_{DD}$ supply while the protection diode is connected to the respective $V_{DD\_CLK\_Bx}$ power supply. Therefore, if $V_{DD\_CLK\_Bx}$ is less than $V_{DD}$ – 0.5 V, a large leakage current would flow from the input pin to the $V_{DD\_CLK\_Bx}$ supply. The device does not permit this condition; it is required that the power supply for the bank ($V_{DD\_CLK\_Bx}$) is more than $V_{DD}$ – 0.5 V.

**Example:** If $V_{DD\_CLK\_B2}$ = 1.8 V, CLK4/FS2 is configured as FS2, and $V_{DD}$ = 3.3 V, there will be a leakage current from FS2 high to $V_{DD\_CLK\_B2}$. The multi-function pin should only be used as clock output if the $V_{DD\_CLK\_Bx}$ is less than $V_{DD}$ – 0.5 V. In other words, when these multi-function programmable pins are configured as input, the power supply for the bank ($V_{DD\_CLK\_Bx}$) should be more than $V_{DD}$ – 0.5 V.

## Absolute Maximum Conditions

| Parameter | Description | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | – | –0.5 | 4.5 | V |
| $V_{DD\_CLK\_BX}$ | Output bank supply voltage | – | –0.5 | 4.5 | V |
| $V_{IN}$ | Input voltage | Relative to $V_{SS}$ | –0.5 | $V_{DD}$+0.5 | V |
| $T_S$ | Temperature, storage | Non functional | –65 | +150 | °C |
| $ESD_{HBM}$ | ESD protection (human body model) | JEDEC EIA/JESD22-A114-E | 2000 | | volts |
| UL-94 | Flammability rating | V-0 at 1/8 in. | – | 10 | ppm |
| MSL | Moisture sensitivity level | – | 3 | | |

## Recommended Operating Conditions

| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | $V_{DD}$ operating voltage | 2.25 | – | 3.60 | V |
| $V_{DD\_CLK\_BX}$ | Output driver voltage for bank 1, 2 and 3 | 1.71 | – | 3.60 | V |
| $T_{AC}$ | Commercial ambient temperature | 0 | – | +70 | °C |
| $T_{AI}$ | Industrial ambient temperature | –40 | -- | +85 | °C |
| $C_{LOAD}$ | Maximum load capacitance | – | – | 15 | pF |
| $t_{PU}$ | Power-up time for all $V_{DD}$ to reach minimum specified voltage (power ramps must be monotonic) | 0.05 | – | 500 | ms |

**Notes**
1. Guaranteed by design but not 100% tested.
2. Configuration dependent.

## DC Electrical Specifications

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 2 mA, drive strength = [00] | – | – | 0.4 | V |
| | | $I_{OL}$ = 3 mA, drive strength = [01] | | | | |
| | | $I_{OL}$ = 7 mA, drive strength = [10] | | | | |
| | | $I_{OL}$ = 12 mA, drive strength = [11] | | | | |
| $V_{OH}$ | Output high voltage | $I_{OH}$ = –2 mA, drive strength = [00] | $V_{DD\_CLK\_BX}$ – 0.4 | – | – | V |
| | | $I_{OH}$ = –3 mA, drive strength = [01] | | | | |
| | | $I_{OH}$ = –7 mA, drive strength = [10] | | | | |
| | | $I_{OH}$ = –12 mA, drive strength = [11] | | | | |
| $V_{IL1}$ | Input low voltage of FS0, OE/FS1, FS2, and SSON | – | – | – | 0.2*$V_{DD}$ | V |
| $V_{IL2}$ | Input low voltage of EXCLKIN | – | – | – | 0.18 | V |
| $V_{IH1}$ | Input high voltage of FS0, OE/FS1, FS2, and SSON | – | 0.8*$V_{DD}$ | – | – | V |
| $V_{IH2}$ | Input high voltage of EXCLKIN | – | 1.62 | – | 2.2 | V |
| $I_{IL1}$ | Input low current of OE/FS1 pin | $V_{IL}$ = 0V | – | – | 10 | µA |
| $I_{IH1}$ | Input high current of OE/FS1 pin | $V_{IH}$ = $V_{DD}$ | – | – | 10 | µA |
| $I_{IL2}$ | Input low current of SSON, FS0 and FS2 pins | $V_{IL}$ = 0V (Internal pull dn = 160k typ) | – | – | 10 | µA |
| $I_{IH2}$ | Input high current of SSON, FS0, and FS2 pins | $V_{IH}$ = $V_{DD}$ (Internal pull dn = 160k typ) | 14 | – | 36 | µA |
| $R_{DN}$ | Pull down resistor of SSON, FS0, and FS2 and off state (CLK1-CLK9) pins | Clock outputs in off-state by setting OE = Low | 100 | 160 | 250 | kΩ |
| $I_{DD}$[1,2] | Supply current for CY25404 | OE = High, No load | – | 22 | – | mA |
| $C_{IN}$[1] | Input capacitance | SSON, CLKIN, FS0, OE/FS1, and FS2 pins | – | | 7 | pF |

## AC Electrical Specifications

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $F_{IN}$ (crystal) | Crystal frequency, XIN | – | 8 | – | 48 | MHz |
| $F_{IN}$ (clock) | Input clock frequency, EXCLKIN | – | 8 | – | 166 | MHz |
| $F_{CLK}$ | Output clock frequency | $V_{DD\_CLK\_Bx}$ = 2.5 V, 3.0 V, 3.3 V | 3 | – | 166 | MHz |
| | | $V_{DD\_CLK\_Bx}$ = 1.8 V | 3 | – | 50 | MHz |
| DC1 | Output duty cycle, All clocks except Ref Out | Duty cycle is defined in Figure 3 on page 8; $t_1/t_2$, measured at 50% of $V_{DD\_CLK\_BX}$ | 45 | 50 | 55 | % |
| DC2 | Ref out duty cycle | Ref In Min 45%, Max 55% | 40 | – | 60 | % |
| $T_{RF1}$[1] | Output rise/fall time | Measured from 20% to 80% of $V_{DD\_CLK\_BX}$, as shown in Figure 4 on page 8, $C_{LOAD}$ = 15 pF, Drive strength [00] | – | 6.8 | – | ns |
| $T_{RF2}$[1] | Output rise/fall time | Measured from 20% to 80% of $V_{DD\_CLK\_BX}$, as shown in Figure 4 on page 8, $C_{LOAD}$ = 15 pF, Drive strength [01] | – | 3.4 | – | ns |
| $T_{RF3}$[1] | Output rise/fall time | Measured from 20% to 80% of $V_{DD\_CLK\_BX}$, as shown in Figure 4 on page 8, $C_{LOAD}$ = 15 pF, Drive strength [10] | – | 2.0 | – | ns |
| $T_{RF4}$[1] | Output rise/fall time | Measured from 20% to 80% of $V_{DD\_CLK\_BX}$, as shown in Figure 4 on page 8, $C_{LOAD}$ = 15 pF, Drive strength [11] | – | 1.0 | – | ns |
| $T_{CCJ}$[1,2] | Cycle-to-cycle jitter (peak) | Configuration dependent. See Table 3 | – | 100 | – | ps |
| $T_{LOCK}$[1] | PLL lock time | Measured from 90% of the applied power supply level | – | 1 | 3 | ms |

**Table 3. Configuration Example for C-C Jitter**

| Ref. Freq. (MHz) | CLK1 Output | | CLK2 Output | | CLK3 Output | | CLK4 Output | | CLK5 Output | |
|---|---|---|---|---|---|---|---|---|---|---|
| | Freq. (MHz) | C-C Jitter Typ (ps) | Freq. (MHz) | C-C Jitter Typ (ps) | Freq. (MHz) | C-C Jitter Typ (ps) | Freq. (MHz) | C-C Jitter Typ (ps) | Freq. (MHz) | C-C Jitter Typ (ps) |
| 14.3181 | 8.0 | 134 | 166 | 103 | 48 | 92 | 74.25 | 81 | Not Used | |
| 19.2 | 74.25 | 99 | 166 | 94 | 8 | 91 | 27 | 110 | 48 | 75 |
| 27 | 48 | 67 | 27 | 109 | 166 | 103 | 74.25 | 97 | Not Used | |
| 48 | 48 | 93 | 27 | 123 | 166 | 137 | 166 | 138 | 8 | 103 |

## Recommended Crystal Specification for SMD Package

| Parameter | Description | Range 1 | Range 2 | Range 3 | Unit |
|---|---|---|---|---|---|
| $F_{IN}$ | Crystal frequency | 8 – 14 | 14 – 28 | 28 – 48 | MHz |
| R1 | Maximum motional resistance (ESR) | 135 | 50 | 30 | Ω |
| CL | Parallel load capacitance (device has internal load capacitance adjustment feature) | 8 – 18 | 8 – 14 | 8 – 12 | pF |
| DL(max) | Maximum crystal drive level | 300 | 300 | 300 | µW |

## Recommended Crystal Specification for Thru-Hole Package

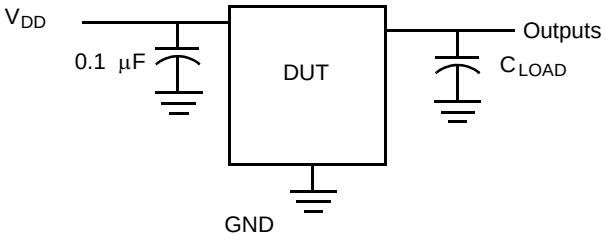
| Parameter | Description | Range 1 | Range 2 | Range 3 | Unit |
|---|---|---|---|---|---|
| $F_{IN}$ | Crystal frequency | 8 – 14 | 14 – 24 | 24 – 32 | MHz |
| R1 | Maximum motional resistance (ESR) | 90 | 50 | 30 | Ω |

## Recommended Crystal Specification for Thru-Hole Package

| Parameter | Description | Range 1 | Range 2 | Range 3 | Unit |
|---|---|---|---|---|---|
| CL | Parallel load capacitance (device has internal load capacitance adjustment feature) | 8 – 18 | 8 – 12 | 8 – 12 | pF |
| DL(max) | Maximum crystal drive level | 1000 | 1000 | 1000 | µW |

## Test and Measurement Setup

**Figure 2. Test and Measurement Setup**




## Voltage and Timing Definitions

**Figure 3. Duty Cycle Definition**

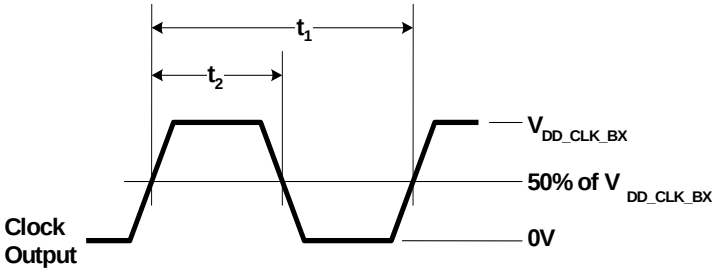
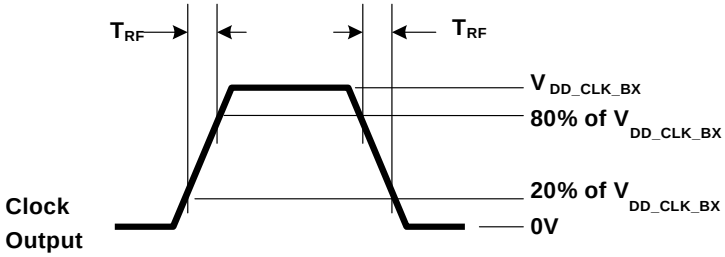



**Figure 4. Rise Time = $T_{RF}$, Fall Time = $T_{RF}$**



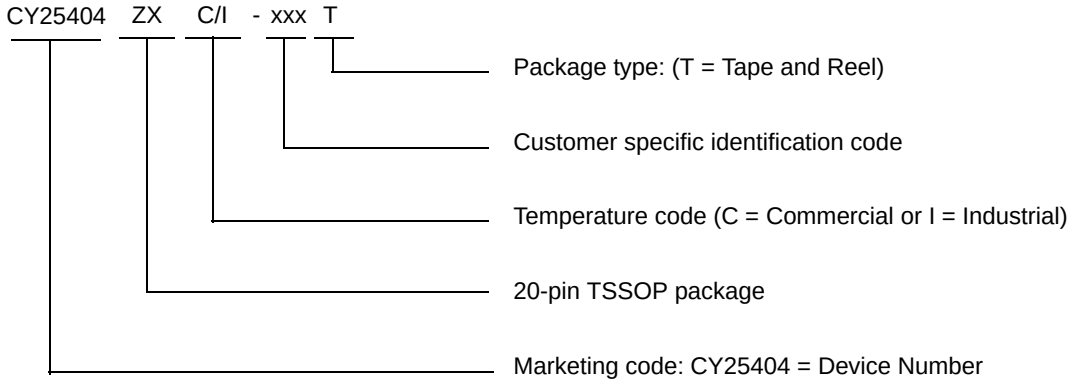
## Ordering Information

Some product offerings are factory-programmed customer-specific devices with customized part numbers. The Possible Configurations table shows the available device types, but not complete part numbers. Contact your local Cypress FAE or sales representative for more information.

### Possible Configurations

| Part Number[3] | Type | Production Flow |
|---|---|---|
| **Pb-free** | | |
| CY25404ZXC-xxx | 20-pin TSSOP | Commercial, 0 °C to 70 °C |
| CY25404ZXC-xxxT | 20-pin TSSOP -Tape and Reel | Commercial, 0 °C to 70 °C |
| CY25404ZXI-xxx | 20-pin TSSOP | Industrial, –40 °C to +85 °C |
| CY25404ZXI-xxxT | 20-pin TSSOP -Tape and Reel | Industrial, –40 °C to +85 °C |

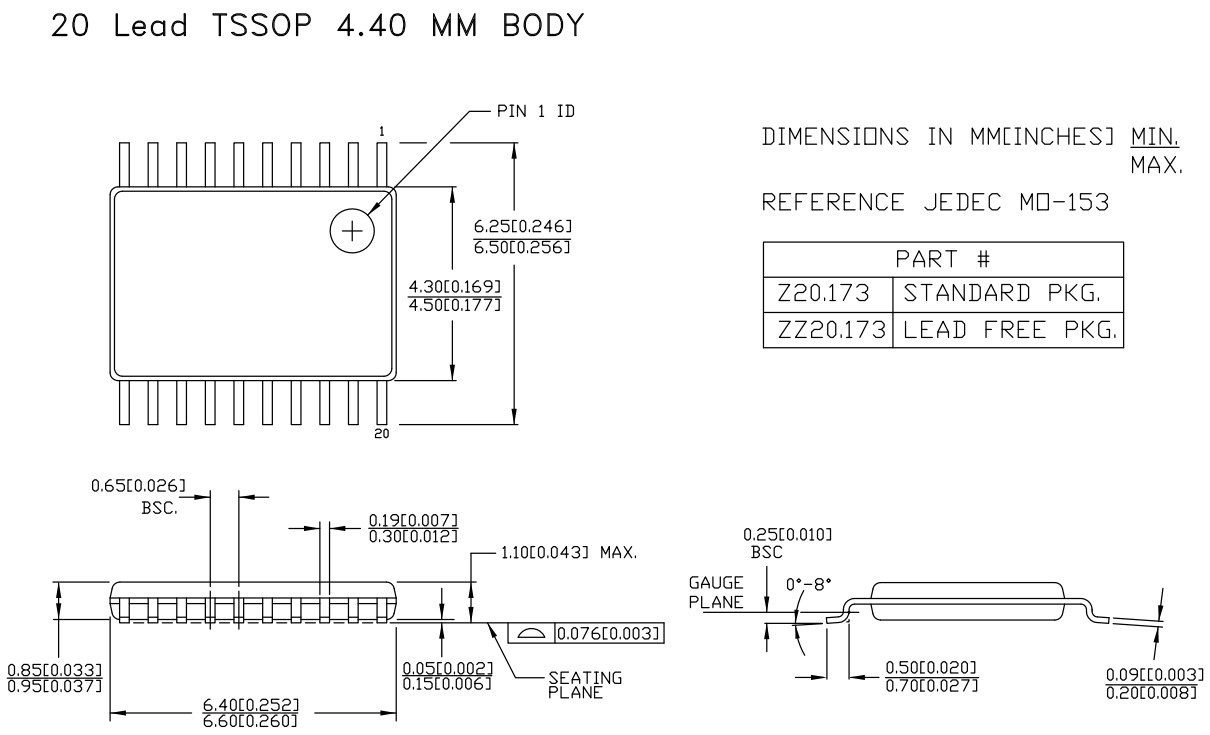
### Ordering Code Definitions




**Note**
3. xxx indicates Factory Programmable and are factory programmed configurations. For more details, contact your local Cypress FAE or sales representative.

## Package Drawing and Dimensions

**Figure 5. 20-LD TSSOP, Thin Shrunk Small Outline Package (4.40 mm Body) ZZ20**

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## Acronyms

| Acronym | Description |
|---|---|
| DL | drive level |
| EMI | electromagnetic interference |
| ESD | electrostatic discharge |
| FAE | field application engineer |
| FS | frequency select |
| JEDEC EIA | Joint Electron Devices Engineering Council Electronic Industries Alliance |
| OE | output enable |
| OSC | oscillator |
| PD | power-down |
| PLL | phase-locked loop |
| PPM | parts per million |
| SS | spread spectrum |
| SSC | spread spectrum clock |
| SSON | spread spectrum on |
| TSSOP | thin shrunk small outline package |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|---|---|
| °C | degrees Celsius |
| fF | femtofarads |
| mA | milliampere |
| MHz | megahertz |
| µs | microseconds |
| ms | millisecond |
| µW | microwatts |
| ns | nanoseconds |
| pF | picofarads |
| ppm | parts per million |
| ps | picoseconds |
| V | volts |
| Ω | ohms |
| W | watts |

## Document History Page

| Document Title: CY25404 Quad PLL Programmable Clock Generator with Spread Spectrum<br>Document Number: 001-43258 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 1793805 | See ECN | DPF/AESA | New data sheet |
| *A | 2748211 | 08/10/09 | TSAI | Posting to external web. |
| *B | 2899300 | 03/26/2010 | CXQ | Updated Ordering Information. Added note regarding Possible Configurations in Ordering Information section.<br>Added Possible Configurations table for “xxx’ parts.<br>Updated Package Drawing and Dimensions |
| *C | 3308261 | 07/11/2011 | BASH | Added Ordering Code Definitions<br>Updated Package Drawing and Dimensions<br>Added Acronyms<br>Added Units of Measure<br>Added Contents |
| *D | 4416418 | 06/30/2014 | XHT | Added 1.8V for output clock voltage in page 1: Features<br>Added 1.8V for Table 1: Pin Definition, $V_{DD\_CLK\_B1}$, $V_{DD\_CLK\_B2}$, and $V_{DD\_CLK\_B3}$<br>Added 1.8V for General Description: Output Bank Settings<br>Changed $V_{DD\_CLK\_BX}$ Min parameter from 2.25 to 1.71<br>Updated package drawing revision *D |
| *E | 4586478 | 03/12/2014 | XHT | Added related documentation hyperlink in page 1.<br>Updated package diagram 51-85118 to current revision. |
| *F | 4794092 | 06/12/2015 | XHT | Updated package revision code<br>Completed sunset review |
| *G | 5778174 | 06/19/2017 | PSR | Added one-time programmability<br>Added spread capability information for outputs<br>Changed output voltage level and added restriction. |

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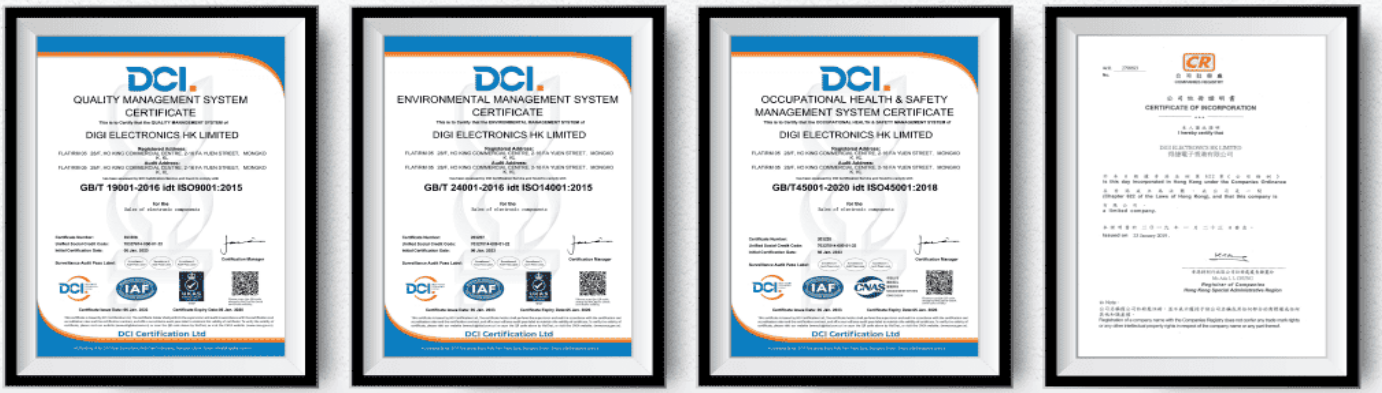



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