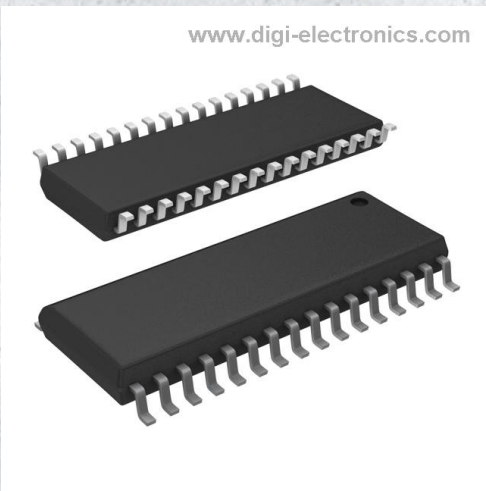
CY62148G-45SXI Datasheet



https://www.DiGi-Electronics.com

DiGi Electronics Part Number	CY62148G-45SXI-DG
Manufacturer	Infineon Technologies
Manufacturer Product Number	CY62148G-45SXI
Description	IC SRAM 4MBIT PARALLEL 32SOIC
Detailed Description	SRAM - Asynchronous Memory IC 4Mbit Parallel 45 ns 32-SOIC

This model CY62148G-45SXI is available at DiGi Electronics.

DiGi Electronics offers a global database of semiconductor and electronic component datasheets.

We welcome your inquiries regarding pricing, lead time, or other product-related questions.

Request a Quote

Datasheet Search

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
CY62148G-45SXI	Infineon Technologies
Series:	Product Status:
MoBL®	Last Time Buy
DiGi-Electronics Programmable:	Memory Type:
Not Verified	Volatile
Memory Format:	Technology:
SRAM	SRAM - Asynchronous
Memory Size:	Memory Organization:
4Mbit	512K x 8
Memory Interface:	Write Cycle Time - Word, Page:
Parallel	45ns
Access Time:	Voltage - Supply:
45 ns	4.5V ~ 5.5V
Operating Temperature:	Mounting Type:
-40°C ~ 85°C (TA)	Surface Mount
Package / Case:	Supplier Device Package:
32-SOIC (0.445", 11.30mm Width)	32-SOIC
Base Product Number:	
CY62148	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	3 (168 Hours)
REACH Status:	ECCN:
REACH Unaffected	3A991B2A
HTSUS:	
8542.32.0041	

4-MB MoBL™ ultra-low-power RAM with ECC

(512K words × 8-bit)

Features

- High speed: 45 ns/55 ns
- Ultra-low standby power
  - Typical standby current: 3.5 µA
  - Maximum standby current: 8.7 µA
- Embedded ECC for single-bit error correction[1]
- Wide voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V
- 1.0-V data retention
- TTL-compatible inputs and outputs
- Pb-free 32-pin SOIC and 32-pin TSOP II/STSOP packages

Functional description

CY62148G is a high-performance CMOS low-power (MoBL™) SRAM device with embedded ECC[1]. This device is offered multiple pin configurations.

Device is accessed by asserting the chip enable ($\overline{CE}$) input LOW. Data writes are performed by asserting the write enable ($\overline{WE}$) input LOW, while providing the data on I/O_0 through I/O_7 and address on A_0 through A_{18} pins.

Data reads are performed by asserting the output enable ($\overline{OE}$) input and providing the required address on the address lines. Read data is accessible on the I/O lines (I/O_0 through I/O_7).

All I/Os (I/O_0 through I/O_7) are placed in a HI-Z state when the device is deselected ($\overline{CE}$ HIGH or control signal $\overline{OE}$ is de-asserted).

See the **"Truth Table – CY62148G"** on page 19 for a complete description of read and write modes.

The logic block diagrams are on page 2.

Note

1. This device does not support automatic write-back on error detection.

Logic block diagram – CY62148G

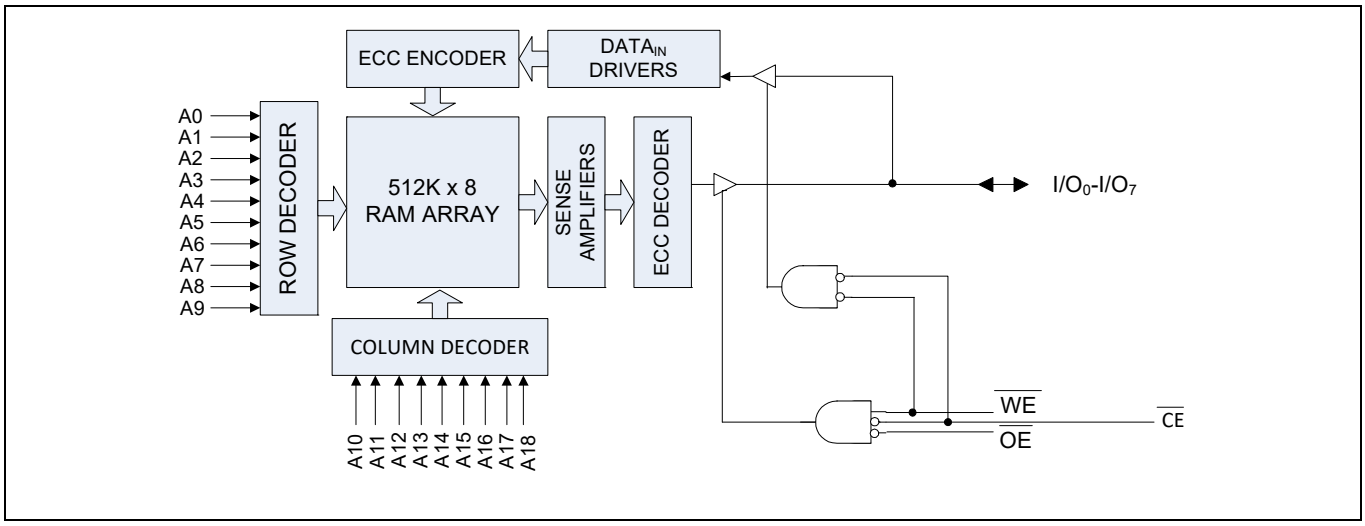


Table of contents

1 Pin configurations

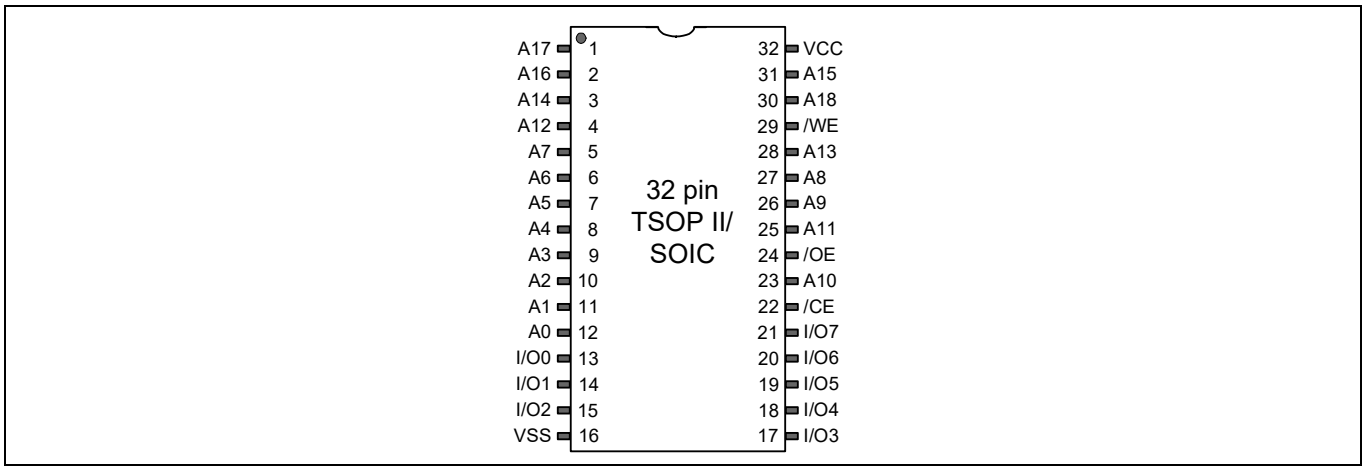


Figure 1 32-pin SOIC/TSOP II pinout

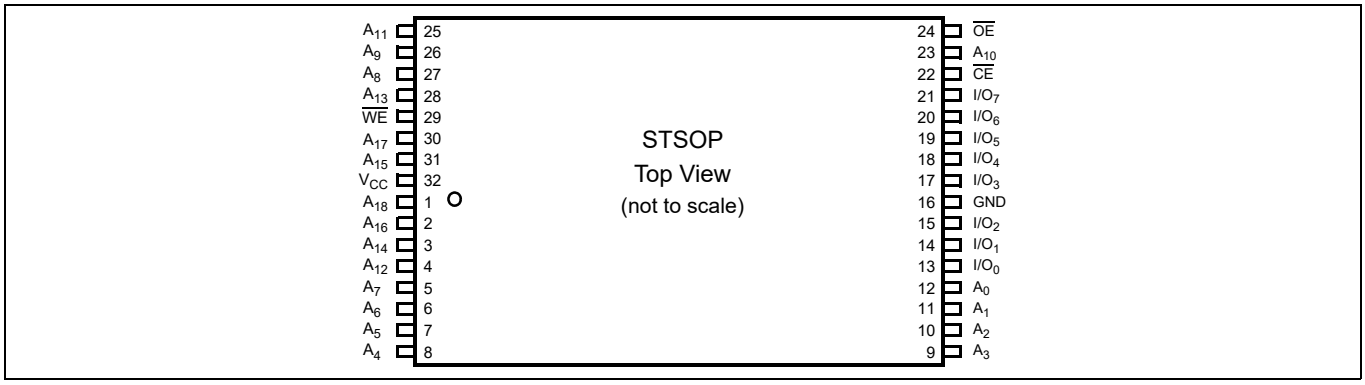


Figure 2 32-pin STSOP (Top view) pinout

2 Product portfolio

Table 1 Product portfolio

Product	Range	V_{CC} Range (V)	Speed (ns)	Power dissipation			
				Operating I_{CC} (mA)		Standby I_{SB2} (µA)	
				$f = f_{max}$			
				Typ[2]	Max	Typ[2]	Max
CY62148G18	Industrial	1.65 V–2.2 V	55	–	20	–	10
CY62148G30		2.2 V–3.6 V	45	–	20	3.5	8.7
CY62148G		4.5 V–5.5 V					

Note
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for a V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for V_{CC} range of 4.5 V–5.5 V), T_A = 25°C.

3 Maximum ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 2 Maximum ratings

Parameter	Max ratings
Storage temperature	–65°C to +150°C
Ambient temperature with power applied	–55°C to +125°C
Supply voltage to ground potential[5]	–0.5 V to V_{CC} + 0.5 V
DC voltage applied to outputs in HI-Z state[5]	–0.5 V to V_{CC} + 0.5 V
DC input voltage[5]	–0.5 V to V_{CC} + 0.5 V
Output current into outputs (in low state)	20 mA
Static discharge voltage (MIL-STD-883, Method 3015)	> 2001 V
Latch-up current	> 140 mA

4 Operating range

Table 3 Operating range

Grade	Ambient temperature	V_{CC}[3]
Industrial	–40°C to +85°C	1.65 V to 2.2 V
		2.2 V to 3.6 V
		4.5 V to 5.5 V

Note
3. Full Device AC operation assumes a 100 µs ramp time from 0 to $V_{CC(min)}$ and 200 µs wait time after V_{CC} stabilization.

5 DC electrical characteristics

Table 4 DC electrical characteristics

Over the operating range of –40°C to 85°C

Parameter	Description		Test conditions		45 ns / 55 ns			Unit
					Min	Typ	Max	
V_{OH}	Output HIGH voltage	1.65 V to 2.2 V	V_{CC} = Min, I_{OH} = –0.1 mA		1.4	–	–	V
		2.2 V to 2.7 V	V_{CC} = Min, I_{OH} = –0.1 mA		2	–	–	
		2.7 V to 3.6 V	V_{CC} = Min, I_{OH} = –1.0 mA		2.2	–	–	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OH} = –1.0 mA		2.4	–	–	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OH} = –0.1 mA		V_{CC} – 0.5[4]	–	–	
V_{OL}	Output LOW voltage	1.65 V to 2.2 V	V_{CC} = Min, I_{OL} = 0.1 mA		–	–	0.2	V
		2.2 V to 2.7 V	V_{CC} = Min, I_{OL} = 0.1 mA		–	–	0.4	
		2.7 V to 3.6 V	V_{CC} = Min, I_{OL} = 2.1 mA		–	–	0.4	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OL} = 2.1 mA		–	–	0.4	
V_{IH}	Input HIGH voltage	1.65 V to 2.2 V	–		1.4	–	V_{CC} + 0.2[5]	V
		2.2 V to 2.7 V	–		1.8	–	V_{CC} + 0.3[5]	
		2.7 V to 3.6 V	–		2	–	V_{CC} + 0.3[5]	
		4.5 V to 5.5 V	–		2.2	–	V_{CC} + 0.5[5]	
V_{IL}	Input LOW voltage	1.65 V to 2.2 V	–		–0.2[5]	–	0.4	V
		2.2 V to 2.7 V	–		–0.3[5]	–	0.6	
		2.7 V to 3.6 V	–		–0.3[5]	–	0.8	
		4.5 V to 5.5 V	–		–0.5[5]	–	0.8	
I_{IX}	Input leakage current		GND ≤ V_{IN} ≤ V_{CC}		–1	–	+1	µA
I_{OZ}	Output leakage current		GND ≤ V_{OUT} ≤ V_{CC}, Output disabled		–1	–	+1	µA
I_{CC}	V_{CC} operating supply current		Max V_{CC}, I_{OUT} = 0 mA, CMOS levels	f = 22.22 MHz (45 ns)	–	–	20	mA
				f = 18.18 MHz (55 ns)	–	–	20	mA
				f = 1 MHz	–	–	6	mA

Notes

4. This parameter is guaranteed by design and not tested.
5. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 2 V for pulse durations of less than 20 ns.

Table 4 DC electrical characteristics (continued)

Over the operating range of –40°C to 85°C

Parameter	Description	Test conditions		45 ns / 55 ns			Unit
				Min	Typ	Max	
I_{SB1} [6]	Automatic power down current – CMOS inputs; V_{CC} = 2.2 V to 3.6 V and 4.5 V to 5.5 V	$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, f = f_{max} (address and data only), f = 0 ($\overline{OE}$, and $\overline{WE}$), Max V_{CC}		–	–	8.7	µA
	Automatic power down current – CMOS inputs V_{CC} = 1.65 V to 2.2 V			–	–	10	
I_{SB2} [6]	Automatic power down current – CMOS inputs V_{CC} = 2.2 V to 3.6 V and 4.5 V to 5.5 V	$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, f = 0, Max V_{CC}	25°C [7]	–	3.5	3.7	µA
			40°C [7]	–	–	4.8	
			70°C [7]	–	–	7	
			85°C	–	–	8.7	
	Automatic power down current – CMOS inputs V_{CC} = 1.65 V to 2.2 V	$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, f = 0, Max V_{CC}	25°C [7]	–	3.5	4.3	
			40°C [7]	–	–	5	
			70°C [7]	–	–	7.5	
			85°C	–	–	10	

Notes

6. Chip enables ($\overline{CE}$ must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
7. The I_{SB2} limits at 25°C, 40°C, 70°C, and typical limit at 85°C are guaranteed by design and not 100% tested.

6 Capacitance

Table 5 Capacitance

Parameter [8]	Description	Test conditions	Max	Unit
C_{IN}	Input capacitance	$T_A = 25°C, f = 1\ MHz, V_{CC} = V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Note
8. Tested initially and after any design or process changes that may affect these parameters.

7 Thermal resistance

Table 6 Thermal resistance

Parameter [9]	Description	Test conditions	32-pin SOIC	32-pin TSOP II	32-pin STSOP	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	51.79	79.03	82.77	°C/W
Θ_{JC}	Thermal resistance (junction to case)		25.12	17.44	12.00	°C/W

Note
9. Tested initially and after any design or process changes that may affect these parameters.

8 AC test loads and waveforms

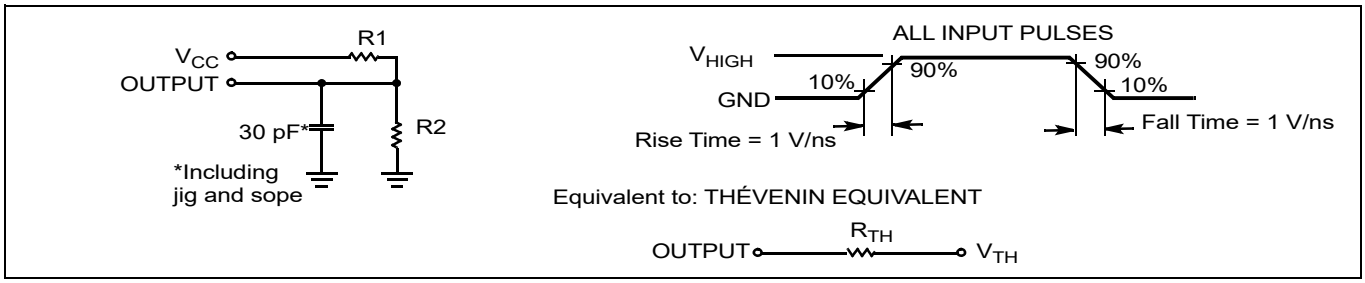


Figure 3 AC test loads and waveforms [10]

Table 7 AC test conditions

Parameters	1.8 V	2.5 V	3.0 V	5.0 V	Unit
R1	13500	16667	1103	1800	Ω
R2	10800	15385	1554	990	Ω
R_{TH}	6000	8000	645	639	Ω
V_{TH}	0.80	1.20	1.75	1.77	V

Note
10.Full-device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100\,\mu s$ or stable at $V_{CC(min)} \geq 100\,\mu s$.

9 Data retention characteristics

Table 8 Data retention characteristics

Over the Operating range

Parameter	Description	Conditions	Min	Typ [11]	Max	Unit
V_{DR}	V_{CC} for data retention		1	–	–	V
I_{CCDR} [12, 13]	Data retention current	V_{CC} = 1.2 V, $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	–	13	µA
t_{CDR} [14, 15]	Chip deselect to data retention time		0	–	–	ns
t_R [15]	Operation recovery time		45/55	–	–	ns

Notes

11. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = 1.8 V (for V_{CC} range of 1.65 V–2.2 V), V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V), and V_{CC} = 5 V (for V_{CC} range of 4.5 V–5.5 V), T_A = 25°C.
12. Chip enables $\overline{CE}$ must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
13. I_{CCDR} is guaranteed only after device is first powered up to $V_{CC(min)}$ and then brought down to V_{DR}.
14. These parameters are guaranteed by design.
15. Full-device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.

10 Data retention waveform

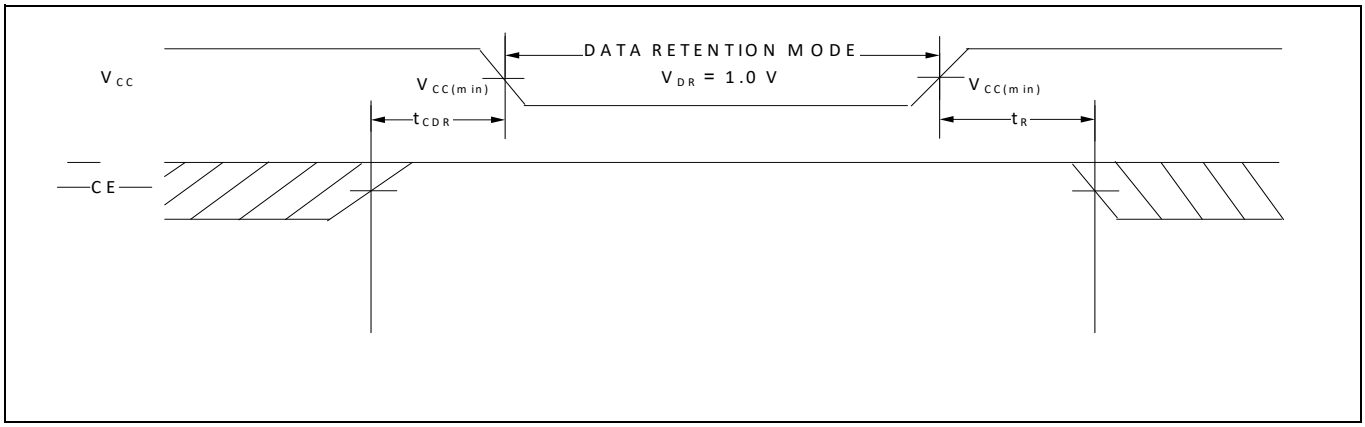


Figure 4 Data retention waveform

11 AC switching characteristics

Table 9 AC switching characteristics

Parameter [16, 17]	Description	45 ns		55 ns		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	45	–	55	–	ns
t_{AA}	Address to data valid	–	45	–	55	ns
t_{OHA}	Data hold from address change	10	–	10	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	45	–	55	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	–	25	ns
t_{LZOE}	$\overline{OE}$ LOW to Low impedance[18]	5	–	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to HI-Z[18, 19]	–	18	–	18	ns
t_{LZCE}	$\overline{CE}$ LOW to Low impedance[18]	10	–	10	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to HI-Z[18, 19]	–	18	–	18	ns
t_{PU}	$\overline{CE}$ LOW to power-up	0	–	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-down	–	45	–	55	ns
Write Cycle [20, 21]						
t_{WC}	Write cycle time	45	–	55	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	35	–	45	–	ns
t_{AW}	Address setup to write end	35	–	45	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	40	–	ns
t_{SD}	Data setup to write end	25	–	25	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to HI-Z[18, 19]	–	18	–	20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low impedance[18]	10	–	10	–	ns

Notes

16. Test conditions assume a signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to V_{CC} (for $V_{CC} < 3$ V). Test conditions for the read cycle use output loading shown in **"AC test loads and waveforms"** on page 12, unless specified otherwise.
17. These parameters are guaranteed by design.
18. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
19. t_{HZOE}, t_{HZCE} and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
20. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
21. The minimum pulse width in Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to sum of t_{SD} and t_{HZWE}.

12 Switching waveforms

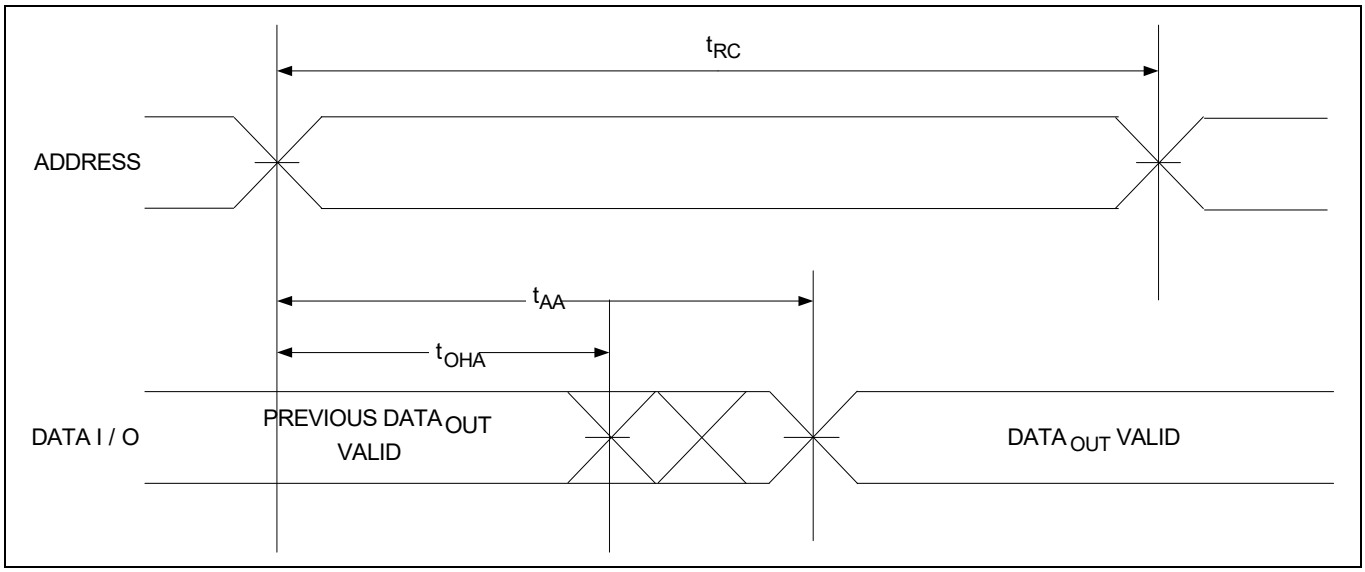


Figure 5 Read Cycle No. 1 (Address Transition Controlled) [22, 23]

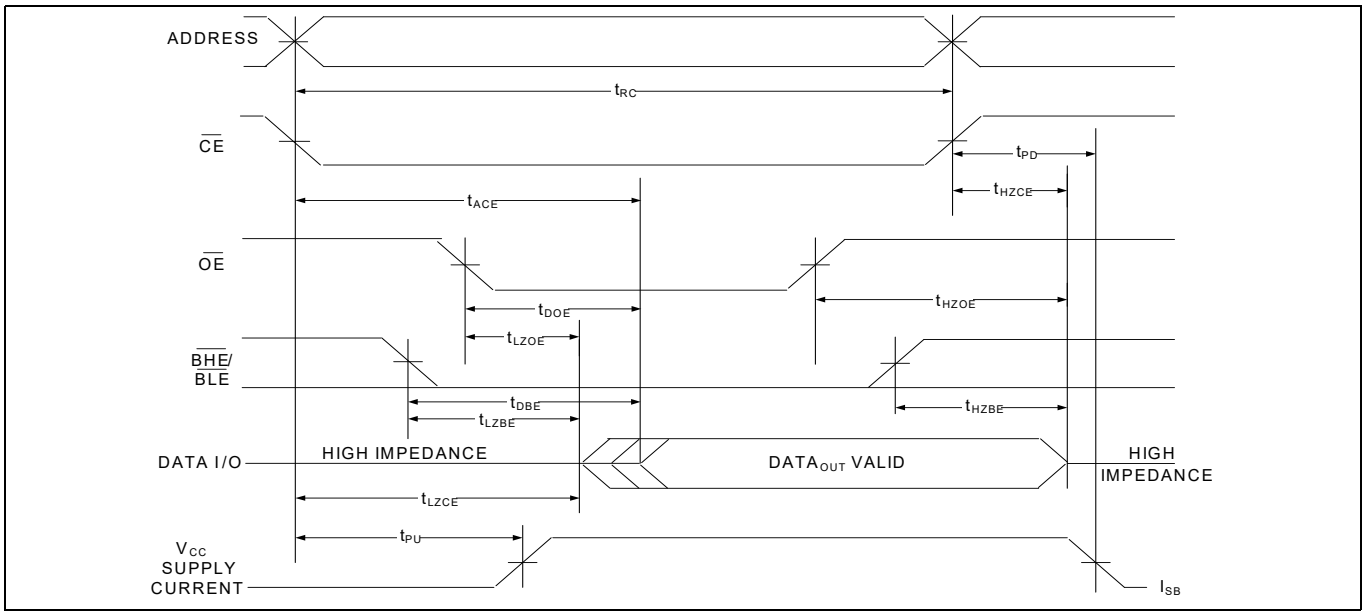


Figure 6 Read Cycle No. 2 (OE Controlled) [23, 24]

Notes
22. The device is continuously selected. $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IL}$.
23. $\overline{WE}$ is HIGH for Read cycle.
24. Address valid prior to or coincident with $\overline{CE}$ LOW transition.

4-MB MoBL™ ultra-low-power RAM with ECC
(512K words × 8-bit)

Switching waveforms

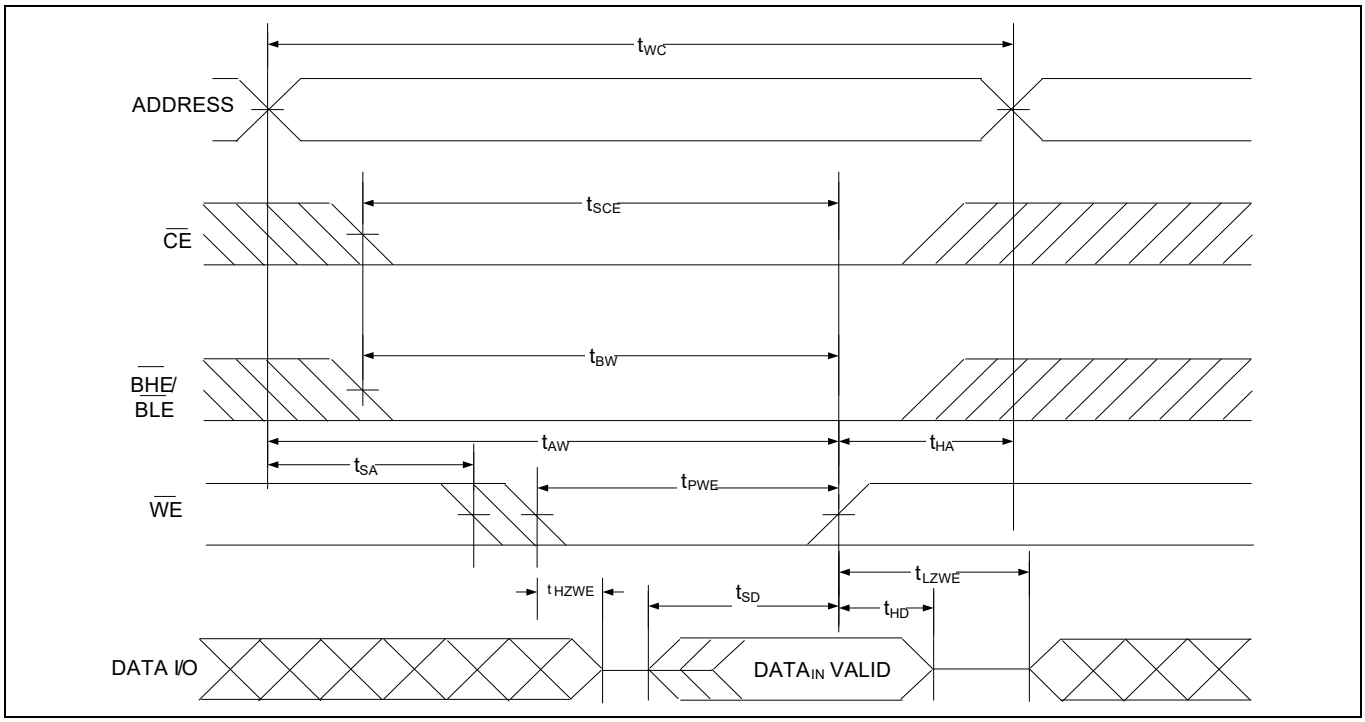


Figure 7 Write Cycle No. 1 (WE Controlled) [25, 26, 27]

Notes

25. WE is HIGH for Read cycle.
26. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$, All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
27. Data I/O is in a HI-Z state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$.

Switching waveforms

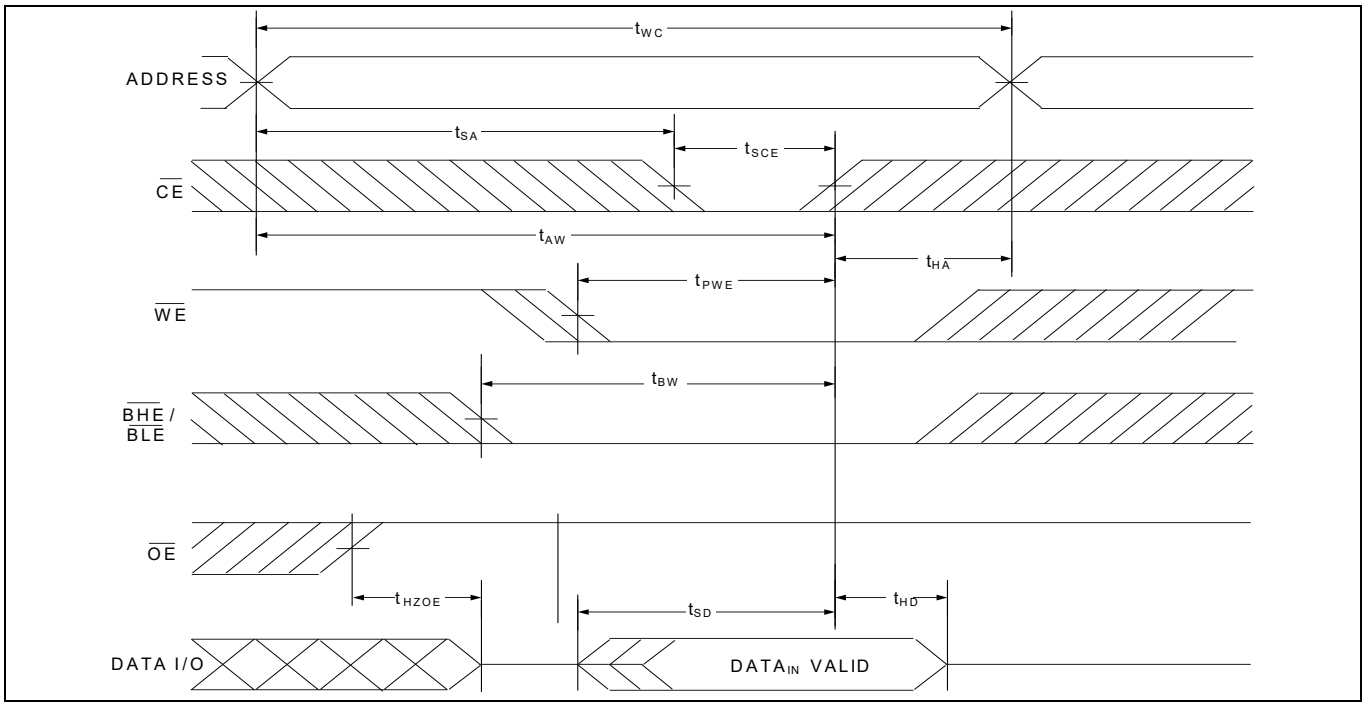


Figure 8 Write Cycle No. 2 ($\overline{CE}$ Controlled) [28, 29]

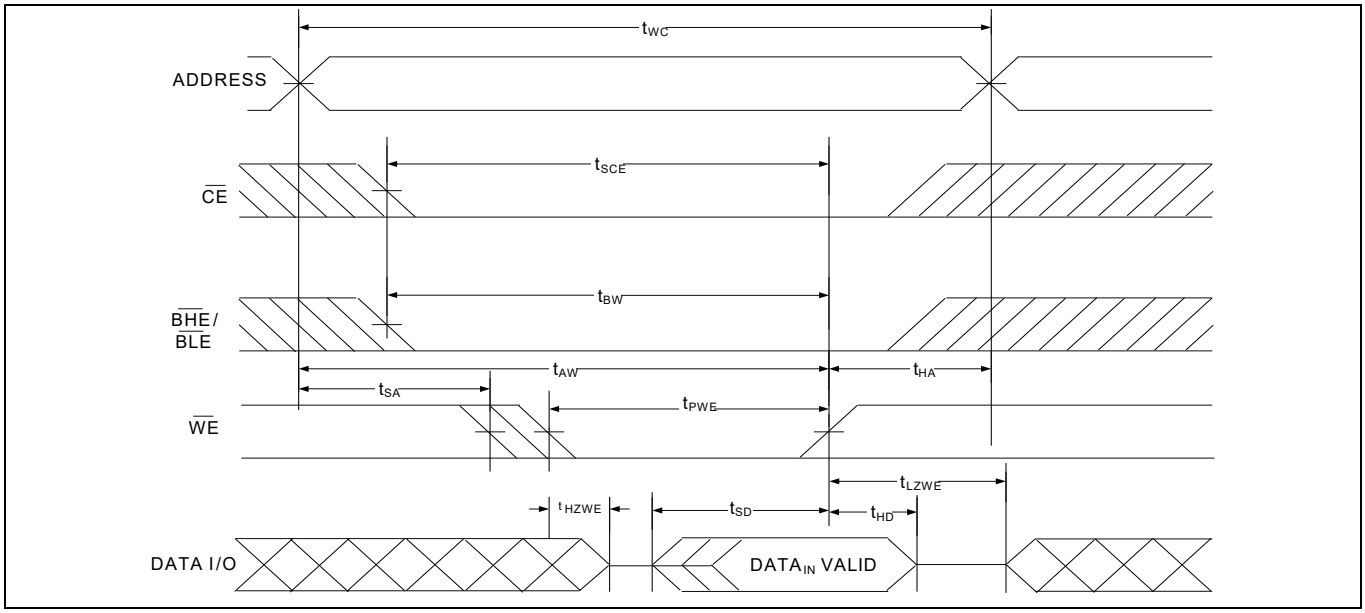


Figure 9 Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [28, 29, 30]

Notes

28. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$, All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
29. Data I/O is in HI-Z state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$
30. The minimum write pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be sum of t_{HZWE} and t_{SD}.

13 Truth Table – CY62148G

Table 10 Truth Table – CY62148G

CE	WE	OE	Inputs/Outputs	Mode	Power	Configuration
H	X[31]	X[31]	HI-Z	Deselect/Power-down	Standby (I_{SB})	512K × 8
L	H	L	Data Out (I/O_0–I/O_7)	Read	Active (I_{CC})	512K × 8
L	H	H	HI-Z	Output disabled	Active (I_{CC})	512K × 8
L	L	X[31]	Data In (I/O_0–I/O_7)	Write	Active (I_{CC})	512K × 8

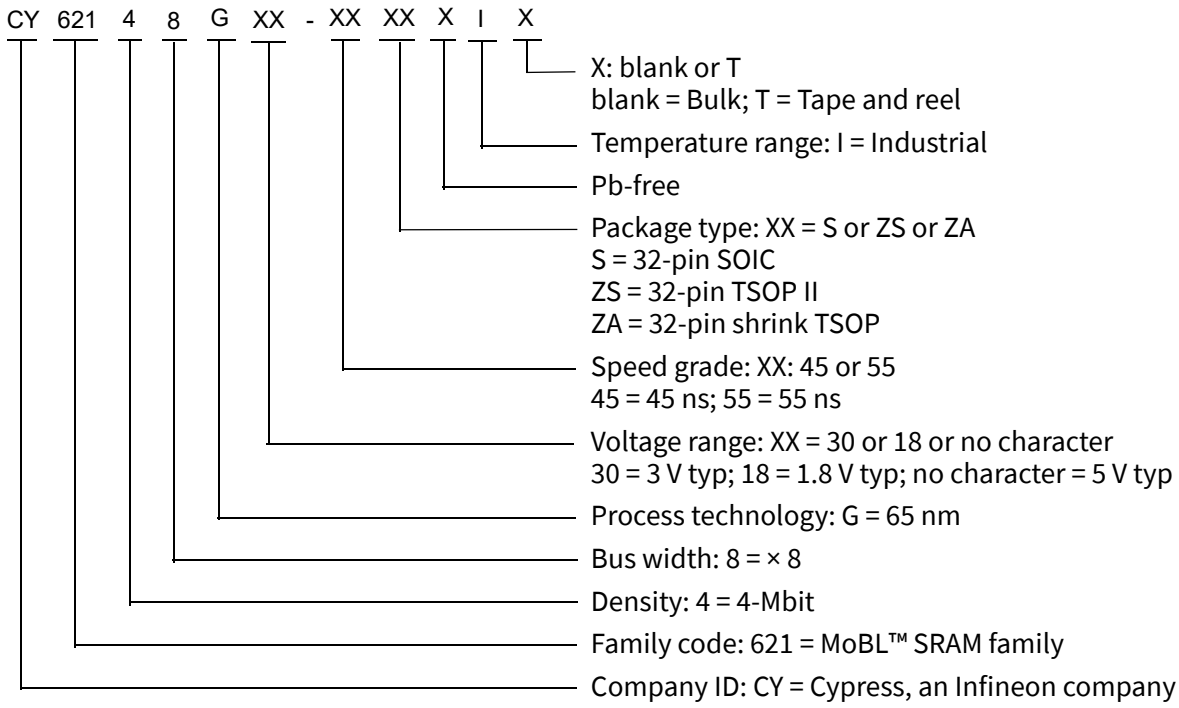
Note
31. The 'X' (Don't care) state for the chip enables refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

14 Ordering information

Table 11 Ordering information

Speed (ns)	Voltage range	Ordering code	Package diagram	Package type	Operating range
45	2.2 V–3.6 V	CY62148G30-45SXI	51-85081	32-pin SOIC (450 Mils)	Industrial
		CY62148G30-45SXIT	51-85081	32-pin SOIC (450 Mils), tape and reel	
		CY62148G30-45ZSXI	51-85095	32-pin TSOP II	
		CY62148G30-45ZSXIT	51-85095	32-pin TSOP II, tape and reel	
		CY62148G30-45ZAXI	001-91156	32-pin shrink TSOP	
		CY62148G30-45ZAXIT	001-91156	32-pin shrink TSOP, tape and reel	
	4.5 V–5.5 V	CY62148G-45SXI	51-85081	32-pin SOIC (450 Mils)	
		CY62148G-45SXIT	51-85081	32-pin SOIC (450 Mils), tape and reel	
		CY62148G-45ZSXI	51-85095	32-pin TSOP II	
		CY62148G-45ZSXIT	51-85095	32-pin TSOP II, tape and reel	
55	1.65 V–2.2 V	CY62148G18-55ZSXI	51-85095	32-pin TSOP II	
		CY62148G18-55ZSXIT	51-85095	32-pin TSOP II, tape and reel	

14.1 Ordering code definitions



15 Package diagrams

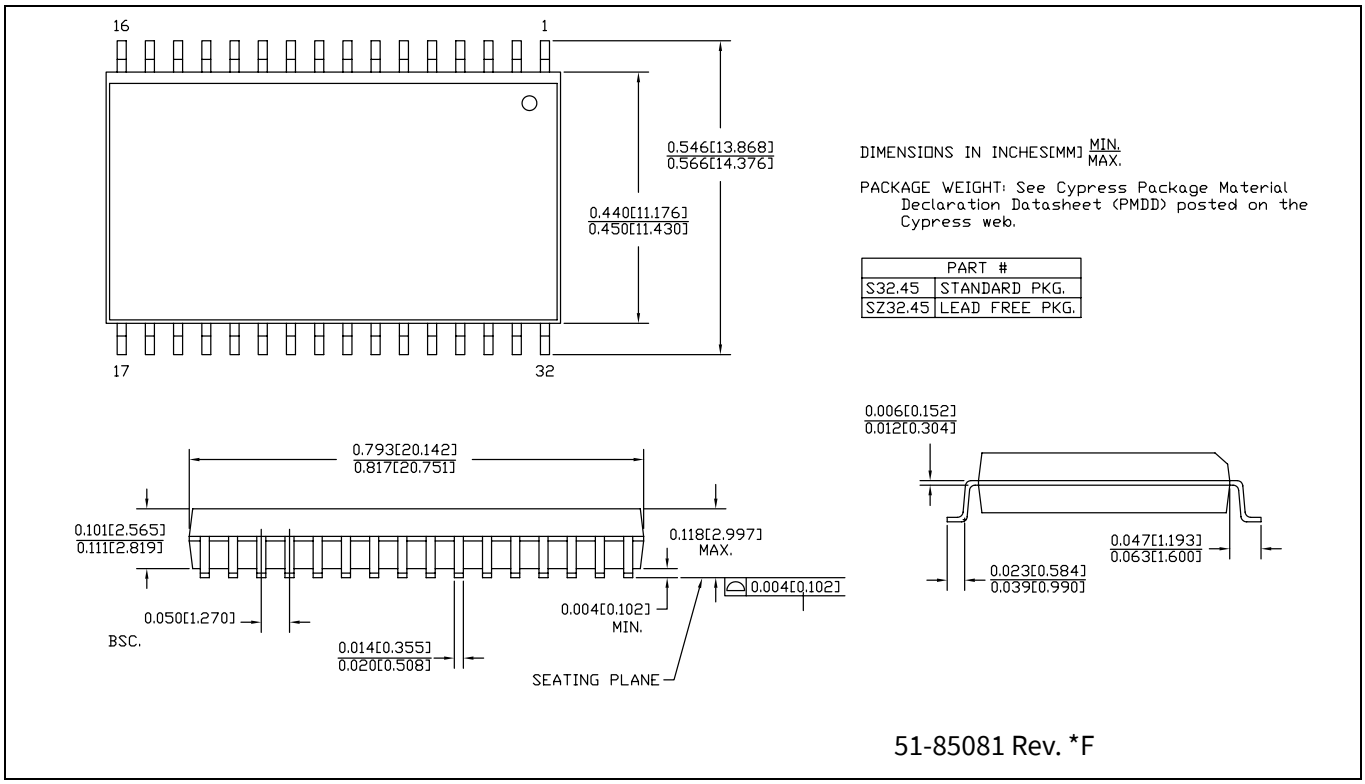


Figure 10 32-pin SOIC (450 Mils) S32.45/SZ32.45 package outline (PG-DSO-32), 51-85081

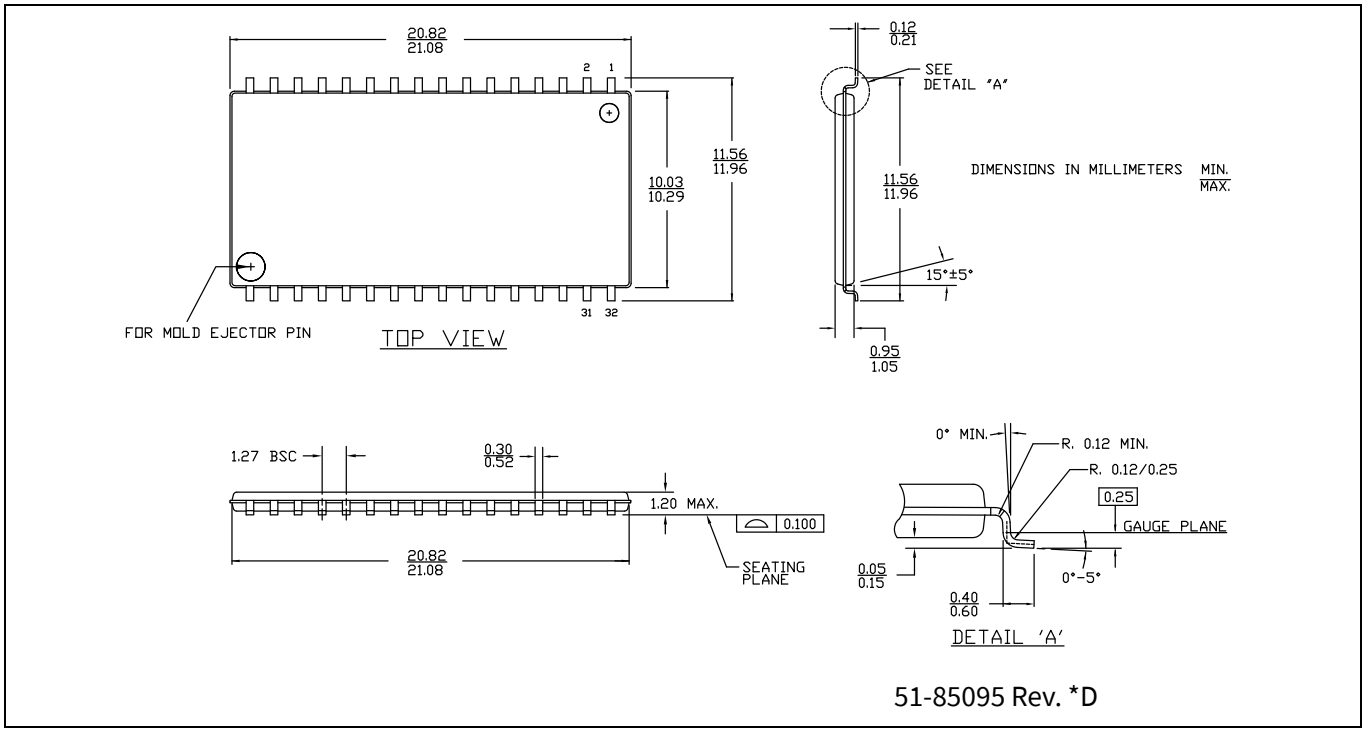


Figure 11 32-pin TSOP II (20.95 × 11.76 × 1.0 mm) ZS32 package outline (PG-TSOP-32), 51-85095

4-MB MoBL™ ultra-low-power RAM with ECC
(512K words × 8-bit)

Package diagrams

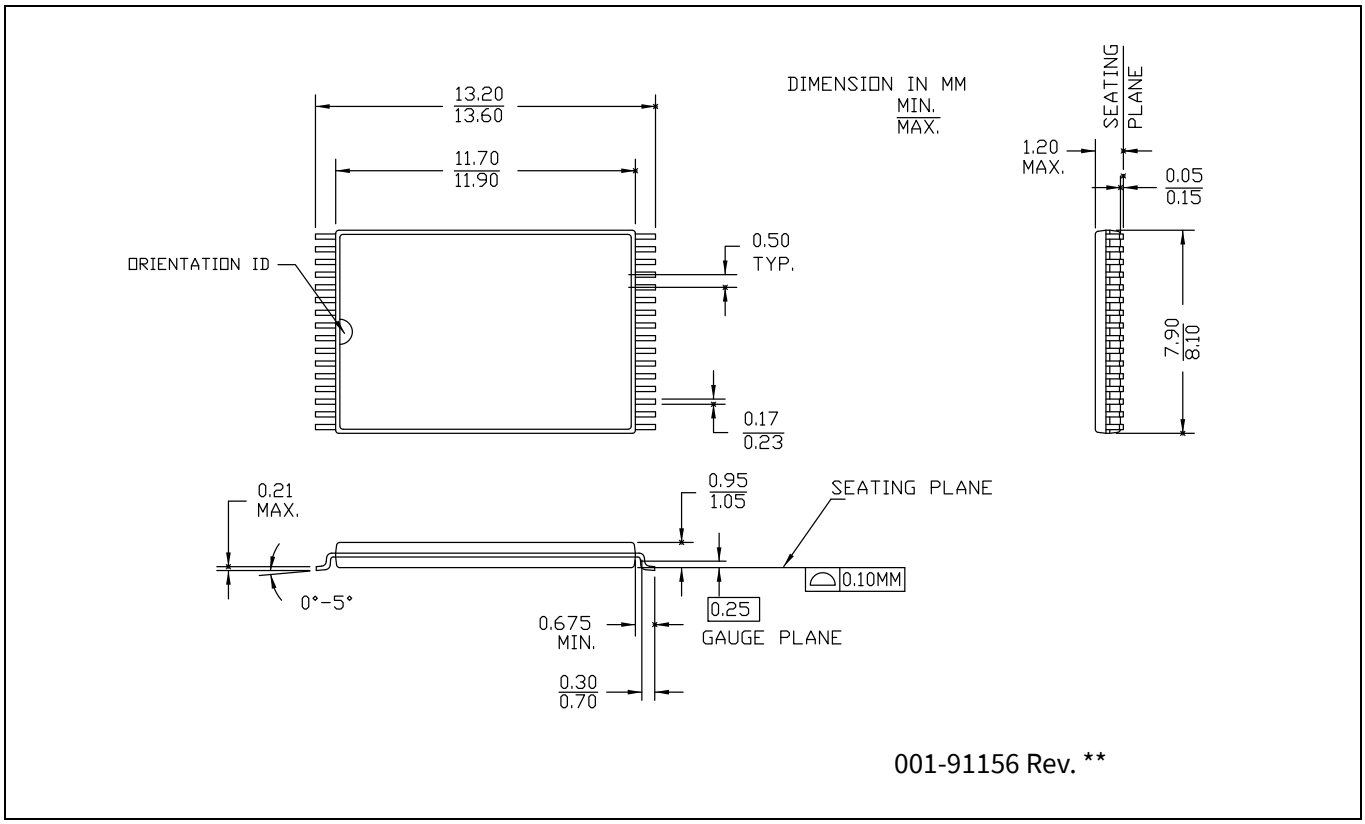


Figure 12 32-pin shrink TSOP (8 × 13.4 × 1.2 mm) ZB32F package outline (PG-TSOP-32), 001-91156

16 Acronyms

Table 12 Acronyms

Acronym	Description
$\overline{CE}$	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
$\overline{OE}$	output enable
SRAM	static random access memory
STSOP	shrink thin small outline package
TSOP	thin small outline package
VFBGA	very fine-pitch ball grid array
$\overline{WE}$	write enable

17 Document conventions

17.1 Units of measure

Table 13 Units of measure

Symbol	Unit of measure
°C	degree Celsius
MHz	megahertz
µA	microamperes
µs	microseconds
mA	milliamperes
mm	millimeters
ns	nanoseconds
Ω	ohms
%	percent
pF	picofarads
V	volts
W	watts

Revision history

Document revision	Date	Description of changes
*B	2015-12-17	Changed status from Preliminary to Final. Post to external web.
*C	2016-01-12	Updated **Ordering information**: Updated **Table 11** (Updated part numbers). Completing Sunset Review.
*D	2016-09-10	Updated **Maximum ratings**: Updated Note 5 (Replaced “2 ns” with “20 ns”). Updated **DC electrical characteristics**: Updated **Table 4**: Changed minimum value of V_{IH} parameter from 2.0 V to 1.8 V corresponding to Operating Range “2.2 V to 2.7 V”. Updated **Ordering information**: Updated **Table 11** (Updated part numbers). Updated to new template.
*E	2017-12-01	Updated Cypress Logo and Copyright.
*F	2023-09-14	Updated Document Title to read as “CY62148G, 4-MB MoBL™ ultra-low-power RAM with ECC (512K words × 8-bit)”. Added 32-pin STSOP package related information in all instances across the document. Updated **Ordering information**: Updated **Table 11** (Updated part numbers). Updated **Ordering code definitions**. Updated **Package diagrams**: spec 51-85081 – Changed revision from *E to *F. Added spec 001-91156 Rev. **. Migrated to Infineon template.

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2023-09-14
Published by

Infineon Technologies AG
81726 Munich, Germany

Do you have a question about this document?
Email:
erratum@infineon.com

Document reference
001-95415 Rev. *F

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics (“Beschaffenheitsgarantie”).

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer’s compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer’s products and any use of the product of Infineon Technologies in customer’s applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer’s technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies’ products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.

OUR CERTIFICATE

DiGi provide top-quality products and perfect service for customer worldwide through standardization, technological innovation and continuous improvement. DiGi through third-party certification, we striciy control the quality of products and services. Welcome your RFQ to Email: Info@DiGi-Electronics.com

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.