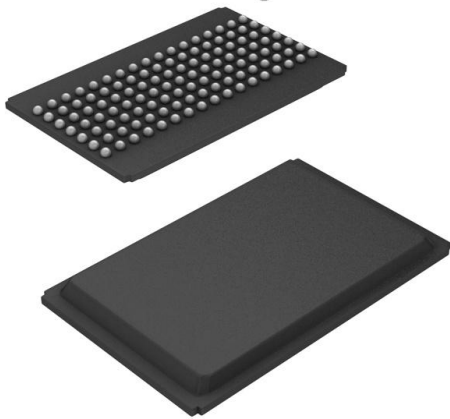


# CY62162G18-55BGXI Datasheet

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DiGi Electronics Part Number	CY62162G18-55BGXI-DG
Manufacturer	<a href="#">Infineon Technologies</a>
Manufacturer Product Number	CY62162G18-55BGXI
Description	IC SRAM 16MBIT PARALLEL 119PBGA
Detailed Description	SRAM - Asynchronous Memory IC 16Mbit Parallel 55 ns 119-PBGA (14x22)

This model CY62162G18-55BGXI is available at DiGi Electronics.

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## Purchase and inquiry

Manufacturer Product Number:

CY62162G18-55BGXI

Series:

MoBL®

DiGi-Electronics Programmable:

Not Verified

Memory Format:

SRAM

Memory Size:

16Mbit

Memory Interface:

Parallel

Access Time:

55 ns

Operating Temperature:

-40°C ~ 85°C (TA)

Package / Case:

119-BGA

Base Product Number:

CY62162

Manufacturer:

Infineon Technologies

Product Status:

Active

Memory Type:

Volatile

Technology:

SRAM - Asynchronous

Memory Organization:

512K x 32

Write Cycle Time - Word, Page:

55ns

Voltage - Supply:

1.65V ~ 2.2V

Mounting Type:

Surface Mount

Supplier Device Package:

119-PBGA (14x22)

## Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.32.0041

Moisture Sensitivity Level (MSL):

3 (168 Hours)

ECCN:

3A991B2A



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**Continuity of ordering part numbers**

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## CY62162G/CY62162GE MoBL

16-Mbit (512K × 32) Static RAM  
with Error-Correcting Code (ECC)

## Features

- Ultra-low standby power
  - Typical standby current: 5.5  $\mu$ A
  - Maximum standby current: 16  $\mu$ A
- High speed: 45 ns/55 ns
- Embedded error-correcting code (ECC) for single-bit error correction
- Wide voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V
- 1.0-V data retention
- Transistor-transistor logic (TTL) compatible inputs and outputs
- ERR pin to indicate 1-bit error detection and correction
- Easy memory expansion with  $\overline{CE}_1$  and  $CE_2$  features
- Available in Pb-free 119-ball PBGA package, 512K × 32 bits SRAM

## Functional Description

The CY62162G and CY62162GE devices are high performance CMOS MoBL SRAM organized as 512K words by 32-bits. Both CY62162G and CY62162GE are available with dual chip enables. CY62162GE includes an error indication pin that signals the host processor in the case of a single bit error-detection and correction event. It is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down

feature that reduces power consumption when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99% when deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW or  $\overline{B}_{A-D}$  HIGH). The input and output pins ( $I/O_0$  through  $I/O_{31}$ ) are placed in a high impedance state when deselected ( $\overline{CE}_1$  HIGH or  $CE_2$  LOW) or outputs are disabled ( $\overline{OE}$  HIGH) or the byte selects are disabled ( $\overline{B}_{A-D}$  HIGH).

To write to the device, take chip enables ( $\overline{CE}_1$  LOW,  $CE_2$  HIGH) and write enable ( $\overline{WE}$ ) input LOW. If byte enable A ( $\overline{B}_A$ ) is LOW, then data from I/O pins ( $I/O_0$  through  $I/O_7$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{18}$ ). If byte enable B ( $\overline{B}_B$ ) is LOW, then data from I/O pins ( $I/O_8$  through  $I/O_{15}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{18}$ ). Likewise,  $\overline{B}_C$  and  $\overline{B}_D$  correspond with the I/O pins  $I/O_{16}$  to  $I/O_{23}$  and  $I/O_{24}$  to  $I/O_{31}$ , respectively.

To read from the device, take chip enables ( $\overline{CE}_1$  LOW,  $CE_2$  HIGH), and output enable ( $\overline{OE}$ ) LOW while forcing the write enable ( $\overline{WE}$ ) HIGH. If the first byte enable ( $\overline{B}_A$ ) is LOW, then data from the memory location specified by the address pins appear on  $I/O_0$  to  $I/O_7$ . If byte enable ( $\overline{B}_B$ ) is LOW, then data from memory appears on  $I/O_8$  to  $I/O_{15}$ . Likewise,  $\overline{B}_C$  and  $\overline{B}_D$  correspond to the third and fourth bytes. During Read operation, in case of a single bit error detection and correction, ERR is asserted HIGH<sup>[1]</sup>. See the [Truth Table – CY62162G/CY62162GE](#) on page 14 for a complete description of read and write modes.

CY62162G and CY62162GE devices are available in a 119-ball PBGA package with center power and ground pinout.

## Product Portfolio

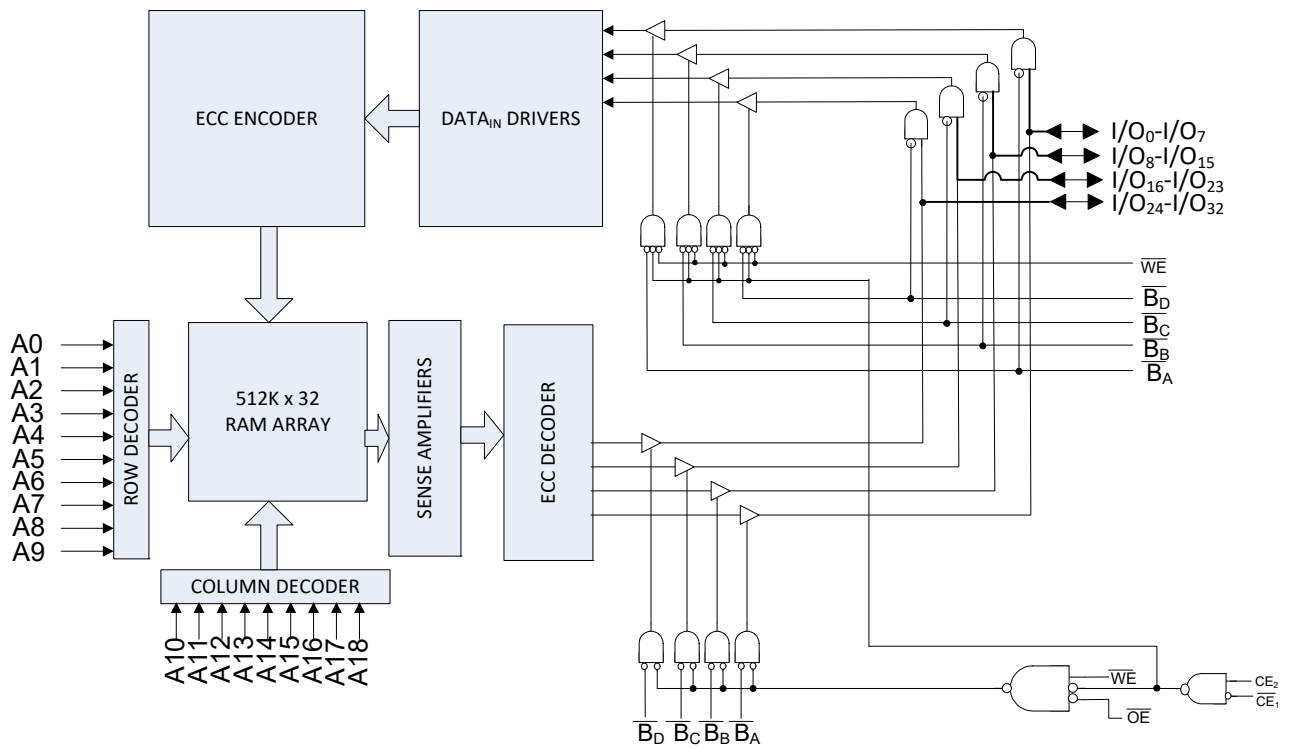
Product	Features and Options (see the Pin Configurations Section)	Range	$V_{CC}$ Range (V)	Speed (ns)	Power Dissipation			
					Operating $I_{CC}$ , (mA)		Standby, $I_{SB2}$ ( $\mu$ A)	
					$f = f_{max}$			
					Typ <sup>[2]</sup>	Max	Typ <sup>[2]</sup>	Max
CY62162G(E)18	Dual Chip Enable Optional Error indication on ERR pinout	Industrial	1.65 V–2.2 V	55	29	32	7	26
CY62162G(E)30			2.2 V–3.6 V	45	29	36	5.5	16

### Notes

1. This device does not support automatic write-back on error detection.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = 1.8$  V (for  $V_{CC}$  range of 1.65 V–2.2 V),  $V_{CC} = 3$  V (for  $V_{CC}$  range of 2.2 V–3.6 V),  $T_A = 25$  °C.

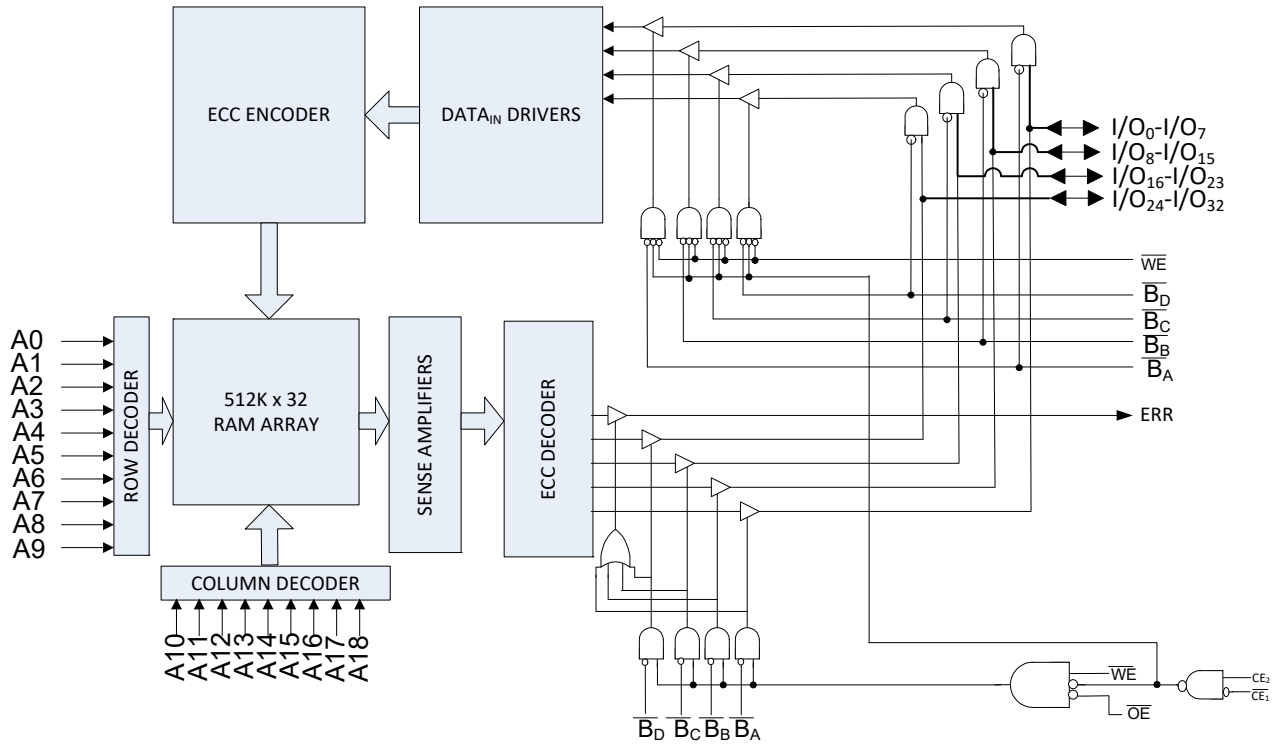


Logic Block Diagram – CY62162G





Logic Block Diagram – CY62162GE





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## Pin Configurations

Figure 1. 119-ball FBGA pinout <sup>[3]</sup>  
CY62162G (512K × 32)

	1	2	3	4	5	6	7
<b>A</b>	I/O <sub>16</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	I/O <sub>0</sub>
<b>B</b>	I/O <sub>17</sub>	A <sub>18</sub>	A <sub>17</sub>	$\overline{CE}_1$	A <sub>16</sub>	A <sub>15</sub>	I/O <sub>1</sub>
<b>C</b>	I/O <sub>18</sub>	$\overline{B}_c$	CE <sub>2</sub>	NC	NC	$\overline{B}_a$	I/O <sub>2</sub>
<b>D</b>	I/O <sub>19</sub>	V <sub>CC</sub>	GND	GND	GND	V <sub>CC</sub>	I/O <sub>3</sub>
<b>E</b>	I/O <sub>20</sub>	GND	V <sub>CC</sub>	GND	V <sub>CC</sub>	GND	I/O <sub>4</sub>
<b>F</b>	I/O <sub>21</sub>	V <sub>CC</sub>	GND	GND	GND	V <sub>CC</sub>	I/O <sub>5</sub>
<b>G</b>	I/O <sub>22</sub>	GND	V <sub>CC</sub>	GND	V <sub>CC</sub>	GND	I/O <sub>6</sub>
<b>H</b>	I/O <sub>23</sub>	V <sub>CC</sub>	GND	GND	GND	V <sub>CC</sub>	I/O <sub>7</sub>
<b>J</b>	NC	GND	V <sub>CC</sub>	GND	V <sub>CC</sub>	GND	NC
<b>K</b>	I/O <sub>24</sub>	V <sub>CC</sub>	GND	GND	GND	V <sub>CC</sub>	I/O <sub>8</sub>
<b>L</b>	I/O <sub>25</sub>	GND	V <sub>CC</sub>	GND	V <sub>CC</sub>	GND	I/O <sub>9</sub>
<b>M</b>	I/O <sub>26</sub>	V <sub>CC</sub>	GND	GND	GND	V <sub>CC</sub>	I/O <sub>10</sub>
<b>N</b>	I/O <sub>27</sub>	GND	V <sub>CC</sub>	GND	V <sub>CC</sub>	GND	I/O <sub>11</sub>
<b>P</b>	I/O <sub>28</sub>	V <sub>CC</sub>	GND	GND	GND	V <sub>CC</sub>	I/O <sub>12</sub>
<b>R</b>	I/O <sub>29</sub>	A <sub>14</sub>	B <sub>d</sub>	NC	B <sub>b</sub>	A <sub>13</sub>	I/O <sub>13</sub>
<b>T</b>	I/O <sub>30</sub>	A <sub>12</sub>	A <sub>11</sub>	$\overline{WE}$	A <sub>10</sub>	A <sub>9</sub>	I/O <sub>14</sub>
<b>U</b>	I/O <sub>31</sub>	A <sub>8</sub>	A <sub>7</sub>	$\overline{OE}$	A <sub>6</sub>	A <sub>5</sub>	I/O <sub>15</sub>

Figure 2. 119-ball FBGA pinout <sup>[3, 4]</sup>  
CY62162GE (512K × 32)

	1	2	3	4	5	6	7
<b>A</b>	I/O <sub>16</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	I/O <sub>0</sub>
<b>B</b>	I/O <sub>17</sub>	A <sub>18</sub>	A <sub>17</sub>	$\overline{CE}_1$	A <sub>16</sub>	A <sub>15</sub>	I/O <sub>1</sub>
<b>C</b>	I/O <sub>18</sub>	$\overline{B}_c$	CE <sub>2</sub>	NC	NC	$\overline{B}_a$	I/O <sub>2</sub>
<b>D</b>	I/O <sub>19</sub>	V <sub>CC</sub>	GND	GND	GND	V <sub>CC</sub>	I/O <sub>3</sub>
<b>E</b>	I/O <sub>20</sub>	GND	V <sub>CC</sub>	GND	V <sub>CC</sub>	GND	I/O <sub>4</sub>
<b>F</b>	I/O <sub>21</sub>	V <sub>CC</sub>	GND	GND	GND	V <sub>CC</sub>	I/O <sub>5</sub>
<b>G</b>	I/O <sub>22</sub>	GND	V <sub>CC</sub>	GND	V <sub>CC</sub>	GND	I/O <sub>6</sub>
<b>H</b>	I/O <sub>23</sub>	V <sub>CC</sub>	GND	GND	GND	V <sub>CC</sub>	I/O <sub>7</sub>
<b>J</b>	ERR	GND	V <sub>CC</sub>	GND	V <sub>CC</sub>	GND	NC
<b>K</b>	I/O <sub>24</sub>	V <sub>CC</sub>	GND	GND	GND	V <sub>CC</sub>	I/O <sub>8</sub>
<b>L</b>	I/O <sub>25</sub>	GND	V <sub>CC</sub>	GND	V <sub>CC</sub>	GND	I/O <sub>9</sub>
<b>M</b>	I/O <sub>26</sub>	V <sub>CC</sub>	GND	GND	GND	V <sub>CC</sub>	I/O <sub>10</sub>
<b>N</b>	I/O <sub>27</sub>	GND	V <sub>CC</sub>	GND	V <sub>CC</sub>	GND	I/O <sub>11</sub>
<b>P</b>	I/O <sub>28</sub>	V <sub>CC</sub>	GND	GND	GND	V <sub>CC</sub>	I/O <sub>12</sub>
<b>R</b>	I/O <sub>29</sub>	A <sub>14</sub>	$\overline{B}_d$	NC	$\overline{B}_b$	A <sub>13</sub>	I/O <sub>13</sub>
<b>T</b>	I/O <sub>30</sub>	A <sub>12</sub>	A <sub>11</sub>	$\overline{WE}$	A <sub>10</sub>	A <sub>9</sub>	I/O <sub>14</sub>
<b>U</b>	I/O <sub>31</sub>	A <sub>8</sub>	A <sub>7</sub>	$\overline{OE}$	A <sub>6</sub>	A <sub>5</sub>	I/O <sub>15</sub>

### Notes

3. NC pins are not connected internally to the die.
4. ERR is an Output pin. If not used, this pin should be left floating.



## CY62162G/CY62162GE MoBL

### Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature  
with power applied ..... -55 °C to +125 °C

Supply voltage to ground potential ..... -0.5 V to  $V_{CC} + 0.5$  V

DC voltage applied to outputs  
in high Z State<sup>[6]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

DC input voltage<sup>[6]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage  
(per MIL-STD-883, method 3015) ..... > 2001 V

Latch-up current ..... > 140 mA

### Operating Range

Device	Range	Ambient Temperature	$V_{CC}$ <sup>[7]</sup>
CY62162G	Industrial	-40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V

### Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	Min	Typ <sup>[8]</sup>	Max	Unit	
$V_{OH}$	Output HIGH voltage	1.65 V to 2.2 V	$V_{CC} = \text{Min}$ , $I_{OH} = -0.1$ mA	1.4	–	–	V
		2.2 V to 2.7 V	$V_{CC} = \text{Min}$ , $I_{OH} = -1.0$ mA	2.0	–	–	
		2.7 V to 3.6 V	$V_{CC} = \text{Min}$ , $I_{OH} = -4.0$ mA	2.2	–	–	
$V_{OL}$	Output LOW voltage	1.65 V to 2.2 V	$V_{CC} = \text{Min}$ , $I_{OL} = 0.1$ mA	–	–	0.2	
		2.2 V to 2.7 V	$V_{CC} = \text{Min}$ , $I_{OL} = 2$ mA	–	–	0.4	
		2.7 V to 3.6 V	$V_{CC} = \text{Min}$ , $I_{OL} = 8$ mA	–	–	0.4	
$V_{IH}$	Input HIGH voltage	1.65 V to 2.2 V	–	1.4	–	$V_{CC} + 0.2$	
		2.2 V to 2.7 V	–	2.0	–	$V_{CC} + 0.3$	
		2.7 V to 3.6 V	–	2.0	–	$V_{CC} + 0.3$	
$V_{IL}$	Input LOW voltage <sup>[6]</sup>	1.65 V to 2.2 V	–	-0.2	–	0.4	
		2.2 V to 2.7 V	–	-0.3	–	0.6	
		2.7 V to 3.6 V	–	-0.3	–	0.8	
$I_{IX}$	Input leakage current	$GND \leq V_{IN} \leq V_{CC}$	-1.0	–	+1.0	$\mu$ A	
$I_{OZ}$	Output leakage current	$GND \leq V_{OUT} \leq V_{CC}$ , Output disabled	-1.0	–	+1.0		
$I_{CC}$	$V_{CC}$ operating supply current	$f = 22.22$ MHz (45 ns)	$V_{CC} = V_{CC(\text{max})}$ , $I_{OUT} = 0$ mA CMOS levels	–	29.0	36.0	mA
		$f = 18.18$ MHz (55 ns)		–	29.0	32.0	
		$f = 1$ MHz		–	7.0	9.0	
$I_{SB1}$ <sup>[9]</sup>	Automatic power down current – CMOS inputs; $V_{CC} = 2.2$ to 3.6 V	$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V	–	5.5	16.0	$\mu$ A	
	Automatic power down current – CMOS inputs; $V_{CC} = 1.65$ to 2.2 V	or $\overline{B}_{A-D} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V, $V_{IN} \leq 0.2$ V, $f = f_{\text{max}}$ (address and data only), $f = 0$ (OE, and WE), $V_{CC} = V_{CC(\text{max})}$	–	7.0	26.0		
$I_{SB2}$ <sup>[9]</sup>	Automatic power down current – CMOS inputs; $V_{CC} = 2.2$ to 3.6 V	$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V	–	5.5	16.0		
	Automatic power down current – CMOS inputs; $V_{CC} = 1.65$ to 2.2 V	or $\overline{B}_{A-D} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, $f = 0$ , $V_{CC} = V_{CC(\text{max})}$	–	7.0	26.0		

#### Notes

- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = 1.8$  V (for  $V_{CC}$  range of 1.65 V–2.2 V),  $V_{CC} = 3$  V (for  $V_{CC}$  range of 2.2 V–3.6 V),  $T_A = 25$  °C.
- $V_{IL(\text{min})} = -2.0$  V and  $V_{IH(\text{max})} = V_{CC} + 2$  V for pulse durations of less than 2 ns.
- Full device AC operation assumes a 100- $\mu$ s ramp time from 0 to  $V_{CC}$  (min) and 200- $\mu$ s wait time after  $V_{CC}$  stabilizes to its operational value.
- Indicates the value for the center of distribution at 3.0 V, 25 °C and not 100% tested.
- Chip enables ( $CE_1$  and  $CE_2$ ) must be tied to CMOS levels to meet the  $I_{SB1}/I_{SB2}/I_{CCDR}$  spec. Other inputs can be left floating.

## Capacitance

Parameter <sup>[10]</sup>	Description	Test Conditions	Max	Unit
$C_{IN}$	Input capacitance	$T_A = 25\text{ }^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = V_{CC(\text{typ})}$	10	pF
$C_{OUT}$	Output capacitance			

## Thermal Resistance

Parameter <sup>[10]</sup>	Description	Test Conditions	119-ball BGA	Unit
$\Theta_{JA}$	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, 2-layer printed circuit board	20.92	$^\circ\text{C/W}$
$\Theta_{JC}$	Thermal resistance (junction to case)		15.84	

## AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms

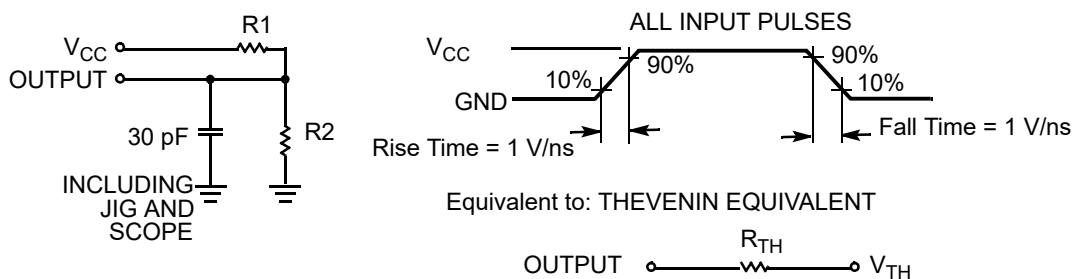


Table 1. AC Test Loads

Parameter	1.8 V	2.5 V	3.0 V	Unit
R1	13500	16667	1103	$\Omega$
R2	10800	15385	1554	
$R_{TH}$	6000	8000	645	
$V_{TH}$	0.8	1.2	1.75	V

### Note

10. Tested initially and after any design or process changes that may affect these parameters.



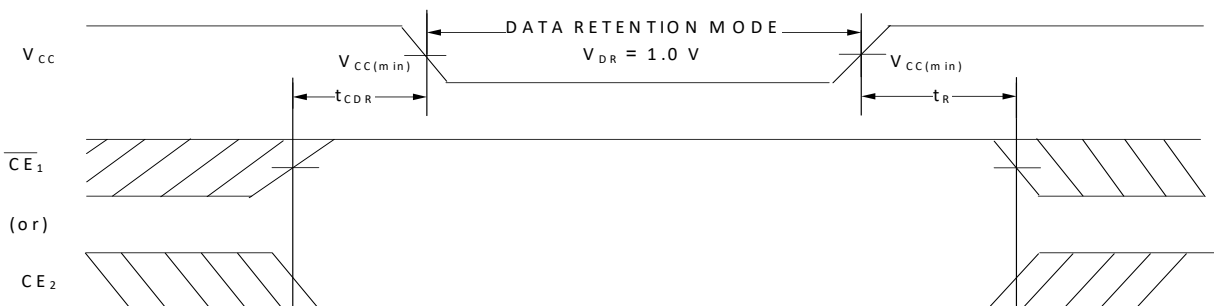
## Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ <sup>[11]</sup>	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		1.0	–	–	V
$I_{CCDR}$ <sup>[12, 13]</sup>	Data retention current	$1.0\text{ V} \leq V_{CC} \leq 2.2\text{ V}$ , $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$ or $\overline{B}_{A-D} \geq V_{CC} - 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	7.0	26.0	$\mu\text{A}$
		$2.2\text{ V} < V_{CC} \leq 3.6\text{ V}$ , $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$ or $\overline{B}_{A-D} \geq V_{CC} - 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	5.5	16.0	
$t_{CDR}$ <sup>[14]</sup>	Chip deselect to data retention time	–	0	–	–	ns
$t_R$ <sup>[14, 15]</sup>	Operation recovery time	–	45 / 55	–	–	

## Data Retention Waveform

Figure 4. Data Retention Waveform



### Notes

- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = 1.8\text{ V}$  for the range  $1.7\text{ V}$  to  $2.2\text{ V}$ ;  $3\text{ V}$  for the range  $2.2\text{ V}$  to  $3.6\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .
- Only chip enables ( $\overline{CE}_1$  and  $CE_2$ ) and all byte enables ( $\overline{B}_{A-D}$ ) need to be tied to CMOS levels to meet the  $I_{SB2}/I_{CCDR}$  spec. Other inputs can be left floating.
- $\overline{B}_{A-D}$  is the AND of  $\overline{B}_A$ ,  $\overline{B}_B$ ,  $\overline{B}_C$  and  $\overline{B}_D$ . Chip is deselected by either disabling the chip enable signals or by disabling all byte enables together.
- These parameters are guaranteed by design and are not tested.
- Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 100\ \mu\text{s}$  or stable at  $V_{CC(min)} \geq 100\ \mu\text{s}$ .



## Switching Characteristics

Over the Operating Range

Parameter <sup>[16, 17]</sup>	Description	45 ns		55 ns		Unit
		Min	Max	Min	Max	
<b>Read Cycle</b>						
$t_{RC}$	Read cycle time	45.0	–	55.0	–	ns
$t_{AA}$	Address to data/ERR valid	–	45.0	–	55.0	
$t_{OHA}$	Data/ERR hold from address change	10	–	10.0	–	
$t_{ACE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to data/ERR valid	–	45.0	–	55.0	
$t_{DOE}$	$\overline{OE}$ LOW to data/ERR valid	–	22.0	–	25.0	
$t_{LZOE}$	$\overline{OE}$ LOW to low Z <sup>[17, 18]</sup>	5.0	–	5.0	–	
$t_{HZOE}$	$\overline{OE}$ HIGH to high Z <sup>[17, 18, 19]</sup>	–	18.0	–	18.0	
$t_{LZCE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to low Z <sup>[17, 18]</sup>	10.0	–	10.0	–	
$t_{HZCE}$	$\overline{CE}_1$ HIGH and $CE_2$ LOW to high Z <sup>[17, 18, 19]</sup>	–	18.0	–	18.0	
$t_{PU}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to power-up <sup>[20]</sup>	0	–	0	–	
$t_{PD}$	$\overline{CE}_1$ HIGH and $CE_2$ LOW to power-down <sup>[20]</sup>	–	45.0	–	55.0	
$t_{DBE}$	Byte enable LOW to data valid	–	45.0	–	55.0	
$t_{LZBE}$	Byte enable LOW to low Z <sup>[17]</sup>	5.0	–	5.0	–	
$t_{HZBE}$	Byte enable HIGH to high Z <sup>[17, 19]</sup>	–	18.0	–	18.0	
<b>Write Cycle <sup>[21, 22]</sup></b>						
$t_{WC}$	Write cycle time	45.0	–	55.0	–	ns
$t_{SCE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to write end	35.0	–	40.0	–	
$t_{AW}$	Address setup to write end	35.0	–	40.0	–	
$t_{HA}$	Address hold from write end	0	–	0	–	
$t_{SA}$	Address setup to write start	0	–	0	–	
$t_{PWE}$	$\overline{WE}$ pulse width	35.0	–	40.0	–	
$t_{BW}$	Byte enable LOW to write end	35.0	–	40.0	–	
$t_{SD}$	Data setup to write end	25.0	–	25.0	–	
$t_{HD}$	Data hold from write end	0	–	0	–	
$t_{HZWE}$	$\overline{WE}$ LOW to high Z <sup>[17, 18, 19]</sup>	–	18.0	–	20.0	
$t_{LZWE}$	$\overline{WE}$ HIGH to low Z <sup>[17, 18]</sup>	10.0	–	10.0	–	

### Notes

- Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 V/ns, timing reference levels of  $V_{TH}$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in Table 1 on page 7.
- At any temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- Tested initially and after any design or process changes that may affect these parameters.
- $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high impedance state.
- These parameters are guaranteed by design and are not tested.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  and  $\overline{WE}$  LOW. Chip enable must be active and  $\overline{WE}$  and byte enables must be LOW to initiate a write, and the transition of any of these signals terminate the write. The input data setup and hold timing are referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle pulse width for Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) should be equal to sum of  $t_{HZWE}$  and  $t_{SD}$ .

## Switching Waveforms

Figure 5. Read Cycle No. 1 of CY62162G (Address Transition Controlled) [23, 24]

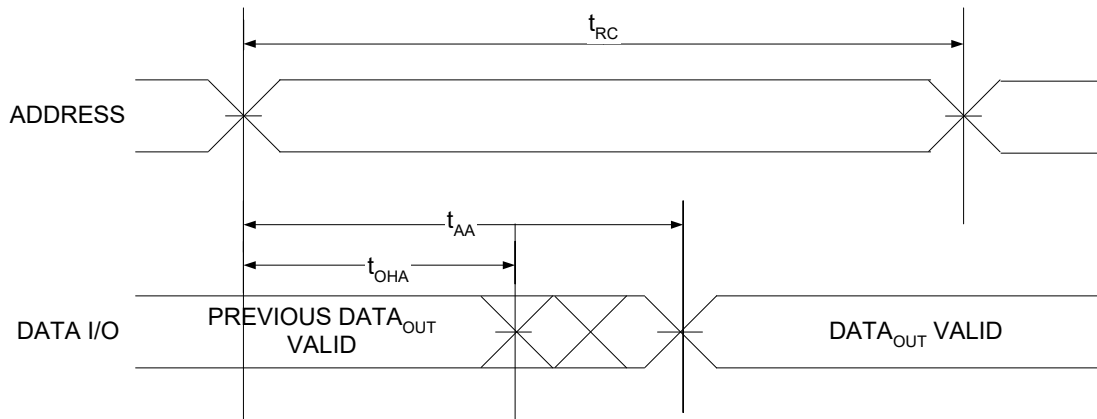
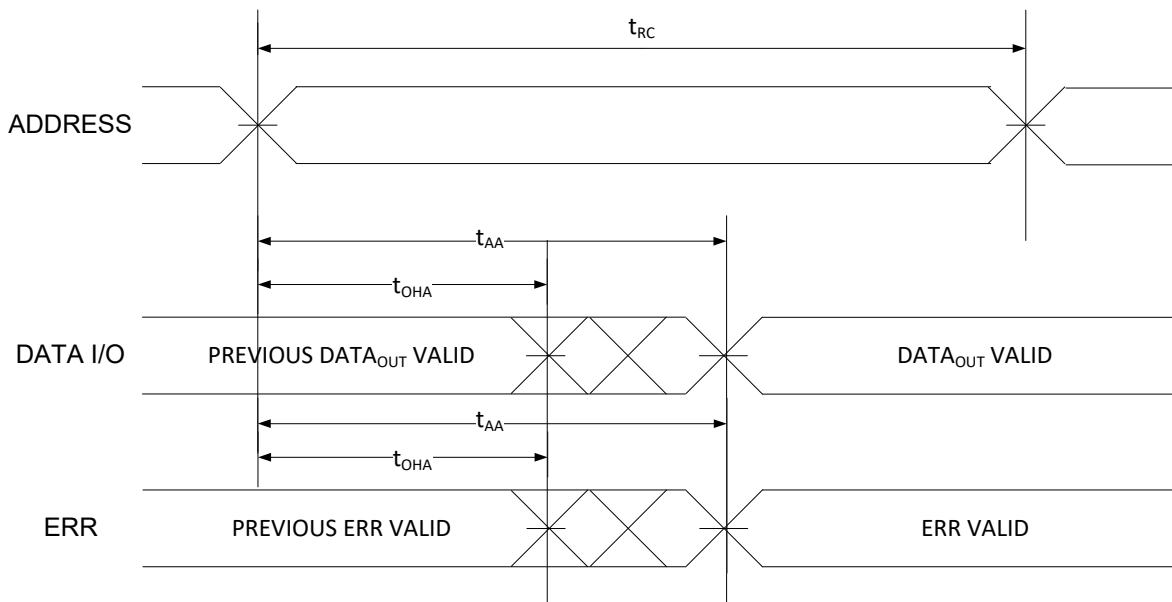


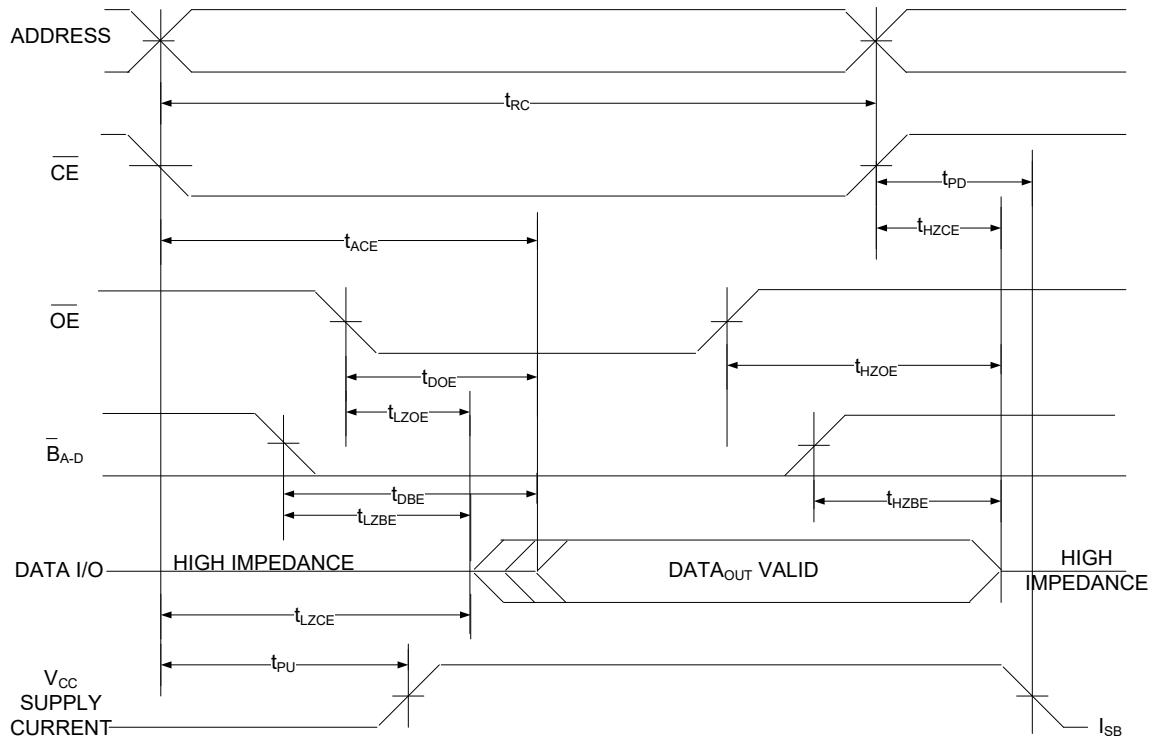
Figure 6. Read Cycle No. 1 of CY62162GE (Address Transition Controlled) [23, 24]



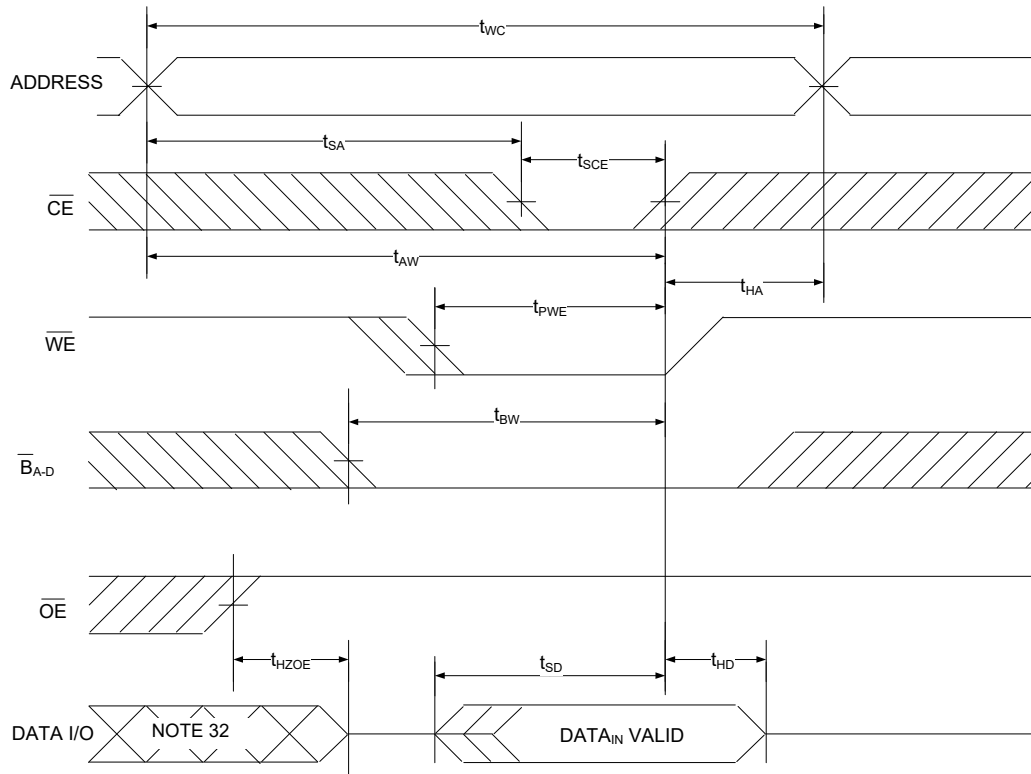
### Notes

23. Device is continuously selected.  $\overline{OE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ .  
 24. WE is HIGH for read cycle.

## Switching Waveforms (continued)

Figure 7. Read Cycle No. 2 ( $\overline{\text{OE}}$  Controlled) [25, 26, 27]**Notes**25.  $\overline{\text{WE}}$  is HIGH for read cycle.26. Address valid before or similar to  $\overline{\text{CE}}$  transition LOW.27.  $\overline{\text{CE}}$  refers to a combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$ .  $\overline{\text{CE}}$  is LOW when  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH.  $\overline{\text{CE}}$  is HIGH when  $\overline{\text{CE}}_1$  is HIGH or  $\text{CE}_2$  is LOW.

## Switching Waveforms (continued)

Figure 8. Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled) [28, 29, 30, 31]**Notes**

28. The internal write time of the memory is defined by the overlap of  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$  LOW. Chip enable must be active and  $\overline{\text{WE}}$  and byte enables must be LOW to initiate a write, and the transition of any of these signals terminate the write. The input data setup and hold timing are referenced to the leading edge of the signal that terminates the write.

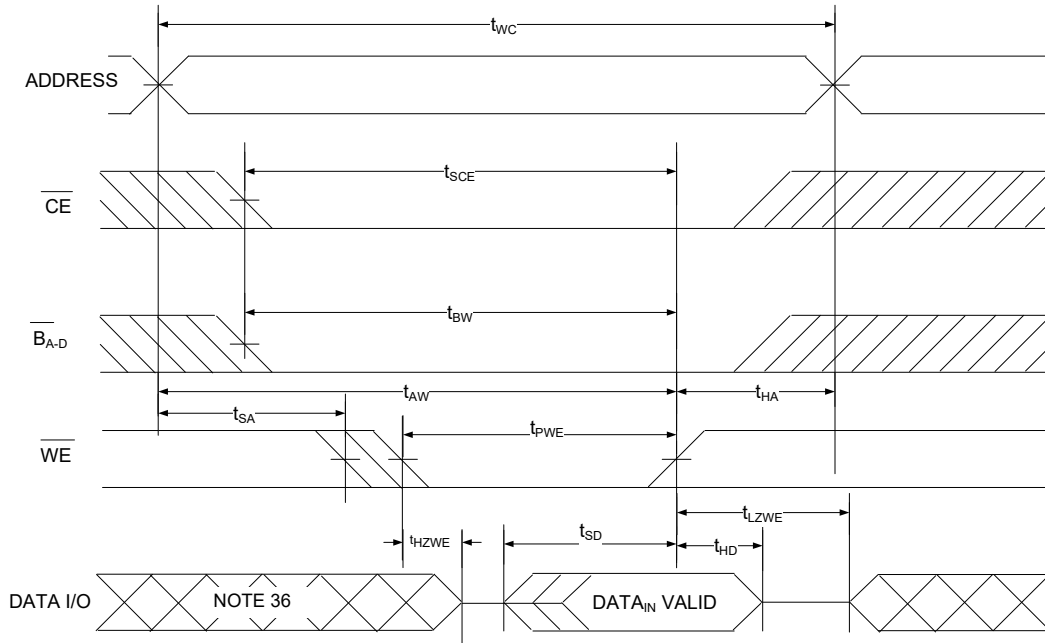
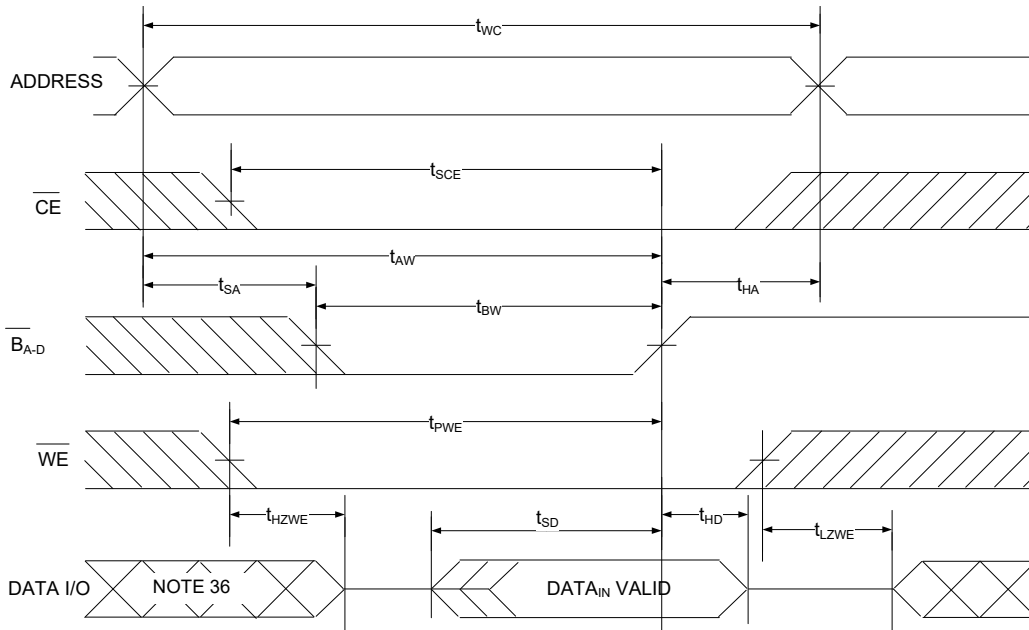
29. Data I/O is high impedance if  $\overline{\text{OE}}$  or  $\overline{\text{B}}_A$ ,  $\overline{\text{B}}_B$ ,  $\overline{\text{B}}_C$ ,  $\overline{\text{B}}_D = V_{IH}$ .

30. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  going HIGH, the output remains in a high impedance state.

31.  $\overline{\text{CE}}$  refers to a combination of  $\overline{\text{CE}}_1$  and  $\text{CE}_2$ .  $\overline{\text{CE}}$  is LOW when  $\overline{\text{CE}}_1$  is LOW and  $\text{CE}_2$  is HIGH.  $\overline{\text{CE}}$  is HIGH when  $\overline{\text{CE}}_1$  is HIGH or  $\text{CE}_2$  is LOW.

32. During this period the I/Os are in output state and input signals should not be applied.

## Switching Waveforms (continued)

Figure 9. Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) [33, 34, 35]Figure 10. Write Cycle No. 3 ( $\overline{BA}$ ,  $\overline{BB}$ ,  $\overline{BC}$ ,  $\overline{BD}$  Controlled,  $\overline{OE}$  LOW) [33, 34]

## Notes

33. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high impedance state.
34.  $\overline{CE}$  refers to a combination of  $\overline{CE}_1$  and  $CE_2$ .  $\overline{CE}$  is LOW when  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH.  $\overline{CE}$  is HIGH when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW.
35. The minimum write cycle pulse width should be equal to the sum of  $t_{HZWE}$  and  $t_{SD}$ .
36. During this period the I/Os are in output state and input signals should not be applied.



## Truth Table – CY62162G/CY62162GE

$\overline{CE}^{[37]}$	$\overline{OE}$	$\overline{WE}$	$\overline{B}_A$	$\overline{B}_B$	$\overline{B}_C$	$\overline{B}_D$	I/O <sub>0</sub> –I/O <sub>7</sub>	I/O <sub>8</sub> –I/O <sub>15</sub>	I/O <sub>16</sub> –I/O <sub>23</sub>	I/O <sub>24</sub> –I/O <sub>31</sub>	Mode	Power
H	X	X	X <sup>[38]</sup>	X <sup>[38]</sup>	X <sup>[38]</sup>	X <sup>[38]</sup>	High Z	High Z	High Z	High Z	Standby	(I <sub>SB</sub> )
X <sup>[38]</sup>	X	X	H	H	H	H	High Z	High Z	High Z	High Z	Standby	(I <sub>SB</sub> )
L	L	H	L	L	L	L	Data out	Data out	Data out	Data out	Read all bits	(I <sub>CC</sub> )
L	L	H	L	H	H	H	Data out	High Z	High Z	High Z	Read byte A bits only	(I <sub>CC</sub> )
L	L	H	H	L	H	H	High Z	Data out	High Z	High Z	Read byte B bits only	(I <sub>CC</sub> )
L	L	H	H	H	L	H	High Z	High Z	Data out	High Z	Read byte C bits only	(I <sub>CC</sub> )
L	L	H	H	H	H	L	High Z	High Z	High Z	Data out	Read byte D bits only	(I <sub>CC</sub> )
L	X	L	L	L	L	L	Data in	Data in	Data in	Data in	Write all bits	(I <sub>CC</sub> )
L	X	L	L	H	H	H	Data in	High Z	High Z	High Z	Write byte A bits only	(I <sub>CC</sub> )
L	X	L	H	L	H	H	High Z	Data in	High Z	High Z	Write byte B bits only	(I <sub>CC</sub> )
L	X	L	H	H	L	H	High Z	High Z	Data in	High Z	Write byte C bits only	(I <sub>CC</sub> )
L	X	L	H	H	H	L	High Z	High Z	High Z	Data in	Write byte D bits only	(I <sub>CC</sub> )
L	H	H	X <sup>[38]</sup>	X <sup>[38]</sup>	X <sup>[38]</sup>	X <sup>[38]</sup>	High Z	High Z	High Z	High Z	Selected, outputs disabled	(I <sub>CC</sub> )

## ERR Output – CY62162GE

Output <sup>[39]</sup>	Mode
0	Read Operation, no single bit error in the stored data.
1	Read Operation, single bit error detected and corrected.
Z	Device deselected / Outputs disabled / Write Operation.

**Note**

37.  $\overline{CE}$  refers to a combination of  $\overline{CE}_1$  and  $CE_2$ .  $\overline{CE}$  is LOW when  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH.  $\overline{CE}$  is HIGH when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW.

38. 'X' refers to  $V_{IL}$  or  $V_{IH}$ . For CMOS voltage levels refer to I<sub>SB2</sub> test conditions in [Electrical Characteristics on page 6](#). Chip enables ( $\overline{CE}_1$  and  $CE_2$ ) and all Byte Enables ( $\overline{B}_{A-D}$ ) must be in CMOS voltage levels to meet the I<sub>SB2</sub>/I<sub>CCDR</sub> spec.

39. ERR is an Output pin. If not used, this pin should be left floating.

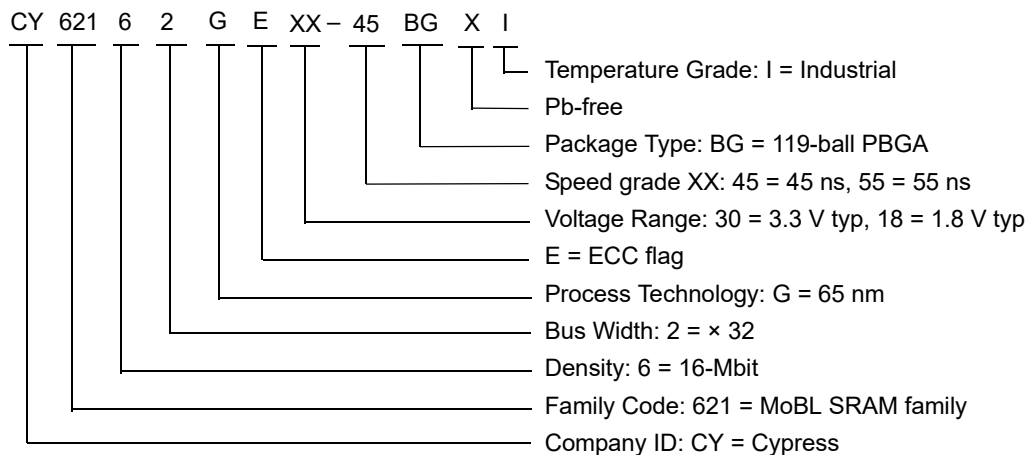


## CY62162G/CY62162GE MoBL

### Ordering Information

Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type (All Pb-free)	Operating Range
45	2.2 V–3.6 V	CY62162G30-45BGXI	51-85115	119-ball PBGA (14 × 22 × 2.4 mm)	Industrial
55	1.65 V–2.2 V	CY62162G18-55BGXI			Industrial

### Ordering Code Definitions

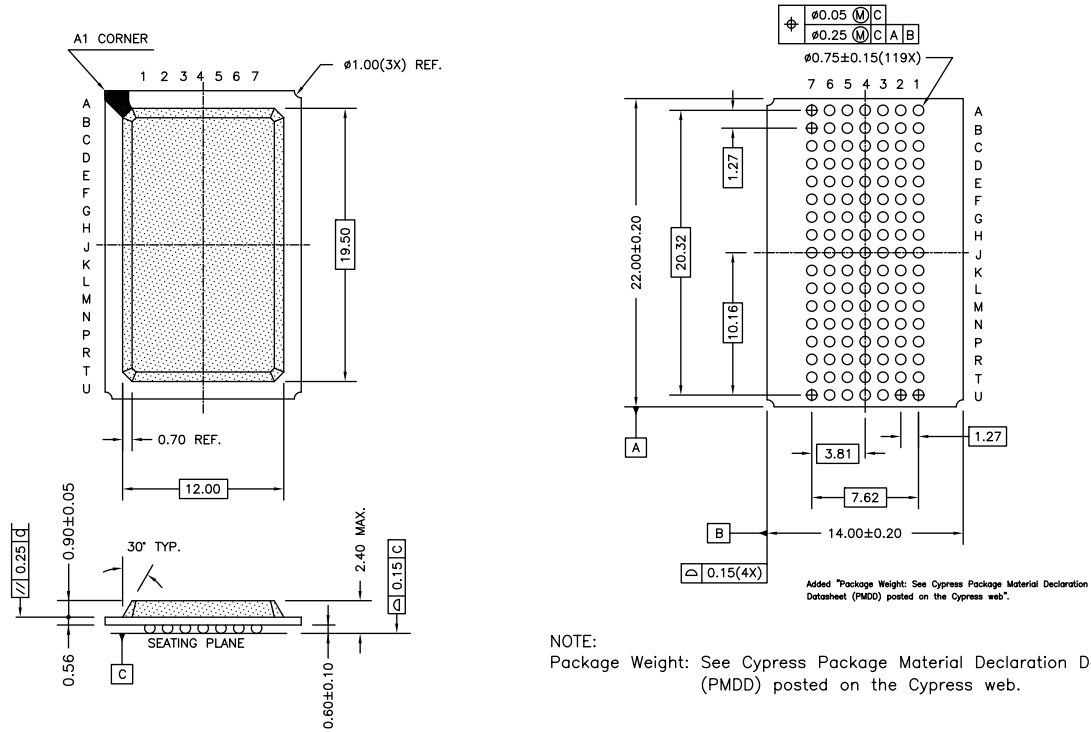




**CY62162G/CY62162GE MoBL**

**Package Diagram**

**Figure 11. 119-ball PBGA (14 × 22 × 2.4 mm) Package Outline, 51-85115**



51-85115 \*D



## Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
FBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
$\overline{WE}$	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
$^{\circ}\text{C}$	degree Celsius
mA	milliampere
MHz	megahertz
mm	millimeter
$\mu\text{A}$	microampere
$\mu\text{s}$	microsecond
ns	nanosecond
$\Omega$	ohm
%	percent
pF	picofarad
V	volt
W	watt



## Document History Page

Document Title: CY62162G/CY62162GE MoBL, 16-Mbit (512K × 32) Static RAM with Error-Correcting Code (ECC) Document Number: 001-81598			
Revision	ECN	Submission Date	Description of Change
*C	4863821	07/31/2015	Changed status from Preliminary to Final.
*D	6012120	01/03/2018	Updated Cypress Logo and Copyright.
*E	6674948	09/27/2019	<p>Updated <a href="#">Product Portfolio</a>:            Added Note "This device is offered with improved I<sub>CC</sub>, I<sub>SB1</sub> and I<sub>SB2</sub> specifications compared to the current revision with same marketing part number. The new device will be in production from WW1952. For more information, please contact Cypress sales representative." and referred the same note in "CY62162G(E)30" under "Product" column.            Added Note "For next version of this device, kindly refer <a href="#">here</a>. Further details about improvement and comparison between current and new versions can be found in the <a href="#">PCN193805</a>." and referred the same note in "CY62162G(E)30" under "Product" column.</p> <p>Updated <a href="#">Pin Configurations</a>:            Updated <a href="#">Figure 1</a>.            Updated <a href="#">Figure 2</a>.            Updated <a href="#">Electrical Characteristics</a>:            Added Note "This device is offered with improved I<sub>CC</sub>, I<sub>SB1</sub> and I<sub>SB2</sub> specifications compared to the current revision with same marketing part number. The new device will be in production from WW1952. For more information, please contact Cypress sales representative." and referred the same note in I<sub>CC</sub>, I<sub>SB1</sub>, I<sub>SB2</sub> parameters.            Added Note "For next version of this device, kindly refer <a href="#">here</a>. Further details about improvement and comparison between current and new versions can be found in the <a href="#">PCN193805</a>." and referred the same note in I<sub>CC</sub>, I<sub>SB1</sub>, I<sub>SB2</sub> parameters.</p> <p>Updated <a href="#">Data Retention Characteristics</a>:            Added Note "This device is offered with improved I<sub>CC</sub>, I<sub>SB1</sub> and I<sub>SB2</sub> specifications compared to the current revision with same marketing part number. The new device will be in production from WW1952. For more information, please contact Cypress sales representative." and referred the same note in I<sub>CCDR</sub> parameter.            Added Note "For next version of this device, kindly refer <a href="#">here</a>. Further details about improvement and comparison between current and new versions can be found in the <a href="#">PCN193805</a>." and referred the same note in I<sub>CCDR</sub> parameter.</p> Updated to new template. Completing Sunset Review.
*F	6822780	03/02/2020	<p>Updated <a href="#">Product Portfolio</a>:            Removed Note "This device is offered with improved I<sub>CC</sub>, I<sub>SB1</sub> and I<sub>SB2</sub> specifications compared to the current revision with same marketing part number. The new device will be in production from WW1952. For more information, please contact Cypress sales representative." and its reference in "CY62162G(E)30" under "Product" column.            Removed Note "For next version of this device, kindly refer <a href="#">here</a>. Further details about improvement and comparison between current and new versions can be found in the <a href="#">PCN193805</a>." and its reference in "CY62162G(E)30" under "Product" column.</p> <p>Updated <a href="#">Electrical Characteristics</a>:            Removed Note "This device is offered with improved I<sub>CC</sub>, I<sub>SB1</sub> and I<sub>SB2</sub> specifications compared to the current revision with same marketing part number. The new device will be in production from WW1952. For more information, please contact Cypress sales representative." and its reference in I<sub>CC</sub>, I<sub>SB1</sub>, I<sub>SB2</sub> parameters.            Removed Note "For next version of this device, kindly refer <a href="#">here</a>. Further details about improvement and comparison between current and new versions can be found in the <a href="#">PCN193805</a>." and its reference in I<sub>CC</sub>, I<sub>SB1</sub>, I<sub>SB2</sub> parameters.</p>



## Document History Page *(continued)*

Document Title: CY62162G/CY62162GE MoBL, 16-Mbit (512K × 32) Static RAM with Error-Correcting Code (ECC) Document Number: 001-81598			
Revision	ECN	Submission Date	Description of Change
*F (cont.)	6822780	03/02/2020	<p>Updated <a href="#">Data Retention Characteristics</a>:</p> <p>Removed Note "This device is offered with improved I<sub>CC</sub>, I<sub>SB1</sub> and I<sub>SB2</sub> specifications compared to the current revision with same marketing part number. The new device will be in production from WW1952. For more information, please contact Cypress sales representative." and its reference in I<sub>CCDR</sub> parameter.</p> <p>Removed Note "For next version of this device, kindly refer <a href="#">here</a>. Further details about improvement and comparison between current and new versions can be found in the <a href="#">PCN193805</a>." and its reference in I<sub>CCDR</sub> parameter.</p> <p>Updated to new template.</p>



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