

CY7C1061G18-15BVJXIT Datasheet



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|------------------------------|--|
| DiGi Electronics Part Number | CY7C1061G18-15BVJXIT-DG |
| Manufacturer | Infineon Technologies |
| Manufacturer Product Number | CY7C1061G18-15BVJXIT |
| Description | IC SRAM 16MBIT PARALLEL 48VFBGA |
| Detailed Description | SRAM - Asynchronous Memory IC 16Mbit Parallel 15 ns 48-VFBGA (6x8) |

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Manufacturer Product Number:

CY7C1061G18-15BVJXIT

Series:

-

DiGi-Electronics Programmable:

Not Verified

Memory Format:

SRAM

Memory Size:

16Mbit

Memory Interface:

Parallel

Access Time:

15 ns

Operating Temperature:

-40°C ~ 85°C (TA)

Package / Case:

48-VFBGA

Base Product Number:

CY7C1061

Manufacturer:

Infineon Technologies

Product Status:

Active

Memory Type:

Volatile

Technology:

SRAM - Asynchronous

Memory Organization:

1M x 16

Write Cycle Time - Word, Page:

15ns

Voltage - Supply:

1.65V ~ 2.2V

Mounting Type:

Surface Mount

Supplier Device Package:

48-VFBGA (6x8)

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.32.0041

Moisture Sensitivity Level (MSL):

3 (168 Hours)

ECCN:

3A991B2A



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The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content

The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.



CY7C1061G/CY7C1061GE

16-Mbit (1M words × 16-bit) Static RAM with Error-Correcting Code (ECC)

Features

- High speed
 - $t_{AA} = 10 \text{ ns}/15 \text{ ns}$
- Embedded error-correcting code (ECC) for single-bit error correction^[1, 2]
- Low active and standby currents
 - $I_{CC} = 90 \text{ mA}$ typical at 100 MHz
 - $I_{SB2} = 20 \text{ mA}$ typical
- Operating voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, and 4.5 V to 5.5 V
- 1.0 V data retention
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Error indication (ERR) pin to indicate 1-bit error detection and correction
- Available in Pb-free 48-pin TSOP I, 54-pin TSOP II, and 48-ball VFBGA packages

Functional Description

CY7C1061G and CY7C1061GE are high-performance CMOS fast static RAM devices with embedded ECC^[1]. Both devices are offered in single and dual chip enable options and in multiple pin configurations. The CY7C1061GE device includes an ERR pin that signals a single-bit error-detection and correction event during a read cycle.

To access devices with a single chip enable input, assert the chip enable (\overline{CE}) input LOW. To access dual chip enable devices, assert both chip enable inputs – \overline{CE}_1 as LOW and \overline{CE}_2 as HIGH.

To perform data writes, assert the Write Enable (\overline{WE}) input LOW, and provide the data and address on the device data pins (I/O_0 through I/O_{15}) and address pins (A_0 through A_{19}) respectively. The Byte High Enable (\overline{BHE}) and Byte Low Enable (\overline{BLE}) inputs control byte writes, and write data on the corresponding I/O lines to the memory location specified. \overline{BHE} controls I/O_8 through I/O_{15} and \overline{BLE} controls I/O_0 through I/O_7 .

To perform data reads, assert the Output Enable (\overline{OE}) input and provide the required address on the address lines. Read data is accessible on I/O lines (I/O_0 through I/O_{15}). You can perform byte accesses by asserting the required byte enable signal (\overline{BHE} or \overline{BLE}) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os (I/O_0 through I/O_{15}) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH for a single chip enable device and \overline{CE}_1 HIGH / \overline{CE}_2 LOW for a dual chip enable device), or control signals are de-asserted (\overline{OE} , \overline{BLE} , \overline{BHE}).

On the CY7C1061GE devices, the detection and correction of a single-bit error in the accessed location is indicated by the assertion of the ERR output (ERR = High). See the [Truth Table on page 16](#) for a complete description of read and write modes.

The logic block diagrams are on page 2.

The CY7C1061G and CY7C1061GE devices are available in 48-pin TSOP I, 54-pin TSOP II, and 48-ball VFBGA packages.

For a complete list of related documentation, click [here](#).

Product Portfolio

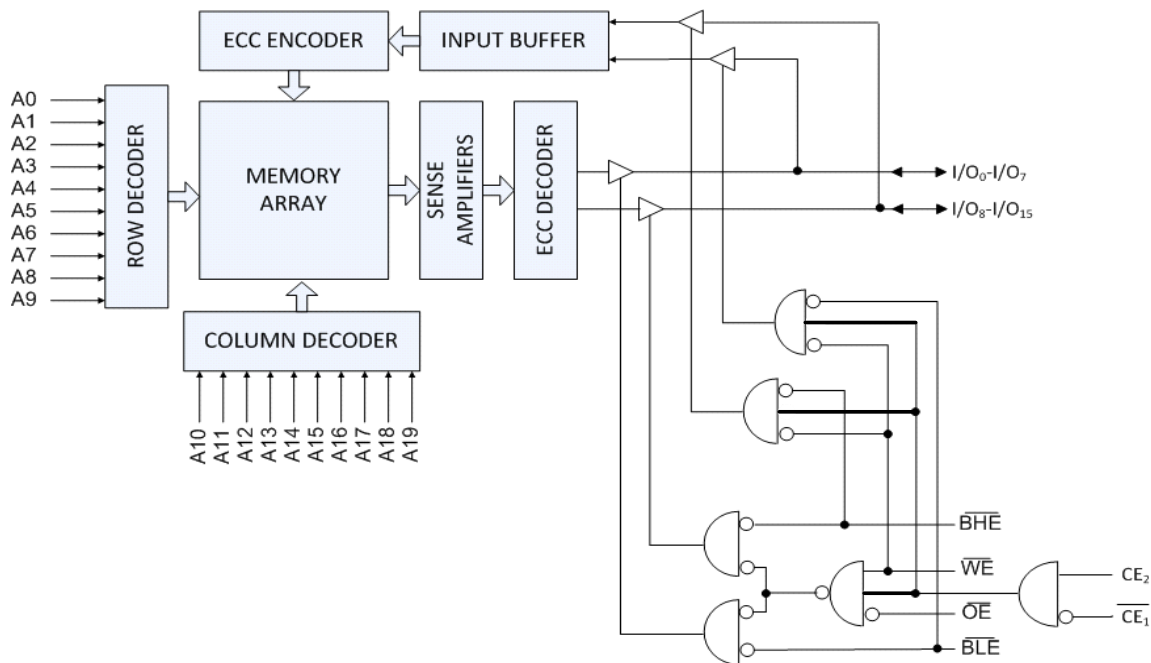
| Product | Features and Options (see Pin Configurations on page 4) | Range | V_{CC} Range (V) | Speed (ns) 10/15 | Current Consumption | | | |
|----------------|--|------------|--------------------|------------------|---------------------------|-----|-------------------------|-----|
| | | | | | $f = f_{max}$ | | Standby, I_{SB2} (mA) | |
| | | | | | Operating I_{CC} , (mA) | | Typ ^[3] | Max |
| CY7C1061G18 | Single or dual chip enables | Industrial | 1.65 V–2.2 V | 15 | 70 | 80 | 20 | 30 |
| CY7C1061G(E)30 | Optional ERR pins | | 2.2 V–3.6 V | 10 | 90 | 110 | | |
| CY7C1061G | Address MSB A_{19} pin placement options compatible with Cypress and other vendors | | 4.5 V–5.5 V | 10 | 90 | 110 | | |

Notes

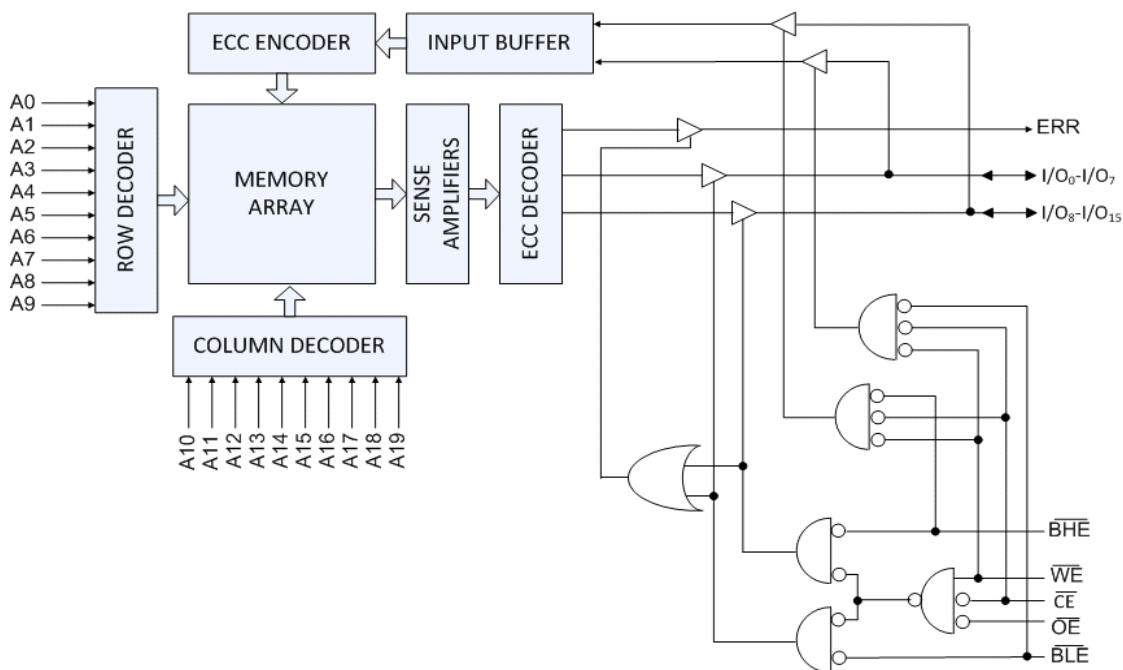
1. This device does not support automatic write-back on error detection.
2. SER FIT Rate < 0.1 FIT/Mb. Refer [AN88889](#) for details.
3. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at $V_{CC} = 1.8 \text{ V}$ (for a V_{CC} range of 1.65 V–2.2 V), $V_{CC} = 3 \text{ V}$ (for a V_{CC} range of 2.2 V–3.6 V), and $V_{CC} = 5 \text{ V}$ (for a V_{CC} range of 4.5 V–5.5 V), $T_A = 25 \text{ }^\circ\text{C}$.



Logic Block Diagram – CY7C1061G



Logic Block Diagram – CY7C1061GE





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Pin Configurations

Figure 1. 48-ball VFBGA (6 × 8 × 1.0 mm) Pinout, Dual Chip Enable without ERR, Address MSB A19 at Ball G2, CY7C1061G^[4] Package/Grade ID: BVJXI

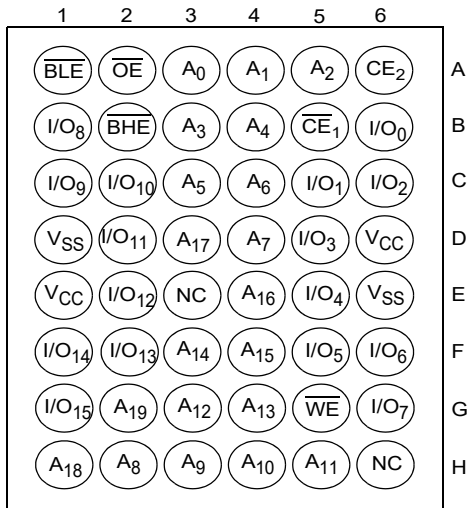


Figure 2. 48-ball VFBGA (6 × 8 × 1.0 mm) Pinout, Dual Chip Enable without ERR, Address MSB A19 at Ball H6, CY7C1061G^[4] Package/Grade ID: BVXI

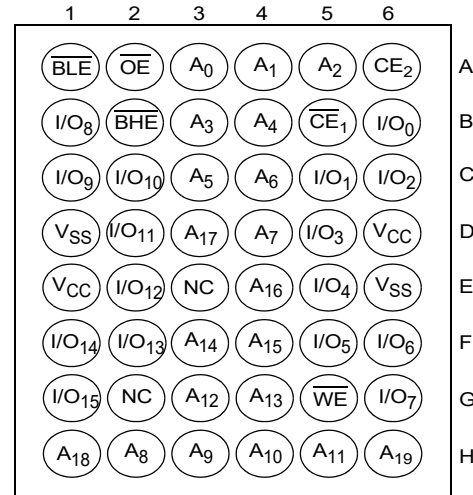
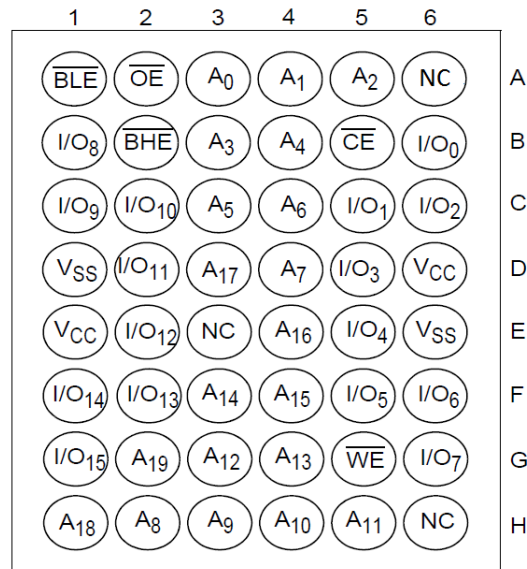


Figure 3. 48-ball VFBGA (6 × 8 × 1.0 mm) Pinout, Single Chip Enable without ERR, Address MSB A19 at Ball G2, CY7C1061G^[4] Package/Grade ID: BV1XI



Note

4. NC pins are not connected internally to the die.



Pin Configurations (continued)

Figure 4. 48-ball VFBGA (6 × 8 × 1.0 mm) Pinout, Single Chip Enable with ERR, Address MSB A19 at Ball G2, CY7C1061GE^[5, 6] Package/Grade ID: BV1XI

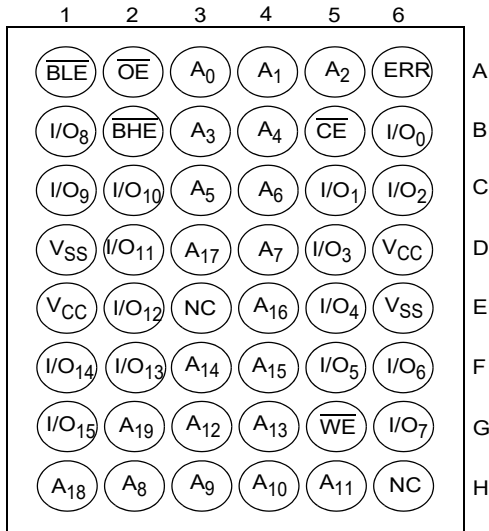


Figure 5. 48-ball VFBGA (6 × 8 × 1.0 mm) Pinout, Dual Chip Enable with ERR, Address MSB A19 at Ball G2, CY7C1061GE^[5, 6] Package/Grade ID: BVJXI

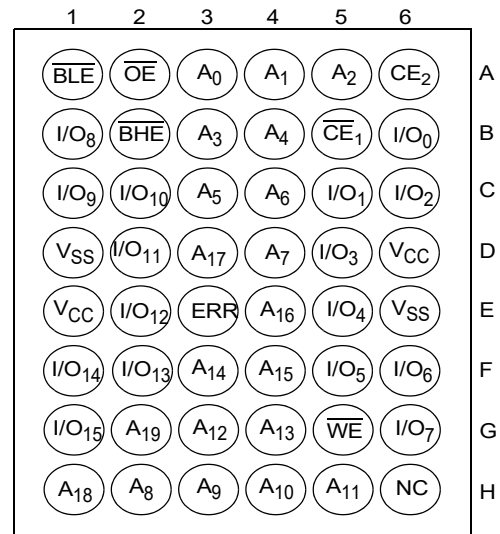
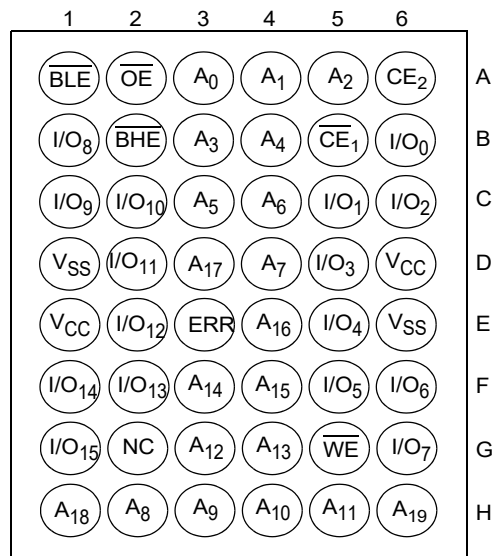


Figure 6. 48-ball VFBGA (6 × 8 × 1.0 mm) Pinout, Dual Chip Enable with ERR, Address MSB A19 at Ball H6, CY7C1061GE^[5, 6] Package/Grade ID: BVXI



Notes

- NC pins are not connected internally to the die.
- ERR is an Output pin. If not used, this pin should be left floating.



CY7C1061G/CY7C1061GE

Pin Configurations (continued)

Figure 7. 48-pin TSOP I (12 × 18.4 × 1 mm) Pinout, Single Chip Enable with ERR, CY7C1061GE^[7, 8]
Package/Grade ID: ZXI

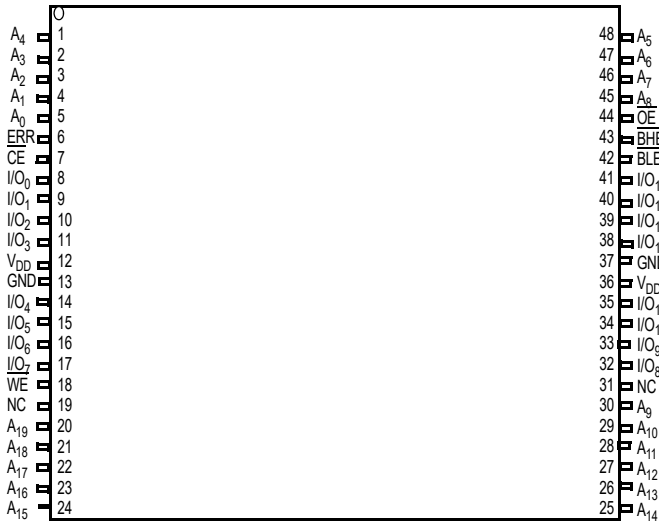


Figure 8. 48-pin TSOP I (12 × 18.4 × 1 mm) Pinout, Single Chip Enable without ERR, CY7C1061G^[7]
Package/Grade ID: ZXI

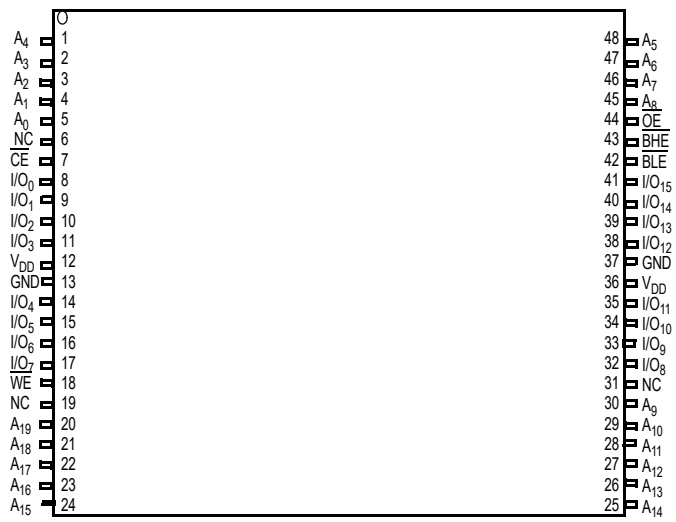


Figure 9. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) pinout, Dual Chip Enable without ERR, CY7C1061G^[7]
Package/Grade ID: ZSXI

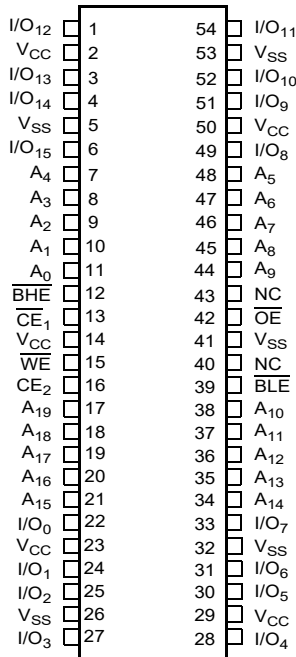
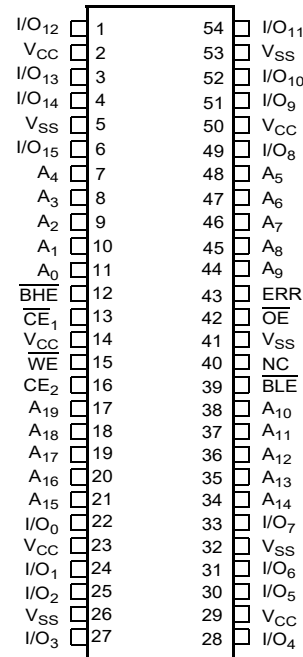


Figure 10. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) pinout, Dual Chip Enable with ERR, CY7C1061GE^[7, 8]
Package/Grade ID: ZSXI



Notes

- 7. NC pins are not connected internally to the die.
- 8. ERR is an Output pin. If not used, this pin should be left floating.



Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature -65 °C to +150 °C

Ambient temperature
with power applied -55 °C to +125 °C

Supply voltage
on V_{CC} relative to GND -0.5 V to $V_{CC} + 0.5$ V

DC voltage applied to outputs
in High Z State ^[9] -0.5 V to $V_{CC} + 0.5$ V

DC input voltage^[9] -0.5 V to $V_{CC} + 0.5$ V

Current into outputs (LOW) 20 mA

Static discharge voltage
(MIL-STD-883, Method 3015) > 2001 V

Latch-up current > 140 mA

Operating Range

| Grade | Ambient Temperature | V_{CC} |
|------------|---------------------|---|
| Industrial | -40 °C to +85 °C | 1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V |

DC Electrical Characteristics

Over the operating range of -40 °C to 85 °C

| Parameter | Description | Test Conditions | 10 ns / 15 ns | | | Unit | |
|-------------------------|---|---|--------------------------------|---------------------|----------------|---------------|----|
| | | | Min | Typ ^[10] | Max | | |
| V_{OH} | Output HIGH voltage | 1.65 V to 2.2 V $V_{CC} = \text{Min}, I_{OH} = -0.1$ mA | 1.4 | - | - | V | |
| | | 2.2 V to 2.7 V $V_{CC} = \text{Min}, I_{OH} = -1.0$ mA | 2.0 | - | - | | |
| | | 2.7 V to 3.0 V $V_{CC} = \text{Min}, I_{OH} = -4.0$ mA | 2.2 | - | - | | |
| | | 3.0 V to 3.6 V $V_{CC} = \text{Min}, I_{OH} = -4.0$ mA | 2.4 | - | - | | |
| | | 4.5 V to 5.5 V $V_{CC} = \text{Min}, I_{OH} = -4.0$ mA | 2.4 | - | - | | |
| | | 4.5 V to 5.5 V $V_{CC} = \text{Min}, I_{OH} = -0.1$ mA | $V_{CC} - 0.4$ ^[11] | - | - | | |
| V_{OL} | Output LOW voltage | 1.65 V to 2.2 V $V_{CC} = \text{Min}, I_{OL} = 0.1$ mA | - | - | 0.2 | V | |
| | | 2.2 V to 2.7 V $V_{CC} = \text{Min}, I_{OL} = 2$ mA | - | - | 0.4 | | |
| | | 2.7 V to 3.6 V $V_{CC} = \text{Min}, I_{OL} = 8$ mA | - | - | 0.4 | | |
| | | 4.5 V to 5.5 V $V_{CC} = \text{Min}, I_{OL} = 8$ mA | - | - | 0.4 | | |
| V_{IH} ^[9] | Input HIGH voltage | 1.65 V to 2.2 V | 1.4 | - | $V_{CC} + 0.2$ | V | |
| | | 2.2 V to 2.7 V | 2.0 | - | $V_{CC} + 0.3$ | | |
| | | 2.7 V to 3.6 V | 2.0 | - | $V_{CC} + 0.3$ | | |
| | | 4.5 V to 5.5 V | 2.0 | - | $V_{CC} + 0.5$ | | |
| V_{IL} ^[9] | Input LOW voltage | 1.65 V to 2.2 V | -0.2 | - | 0.4 | V | |
| | | 2.2 V to 2.7 V | -0.3 | - | 0.6 | | |
| | | 2.7 V to 3.6 V | -0.3 | - | 0.8 | | |
| | | 4.5 V to 5.5 V | -0.5 | - | 0.8 | | |
| I_{IX} | Input leakage current | $GND \leq V_{IN} \leq V_{CC}$ | -1.0 | - | +1.0 | μA | |
| I_{OZ} | Output leakage current | $GND \leq V_{OUT} \leq V_{CC}$, Output disabled | -1.0 | - | +1.0 | μA | |
| I_{CC} | Operating supply current | $V_{CC} = \text{Max}, I_{OUT} = 0$ mA, CMOS levels | f = 100 MHz | - | 90.0 | 110.0 | mA |
| | | | f = 66.7 MHz | - | 70.0 | 80.0 | |
| I_{SB1} | Automatic CE power down current – TTL inputs | Max V_{CC} , $\overline{CE} \geq V_{IH}$ ^[12] , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f _{MAX} | - | - | 40.0 | mA | |
| I_{SB2} | Automatic CE power down current – CMOS inputs | Max V_{CC} , $\overline{CE} \geq V_{CC} - 0.2$ V ^[12] , $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, f = 0 | - | 20.0 | 30.0 | mA | |

Notes

9. $V_{IL(\text{min})} = -2.0$ V and $V_{IH(\text{max})} = V_{CC} + 2$ V for pulse durations of less than 20 ns.

10. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at $V_{CC} = 1.8$ V (for a V_{CC} range of 1.65 V–2.2 V), $V_{CC} = 3$ V (for a V_{CC} range of 2.2 V–3.6 V), and $V_{CC} = 5$ V (for a V_{CC} range of 4.5 V–5.5 V), $T_A = 25$ °C.

11. This parameter is guaranteed by design and is not tested.

12. For all dual chip enable devices, \overline{CE} is the logical combination of \overline{CE}_1 and CE_2 . When \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or CE_2 is LOW, \overline{CE} is HIGH.



Capacitance

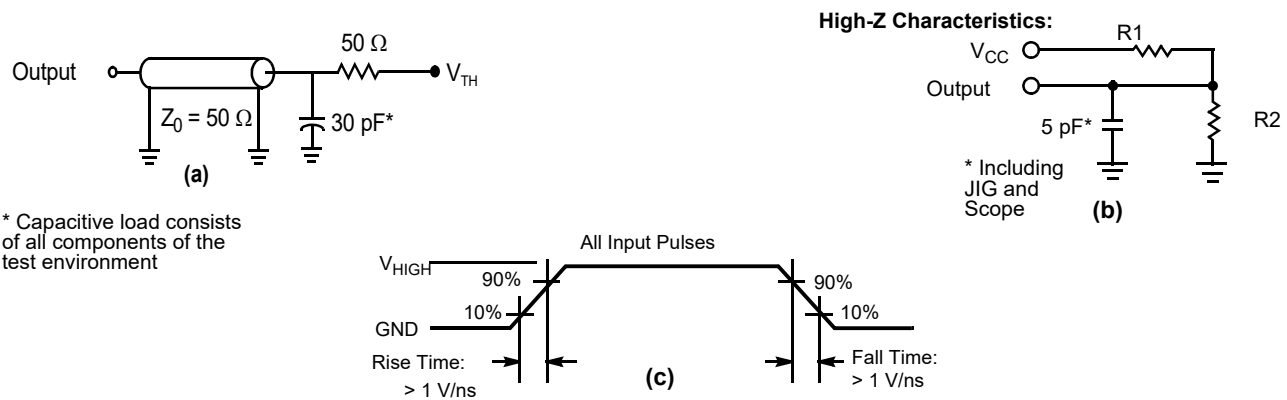
| Parameter ^[13] | Description | Test Conditions | 54-pin TSOP II | 48-ball VFBGA | 48-pin TSOP I | Unit |
|---------------------------|-------------------|---|----------------|---------------|---------------|------|
| C_{IN} | Input capacitance | $T_A = 25\text{ }^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = V_{CC(\text{typ})}$ | 10 | 10 | 10 | pF |
| C_{OUT} | I/O capacitance | | 10 | 10 | 10 | pF |

Thermal Resistance

| Parameter ^[13] | Description | Test Conditions | 54-pin TSOP II | 48-ball VFBGA | 48-pin TSOP I | Unit |
|---------------------------|--|---|----------------|---------------|---------------|--------------------|
| θ_{JA} | Thermal resistance (junction to ambient) | Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board | 93.63 | 31.50 | 57.99 | $^\circ\text{C/W}$ |
| θ_{JC} | Thermal resistance (junction to case) | | 21.58 | 15.75 | 13.42 | $^\circ\text{C/W}$ |

AC Test Loads and Waveforms

Figure 11. AC Test Loads and Waveforms^[14]



| Parameters | 1.8 V | 3.0 V | 5.0 V | Unit |
|------------|-------|-------|-------|----------|
| R1 | 1667 | 317 | 317 | Ω |
| R2 | 1538 | 351 | 351 | Ω |
| V_{TH} | 0.9 | 1.5 | 1.5 | V |
| V_{HIGH} | 1.8 | 3 | 3 | V |

Notes

13. Tested initially and after any design or process changes that may affect these parameters.

14. Full-device AC operation assumes a 100- μs ramp time from 0 to V_{CC} (min) and 100- μs wait time after V_{CC} stabilizes to its operational value.



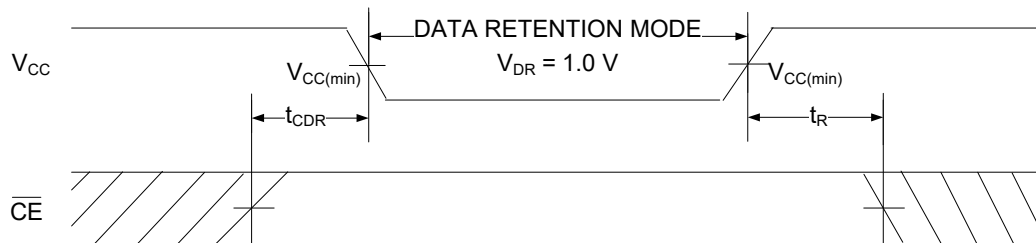
Data Retention Characteristics

Over the operating range of $-40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$

| Parameter | Description | Conditions | Min | Max | Unit |
|------------------|--------------------------------------|--|------|------|------|
| V_{DR} | V_{CC} for data retention | | 1.0 | – | V |
| I_{CCDR} | Data retention current | $V_{CC} = V_{DR}$, $\overline{CE} \geq V_{CC} - 0.2\text{ V}^{[15]}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$ | – | 30.0 | mA |
| $t_{CDR}^{[16]}$ | Chip deselect to data retention time | | 0 | – | ns |
| $t_R^{[16, 17]}$ | Operation recovery time | $V_{CC} \geq 2.2\text{ V}$ | 10.0 | – | ns |
| | | $V_{CC} < 2.2\text{ V}$ | 15.0 | – | ns |

Data Retention Waveform

Figure 12. Data Retention Waveform ^[15]



Notes

15. For all dual chip enable devices, \overline{CE} is the logical combination of \overline{CE}_1 and CE_2 . When \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or CE_2 is LOW, \overline{CE} is HIGH.
16. This parameter is guaranteed by design and is not tested
17. Full-device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC}(\text{min}) \geq 100\text{ }\mu\text{s}$ or stable at $V_{CC}(\text{min}) \geq 100\text{ }\mu\text{s}$.



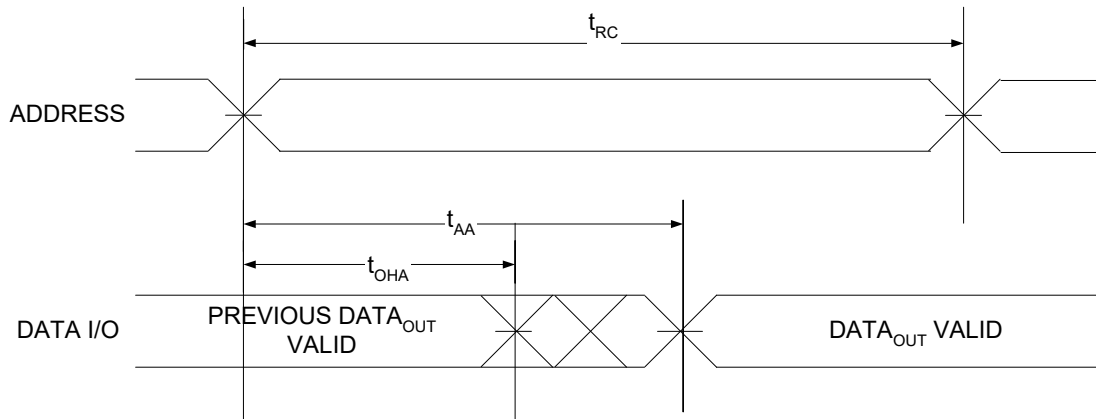
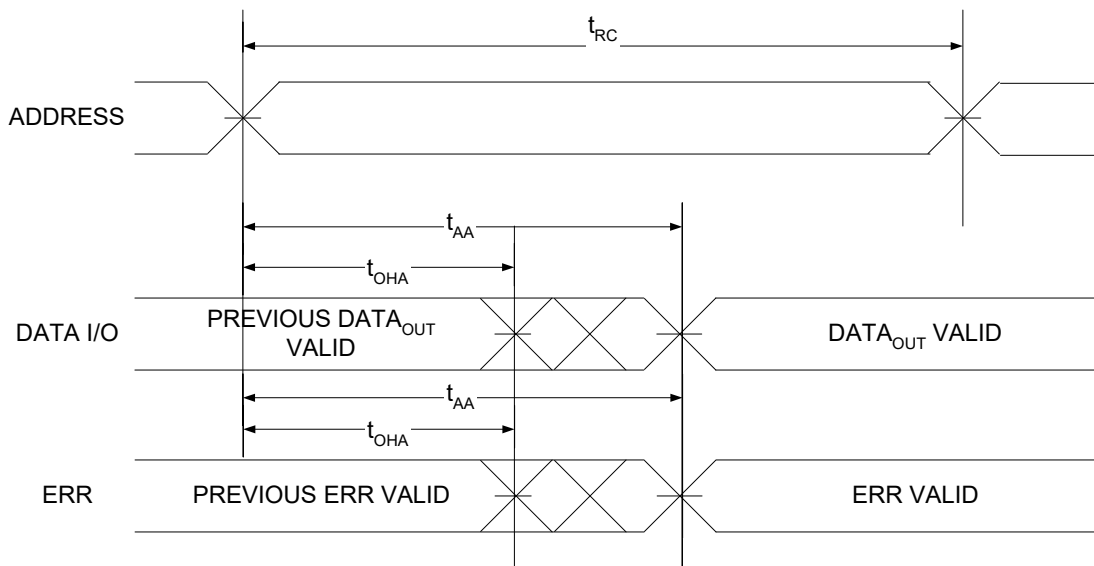
AC Switching Characteristics

Over the operating range of $-40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$

| Parameter ^[18] | Description | 10 ns | | 15 ns | | Unit |
|--|---|-------|------|-------|------|---------------|
| | | Min | Max | Min | Max | |
| Read Cycle | | | | | | |
| t_{POWER} | V_{CC} (stable) to the first access ^[19, 20] | 100.0 | – | 100.0 | – | μs |
| t_{RC} | Read cycle time | 10.0 | – | 15.0 | – | ns |
| t_{AA} | Address to data / ERR valid | – | 10.0 | – | 15.0 | ns |
| t_{OHA} | Data / ERR hold from address change | 3.0 | – | 3.0 | – | ns |
| t_{ACE} | $\overline{\text{CE}}$ LOW to data / ERR valid ^[21] | – | 10.0 | – | 15.0 | ns |
| t_{DOE} | $\overline{\text{OE}}$ LOW to data / ERR valid | – | 5.0 | – | 8.0 | ns |
| t_{LZOE} | $\overline{\text{OE}}$ LOW to low Z ^[22, 23, 24] | 0 | – | 1.0 | – | ns |
| t_{HZOE} | $\overline{\text{OE}}$ HIGH to high Z ^[22, 23, 24] | – | 5.0 | – | 8.0 | ns |
| t_{LZCE} | $\overline{\text{CE}}$ LOW to low Z ^[21, 22, 23, 24] | 3.0 | – | 3.0 | – | ns |
| t_{HZCE} | $\overline{\text{CE}}$ HIGH to high Z ^[21, 22, 23, 24] | – | 5.0 | – | 8.0 | ns |
| t_{PU} | $\overline{\text{CE}}$ LOW to power-up ^[20, 21] | 0 | – | 0 | – | ns |
| t_{PD} | $\overline{\text{CE}}$ HIGH to power-down ^[20, 21] | – | 10.0 | – | 15.0 | ns |
| t_{DBE} | Byte enable to data valid | – | 5.0 | – | 8.0 | ns |
| t_{LZBE} | Byte enable to low Z ^[22, 23] | 0 | – | 1.0 | – | ns |
| t_{HZBE} | Byte disable to high Z ^[22, 23] | – | 6.0 | – | 8.0 | ns |
| Write Cycle ^[25, 26] | | | | | | |
| t_{WC} | Write cycle time | 10.0 | – | 15.0 | – | ns |
| t_{SCE} | $\overline{\text{CE}}$ LOW to write end ^[21] | 7.0 | – | 12.0 | – | ns |
| t_{AW} | Address setup to write end | 7.0 | – | 12.0 | – | ns |
| t_{HA} | Address hold from write end | 0 | – | 0 | – | ns |
| t_{SA} | Address setup to write start | 0 | – | 0 | – | ns |
| t_{PWE} | $\overline{\text{WE}}$ pulse width | 7.0 | – | 12.0 | – | ns |
| t_{SD} | Data setup to write end | 5.0 | – | 8.0 | – | ns |
| t_{HD} | Data hold from write end | 0 | – | 0 | – | ns |
| t_{LZWE} | $\overline{\text{WE}}$ HIGH to low Z ^[22, 23, 24] | 3.0 | – | 3.0 | – | ns |
| t_{HZWE} | $\overline{\text{WE}}$ LOW to high Z ^[22, 23, 24] | – | 5.0 | – | 8.0 | ns |
| t_{BW} | Byte Enable to write end | 7.0 | – | 12.0 | – | ns |

Notes

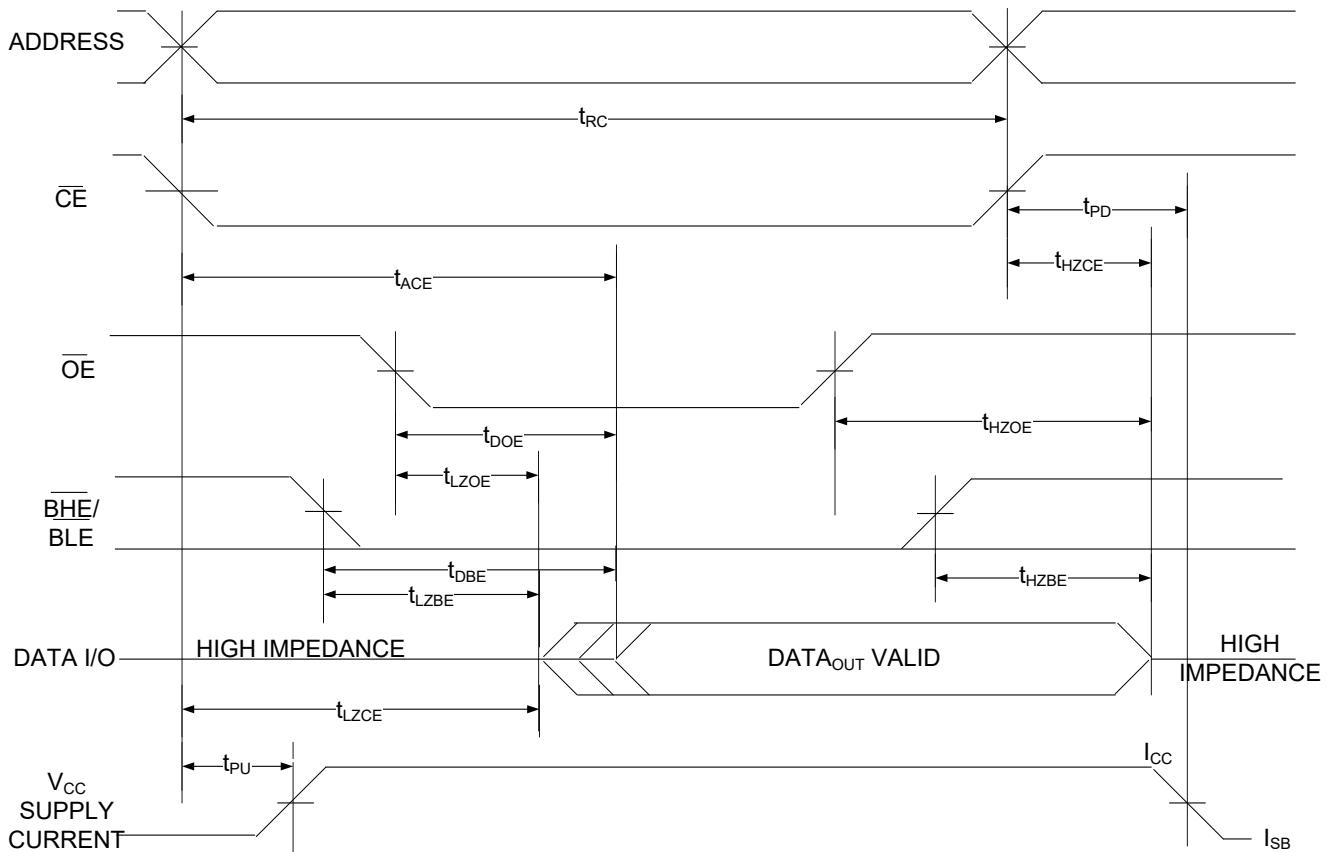
18. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{\text{CC}} \geq 3\text{ V}$) and $V_{\text{CC}}/2$ (for $V_{\text{CC}} < 3\text{ V}$), and input pulse levels of 0 to 3 V (for $V_{\text{CC}} \geq 3\text{ V}$) and 0 to V_{CC} (for $V_{\text{CC}} < 3\text{ V}$). Test conditions for the read cycle use the output loading, shown in part (a) of [Figure 11 on page 8](#), unless specified otherwise.
19. t_{POWER} gives the minimum amount of time that the power supply is at stable V_{CC} until the first memory access is performed.
20. These parameters are guaranteed by design and are not tested.
21. For all dual chip enable devices, $\overline{\text{CE}}$ is the logical combination of $\overline{\text{CE}}_1$ and CE_2 . When $\overline{\text{CE}}_1$ is LOW and CE_2 is HIGH, $\overline{\text{CE}}$ is LOW; when $\overline{\text{CE}}_1$ is HIGH or CE_2 is LOW, $\overline{\text{CE}}$ is HIGH.
22. t_{HZOE} , t_{HZCE} , t_{HZWE} , and t_{HZBE} are specified with a load capacitance of 5 pF, as shown in part (b) of [Figure 11 on page 8](#). Hi-Z, Lo-Z transition is measured $\pm 200\text{ mV}$ from steady state voltage.
23. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.
24. Tested initially and after any design or process changes that may affect these parameters.
25. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}} = V_{\text{IL}}$, $\overline{\text{CE}} = V_{\text{IL}}$, and $\overline{\text{BHE}}$ or $\overline{\text{BLE}} = V_{\text{IL}}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
26. The minimum write pulse width for Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) should be sum of t_{HZWE} and t_{SD} .

Switching Waveforms**Figure 13. Read Cycle No. 1 of CY7C1061G (Address Transition Controlled)** [27, 28]**Figure 14. Read Cycle No. 2 of CY7C1061GE (Address Transition Controlled)** [27, 28]**Notes**

27. The device is continuously selected, $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IL}$, \overline{BHE} or \overline{BLE} or both = V_{IL} .
 28. \overline{WE} is HIGH for read cycle.



Switching Waveforms (continued)

Figure 15. Read Cycle No. 3 ($\overline{\text{OE}}$ Controlled) [29, 30, 31]**Notes**

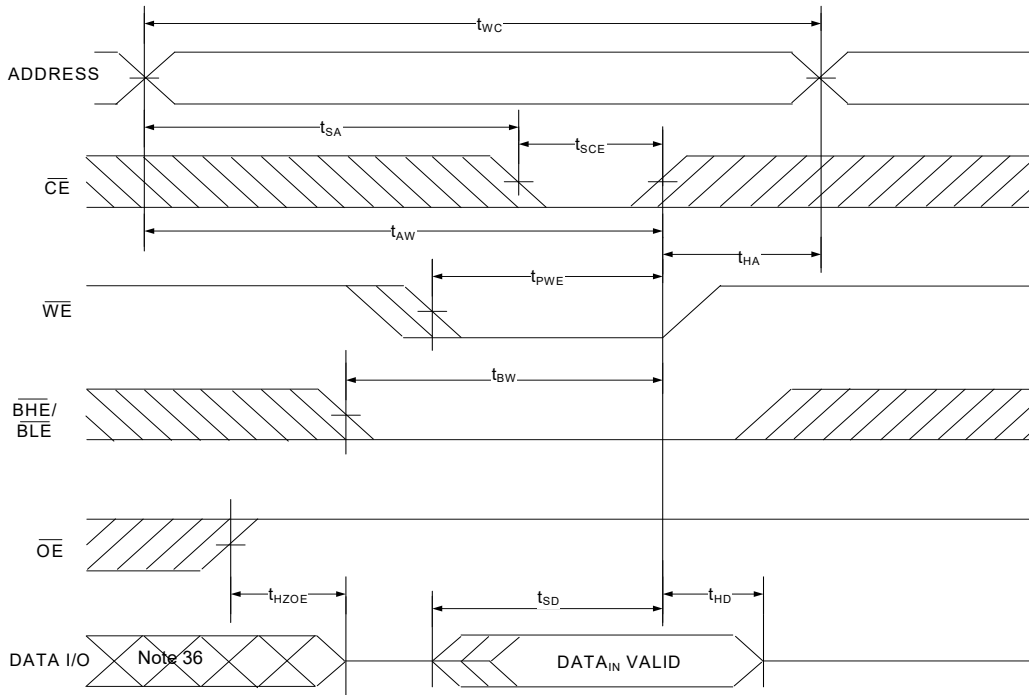
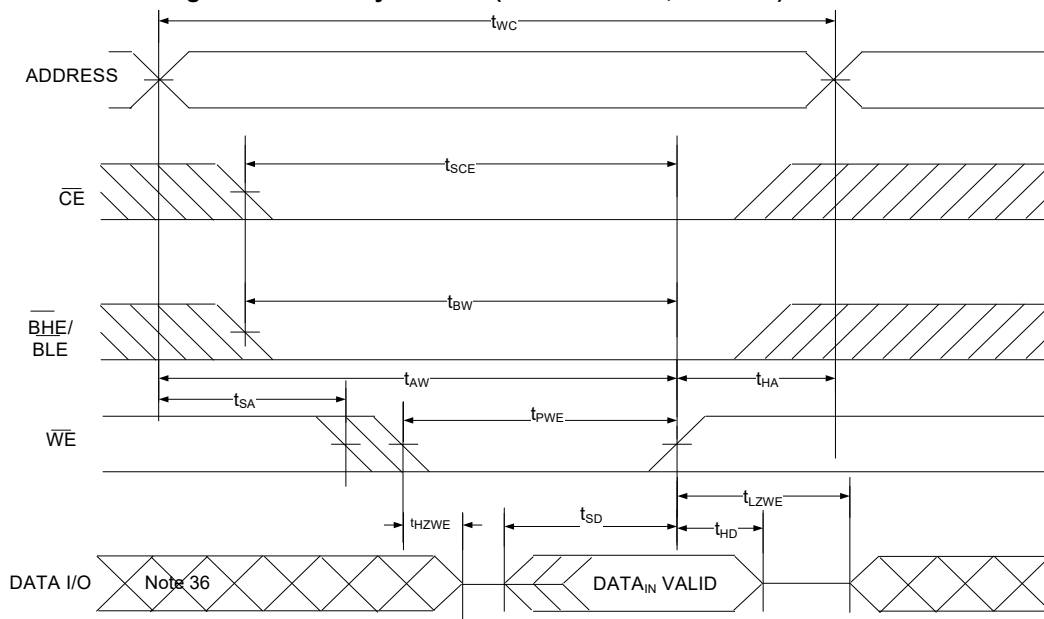
29. For all dual chip enable devices, $\overline{\text{CE}}$ is the logical combination of $\overline{\text{CE}}_1$ and CE_2 . When $\overline{\text{CE}}_1$ is LOW and CE_2 is HIGH, $\overline{\text{CE}}$ is LOW; when $\overline{\text{CE}}_1$ is HIGH or CE_2 is LOW, $\overline{\text{CE}}$ is HIGH.

30. $\overline{\text{WE}}$ is HIGH for read cycle.

31. Address valid prior to or coincident with $\overline{\text{CE}}$ LOW transition.



Switching Waveforms (continued)

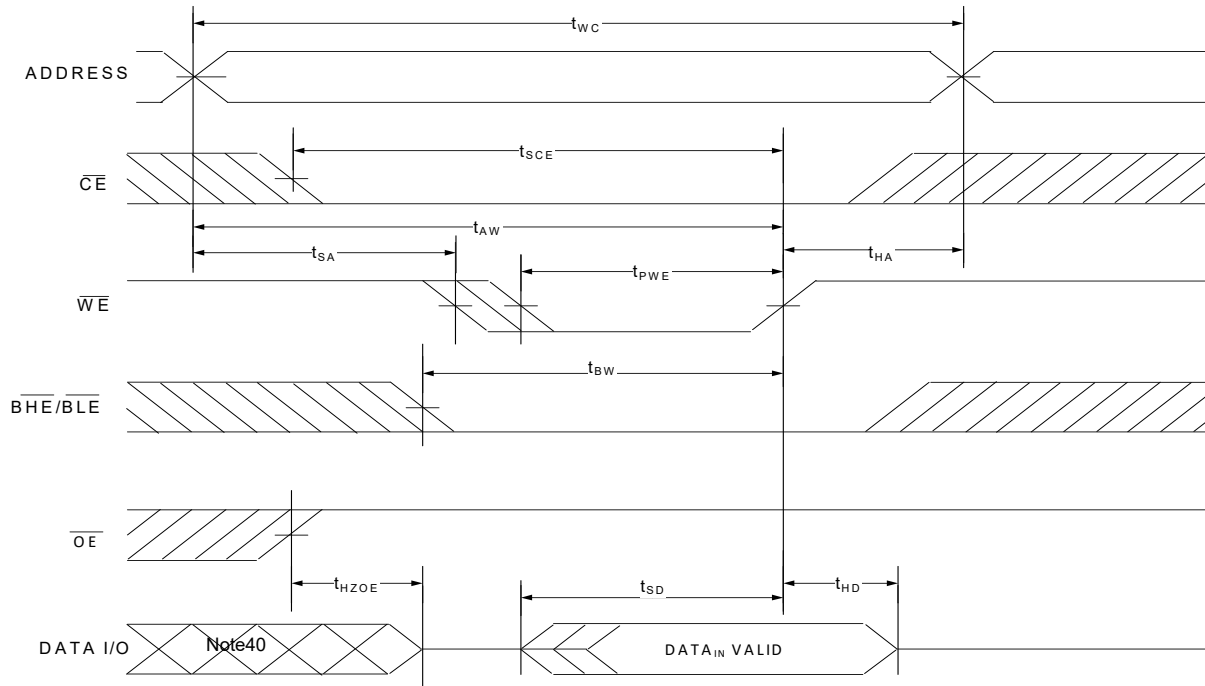
Figure 16. Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled) [32, 33, 34]Figure 17. Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW) [32, 33, 34, 35]

Notes

32. For all dual chip enable devices, $\overline{\text{CE}}$ is the logical combination of $\overline{\text{CE}}_1$ and CE_2 . When $\overline{\text{CE}}_1$ is LOW and CE_2 is HIGH, $\overline{\text{CE}}$ is LOW; when $\overline{\text{CE}}_1$ is HIGH or CE_2 is LOW, $\overline{\text{CE}}$ is HIGH.
33. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}} = V_{\text{IL}}$, $\overline{\text{CE}} = V_{\text{IL}}$ and $\overline{\text{BHE}}$ or $\overline{\text{BLE}} = V_{\text{IL}}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
34. Data I/O is in high-impedance state if $\overline{\text{CE}} = V_{\text{IH}}$, or $\overline{\text{OE}} = V_{\text{IH}}$ or $\overline{\text{BHE}}$, and/or $\overline{\text{BLE}} = V_{\text{IH}}$.
35. The minimum write cycle pulse width should be equal to sum of t_{HZWE} and t_{SD} .
36. During this period the I/Os are in output state. Do not apply input signals.



Switching Waveforms (continued)

Figure 18. Write Cycle No. 3 (\overline{WE} Controlled) [37, 38, 39]**Notes**

37. For all dual chip enable devices, \overline{CE} is the logical combination of \overline{CE}_1 and CE_2 . When \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or CE_2 is LOW, \overline{CE} is HIGH.

38. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$ and \overline{BHE} or $\overline{BLE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.

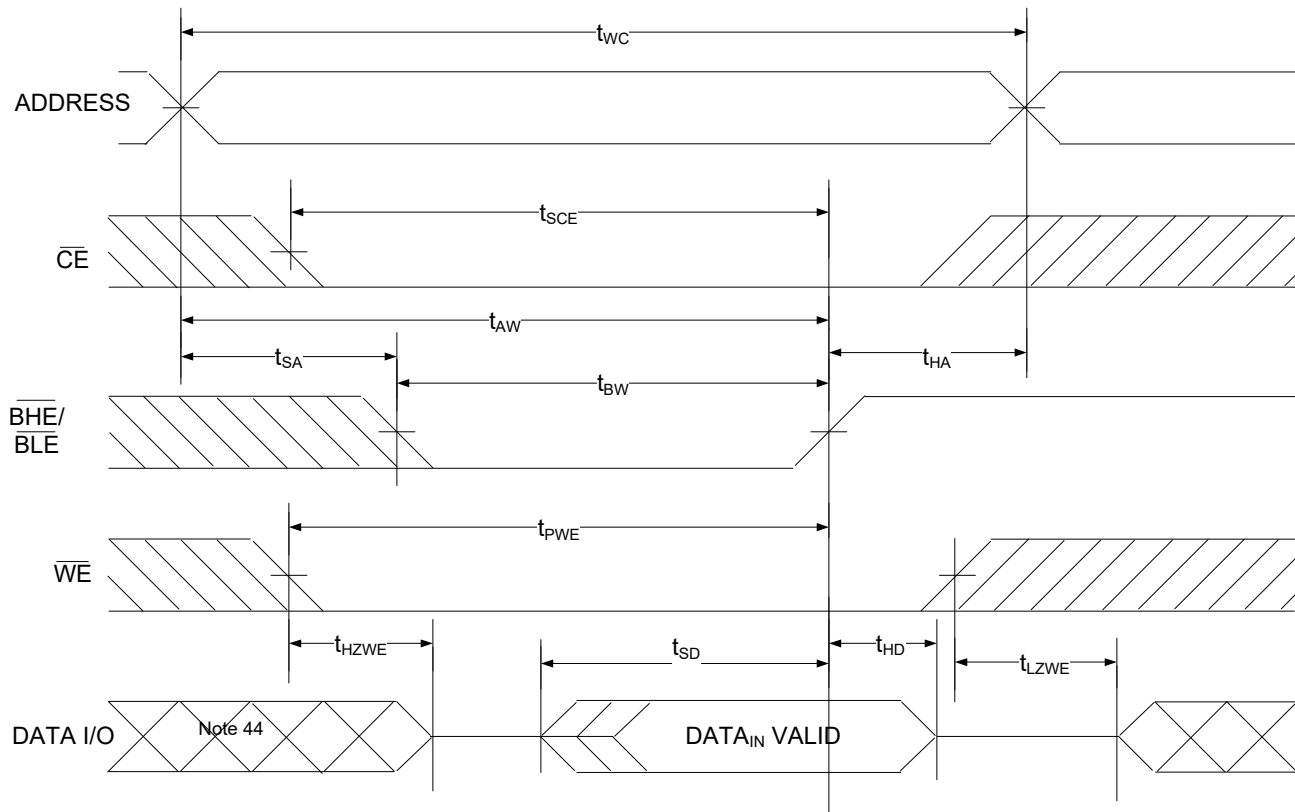
39. Data I/O is in high-impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$ or \overline{BHE} , and/or $\overline{BLE} = V_{IH}$.

40. During this period, the I/Os are in output state. Do not apply input signals.



Switching Waveforms (continued)

Figure 19. Write Cycle No. 4 (BLE or BHE Controlled) [41, 42, 43]



Notes

41. For all dual chip enable devices, \overline{CE} is the logical combination of \overline{CE}_1 and CE_2 . When \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or CE_2 is LOW, \overline{CE} is HIGH.
42. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$ and \overline{BHE} or $\overline{BLE} = V_{IL}$. These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
43. Data I/O is in high-impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$ or \overline{BHE} , and/or $\overline{BLE} = V_{IH}$.
44. During this period, the I/Os are in output state. Do not apply input signals.



Truth Table

| \overline{CE} [45] | \overline{OE} | \overline{WE} | \overline{BLE} | \overline{BHE} | I/O ₀ -I/O ₇ | I/O ₈ -I/O ₁₅ | Mode | Power |
|----------------------|-------------------|-------------------|-------------------|-------------------|------------------------------------|-------------------------------------|----------------------------|----------------------------|
| H | X ^[46] | X ^[46] | X ^[46] | X ^[46] | High-Z | High-Z | Power down | Standby (I _{SB}) |
| L | L | H | L | L | Data out | Data out | Read all bits | Active (I _{CC}) |
| L | L | H | L | H | Data out | High-Z | Read lower bits only | Active (I _{CC}) |
| L | L | H | H | L | High-Z | Data out | Read upper bits only | Active (I _{CC}) |
| L | X | L | L | L | Data in | Data in | Write all bits | Active (I _{CC}) |
| L | X | L | L | H | Data in | High-Z | Write lower bits only | Active (I _{CC}) |
| L | X | L | H | L | High-Z | Data in | Write upper bits only | Active (I _{CC}) |
| L | H | H | X | X | High-Z | High-Z | Selected, outputs disabled | Active (I _{CC}) |
| L | X | X | H | H | High-Z | High-Z | Selected, outputs disabled | Active (I _{CC}) |

ERR Output – CY7C1061GE

| Output [47] | Mode |
|-------------|--|
| 0 | Read operation, no single-bit error in the stored data. |
| 1 | Read operation, single-bit error detected and corrected. |
| High-Z | Device deselected or outputs disabled or Write operation |

Notes

45. For all dual chip enable devices, \overline{CE} is the logical combination of \overline{CE}_1 and CE_2 . When \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or CE_2 is LOW, \overline{CE} is HIGH.

46. The input voltage levels on these pins should be either at V_{IH} or V_{IL} .

47. ERR is an Output pin. If not used, this pin should be left floating.



Ordering Information

| Speed (ns) | Voltage Range | Ordering Code | Package Diagram | Package Type (all Pb-free) | Key Features / Differentiators | ERR Pin / Ball | Operating Range | | | |
|--------------------|------------------|----------------------|----------------------|----------------------------|--|--|--|--|--|-----|
| 10 | 4.5 V–5.5 V | CY7C1061G-10BV1XI | 51-85150 | 48-ball VFBGA | Single Chip Enable, Address MSB A19 at ball G2 | No | Industrial | | | |
| | | CY7C1061GE-10BV1XI | | | | Yes | | | | |
| | | CY7C1061G-10BVJXI | | | 51-85160 | 54-pin TSOP II | | Dual Chip Enable, Address MSB A19 at ball G2 | No | |
| | | CY7C1061GE-10BVJXI | | | | | | | Yes | |
| | | CY7C1061G-10BVXI | | | 51-85183 | 48-pin TSOP I | | Single Chip Enable | No | |
| | | CY7C1061GE-10BVXI | | | | | | | Yes | |
| | | CY7C1061G-10ZSXI | | | 51-85160 | 54-pin TSOP II | | Dual Chip Enable | No | |
| | | CY7C1061GE-10ZSXI | | | | | | | Yes | |
| | | CY7C1061G-10ZXI | | | 51-85183 | 48-pin TSOP I | | Single Chip Enable | No | |
| | CY7C1061GE-10ZXI | Yes | | | | | | | | |
| | 2.2 V–3.6 V | 2.2 V–3.6 V | CY7C1061G30-10BV1XI | 51-85150 | 48-ball VFBGA | Single Chip Enable, Address MSB A19 at ball G2 | | No | | |
| | | | CY7C1061GE30-10BV1XI | | | | | Yes | | |
| | | | CY7C1061G30-10BVJXI | | | 51-85160 | | 54-pin TSOP II | Dual Chip Enable, Address MSB A19 at ball G2 | No |
| | | | CY7C1061GE30-10BVJXI | | | | | | | Yes |
| | | | CY7C1061G30-10BVXI | | | 51-85183 | | 48-pin TSOP I | Single Chip Enable | No |
| | | | CY7C1061GE30-10BVXI | | | | | | | Yes |
| | | | CY7C1061G30-10ZSXI | | | 51-85160 | | 54-pin TSOP II | Dual Chip Enable | No |
| | | | CY7C1061GE30-10ZSXI | | | | | | | Yes |
| CY7C1061G30-10ZXI | | | 51-85183 | | | 48-pin TSOP I | Single Chip Enable | No | | |
| CY7C1061GE30-10ZXI | Yes | | | | | | | | | |
| 15 | 1.65 V–2.2 V | CY7C1061GE18-15BV1XI | 51-85150 | 48-ball VFBGA | Single Chip Enable, Address MSB A19 at ball G2 | Yes | | | | |
| | | CY7C1061G18-15BV1XI | | | | No | | | | |
| | | CY7C1061GE18-15BVJXI | | | 51-85160 | 54-pin TSOP II | Dual Chip Enable, Address MSB A19 at ball G2 | Yes | | |
| | | CY7C1061G18-15BVJXI | | | | | | No | | |
| | | CY7C1061GE18-15BVXI | | | 51-85183 | 48-pin TSOP I | Dual Chip Enable, Address MSB A19 at ball H6 | Yes | | |
| | | CY7C1061G18-15BVXI | | | | | | No | | |
| | | CY7C1061GE18-15ZSXI | | | 51-85160 | 54-pin TSOP II | Dual Chip Enable | Yes | | |
| | | CY7C1061G18-15ZSXI | | | | | | No | | |
| | | CY7C1061GE18-15ZXI | | | 51-85183 | 48-pin TSOP I | Single Chip Enable | Yes | | |
| | | CY7C1061G18-15ZXI | | | | | | No | | |



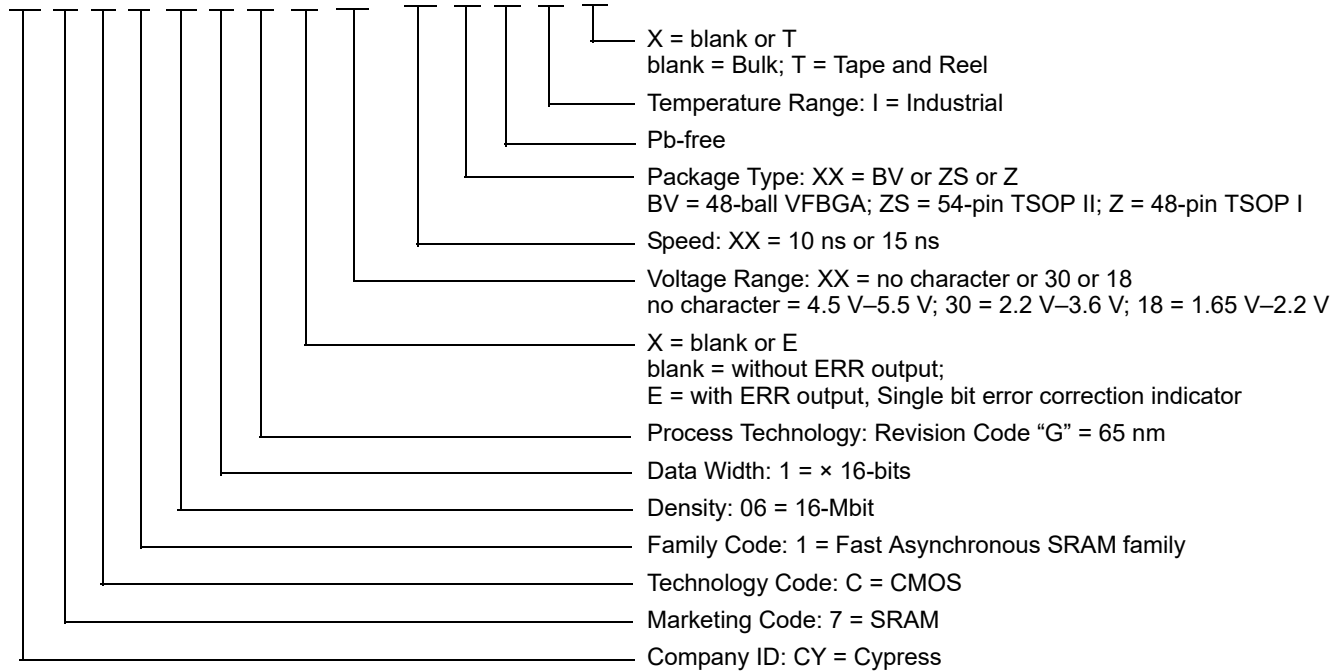
Ordering Information (continued)

| Speed (ns) | Voltage Range | Ordering Code | Package Diagram | Package Type (all Pb-free) | Key Features / Differentiators | ERR Pin / Ball | Operating Range | | |
|---------------------|-------------------|-----------------------|-----------------|-----------------------------------|---|---|-----------------------------------|-----------------------------------|----|
| 10 | 4.5 V–5.5 V | CY7C1061G-10BV1XIT | 51-85150 | 48-ball VFBGA | Single Chip Enable, Address MSB A19 at ball G2, Tape and Reel | No | Industrial | | |
| | | CY7C1061GE-10BV1XIT | | | | Yes | | | |
| | | CY7C1061G-10BVJXIT | | | Dual Chip Enable, Address MSB A19 at ball G2, Tape and Reel | No | | | |
| | | CY7C1061GE-10BVJXIT | | | | Yes | | | |
| | | CY7C1061G-10BVXIT | | | Dual Chip Enable, Address MSB A19 at ball H6, Tape and Reel | No | | | |
| | | CY7C1061GE-10BVXIT | | | | Yes | | | |
| | | CY7C1061G-10ZSXIT | | | 51-85160 | 54-pin TSOP II | | Dual Chip Enable, Tape and Reel | No |
| | | CY7C1061GE-10ZSXIT | | | Yes | | | | |
| | | CY7C1061G-10ZXIT | | | 51-85183 | 48-pin TSOP I | | Single Chip Enable, Tape and Reel | No |
| | CY7C1061GE-10ZXIT | Yes | | | | | | | |
| | 2.2 V–3.6 V | CY7C1061G30-10BV1XIT | 51-85150 | 48-ball VFBGA | Single Chip Enable, Address MSB A19 at ball G2, Tape and Reel | No | | | |
| | | | | | | CY7C1061GE30-10BV1XIT | | Yes | |
| | | | | | CY7C1061G30-10BVJXIT | Dual Chip Enable, Address MSB A19 at ball G2, Tape and Reel | | No | |
| | | | | | CY7C1061GE30-10BVJXIT | | | Yes | |
| | | | | | CY7C1061G30-10BVXIT | Dual Chip Enable, Address MSB A19 at ball H6, Tape and Reel | | No | |
| | | | | | CY7C1061GE30-10BVXIT | | | Yes | |
| | | CY7C1061G30-10ZSXIT | 51-85160 | 54-pin TSOP II | Dual Chip Enable, Tape and Reel | No | | | |
| | | CY7C1061GE30-10ZSXIT | Yes | | | | | | |
| CY7C1061G30-10ZXIT | | 51-85183 | 48-pin TSOP I | Single Chip Enable, Tape and Reel | No | | | | |
| CY7C1061GE30-10ZXIT | Yes | | | | | | | | |
| 15 | 1.65 V–2.2 V | CY7C1061GE18-15BV1XIT | 51-85150 | 48-ball VFBGA | Single Chip Enable, Address MSB A19 at ball G2, Tape and Reel | Yes | | | |
| | | CY7C1061G18-15BV1XIT | | | | No | | | |
| | | CY7C1061GE18-15BVJXIT | | | Dual Chip Enable, Address MSB A19 at ball G2, Tape and Reel | Yes | | | |
| | | CY7C1061G18-15BVJXIT | | | | No | | | |
| | | CY7C1061GE18-15BVXIT | | | Dual Chip Enable, Address MSB A19 at ball H6, Tape and Reel | Yes | | | |
| | | CY7C1061G18-15BVXIT | | | | No | | | |
| | | CY7C1061GE18-15ZSXIT | | | 51-85160 | 54-pin TSOP II | Dual Chip Enable, Tape and Reel | Yes | |
| | | CY7C1061G18-15ZSXIT | | | No | | | | |
| | | CY7C1061GE18-15ZXIT | | | 51-85183 | 48-pin TSOP I | Single Chip Enable, Tape and Reel | Yes | |
| | | CY7C1061G18-15ZXIT | | | No | | | | |



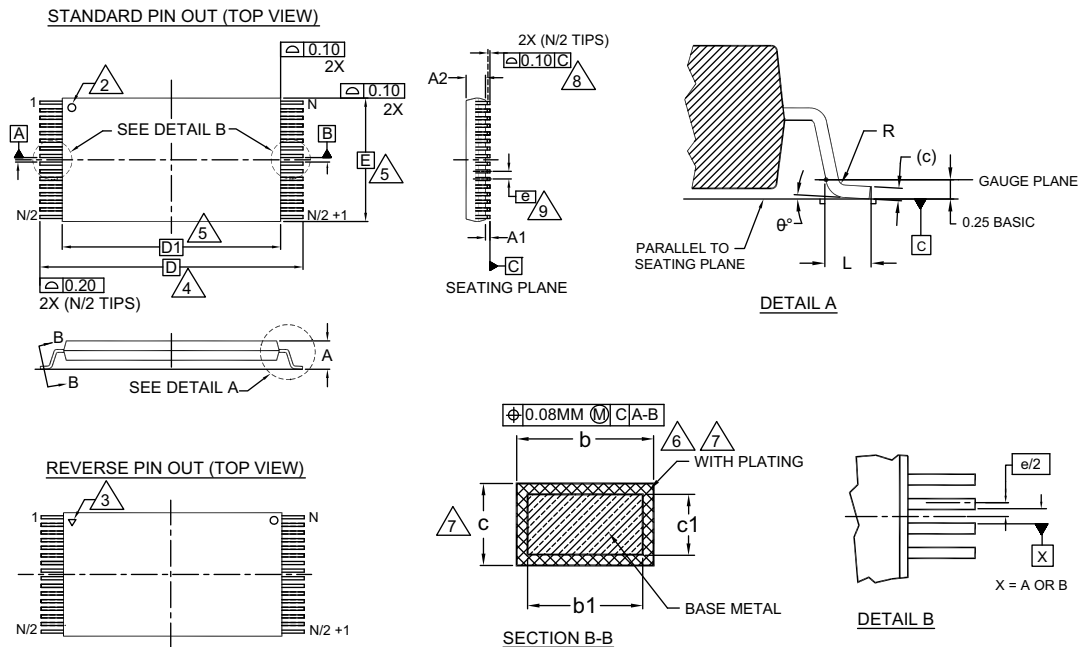
Ordering Code Definitions

CY 7 C 1 06 1 G E XX - XX XX X I X



Package Diagrams

Figure 20. 48-pin TSOP I (12 × 18.4 × 1.0 mm) Z48A Package Outline, 51-85183



| SYMBOL | DIMENSIONS | | |
|----------|-------------|------|------|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.20 |
| A1 | 0.05 | — | 0.15 |
| A2 | 0.95 | 1.00 | 1.05 |
| b1 | 0.17 | 0.20 | 0.23 |
| b | 0.17 | 0.22 | 0.27 |
| c1 | 0.10 | — | 0.16 |
| c | 0.10 | — | 0.21 |
| D | 20.00 BASIC | | |
| D1 | 18.40 BASIC | | |
| E | 12.00 BASIC | | |
| e | 0.50 BASIC | | |
| L | 0.50 | 0.60 | 0.70 |
| θ | 0° | — | 8 |
| R | 0.08 | — | 0.20 |
| N | 48 | | |

NOTES:

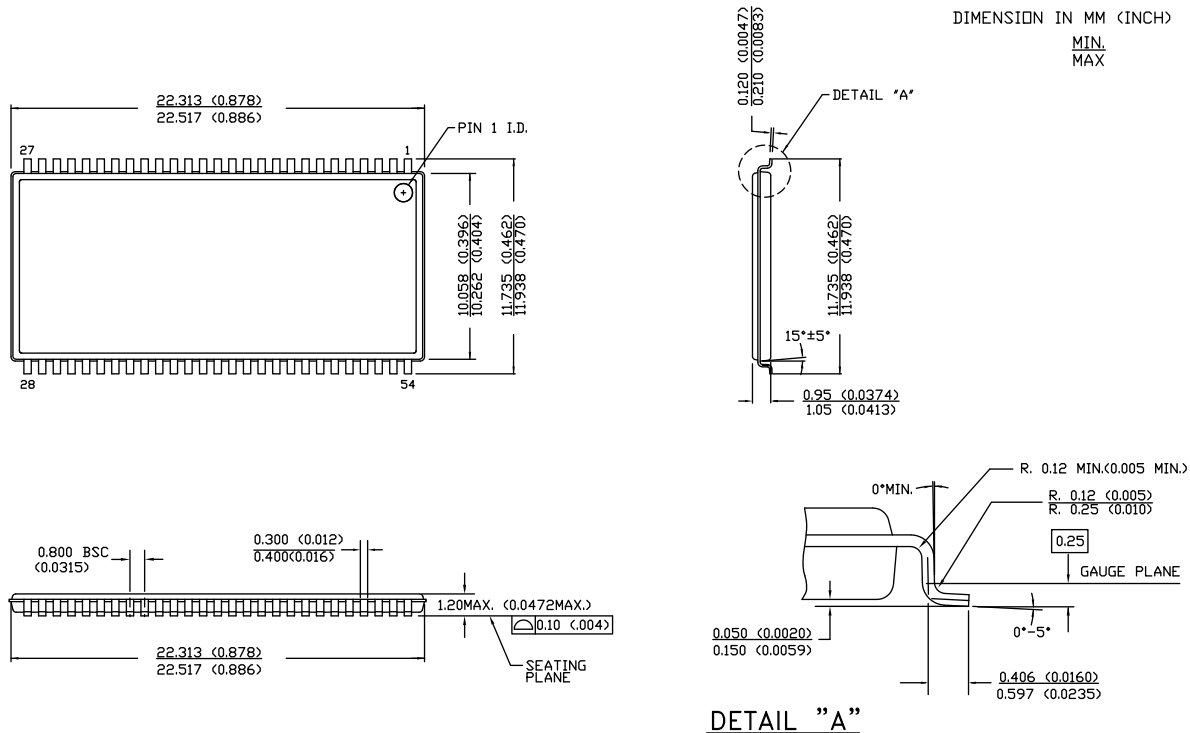
1. DIMENSIONS ARE IN MILLIMETERS (mm).
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE [C]. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm.
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.
10. JEDEC SPECIFICATION NO. REF: MO-142(D)DD.

51-85183 *F



Package Diagrams (continued)

Figure 21. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) Z54-II Package Outline, 51-85160

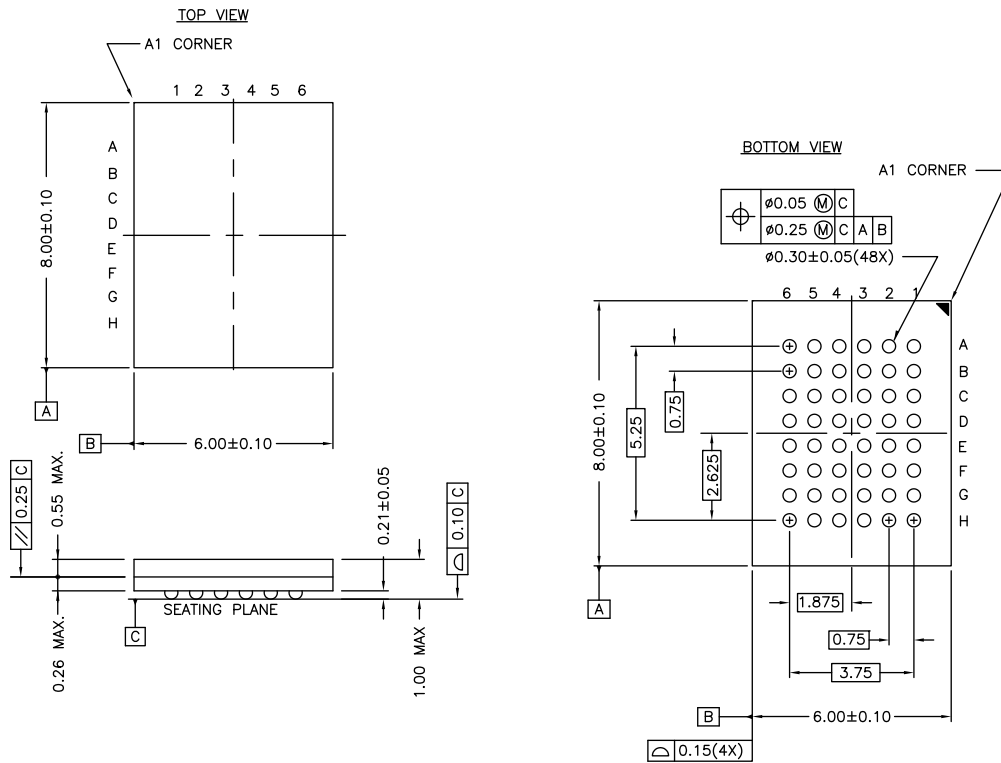


51-85160 *E



Package Diagrams (continued)

Figure 22. 48-ball VFBGA (6 × 8 × 1.0 mm) BV48/BZ48 Package Outline, 51-85150



NOTE:
 PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H



Acronyms

| Acronym | Description |
|-------------------------|---|
| $\overline{\text{BHE}}$ | Byte High Enable |
| $\overline{\text{BLE}}$ | Byte Low Enable |
| $\overline{\text{CE}}$ | Chip Enable |
| CMOS | Complementary Metal Oxide Semiconductor |
| I/O | Input/Output |
| $\overline{\text{OE}}$ | Output Enable |
| SRAM | Static Random Access Memory |
| TSOP | Thin Small Outline Package |
| TTL | Transistor-Transistor Logic |
| VFBGA | Very Fine-Pitch Ball Grid Array |
| $\overline{\text{WE}}$ | Write Enable |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|--------------------|-----------------|
| $^{\circ}\text{C}$ | degree Celsius |
| MHz | megahertz |
| μA | microampere |
| μs | microsecond |
| mA | milliampere |
| mm | millimeter |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| V | volt |
| W | watt |



Document History Page

| Document Title: CY7C1061G/CY7C1061GE, 16-Mbit (1M words × 16-bit) Static RAM with Error-Correcting Code (ECC) Document Number: 001-81540 | | | | |
|---|---------|-----------------|-----------------|---|
| Rev. | ECN No. | Orig. of Change | Submission Date | Description of Change |
| *P | 4791835 | NILE | 06/09/2015 | Changed status from Preliminary to Final. |
| *Q | 5436639 | NILE | 09/14/2016 | Updated Maximum Ratings : Updated Note 9 (Replaced “2 ns” with “20 ns”). Updated DC Electrical Characteristics : Removed Operating Range “2.7 V to 3.6 V” and all values corresponding to V _{OH} parameter. Included Operating Ranges “2.7 V to 3.0 V” and “3.0 V to 3.6 V” and all values corresponding to V _{OH} parameter. Changed minimum value of V _{IH} parameter from 2.2 V to 2 V corresponding to Operating Range “4.5 V to 5.5 V”. Updated Ordering Information : Updated part numbers. Updated to new template. |
| *R | 5580947 | NILE | 01/10/2017 | Updated Logic Block Diagram – CY7C1061G . Updated Package Diagrams : spec 51-85183 – Changed revision from *D to *F. Updated to new template. |
| *S | 5775815 | AESATMP9 | 06/16/2017 | Updated logo and copyright. |
| *T | 6245720 | NILE | 07/13/2018 | Updated Features : Added Note 2 and referred the same note in “Embedded error-correcting code (ECC) for single-bit error correction”. Updated to new template. Completing Sunset Review. |



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