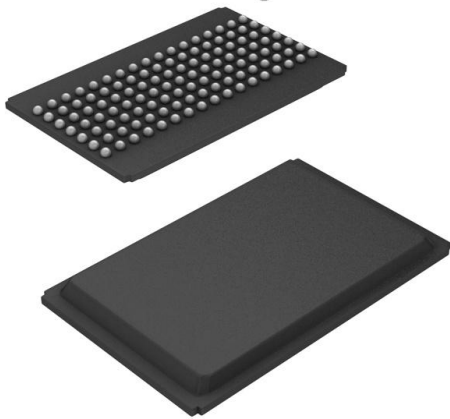


# CY7C1062GE30-10BGXI Datasheet

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DiGi Electronics Part Number	CY7C1062GE30-10BGXI-DG
Manufacturer	<a href="#">Infineon Technologies</a>
Manufacturer Product Number	CY7C1062GE30-10BGXI
Description	IC SRAM 16MBIT PARALLEL 119PBGA
Detailed Description	SRAM - Asynchronous Memory IC 16Mbit Parallel 10 ns 119-PBGA (14x22)

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## Purchase and inquiry

Manufacturer Product Number:

CY7C1062GE30-10BGXI

Series:

-

DiGi-Electronics Programmable:

Not Verified

Memory Format:

SRAM

Memory Size:

16Mbit

Memory Interface:

Parallel

Access Time:

10 ns

Operating Temperature:

-40°C ~ 85°C (TA)

Package / Case:

119-BGA

Base Product Number:

CY7C1062

Manufacturer:

Infineon Technologies

Product Status:

Active

Memory Type:

Volatile

Technology:

SRAM - Asynchronous

Memory Organization:

512K x 32

Write Cycle Time - Word, Page:

10ns

Voltage - Supply:

2.2V ~ 3.6V

Mounting Type:

Surface Mount

Supplier Device Package:

119-PBGA (14x22)

## Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.32.0041

Moisture Sensitivity Level (MSL):

3 (168 Hours)

ECCN:

3A991B2A



**CY7C1062G**  
**CY7C1062GE**

## 16-Mbit (512 K words × 32 bits) Static RAM with Error-Correcting Code (ECC)

### Features

- High speed
  - $t_{AA} = 10 \text{ ns}/15 \text{ ns}$
- Embedded error-correcting code (ECC) for single-bit error correction
- Low active and standby current
  - $I_{CC} = 90 \text{ mA}$  typical
  - $I_{SB2} = 20 \text{ mA}$  typical
- Operating voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V
- 1.0-V data retention
- Automatic power-down when deselected
- Transistor-transistor logic (TTL) compatible inputs and outputs
- ERR pin to indicate 1-bit error detection and correction
- Available in Pb-free 119-ball plastic ball grid array (PBGA) package

### Functional Description

CY7C1062G and CY7C1062GE are high-performance CMOS fast static RAM devices with embedded ECC. Both have three chip enables, giving easy memory expansion features. The CY7C1062GE device includes an error indication pin that signals the host processor in the case of a single bit error-detection and correction event.

To write to the device, take Chip Enables ( $\overline{CE}_1$ ,  $\overline{CE}_2$ , and  $\overline{CE}_3$  LOW) and Write Enable ( $\overline{WE}$ ) input LOW. If Byte Enable A ( $\overline{B}_A$ ) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>18</sub>). If Byte Enable B ( $\overline{B}_B$ ) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>18</sub>). Likewise,  $\overline{B}_C$  and  $\overline{B}_D$  correspond with the I/O pins I/O<sub>16</sub> to I/O<sub>23</sub> and I/O<sub>24</sub> to I/O<sub>31</sub>, respectively.

To read from the device, take Chip Enables ( $\overline{CE}_1$ ,  $\overline{CE}_2$ , and  $\overline{CE}_3$  LOW) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If the first  $\overline{B}_A$  is LOW, then data from the memory location specified by the address pins appear on I/O<sub>0</sub> to I/O<sub>7</sub>. If  $\overline{B}_B$  is LOW, then data from memory appears on I/O<sub>8</sub> to I/O<sub>15</sub>. Likewise,  $\overline{B}_C$  and  $\overline{B}_D$  correspond to the third and fourth bytes. See [Truth Table – CY7C1062G/CY7C1062GE on page 15](#) for a complete description of read and write modes.

The input and output pins (I/O<sub>0</sub> through I/O<sub>31</sub>) are placed in a high-impedance state when the device is deselected ( $\overline{CE}_1$ ,  $\overline{CE}_2$ , or  $\overline{CE}_3$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), the byte selects are disabled ( $\overline{B}_{A-D}$  HIGH), or during a write operation ( $\overline{CE}_1$ ,  $\overline{CE}_2$  and  $\overline{CE}_3$  LOW and  $\overline{WE}$  LOW).

On the CY7C1062GE device, the detection and correction of a single-bit error in the accessed location is indicated by the assertion of the ERR output (ERR = High)<sup>1</sup>.

CY7C1062G and CY7C1062GE devices are available in Pb-free 119-ball plastic ball grid array (PBGA) package.

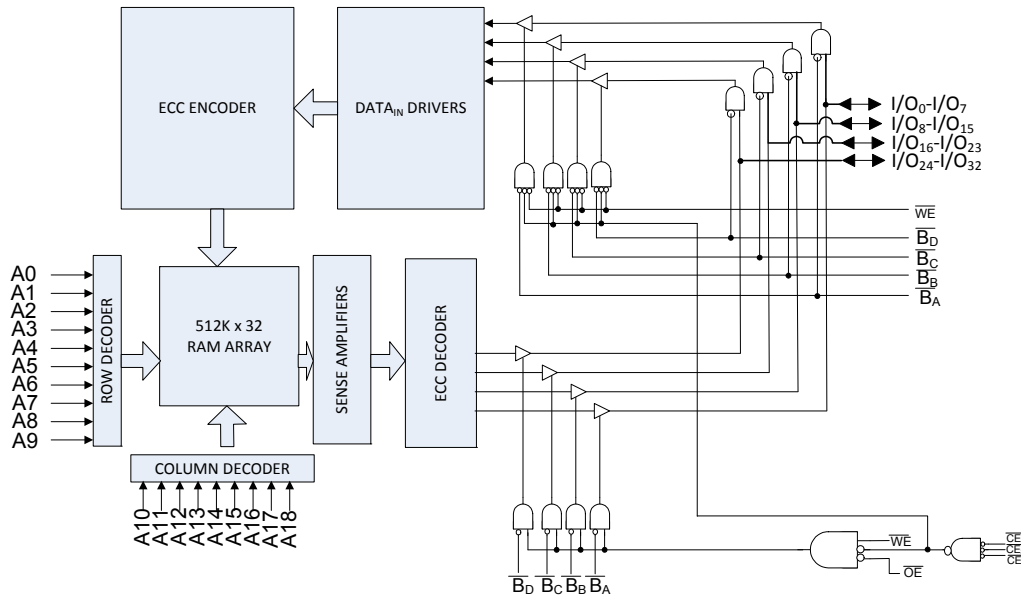
For a complete list of related documentation, click [here](#).

#### Note

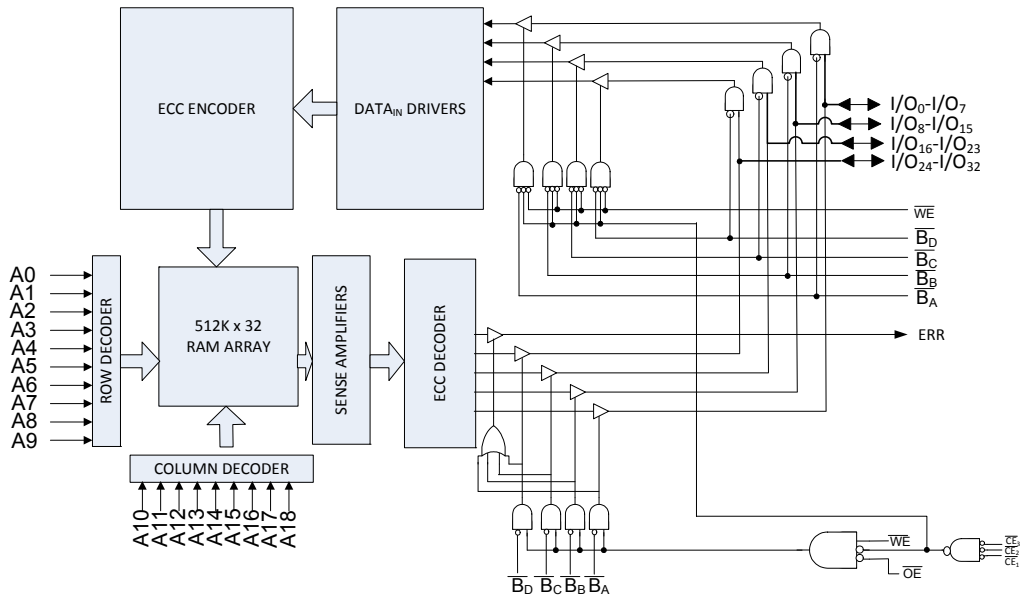
1. This device does not support automatic write-back on error detection.



**Logic Block Diagram – CY7C1062G**



**Logic Block Diagram – CY7C1062GE**





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## Pin Configurations

**Figure 1. 119-ball PBGA Pinout (Top View) - CY7C1062G [2]**

	1	2	3	4	5	6	7
<b>A</b>	I/O <sub>16</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	I/O <sub>0</sub>
<b>B</b>	I/O <sub>17</sub>	A <sub>18</sub>	A <sub>17</sub>	$\overline{CE}_1$	A <sub>16</sub>	A <sub>15</sub>	I/O <sub>1</sub>
<b>C</b>	I/O <sub>18</sub>	$\overline{B}_c$	$\overline{CE}_2$	NC	$\overline{CE}_3$	$\overline{B}_a$	I/O <sub>2</sub>
<b>D</b>	I/O <sub>19</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	I/O <sub>3</sub>
<b>E</b>	I/O <sub>20</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	I/O <sub>4</sub>
<b>F</b>	I/O <sub>21</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	I/O <sub>5</sub>
<b>G</b>	I/O <sub>22</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	I/O <sub>6</sub>
<b>H</b>	I/O <sub>23</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	I/O <sub>7</sub>
<b>J</b>	NC	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	NC
<b>K</b>	I/O <sub>24</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	I/O <sub>8</sub>
<b>L</b>	I/O <sub>25</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	I/O <sub>9</sub>
<b>M</b>	I/O <sub>26</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	I/O <sub>10</sub>
<b>N</b>	I/O <sub>27</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	I/O <sub>11</sub>
<b>P</b>	I/O <sub>28</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	I/O <sub>12</sub>
<b>R</b>	I/O <sub>29</sub>	A <sub>14</sub>	B <sub>d</sub>	NC	B <sub>b</sub>	A <sub>13</sub>	I/O <sub>13</sub>
<b>T</b>	I/O <sub>30</sub>	A <sub>12</sub>	A <sub>11</sub>	$\overline{WE}$	A <sub>10</sub>	A <sub>9</sub>	I/O <sub>14</sub>
<b>U</b>	I/O <sub>31</sub>	A <sub>8</sub>	A <sub>7</sub>	$\overline{OE}$	A <sub>6</sub>	A <sub>5</sub>	I/O <sub>15</sub>

**Figure 2. 119-ball PBGA Pinout (Top View) - CY7C1062GE [2]**

	1	2	3	4	5	6	7
<b>A</b>	I/O <sub>16</sub>	A <sub>4</sub>	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	I/O <sub>0</sub>
<b>B</b>	I/O <sub>17</sub>	A <sub>18</sub>	A <sub>17</sub>	$\overline{CE}_1$	A <sub>16</sub>	A <sub>15</sub>	I/O <sub>1</sub>
<b>C</b>	I/O <sub>18</sub>	$\overline{B}_c$	$\overline{CE}_2$	NC	$\overline{CE}_3$	$\overline{B}_a$	I/O <sub>2</sub>
<b>D</b>	I/O <sub>19</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	I/O <sub>3</sub>
<b>E</b>	I/O <sub>20</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	I/O <sub>4</sub>
<b>F</b>	I/O <sub>21</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	I/O <sub>5</sub>
<b>G</b>	I/O <sub>22</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	I/O <sub>6</sub>
<b>H</b>	I/O <sub>23</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	I/O <sub>7</sub>
<b>J</b>	ERR	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	NC
<b>K</b>	I/O <sub>24</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	I/O <sub>8</sub>
<b>L</b>	I/O <sub>25</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	I/O <sub>9</sub>
<b>M</b>	I/O <sub>26</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	I/O <sub>10</sub>
<b>N</b>	I/O <sub>27</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>SS</sub>	I/O <sub>11</sub>
<b>P</b>	I/O <sub>28</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DD</sub>	I/O <sub>12</sub>
<b>R</b>	I/O <sub>29</sub>	A <sub>14</sub>	B <sub>d</sub>	NC	B <sub>b</sub>	A <sub>13</sub>	I/O <sub>13</sub>
<b>T</b>	I/O <sub>30</sub>	A <sub>12</sub>	A <sub>11</sub>	$\overline{WE}$	A <sub>10</sub>	A <sub>9</sub>	I/O <sub>14</sub>
<b>U</b>	I/O <sub>31</sub>	A <sub>8</sub>	A <sub>7</sub>	$\overline{OE}$	A <sub>6</sub>	A <sub>5</sub>	I/O <sub>15</sub>

**Note**

- NC pins are not connected internally to the die.
- ERR is an Output pin. If not used, this pin should be left floating.



## Product Portfolio

Product	Features and Options (see <a href="#">Pin Configurations on page 4</a> )	Range	V <sub>CC</sub> Range (V)	Speed (ns)	Power Dissipation			
					Operating I <sub>CC</sub> , (mA)		Standby, I <sub>SB2</sub> (mA)	
					f = f <sub>max</sub>			
		Typ <sup>[4]</sup>	Max	Typ <sup>[4]</sup>	Max			
CY7C1062G18	Embedded ECC. No ERR output pin	Industrial	1.65 V–2.2 V	15	70	80	20	30
CY7C1062G30			2.2 V–3.6 V	10	90	110		
CY7C1062GE18	Embedded ECC. Optional ERR output pin		1.65 V–2.2 V	15	70	80		
CY7C1062GE30			2.2 V–3.6 V	10	90	110		

### Notes

4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = 1.8 V (for V<sub>CC</sub> range of 1.65 V–2.2 V), V<sub>CC</sub> = 3 V and (for V<sub>CC</sub> range of 2.2 V–3.6 V), T<sub>A</sub> = 25 °C.



## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature with power applied ..... -55 °C to +125 °C

Supply voltage on  $V_{CC}$  relative to GND ..... -0.5 V to  $V_{CC} + 0.5$  V

DC voltage applied to outputs in High Z State <sup>[5]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

DC input voltage <sup>[5]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

Current into outputs (LOW) ..... 20 mA

Static Discharge Voltage (MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up current ..... > 140 mA

## Operating Range

Grade	Ambient Temperature	$V_{CC}$
Industrial	-40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V

## DC Electrical Characteristics

Over the Operating Range of -40 °C to 85 °C

Parameter	Description	Test Conditions	10 ns / 15 ns			Unit	
			Min	Typ <sup>[6]</sup>	Max		
$V_{OH}$	Output HIGH Voltage	1.65 V to 2.2 V	$V_{CC} = \text{Min}, I_{OH} = -0.1$ mA	1.4	-	-	V
		2.2 V to 2.7 V	$V_{CC} = \text{Min}, I_{OH} = -1.0$ mA	2.0	-	-	
		2.7 V to 3.0 V	$V_{CC} = \text{Min}, I_{OH} = -4.0$ mA	2.2	-	-	
		3.0 V to 3.6 V	$V_{CC} = \text{Min}, I_{OH} = -4.0$ mA	2.4	-	-	
$V_{OL}$	Output LOW Voltage	1.65 V to 2.2 V	$V_{CC} = \text{Min}, I_{OL} = 0.1$ mA	-	-	0.2	
		2.2 V to 2.7 V	$V_{CC} = \text{Min}, I_{OL} = 2$ mA	-	-	0.4	
		2.7 V to 3.6 V	$V_{CC} = \text{Min}, I_{OL} = 8$ mA	-	-	0.4	
$V_{IH}$	Input HIGH Voltage	1.65 V to 2.2 V	-	1.4	-	$V_{CC} + 0.2$	
		2.2 V to 2.7 V	-	2.0	-	$V_{CC} + 0.3$	
		2.7 V to 3.6 V	-	2.0	-	$V_{CC} + 0.3$	
$V_{IL}$	Input LOW Voltage <sup>[5]</sup>	1.65 V to 2.2 V	-	-0.2	-	0.4	
		2.2 V to 2.7 V	-	-0.3	-	0.6	
		2.7 V to 3.6 V	-	-0.3	-	0.8	
$I_{IX}$	Input Leakage Current	$GND \leq V_{IN} \leq V_{CC}$	-1.0	-	+1.0	$\mu$ A	
$I_{OZ}$	Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC}$ , Output disabled	-1.0	-	+1.0	$\mu$ A	
$I_{CC}$	Operating Supply Current	$V_{CC} = \text{Max}, I_{OUT} = 0$ mA, CMOS levels	f = 100 MHz	-	90.0	110.0	mA
			f = 66.7 MHz	-	70.0	80.0	
$I_{SB1}$	Automatic CE Power-down Current – TTL Inputs	Max $V_{CC}$ , $\overline{CE} \geq V_{IH}$ <sup>[7]</sup> , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , f = $f_{MAX}$	-	-	40.0		
$I_{SB2}$	Automatic CE Power-down Current – CMOS Inputs	Max $V_{CC}$ , $\overline{CE} \geq V_{CC} - 0.2$ V <sup>[7]</sup> , $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, f = 0	-	20.0	30.0		

### Notes

5.  $V_{IL(\text{min})} = -2.0$  V and  $V_{IH(\text{max})} = V_{CC} + 2$  V for pulse durations of less than 20 ns.

6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at  $V_{CC} = 1.8$  V (for  $V_{CC}$  range of 1.65 V–2.2 V),  $V_{CC} = 3$  V (for  $V_{CC}$  range of 2.2 V–3.6 V), and  $T_A = 25$  °C.

7.  $\overline{CE}$  indicates a combination of all three chip enables. When active LOW,  $\overline{CE}$  indicates the  $\overline{CE}_1$ ,  $\overline{CE}_2$ , and  $\overline{CE}_3$  LOW. When HIGH,  $\overline{CE}$  indicates the  $\overline{CE}_1$ ,  $\overline{CE}_2$ , or  $\overline{CE}_3$  HIGH.



## Capacitance

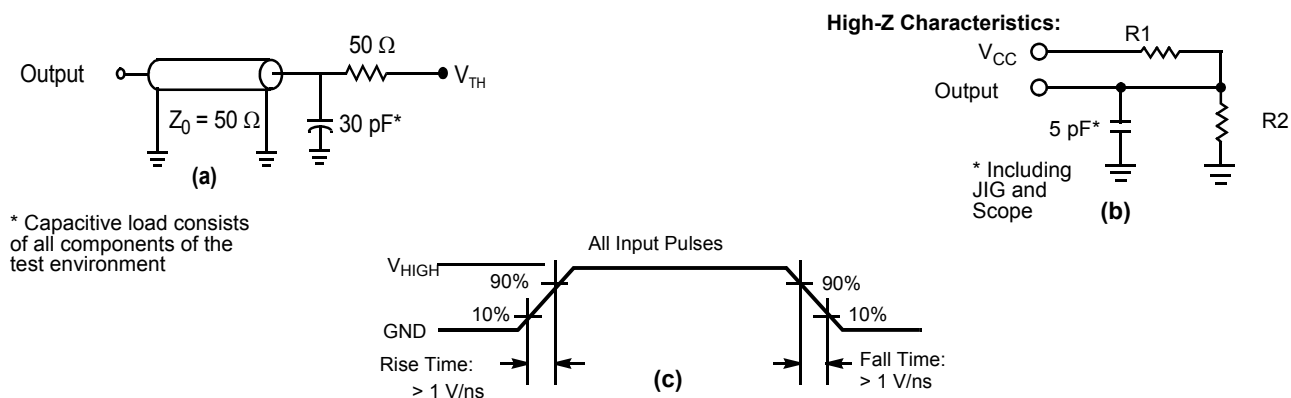
Parameter [8]	Description	Test Conditions	119-ball PBGA	Unit
$C_{IN}$	Input Capacitance	$T_A = 25\text{ }^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = V_{CC}(\text{typ})$	10	pF
$C_{OUT}$	I/O Capacitance			

## Thermal Resistance

Parameter [8]	Description	Test Conditions	119-ball PBGA	Unit
$\Theta_{JA}$	Thermal Resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board	20.92	$^\circ\text{C/W}$
$\Theta_{JC}$	Thermal Resistance (junction to case)		15.84	

## AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms [9]



Parameters	1.8 V	3.0 V	Unit
R1	1667	317	$\Omega$
R2	1538	351	
$V_{TH}$	0.9	1.5	V
$V_{HIGH}$	1.8	3.0	

### Notes

- Tested initially and after any design or process changes that may affect these parameters.
- Full-device AC operation assumes a 100- $\mu\text{s}$  ramp time from 0 to  $V_{CC}$  (min) and 100- $\mu\text{s}$  wait time after  $V_{CC}$  stabilizes to its operational value.



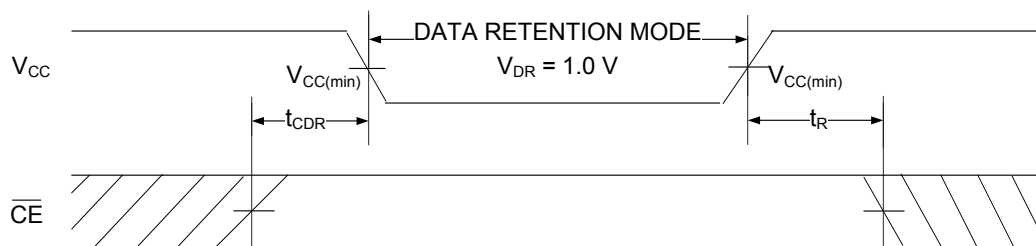
## Data Retention Characteristics

Over the Operating Range of  $-40\text{ }^{\circ}\text{C}$  to  $85\text{ }^{\circ}\text{C}$

Parameter	Description	Conditions	Min	Max	Unit
$V_{DR}$	$V_{CC}$ for Data Retention	–	1.0	–	V
$I_{CCDR}$	Data Retention Current	$V_{CC} = V_{DR}$ , $\overline{CE} \geq V_{CC} - 0.2\text{ V}$ [10], $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	30.0	mA
$t_{CDR}$ [11]	Chip Deselect to Data Retention Time	–	0.0	–	ns
$t_R$ [11, 12]	Operation Recovery Time	$V_{CC} \geq 2.2\text{ V}$ $V_{CC} < 2.2\text{ V}$	10.0 15.0	– –	

## Data Retention Waveform

Figure 4. Data Retention Waveform [10]



### Notes

10.  $\overline{CE}$  indicates a combination of all three chip enables. When active LOW,  $\overline{CE}$  indicates the  $\overline{CE}_1$ ,  $\overline{CE}_2$ , and  $\overline{CE}_3$  LOW. When HIGH,  $\overline{CE}$  indicates the  $\overline{CE}_1$ ,  $\overline{CE}_2$ , or  $\overline{CE}_3$  HIGH.
11. Tested initially and after any design or process changes that may affect these parameters.
12. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min.)} \geq 100\text{ }\mu\text{s}$  or stable at  $V_{CC(min.)} \geq 100\text{ }\mu\text{s}$ .



## AC Switching Characteristics

Over the Operating Range of  $-40\text{ }^{\circ}\text{C}$  to  $85\text{ }^{\circ}\text{C}$

Parameter <sup>[13]</sup>	Description	10 ns		15 ns		Unit
		Min	Max	Min	Max	
<b>Read Cycle</b>						
$t_{\text{POWER}}$	$V_{\text{CC}}$ (stable) to the first access <sup>[14, 15]</sup>	100.0	–	100.0	–	$\mu\text{s}$
$t_{\text{RC}}$	Read cycle time	10.0	–	15.0	–	ns
$t_{\text{AA}}$	Address to data / ERR valid	–	10.0	–	15.0	
$t_{\text{OHA}}$	Data / ERR hold from address change	3.0	–	3.0	–	
$t_{\text{ACE}}$	$\overline{\text{CE}}$ LOW to data / ERR valid <sup>[16]</sup>	–	10.0	–	15.0	
$t_{\text{DOE}}$	$\overline{\text{OE}}$ LOW to data / ERR valid	–	5.0	–	8.0	
$t_{\text{LZOE}}$	$\overline{\text{OE}}$ LOW to low Z <sup>[17, 18]</sup>	0.0	–	1.0	–	
$t_{\text{HZOE}}$	$\overline{\text{OE}}$ HIGH to high Z <sup>[17, 18]</sup>	–	5.0	–	8.0	
$t_{\text{LZCE}}$	$\overline{\text{CE}}$ LOW to low Z <sup>[16, 17, 18]</sup>	3.0	–	3.0	–	
$t_{\text{HZCE}}$	$\overline{\text{CE}}$ HIGH to high Z <sup>[16, 17, 18]</sup>	–	5.0	–	8.0	
$t_{\text{PU}}$	$\overline{\text{CE}}$ LOW to power-up <sup>[15, 16]</sup>	0.0	–	0.0	–	
$t_{\text{PD}}$	$\overline{\text{CE}}$ HIGH to power-down <sup>[15, 16]</sup>	–	10.0	–	15.0	
$t_{\text{DBE}}$	Byte enable to data valid	–	5.0	–	8.0	
$t_{\text{LZBE}}$	Byte enable to low Z	0.0	–	1.0	–	
$t_{\text{HZBE}}$	Byte disable to high Z	–	6.0	–	8.0	
<b>Write Cycle</b> <sup>[19, 20]</sup>						
$t_{\text{WC}}$	Write cycle time	10.0	–	15.0	–	ns
$t_{\text{SCE}}$	$\overline{\text{CE}}$ LOW to write end <sup>[16]</sup>	7.0	–	12.0	–	
$t_{\text{AW}}$	Address setup to write end	7.0	–	12.0	–	
$t_{\text{HA}}$	Address hold from write end	0.0	–	0.0	–	
$t_{\text{SA}}$	Address setup to write start	0.0	–	0.0	–	
$t_{\text{PWE}}$	$\overline{\text{WE}}$ pulse width	7.0	–	12.0	–	
$t_{\text{SD}}$	Data setup to write end	5.0	–	8.0	–	
$t_{\text{HD}}$	Data hold from write end	0.0	–	0.0	–	
$t_{\text{LZWE}}$	$\overline{\text{WE}}$ HIGH to low Z <sup>[17, 18]</sup>	3.0	–	3.0	–	
$t_{\text{HZWE}}$	$\overline{\text{WE}}$ LOW to high Z <sup>[17, 18]</sup>	–	5.0	–	8.0	
$t_{\text{BW}}$	Byte Enable to write end	7.0	–	12.0	–	

### Notes

13. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for  $V_{\text{CC}} \geq 3\text{ V}$ ) and  $V_{\text{CC}}/2$  (for  $V_{\text{CC}} < 3\text{ V}$ ), and input pulse levels of 0 to 3 V (for  $V_{\text{CC}} \geq 3\text{ V}$ ) and 0 to  $V_{\text{CC}}$  (for  $V_{\text{CC}} < 3\text{ V}$ ). Test conditions for the read cycle use output loading shown in part (a) of Figure 3 on page 7, unless specified otherwise.
14.  $t_{\text{POWER}}$  gives minimum amount of time that the power supply is at stable  $V_{\text{CC}}$  until first memory access is performed.
15. These parameters are guaranteed by design and are not tested.
16.  $\overline{\text{CE}}$  indicates a combination of all three chip enables. When active LOW,  $\overline{\text{CE}}$  indicates the  $\overline{\text{CE}}_1$ ,  $\overline{\text{CE}}_2$  and  $\overline{\text{CE}}_3$  LOW. When HIGH,  $\overline{\text{CE}}$  indicates the  $\overline{\text{CE}}_1$ ,  $\overline{\text{CE}}_2$  or  $\overline{\text{CE}}_3$  HIGH.
17.  $t_{\text{HZOE}}$ ,  $t_{\text{HZCE}}$ ,  $t_{\text{HZWE}}$ ,  $t_{\text{LZOE}}$ ,  $t_{\text{LZCE}}$ ,  $t_{\text{LZWE}}$ , and  $t_{\text{LZBE}}$  are specified with a load capacitance of 5 pF as in (b) of Figure 3 on page 7. Transition is measured  $\pm 200\text{ mV}$  from steady state voltage.
18. Tested initially and after any design or process changes that may affect these parameters.
19. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}} = V_{\text{IL}}$ ,  $\overline{\text{CE}} = V_{\text{IL}}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
20. The minimum write pulse width for Write Cycle No. 2 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  Low) should be sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .

## Switching Waveforms

Figure 5. Read Cycle No. 1 of CY7C1062G (Address Transition Controlled) [21, 22]

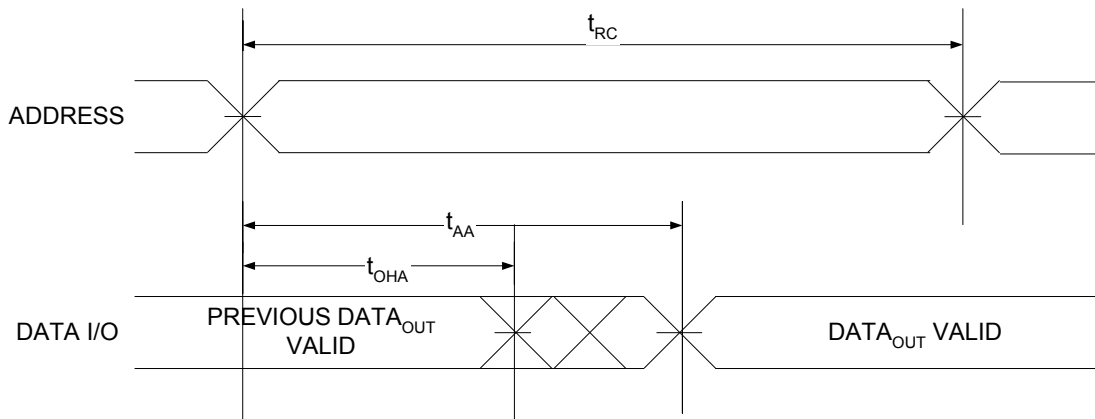
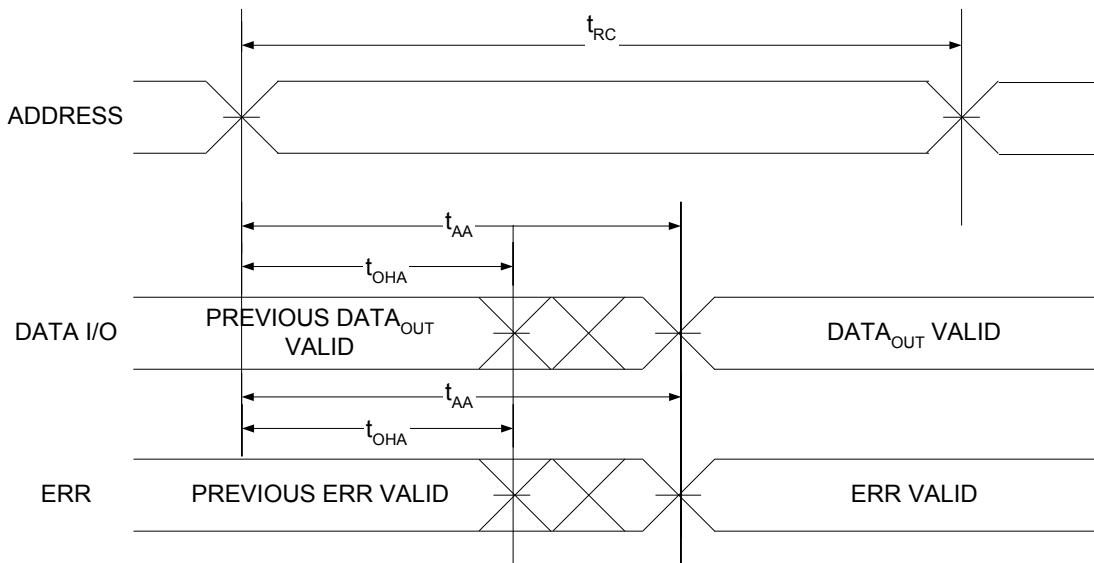


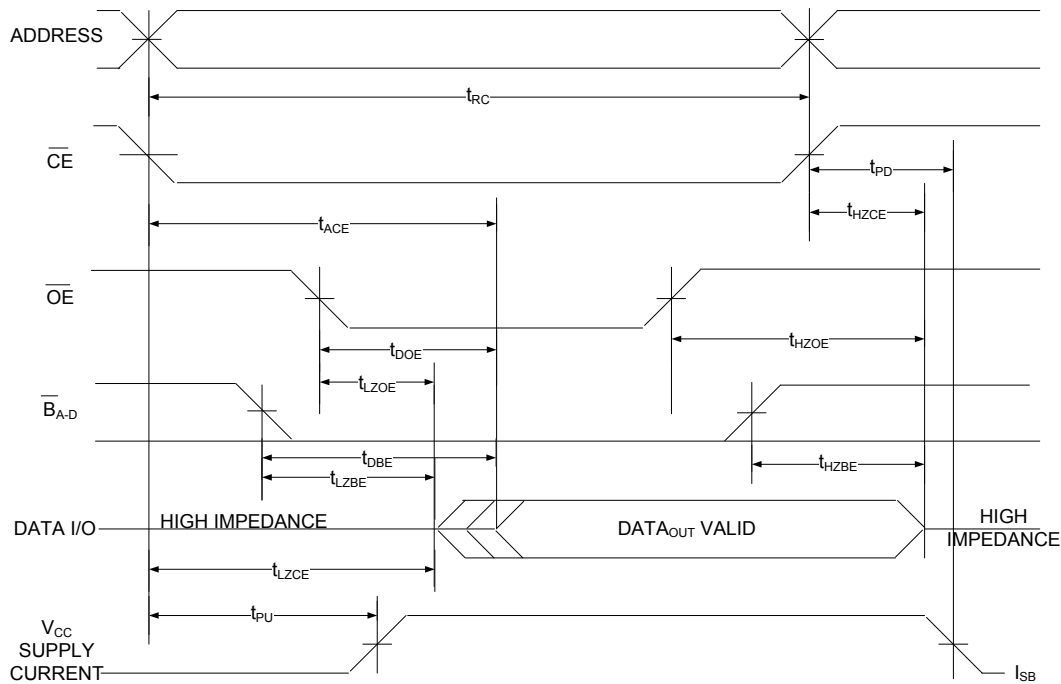
Figure 6. Read Cycle No. 1 of CY7C1062GE (Address Transition Controlled) [21, 22]



### Notes

21. The device is continuously selected,  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BA}$ ,  $\overline{BB}$ ,  $\overline{BC}$ ,  $\overline{BD}$  =  $V_{IL}$ .  
 22.  $\overline{WE}$  is HIGH for read cycle.

**Switching Waveforms** (continued)

**Figure 7. Read Cycle No. 2 ( $\overline{\text{OE}}$  Controlled)** [23, 24, 25]

**Notes**

23.  $\overline{\text{CE}}$  indicates a combination of all three chip enables. When active LOW,  $\overline{\text{CE}}$  indicates the  $\overline{\text{CE}}_1$ ,  $\overline{\text{CE}}_2$ , and  $\overline{\text{CE}}_3$  LOW. When HIGH,  $\overline{\text{CE}}$  indicates the  $\overline{\text{CE}}_1$ ,  $\overline{\text{CE}}_2$ , or  $\overline{\text{CE}}_3$  HIGH.

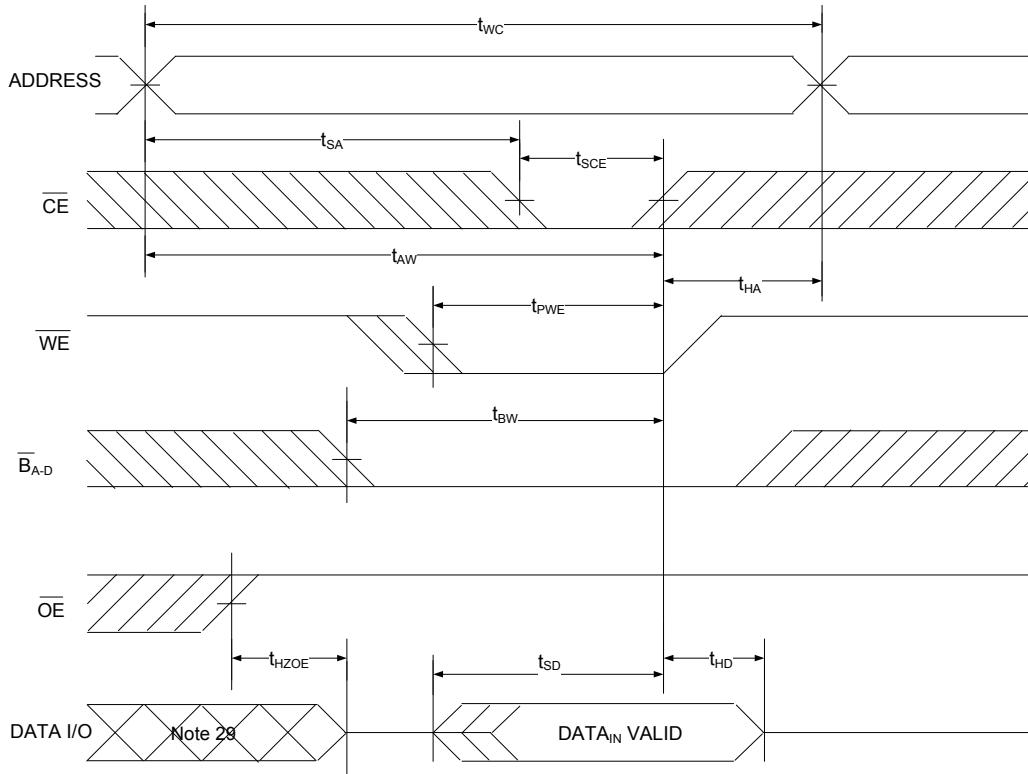
24.  $\overline{\text{WE}}$  is HIGH for read cycle.

25. Address valid before or similar to  $\overline{\text{CE}}$  transition LOW.



## Switching Waveforms (continued)

Figure 8. Write Cycle No. 1 ( $\overline{\text{CE}}$  Controlled) [26, 27, 28]



### Notes

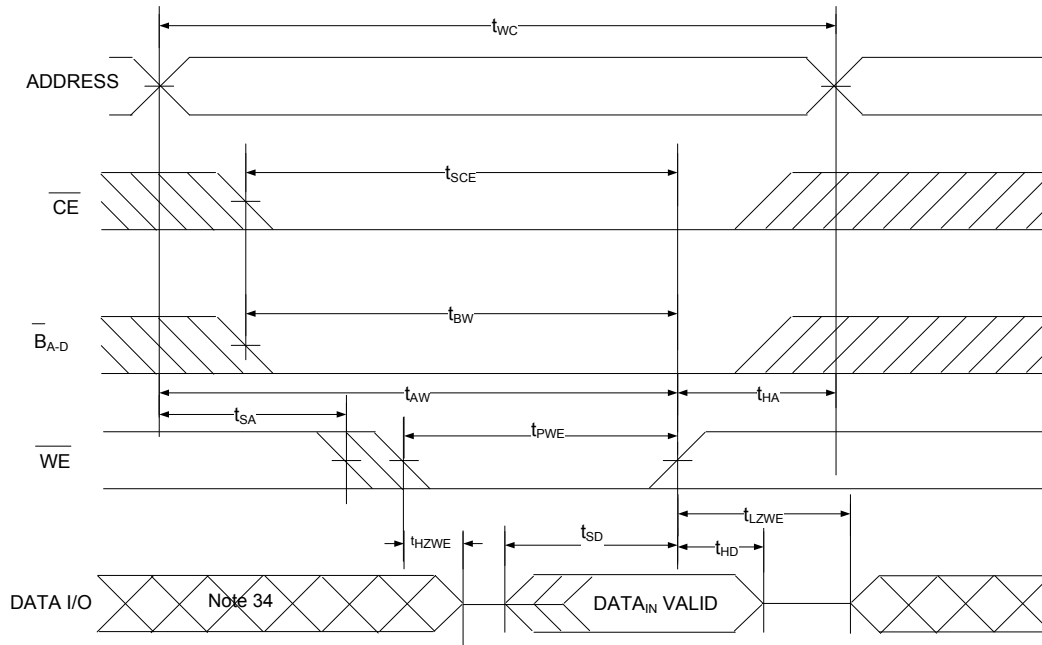
26.  $\overline{\text{CE}}$  indicates a combination of all three chip enables. When active LOW,  $\overline{\text{CE}}$  indicates the  $\overline{\text{CE}}_1$ ,  $\overline{\text{CE}}_2$ , and  $\overline{\text{CE}}_3$  LOW. When HIGH,  $\overline{\text{CE}}$  indicates the  $\overline{\text{CE}}_1$ ,  $\overline{\text{CE}}_2$ , or  $\overline{\text{CE}}_3$  HIGH.

27. The internal write time of the memory is defined by the overlap of  $\overline{\text{WE}} = V_{\text{IH}}$ ,  $\overline{\text{CE}} = V_{\text{IH}}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.

28. Data I/O is high impedance if  $\overline{\text{CE}}$  or  $\overline{\text{OE}}$  or  $\overline{\text{B}}_{\text{A}}$ ,  $\overline{\text{B}}_{\text{B}}$ ,  $\overline{\text{B}}_{\text{C}}$ ,  $\overline{\text{B}}_{\text{D}} = V_{\text{IH}}$ .

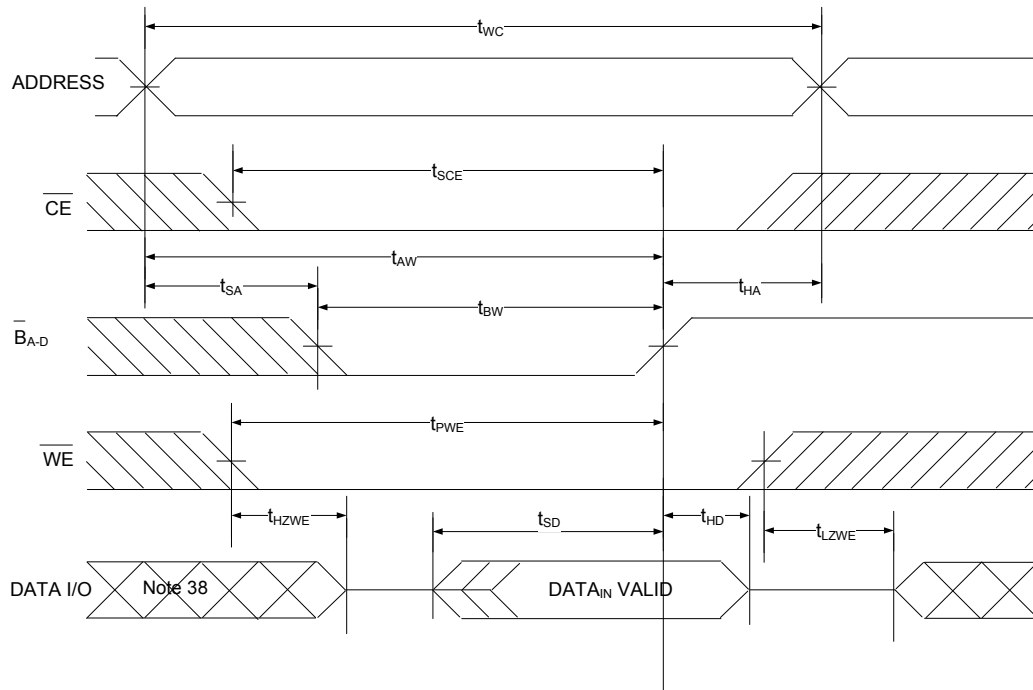
29. During this period I/O are in output state. Do not apply input signals.


**Switching Waveforms** (continued)

**Figure 9. Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  Low)** [30, 31, 32, 33]

**Notes**

30.  $\overline{CE}$  indicates a combination of all three chip enables. When active LOW,  $\overline{CE}$  indicates the  $\overline{CE}_1$ ,  $\overline{CE}_2$ , and  $\overline{CE}_3$  LOW. When HIGH,  $\overline{CE}$  indicates the  $\overline{CE}_1$ ,  $\overline{CE}_2$ , or  $\overline{CE}_3$  HIGH.
31. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
32. Data I/O is high impedance if  $\overline{OE}$  or  $\overline{B}_A$ ,  $\overline{B}_B$ ,  $\overline{B}_C$ ,  $\overline{B}_D = V_{IH}$ .
33. The minimum write cycle pulse width should be equal to sum of  $t_{HZWE}$  and  $t_{SD}$ .
34. During this period I/O are in output state. Do not apply input signals.


**Switching Waveforms** (continued)

**Figure 10. Write Cycle No. 3 ( $\overline{B}_A$ ,  $\overline{B}_B$ ,  $\overline{B}_C$ ,  $\overline{B}_D$  Controlled)** [35, 36, 37]

**Notes**

35.  $\overline{CE}$  indicates a combination of all three chip enables. When active LOW,  $\overline{CE}$  indicates the  $\overline{CE}_1$ ,  $\overline{CE}_2$ , and  $\overline{CE}_3$  LOW. When HIGH,  $\overline{CE}$  indicates the  $\overline{CE}_1$ ,  $\overline{CE}_2$ , or  $\overline{CE}_3$  HIGH.
36. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
37. Data I/O is high impedance if  $\overline{OE}$  or  $\overline{B}_A$ ,  $\overline{B}_B$ ,  $\overline{B}_C$ ,  $\overline{B}_D = V_{IH}$ .
38. During this period I/O are in output state. Do not apply input signals.


**Truth Table – CY7C1062G/CY7C1062GE**

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{CE}_3$	$\overline{OE}$	$\overline{WE}$	$\overline{B}_A$	$\overline{B}_B$	$\overline{B}_C$	$\overline{B}_D$	I/O <sub>0</sub> –I/O <sub>7</sub>	I/O <sub>8</sub> –I/O <sub>15</sub>	I/O <sub>16</sub> –I/O <sub>23</sub>	I/O <sub>24</sub> –I/O <sub>31</sub>	Mode	Power
H	X <sup>[39]</sup>	X <sup>[39]</sup>	X <sup>[39]</sup>	X <sup>[39]</sup>	X <sup>[39]</sup>	X <sup>[39]</sup>	X <sup>[39]</sup>	X <sup>[39]</sup>	High Z	High Z	High Z	High Z	power-down	(I <sub>SB</sub> )
X <sup>[39]</sup>	H	X <sup>[39]</sup>	X <sup>[39]</sup>	X <sup>[39]</sup>	X <sup>[39]</sup>	X <sup>[39]</sup>	X <sup>[39]</sup>	X <sup>[39]</sup>	High Z	High Z	High Z	High Z	power-down	(I <sub>SB</sub> )
X <sup>[39]</sup>	X <sup>[39]</sup>	H	X <sup>[39]</sup>	X <sup>[39]</sup>	X <sup>[39]</sup>	X <sup>[39]</sup>	X <sup>[39]</sup>	X <sup>[39]</sup>	High Z	High Z	High Z	High Z	power-down	(I <sub>SB</sub> )
L	L	L	L	H	L	L	L	L	Data out	Data out	Data out	Data out	Read all bits	(I <sub>CC</sub> )
L	L	L	L	H	L	H	H	H	Data out	High Z	High Z	High Z	Read byte A bits only	(I <sub>CC</sub> )
L	L	L	L	H	H	L	H	H	High Z	Data out	High Z	High Z	Read byte B bits only	(I <sub>CC</sub> )
L	L	L	L	H	H	H	L	H	High Z	High Z	Data out	High Z	Read byte C bits only	(I <sub>CC</sub> )
L	L	L	L	H	H	H	H	L	High Z	High Z	High Z	Data out	Read Byte D bits only	(I <sub>CC</sub> )
L	L	L	X <sup>[39]</sup>	L	L	L	L	L	Data in	Data in	Data in	Data in	Write all bits	(I <sub>CC</sub> )
L	L	L	X <sup>[39]</sup>	L	L	H	H	H	Data in	High Z	High Z	High Z	Write byte A bits only	(I <sub>CC</sub> )
L	L	L	X <sup>[39]</sup>	L	H	L	H	H	High Z	Data in	High Z	High Z	Write byte B bits only	(I <sub>CC</sub> )
L	L	L	X <sup>[39]</sup>	L	H	H	L	H	High Z	High Z	Data in	High Z	Write byte C bits only	(I <sub>CC</sub> )
L	L	L	X <sup>[39]</sup>	L	H	H	H	L	High Z	High Z	High Z	Data in	Write byte D bits only	(I <sub>CC</sub> )
L	L	L	H	H	X <sup>[39]</sup>	X <sup>[39]</sup>	X <sup>[39]</sup>	X <sup>[39]</sup>	High Z	High Z	High Z	High Z	Selected, outputs disabled	(I <sub>CC</sub> )
L	L	L	X <sup>[39]</sup>	X <sup>[39]</sup>	H	H	H	H	High Z	High Z	High Z	High Z	Selected, outputs disabled	(I <sub>CC</sub> )

**ERR Output – CY7C1062GE**

Output <sup>[40]</sup>	Mode
0	Read Operation, no single-bit error in the stored data.
1	Read Operation, single bit error detected and corrected.
High Z	Device deselected or Outputs disabled or Write Operation.

**Notes**

39. The input voltage levels on these pins should be either at V<sub>IH</sub> or V<sub>IL</sub>.

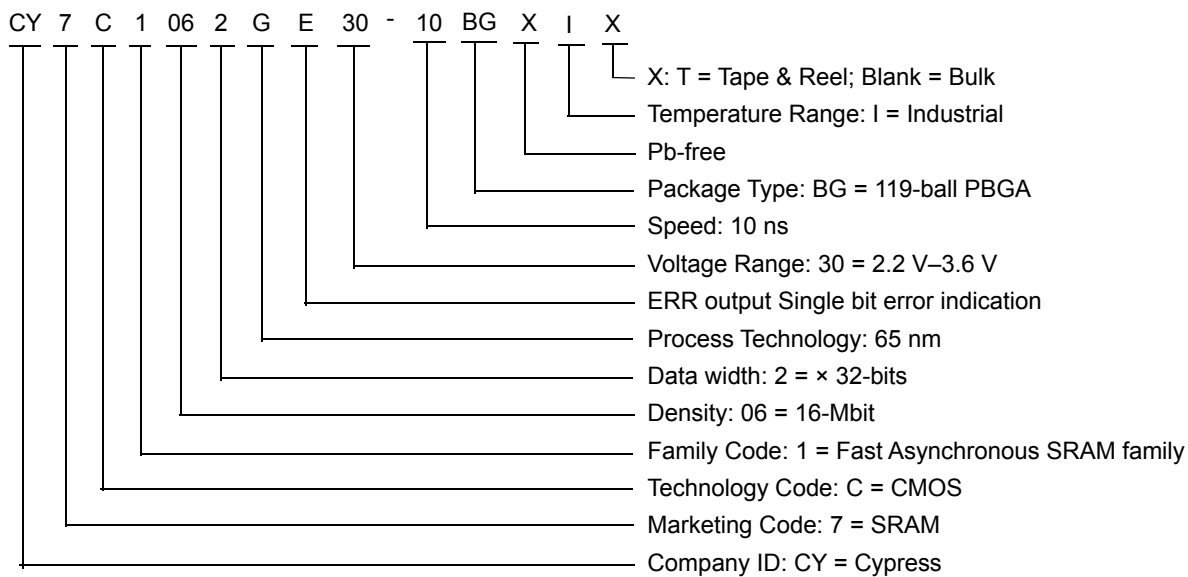
40. ERR is an Output pin. If not used, this pin should be left floating.



## Ordering Information

Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type (Pb-free)	ERR Ball	Operating Range
10	2.2 V–3.6 V	CY7C1062G30-10BGXI	51-85115	119-ball PBGA	No	Industrial
		CY7C1062G30-10BGXIT		119-ball PBGA, Tape & Reel	No	
		CY7C1062GE30-10BGXI		119-ball PBGA	Yes	
		CY7C1062GE30-10BGXIT		119-ball PBGA, Tape & Reel	Yes	

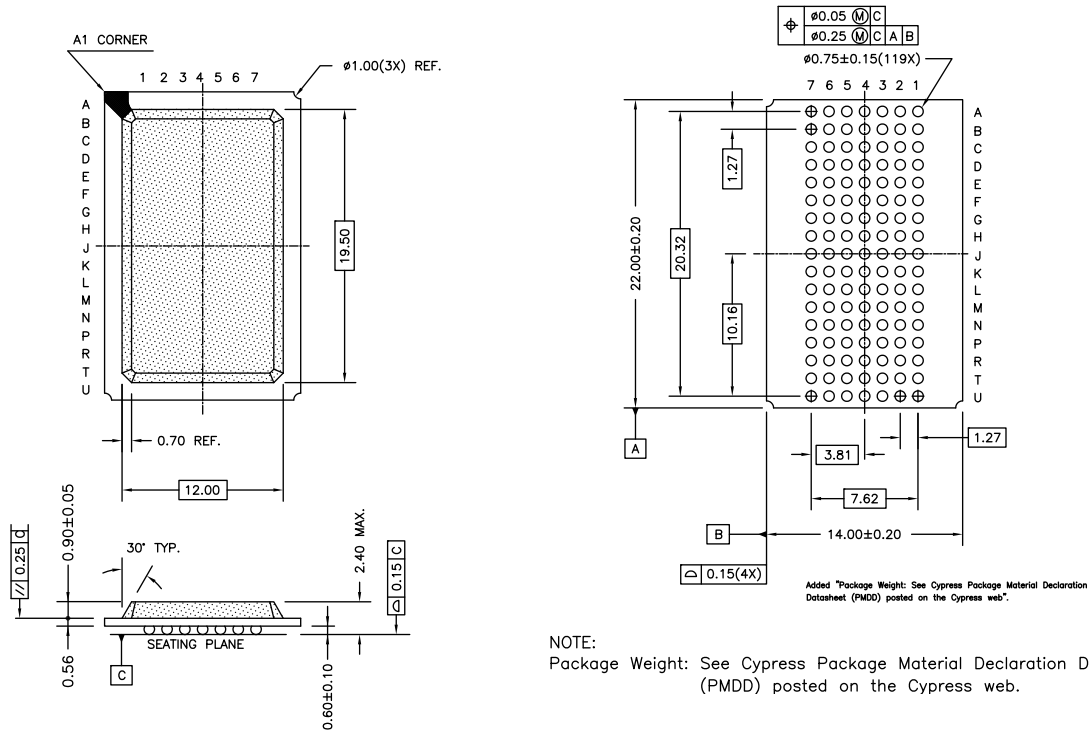
## Ordering Code Definitions





**Package Diagrams**

**Figure 11. 119-pin PBGA (14 × 22 × 2.4 mm) BG119 Package Outline, 51-85115**



NOTE:  
Package Weight: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85115 \*D



## Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
PBGA	Plastic Ball Grid Array
SRAM	Static Random Access Memory
TTL	Transistor-Transistor Logic
$\overline{WE}$	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
$^{\circ}\text{C}$	degree Celsius
MHz	megahertz
$\mu\text{A}$	microampere
$\mu\text{s}$	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
$\Omega$	ohm
%	percent
pF	picofarad
V	volt
W	watt



## Document History Page

Document Title: CY7C1062G/CY7C1062GE, 16-Mbit (512 K words × 32 bits) Static RAM with Error-Correcting Code (ECC)  
Document Number: 001-81609

Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*E	4800546	NILE	07/31/2015	Changed status from Preliminary to Final.
*F	5434962	NILE	09/13/2016	Updated <a href="#">DC Electrical Characteristics</a> : Enhanced V <sub>OH</sub> for voltage range 3.0 V to 3.6 V from 2.2 V to 2.4 V. Updated Footnote 5. Updated part numbers in <a href="#">Ordering Information</a> . Added Tape & Reel ordering codes. Updated copyright notice and <a href="#">Sales, Solutions, and Legal Information</a> .
*G	5975045	AESATP12	11/30/2017	Updated logo and copyright.



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