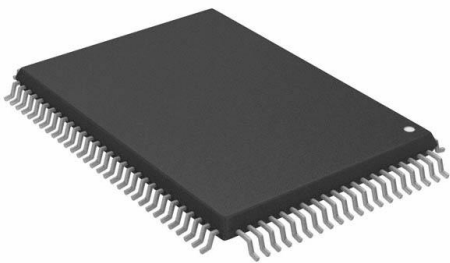


CY7C1325H-133AXI Datasheet

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| | |
|------------------------------|--|
| DiGi Electronics Part Number | CY7C1325H-133AXI-DG |
| Manufacturer | Infineon Technologies |
| Manufacturer Product Number | CY7C1325H-133AXI |
| Description | IC SRAM 4.5MBIT PAR 100TQFP |
| Detailed Description | SRAM - Synchronous, SDR Memory IC 4.5Mbit Parallel 133 MHz 6.5 ns 100-TQFP (14x20) |

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Purchase and inquiry

Manufacturer Product Number:

CY7C1325H-133AXI

Series:

-

DiGi-Electronics Programmable:

Not Verified

Memory Format:

SRAM

Memory Size:

4.5Mbit

Memory Interface:

Parallel

Write Cycle Time - Word, Page:

-

Voltage - Supply:

3.135V ~ 3.6V

Mounting Type:

Surface Mount

Supplier Device Package:

100-TQFP (14x20)

Manufacturer:

Infineon Technologies

Product Status:

Obsolete

Memory Type:

Volatile

Technology:

SRAM - Synchronous, SDR

Memory Organization:

256K x 18

Clock Frequency:

133 MHz

Access Time:

6.5 ns

Operating Temperature:

-40°C ~ 85°C (TA)

Package / Case:

100-LQFP

Base Product Number:

CY7C1325

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.32.0041

Moisture Sensitivity Level (MSL):

3 (168 Hours)

ECCN:

3A991B2A

**CY7C1325H**

4-Mbit (256K × 18) Flow-Through Sync SRAM

Features

- 256K × 18 common I/O
- 3.3 V core power supply (V_{DD})
- 2.5 V or 3.3 V I/O power supply (V_{DDQ})
- Fast clock-to-output times
- 6.5 ns (133 MHz version)
- Provide high performance 2-1-1-1 access rate
- User selectable burst counter supporting Intel Pentium interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self timed write
- Asynchronous output enable
- Available in Pb-free 100-pin TQFP package
- “ZZ” sleep mode option

Functional Description

The CY7C1325H is a 256K × 18 synchronous cache RAM designed to interface with high speed microprocessors with minimum glue logic. Maximum access delay from clock rise is

6.5 ns (133 MHz version). A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access. All synchronous inputs are gated by registers controlled by a positive-edge-triggered Clock Input (CLK). The synchronous inputs include all addresses, all data inputs, address-pipelining chip enable (CE_1), depth-expansion chip enables (CE_2 and CE_3), burst control inputs (ADSC, ADSP, and ADV), write enables ($BW_{[A:B]}$, and BWE), and global write (GW). Asynchronous inputs include the output enable (OE) and the ZZ pin.

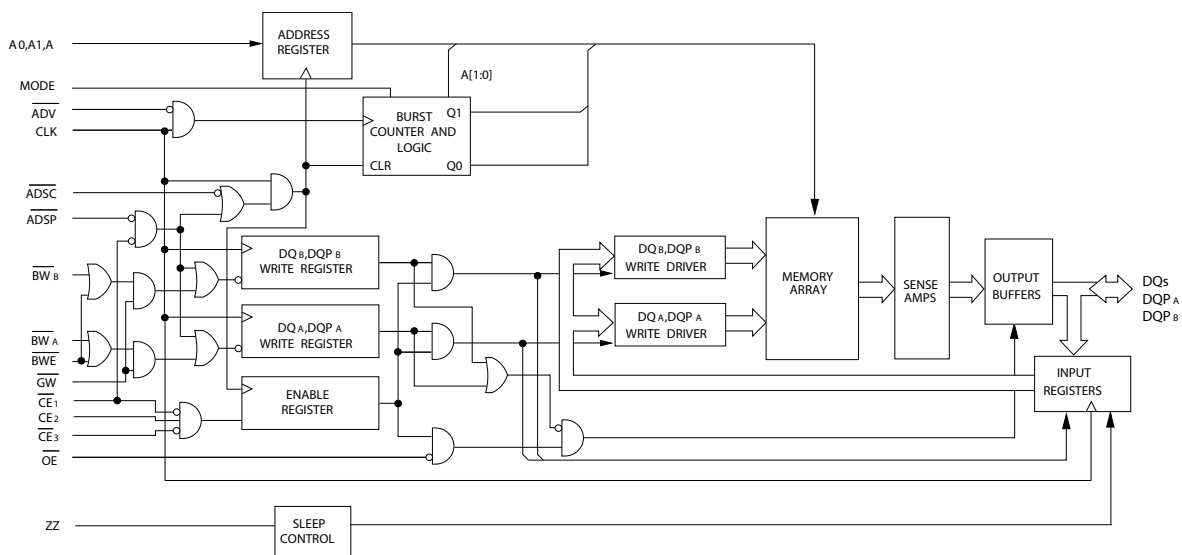
The CY7C1325H allows either interleaved or linear burst sequences, selected by the MODE input pin. A HIGH selects an interleaved burst sequence, while a LOW selects a linear burst sequence. Burst accesses can be initiated with the processor address strobe (ADSP) or the cache controller address strobe (ADSC) inputs.

Addresses and chip enables are registered at rising edge of clock when either address strobe processor (ADSP) or address strobe controller (ADSC) are active. Subsequent burst addresses can be internally generated as controlled by the advance pin (ADV).

The CY7C1325H operates from a +3.3 V core power supply while all outputs may operate with either a +2.5 or +3.3 V supply. All inputs and outputs are JEDEC-standard JESD8-5-compatible.

For a complete list of related documentation, click [here](#).

Logic Block Diagram





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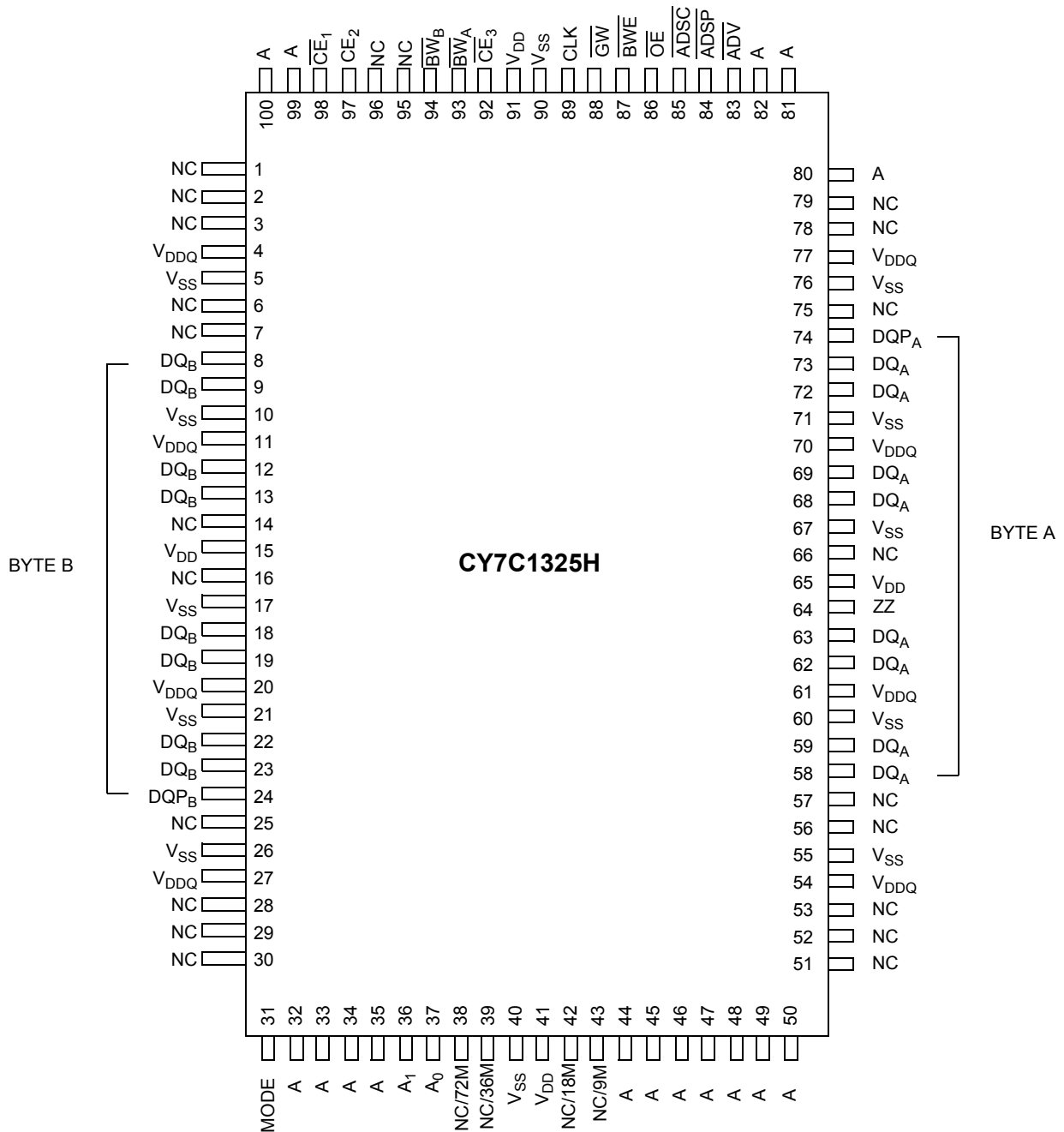


Selection Guide

| Description | 133 MHz | Unit |
|---------------------------|---------|------|
| Maximum access time | 6.5 | ns |
| Maximum operating current | 225 | mA |
| Maximum standby current | 40 | mA |

Pin Configurations

Figure 1. 100-pin TQFP (14 × 20 × 1.4 mm) pinout





Pin Definitions

| Name | I/O | Description |
|--|--------------------|---|
| A_0, A_1, A | Input-synchronous | Address inputs used to select one of the 256 K address locations. Sampled at the rising edge of the CLK if \overline{ADSP} or \overline{ADSC} is active LOW, and $\overline{CE}_1, \overline{CE}_2,$ and \overline{CE}_3 are sampled active. $A_{[1:0]}$ feed the 2 bit counter. |
| $\overline{BW}_A, \overline{BW}_B$ | Input-synchronous | Byte write select inputs, active LOW. Qualified with \overline{BWE} to conduct byte writes to the SRAM. Sampled on the rising edge of CLK. |
| \overline{GW} | Input-synchronous | Global write enable input, active LOW. When asserted LOW on the rising edge of CLK, a global write is conducted (all bytes are written, regardless of the values on $\overline{BW}_{[A:B]}$ and \overline{BWE}). |
| \overline{BWE} | Input-synchronous | Byte write enable input, active LOW. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write. |
| CLK | Input-clock | Clock input. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when \overline{ADV} is asserted LOW, during a burst operation. |
| \overline{CE}_1 | Input-synchronous | Chip enable 1 input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with \overline{CE}_2 and \overline{CE}_3 to select/deselect the device. \overline{ADSP} is ignored if \overline{CE}_1 is HIGH. \overline{CE}_1 is sampled only when a new external address is loaded. |
| \overline{CE}_2 | Input-synchronous | Chip enable 2 input, active HIGH. Sampled on the rising edge of CLK. Used in conjunction with \overline{CE}_1 and \overline{CE}_3 to select/deselect the device. \overline{CE}_2 is sampled only when a new external address is loaded. |
| \overline{CE}_3 | Input-synchronous | Chip enable 3 input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with \overline{CE}_1 and \overline{CE}_2 to select/deselect the device. \overline{CE}_3 is sampled only when a new external address is loaded. |
| \overline{OE} | Input-asynchronous | Output enable, asynchronous input, active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pins. \overline{OE} is masked during the first clock of a read cycle when emerging from a deselected state. |
| \overline{ADV} | Input-synchronous | Advance input signal, sampled on the rising edge of CLK. When asserted, it automatically increments the address in a burst cycle. |
| \overline{ADSP} | Input-synchronous | Address strobe from processor, sampled on the rising edge of CLK, active LOW. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When \overline{ADSP} and \overline{ADSC} are both asserted, only \overline{ADSP} is recognized. \overline{ADSP} is ignored when \overline{CE}_1 is deasserted HIGH. |
| \overline{ADSC} | Input-synchronous | Address strobe from controller, sampled on the rising edge of CLK, active LOW. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When \overline{ADSP} and \overline{ADSC} are both asserted, only \overline{ADSP} is recognized. |
| \overline{ZZ} | Input-asynchronous | ZZ "sleep" input, active HIGH. When asserted HIGH places the device in a non-time-critical "sleep" condition with data integrity preserved. During normal operation, this pin has to be low or left floating. \overline{ZZ} pin has an internal pull-down. |
| \overline{DQ}_s $\overline{DQP}_A,$ \overline{DQP}_B | I/O-synchronous | Bidirectional data I/O lines. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by \overline{OE} . When \overline{OE} is asserted LOW, the pins behave as outputs. When HIGH, \overline{DQ}_s and $\overline{DQP}_{[A:B]}$ are placed in a tristate condition. |
| V_{DD} | Power supply | Power supply inputs to the core of the device. |
| V_{SS} | Ground | Ground for the core of the device. |
| V_{DDQ} | I/O power supply | Power supply for the I/O circuitry. |
| MODE | Input-static | Selects burst order. When tied to GND selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. Mode pin has an internal pull-up. |
| NC | – | No connects. Not Internally connected to the die. |



Pin Definitions *(continued)*

| Name | I/O | Description |
|--|-----|--|
| NC/9M, NC/18M, NC/36M, NC/72M, NC/144M, NC/288M, NC/576M, NC/1G | – | No connects. Not internally connected to the die. NC/9M, NC/18M, NC/36M, NC/72M, NC/144M, NC/288M, NC/576M and NC/1G are address expansion pins that are not internally connected to the die. |

Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CDV}) is 6.5 ns (133 MHz device).

The CY7C1325H supports secondary cache in systems utilizing either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486 processors. The linear burst sequence is suited for processors that utilize a linear burst sequence. The burst order is user-selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the processor address strobe (ADSP) or the controller address strobe (ADSC). Address advancement through the burst sequence is controlled by the ADV input. A two bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the byte write enable (BWE) and byte write select ($BW_{[A:B]}$) inputs. A global write enable (GW) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self timed write circuitry.

Three synchronous chip selects (\overline{CE}_1 , CE_2 , \overline{CE}_3) and an asynchronous output enable (OE) provide for easy bank selection and output tristate control. ADSP is ignored if \overline{CE}_1 is HIGH.

Single Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise: (1) \overline{CE}_1 , CE_2 , and \overline{CE}_3 are all asserted active, and (2) ADSP or ADSC is asserted LOW (if the access is initiated by ADSC, the write inputs must be deasserted during this first cycle). The address presented to the address inputs is latched into the address register and the burst counter/control logic and presented to the memory core. If the OE input is asserted LOW, the requested data is available at the data outputs, a maximum to t_{CDV} after clock rise. ADSP is ignored if \overline{CE}_1 is HIGH.

Single Write Accesses Initiated by \overline{ADSP}

This access is initiated when the following conditions are satisfied at clock rise: (1) \overline{CE}_1 , CE_2 , \overline{CE}_3 are all asserted active, and (2) ADSP is asserted LOW. The addresses presented are loaded into the address register and the burst inputs (GW, BWE, and $BW_{[A:B]}$) are ignored during this first clock cycle. If the write inputs are asserted active (see Write Cycle Descriptions table for appropriate states that indicate a write) on the next clock rise, the

appropriate data is latched and written into the device. Byte writes are allowed. During byte writes, BW_A controls DQ_A and BW_B controls DQ_B . All I/Os are tristated during a byte write. Since this is a common I/O device, the asynchronous OE input signal must be deasserted and the I/Os must be tristated prior to the presentation of data to DQ_S . As a safety precaution, the data lines are tristated after a write cycle is detected, regardless of the state of OE.

Single Write Accesses Initiated by \overline{ADSC}

This write access is initiated when the following conditions are satisfied at clock rise: (1) \overline{CE}_1 , CE_2 , and \overline{CE}_3 are all asserted active, (2) ADSC is asserted LOW, (3) ADSP is deasserted HIGH, and (4) the write input signals (GW, BWE, and $BW_{[A:B]}$) indicate a write access. ADSC is ignored if ADSP is active LOW.

The addresses presented are loaded into the address register and the burst counter/control logic and delivered to the memory core. The information presented to $DQ_{[A:D]}$ is written into the specified address location. Byte writes are allowed. During byte writes, BW_A controls DQ_A , BW_B controls DQ_B . All I/Os are tristated when a write is detected, even a byte write. Since this is a common I/O device, the asynchronous OE input signal must be deasserted and the I/Os must be tristated prior to the presentation of data to DQ_S . As a safety precaution, the data lines are tristated after a write cycle is detected, regardless of the state of OE.

Burst Sequences

The CY7C1325H provides an on-chip two bit wraparound burst counter inside the SRAM. The burst counter is fed by $A_{[1:0]}$, and can follow either a linear or interleaved burst order. The burst order is determined by the state of the MODE input. A LOW on MODE selects a linear burst sequence. A HIGH on MODE selects an interleaved burst order. Leaving MODE unconnected causes the device to default to a interleaved burst sequence.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation "sleep" mode. Two clock cycles are required to enter into or exit from this "sleep" mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the "sleep" mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the "sleep" mode. \overline{CE}_S , ADSP, and ADSC must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

**Interleaved Burst Address Table**(MODE = Floating or V_{DD})

| First Address A1:A0 | Second Address A1:A0 | Third Address A1:A0 | Fourth Address A1:A0 |
|------------------------|-------------------------|------------------------|-------------------------|
| 00 | 01 | 10 | 11 |
| 01 | 00 | 11 | 10 |
| 10 | 11 | 00 | 01 |
| 11 | 10 | 01 | 00 |

Linear Burst Address Table

(MODE = GND)

| First Address A1:A0 | Second Address A1:A0 | Third Address A1:A0 | Fourth Address A1:A0 |
|------------------------|-------------------------|------------------------|-------------------------|
| 00 | 01 | 10 | 11 |
| 01 | 10 | 11 | 00 |
| 10 | 11 | 00 | 01 |
| 11 | 00 | 01 | 10 |

ZZ Mode Electrical Characteristics

| Parameter | Description | Test Conditions | Min | Max | Unit |
|-------------|-----------------------------------|---------------------------|------------|------------|------|
| I_{DDZZ} | Sleep mode standby current | $ZZ \geq V_{DD} - 0.2 V$ | – | 40 | mA |
| t_{ZZS} | Device operation to ZZ | $ZZ \geq V_{DD} - 0.2 V$ | – | $2t_{CYC}$ | ns |
| t_{ZZREC} | ZZ recovery time | $ZZ \leq 0.2 V$ | $2t_{CYC}$ | – | ns |
| t_{ZZI} | ZZ active to sleep current | This parameter is sampled | – | $2t_{CYC}$ | ns |
| t_{RZZI} | ZZ inactive to exit sleep current | This parameter is sampled | 0 | – | ns |



Truth Table

The Truth Table for part CY7C1325H is as follows. [1, 2, 3, 4, 5]

| Cycle Description | Address Used | \overline{CE}_1 | CE_2 | \overline{CE}_3 | ZZ | \overline{ADSP} | \overline{ADSC} | \overline{ADV} | \overline{WRITE} | \overline{OE} | CLK | DQ |
|------------------------------|--------------|-------------------|--------|-------------------|----|-------------------|-------------------|------------------|--------------------|-----------------|-----|-----------|
| Deselected cycle, power-down | None | H | X | X | L | X | L | X | X | X | L-H | Tri-state |
| Deselected cycle, power-down | None | L | L | X | L | L | X | X | X | X | L-H | Tri-state |
| Deselected cycle, power-down | None | L | X | H | L | L | X | X | X | X | L-H | Tri-state |
| Deselected cycle, power-down | None | L | L | X | L | H | L | X | X | X | L-H | Tri-state |
| Deselected cycle, power-down | None | X | X | H | L | H | L | X | X | X | L-H | Tri-state |
| Sleep mode, power-down | None | X | X | X | H | X | X | X | X | X | X | Tri-state |
| Read cycle, begin burst | External | L | H | L | L | L | X | X | X | L | L-H | Q |
| Read cycle, begin burst | External | L | H | L | L | L | X | X | X | H | L-H | Tri-state |
| Write cycle, begin burst | External | L | H | L | L | H | L | X | L | X | L-H | D |
| Read cycle, begin burst | External | L | H | L | L | H | L | X | H | L | L-H | Q |
| Read cycle, begin burst | External | L | H | L | L | H | L | X | H | H | L-H | Tri-state |
| Read cycle, continue burst | Next | X | X | X | L | H | H | L | H | L | L-H | Q |
| Read cycle, continue burst | Next | X | X | X | L | H | H | L | H | H | L-H | Tri-state |
| Read cycle, continue burst | Next | H | X | X | L | X | H | L | H | L | L-H | Q |
| Read cycle, continue burst | Next | H | X | X | L | X | H | L | H | H | L-H | Tri-state |
| Write cycle, continue burst | Next | X | X | X | L | H | H | L | L | X | L-H | D |
| Write cycle, continue burst | Next | H | X | X | L | X | H | L | L | X | L-H | D |
| Read cycle, suspend burst | Current | X | X | X | L | H | H | H | H | L | L-H | Q |
| Read cycle, suspend burst | Current | X | X | X | L | H | H | H | H | H | L-H | Tri-state |
| Read cycle, suspend burst | Current | H | X | X | L | X | H | H | H | L | L-H | Q |
| Read cycle, suspend burst | Current | H | X | X | L | X | H | H | H | H | L-H | Tri-state |
| Write cycle, suspend burst | Current | X | X | X | L | H | H | H | L | X | L-H | D |
| Write cycle, suspend burst | Current | H | X | X | L | X | H | H | L | X | L-H | D |

Notes

- X = "Don't Care." H = Logic HIGH, L = Logic LOW.
- $\overline{WRITE} = L$ when any one or more Byte Write enable signals (\overline{BW}_A , \overline{BW}_B) and $\overline{BWE} = L$ or $\overline{GW} = L$. $\overline{WRITE} = H$ when all Byte write enable signals (\overline{BW}_A , \overline{BW}_B), \overline{BWE} , $\overline{GW} = H$.
- The DQ pins are controlled by the current cycle and the \overline{OE} signal. \overline{OE} is asynchronous and is not sampled with the clock.
- The SRAM always initiates a read cycle when \overline{ADSP} is asserted, regardless of the state of \overline{GW} , \overline{BWE} , or $\overline{BW}_{[A, B]}$. Writes may occur only on subsequent clocks after the \overline{ADSP} or with the assertion of \overline{ADSC} . As a result, \overline{OE} must be driven HIGH prior to the start of the write cycle to allow the outputs to tristate. \overline{OE} is a don't care for the remainder of the write cycle.
- \overline{OE} is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are tristate when \overline{OE} is inactive or when the device is deselected, and all data bits behave as output when \overline{OE} is active (LOW).



Truth Table for Read/Write

The Truth Table for Read/Write for part CY7C1325H is as follows. ^[6]

| Function | \overline{GW} | \overline{BWE} | \overline{BW}_B | \overline{BW}_A |
|--|-----------------|------------------|-------------------|-------------------|
| Read | H | H | X | X |
| Read | H | L | H | H |
| Write byte A – (DQ _A and DQP _A) | H | L | H | L |
| Write byte B – (DQ _B and DQP _B) | H | L | L | H |
| Write all bytes | H | L | L | L |
| Write all bytes | L | X | X | X |

Note

6. X = "Don't Care." H = Logic HIGH, L = Logic LOW.



Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

| | |
|--|------------------------------------|
| Storage temperature | -65 °C to +150 °C |
| Ambient temperature with power applied | -55 °C to +125 °C |
| Supply voltage on V _{DD} relative to GND | -0.5 V to +4.6 V |
| Supply voltage on V _{DDQ} relative to GND | -0.5 V to +V _{DD} |
| DC voltage applied to outputs in tristate | -0.5 V to V _{DDQ} + 0.5 V |
| DC input voltage | -0.5 V to V _{DD} + 0.5 V |
| Current into outputs (LOW) | 20 mA |
| Static discharge voltage (per MIL-STD-883, method 3015) | > 2001 V |
| Latch-up current | > 200 mA |

Operating Range

| Range | Ambient Temperature | V _{DD} | V _{DDQ} |
|------------|---------------------|--------------------|-------------------------------|
| Industrial | -40 °C to +85 °C | 3.3 V – 5% / + 10% | 2.5 V – 5% to V _{DD} |

Neutron Soft Error Immunity

| Parameter | Description | Test Conditions | Typ | Max* | Unit |
|-----------|---------------------------|-----------------|-----|------|---------|
| LSBU | Logical single bit upsets | 25 °C | 361 | 394 | FIT/Mb |
| LMBU | Logical multi bit upsets | 25 °C | 0 | 0.01 | FIT/Mb |
| SEL | Single event latch up | 85 °C | 0 | 0.1 | FIT/Dev |

* No LMBU or SEL events occurred during testing; this column represents a statistical χ^2 , 95% confidence limit calculation. For more details refer to Application Note AN54908 "Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates".

Electrical Characteristics

Over the Operating Range

| Parameter [7, 8] | Description | Test Conditions | Min | Max | Unit |
|-------------------------|--|--|-------|-----------------------|------|
| V _{DD} | Power supply voltage | | 3.135 | 3.6 | V |
| V _{DDQ} | I/O supply voltage | | 2.375 | V _{DD} | V |
| V _{OH} | Output HIGH voltage | for 3.3 V I/O, I _{OH} = -4.0 mA | 2.4 | - | V |
| | | for 2.5 V I/O, I _{OH} = -1.0 mA | 2.0 | - | V |
| V _{OL} | Output LOW voltage | for 3.3 V I/O, I _{OL} = 8.0 mA | - | 0.4 | V |
| | | for 2.5 V I/O, I _{OL} = 1.0 mA | - | 0.4 | V |
| V _{IH} | Input HIGH voltage | for 3.3 V I/O | 2.0 | V _{DD} + 0.3 | V |
| | | for 2.5 V I/O | 1.7 | V _{DD} + 0.3 | V |
| V _{IL} | Input LOW voltage ^[7] | for 3.3 V I/O | -0.3 | 0.8 | V |
| | | for 2.5 V I/O | -0.3 | 0.7 | V |
| I _X | Input leakage current except ZZ and MODE | GND ≤ V _I ≤ V _{DDQ} | -5 | 5 | μA |
| | Input current of MODE | Input = V _{SS} | -30 | - | μA |
| | | Input = V _{DD} | - | 5 | μA |
| | Input current of ZZ | Input = V _{SS} | -5 | - | μA |
| Input = V _{DD} | | - | 30 | μA | |
| I _{OZ} | Output leakage current | GND ≤ V _I ≤ V _{DDQ} , output disabled | -5 | 5 | μA |
| I _{DD} | V _{DD} operating supply current | V _{DD} = Max, I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{CYC} | | | |
| | | 7.5 ns cycle, 133 MHz | - | 225 | mA |

Notes

- Overshoot: V_{IH(AC)} < V_{DD} + 1.5 V (Pulse width less than t_{CYC}/2), undershoot: V_{IL(AC)} > -2 V (Pulse width less than t_{CYC}/2).
- T_{power up}: Assumes a linear ramp from 0 V to V_{DD(min)} within 200 ms. During this time V_{IH} < V_{DD} and V_{DDQ} ≤ V_{DD}.



Electrical Characteristics *(continued)*

Over the Operating Range

| Parameter [7, 8] | Description | Test Conditions | Min | Max | Unit |
|------------------|---|--|-----|-----|------|
| I_{SB1} | Automatic CE power-down current – TTL inputs | Max V_{DD} , device deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$, inputs switching | – | 90 | mA |
| I_{SB2} | Automatic CE power-down current – CMOS inputs | Max V_{DD} , device deselected, $V_{IN} \geq V_{DD} - 0.3$ V or $V_{IN} \leq 0.3$ V, $f = 0$, inputs static | – | 40 | mA |
| I_{SB3} | Automatic CE power-down current – CMOS inputs | Max V_{DD} , device deselected, $V_{IN} \geq V_{DDQ} - 0.3$ V or $V_{IN} \leq 0.3$ V, $f = f_{MAX}$, inputs switching | – | 75 | mA |
| I_{SB4} | Automatic CE power-down current – TTL inputs | Max V_{DD} , device deselected, $V_{IN} \geq V_{DD} - 0.3$ V or $V_{IN} \leq 0.3$ V, $f = 0$, inputs static | – | 45 | mA |

Capacitance

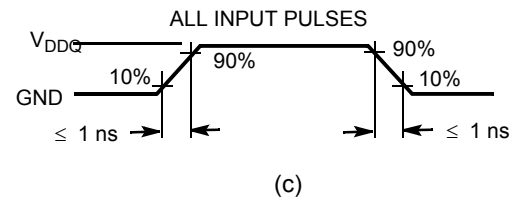
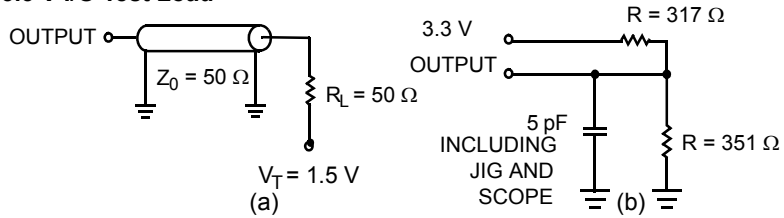
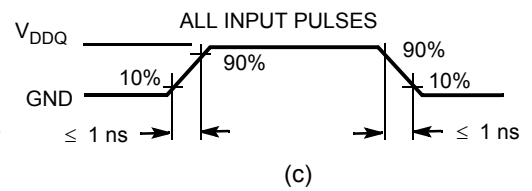
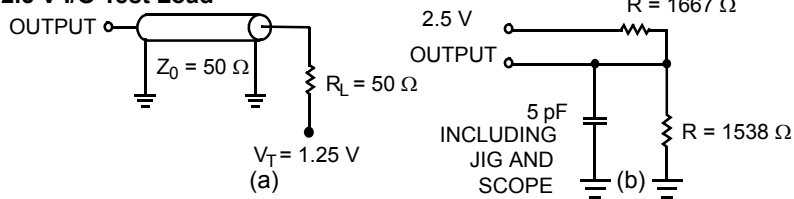
| Parameter [9] | Description | Test Conditions | 100-pin TQFP Max | Unit |
|---------------|--------------------------|--|------------------|------|
| C_{IN} | Input capacitance | $T_A = 25$ °C, $f = 1$ MHz, $V_{DD} = 3.3$ V, $V_{DDQ} = 3.3$ V | 5 | pF |
| C_{CLK} | Clock input capacitance | | 5 | pF |
| $C_{I/O}$ | Input/Output capacitance | | 5 | pF |

Thermal Resistance

| Parameter [9] | Description | Test Conditions | 100-pin TQFP Package | Unit |
|---------------|--|--|----------------------|------|
| Θ_{JA} | Thermal resistance (junction to ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51. | 30.32 | °C/W |
| Θ_{JC} | Thermal resistance (junction to case) | | 6.85 | °C/W |

Note

9. Tested initially and after any design or process change that may affect these parameters.

AC Test Loads and Waveforms**Figure 2. AC Test Loads and Waveforms****3.3 V I/O Test Load****2.5 V I/O Test Load**



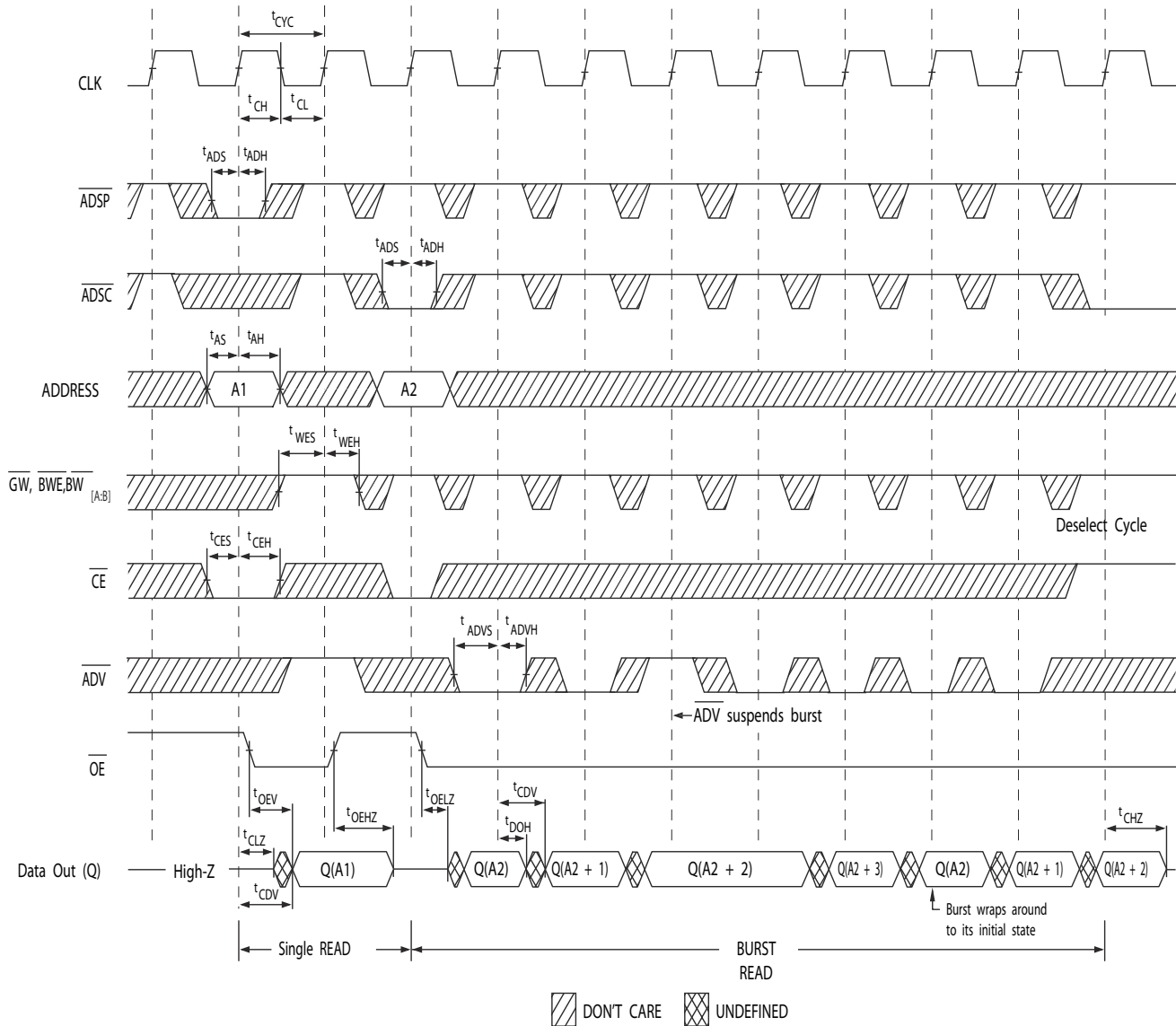
Switching Characteristics

Over the Operating Range

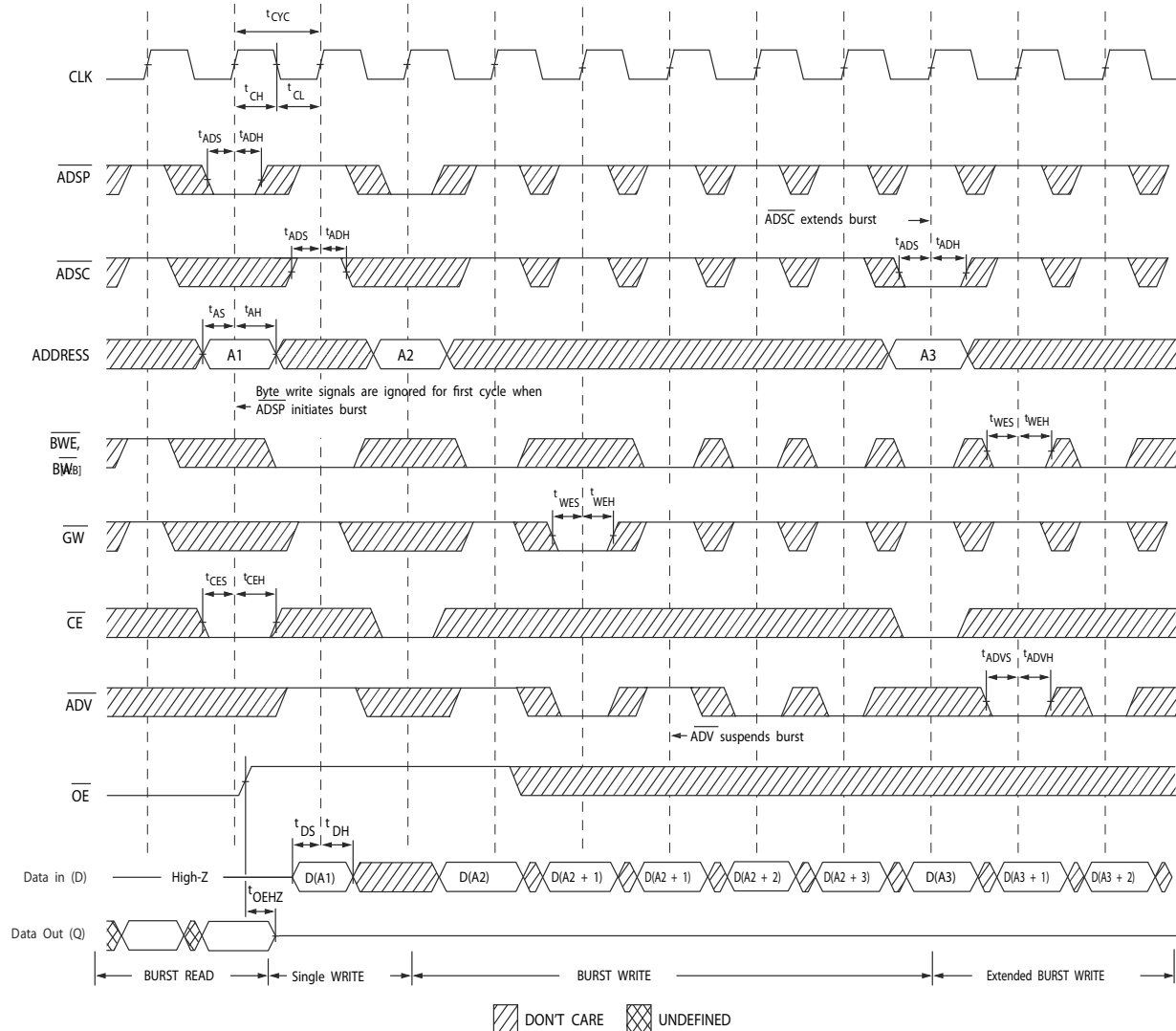
| Parameter ^[10, 11] | Description | -133 | | Unit |
|-------------------------------|---|------|-----|------|
| | | Min | Max | |
| t _{POWER} | V _{DD} (typical) to the first access ^[12] | 1 | – | ms |
| Clock | | | | |
| t _{CYC} | Clock cycle time | 7.5 | – | ns |
| t _{CH} | Clock HIGH | 2.5 | – | ns |
| t _{CL} | Clock LOW | 2.5 | – | ns |
| Output Times | | | | |
| t _{CDV} | Data output valid after CLK rise | – | 6.5 | ns |
| t _{DOH} | Data output hold after CLK rise | 2.0 | – | ns |
| t _{CLZ} | Clock to low Z ^[13, 14, 15] | 0 | – | ns |
| t _{CHZ} | Clock to high Z ^[13, 14, 15] | – | 3.5 | ns |
| t _{OEV} | $\overline{\text{OE}}$ LOW to output valid | – | 3.5 | ns |
| t _{OELZ} | $\overline{\text{OE}}$ LOW to output low Z ^[13, 14, 15] | 0 | – | ns |
| t _{OEHZ} | $\overline{\text{OE}}$ HIGH to output high Z ^[13, 14, 15] | – | 3.5 | ns |
| Setup Times | | | | |
| t _{AS} | Address setup before CLK rise | 1.5 | – | ns |
| t _{ADS} | ADSP, ADSC setup before CLK rise | 1.5 | – | ns |
| t _{ADVS} | $\overline{\text{ADV}}$ setup before CLK rise | 1.5 | – | ns |
| t _{WES} | $\overline{\text{GW}}$, $\overline{\text{BWE}}$, $\overline{\text{BW}}_x$ setup before CLK rise | 1.5 | – | ns |
| t _{DS} | Data input setup before CLK rise | 1.5 | – | ns |
| t _{CES} | Chip enable setup | 1.5 | – | ns |
| Hold Times | | | | |
| t _{AH} | Address hold after CLK rise | 0.5 | – | ns |
| t _{ADH} | ADSP, ADSC hold after CLK rise | 0.5 | – | ns |
| t _{WEH} | $\overline{\text{GW}}$, $\overline{\text{BWE}}$, $\overline{\text{BW}}_x$ hold after CLK rise | 0.5 | – | ns |
| t _{ADVH} | $\overline{\text{ADV}}$ hold after CLK rise | 0.5 | – | ns |
| t _{DH} | Data input hold after CLK rise | 0.5 | – | ns |
| t _{CEH} | Chip enable hold after CLK rise | 0.5 | – | ns |

Notes

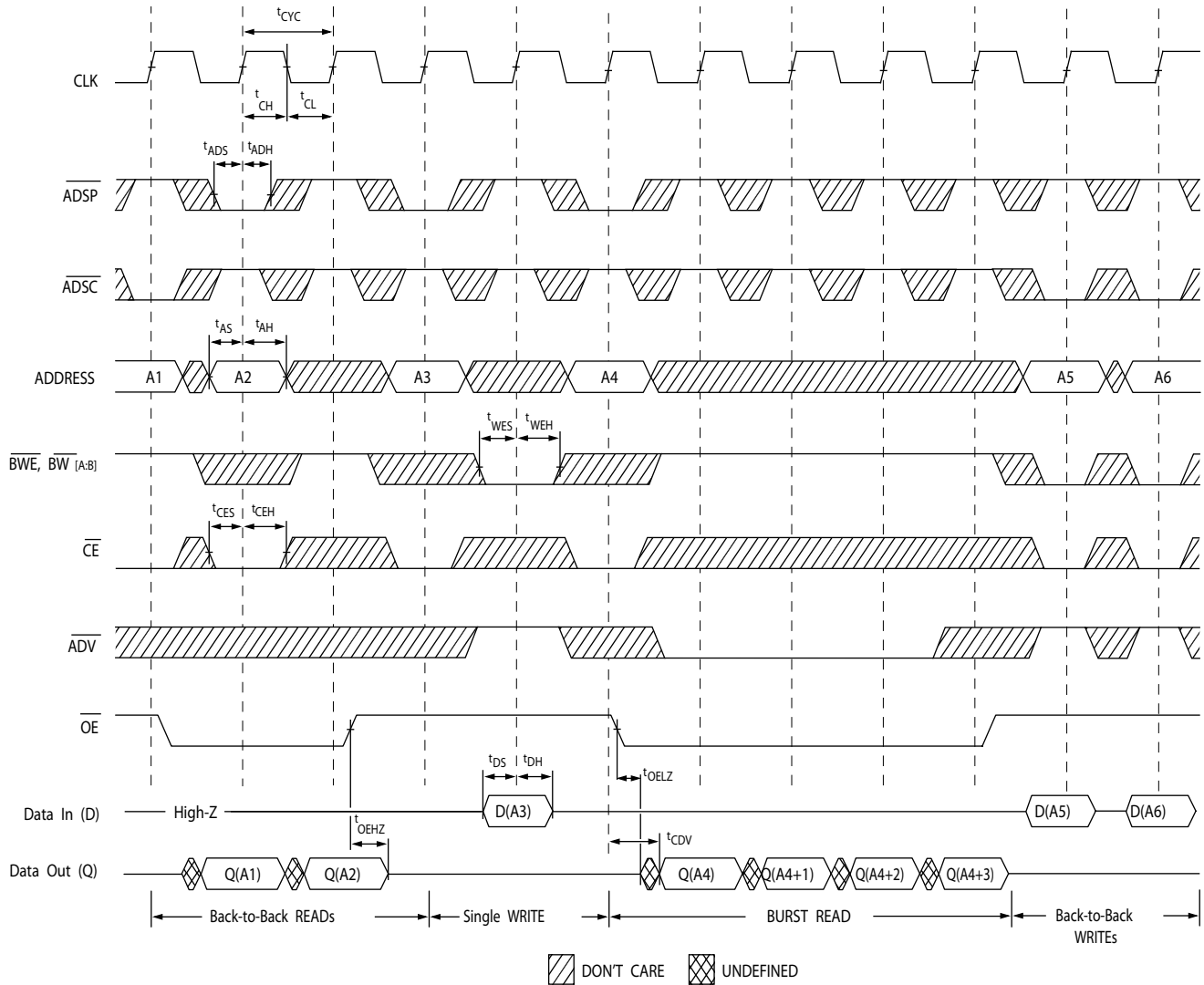
10. Timing reference level is 1.5 V when V_{DDQ} = 3.3 V and is 1.25 V when V_{DDQ} = 2.5 V.
11. Test conditions shown in (a) of [Figure 2 on page 11](#) unless otherwise noted.
12. This part has a voltage regulator internally; t_{POWER} is the time that the power needs to be supplied above V_{DD(minimum)} initially before a read or write operation can be initiated.
13. t_{CHZ}, t_{CLZ}, t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of [Figure 2 on page 11](#). Transition is measured ± 200 mV from steady-state voltage.
14. At any voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve high Z prior to low Z under the same system conditions.
15. This parameter is sampled and not 100% tested.

Timing Diagrams**Figure 3. Read Cycle Timing** [16]**Note**

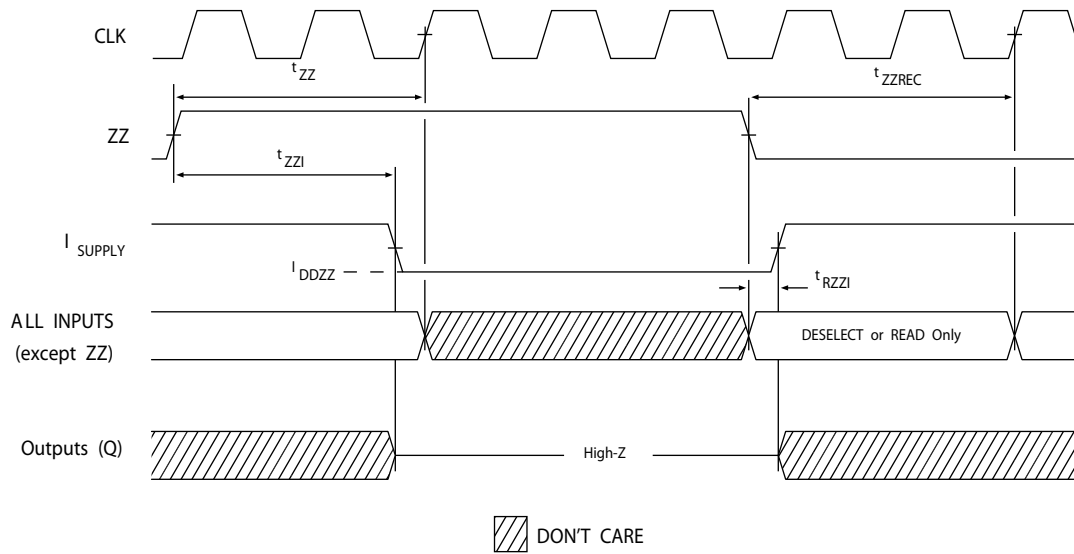
16. On this diagram, when \overline{CE} is LOW: \overline{CE}_1 is LOW, CE_2 is HIGH and \overline{CE}_3 is LOW. When \overline{CE} is HIGH: \overline{CE}_1 is HIGH or CE_2 is LOW or \overline{CE}_3 is HIGH.

Timing Diagrams (continued)**Figure 4. Write Cycle Timing** [17, 18]**Notes**

17. On this diagram, when \overline{CE} is LOW: \overline{CE}_1 is LOW, CE_2 is HIGH and \overline{CE}_3 is LOW. When \overline{CE} is HIGH: \overline{CE}_1 is HIGH or CE_2 is LOW or \overline{CE}_3 is HIGH.
 18. Full width write can be initiated by either GW LOW; or by GW HIGH, BWE LOW and $BW_{[A:B]}$ LOW.

Timing Diagrams (continued)**Figure 5. Read/Write Timing** [19, 20, 21]**Notes**

19. On this diagram, when \overline{CE} is LOW: \overline{CE}_1 is LOW, \overline{CE}_2 is HIGH and \overline{CE}_3 is LOW. When \overline{CE} is HIGH: \overline{CE}_1 is HIGH or \overline{CE}_2 is LOW or \overline{CE}_3 is HIGH.
 20. The data bus (Q) remains in High Z following a WRITE cycle, unless a new read access is initiated by ADSP or ADSC.
 21. \overline{GW} is HIGH.

Timing Diagrams (continued)**Figure 6. ZZ Mode Timing** [22, 23]**Notes**

22. Device must be deselected when entering ZZ mode. See Cycle Descriptions table for all possible signal conditions to deselect the device.
 23. DQs are in High Z when exiting ZZ sleep mode.



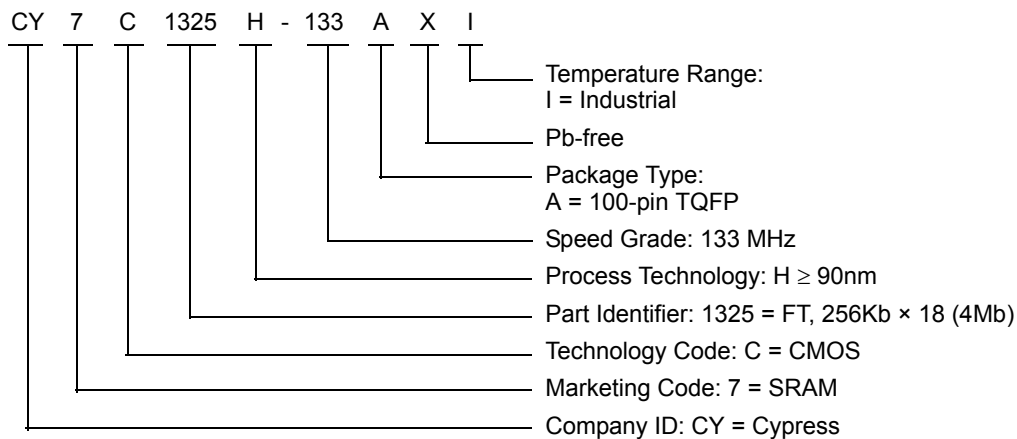
Ordering Information

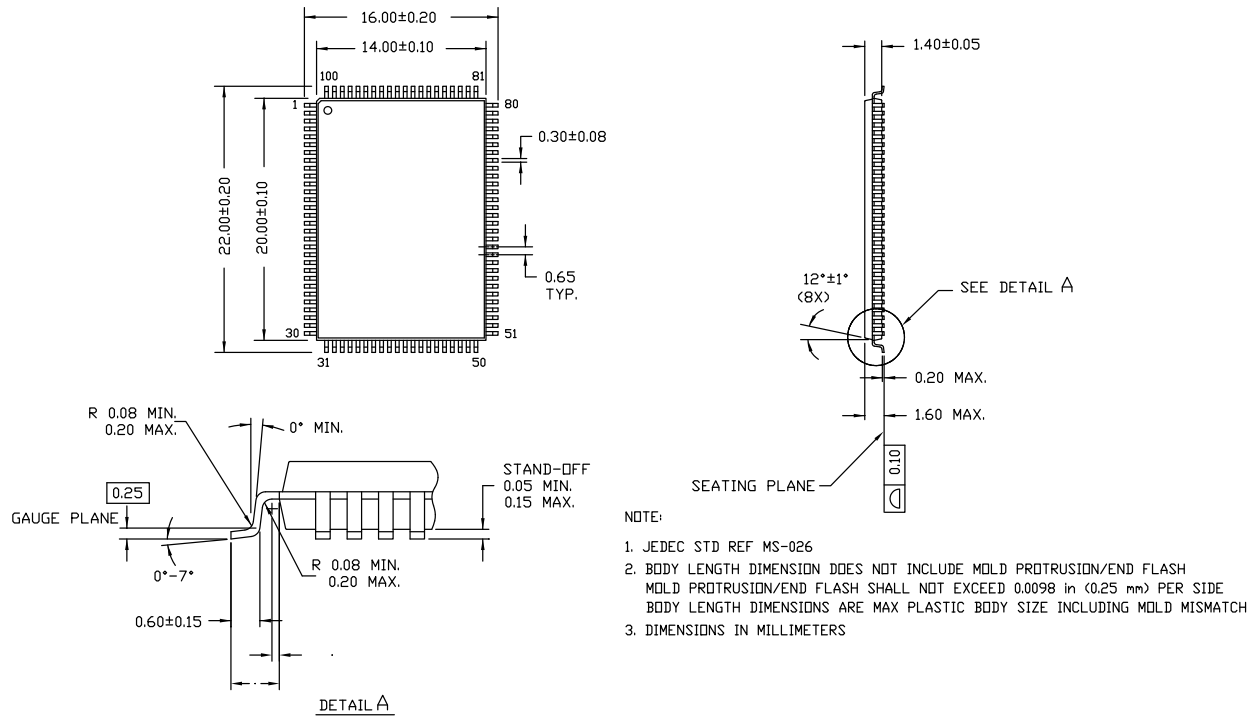
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| Speed (MHz) | Ordering Code | Package Diagram | Part and Package Type | Operating Range |
|-------------|------------------|-----------------|---|-----------------|
| 133 | CY7C1325H-133AXI | 51-85050 | 100-pin TQFP (14 × 20 × 1.4 mm) Pb-free | Industrial |

Ordering Code Definitions



Package Diagrams**Figure 7. 100-pin TQFP (14 × 20 × 1.4 mm) Package Outline, 51-85050**

51-85050 *E



Acronyms

| Acronym | Description |
|-----------------|--|
| CMOS | Complementary Metal Oxide Semiconductor |
| \overline{CE} | Chip Enable |
| CEN | Clock Enable |
| EIA | Electronic Industries Alliance |
| I/O | Input/Output |
| JEDEC | Joint Electron Devices Engineering Council |
| \overline{OE} | Output Enable |
| SRAM | Static Random Access Memory |
| TQFP | Thin Quad Flat Pack |
| TTL | Transistor-Transistor Logic |
| \overline{WE} | Write Enable |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|---------------|-----------------|
| °C | degree Celsius |
| MHz | megahertz |
| μA | microampere |
| mA | milliampere |
| mm | millimeter |
| ms | millisecond |
| mV | millivolt |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| V | volt |
| W | watt |



Document History Page

| Document Title: CY7C1325H, 4-Mbit (256K × 18) Flow-Through Sync SRAM Document Number: 001-86114 | | | | |
|--|---------|-----------------|-----------------|--|
| Rev. | ECN No. | Orig. of Change | Submission Date | Description of Change |
| ** | 3908939 | PRIT | 02/20/2013 | New data sheet. |
| *A | 4291116 | PRIT | 02/25/2014 | Updated Package Diagrams : spec 51-85050 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review. |
| *B | 4571750 | PRIT | 11/18/2014 | Updated Functional Description : Added “For a complete list of related documentation, click here .” at the end. |
| *C | 5097432 | PRIT | 01/21/2016 | Updated to new template. Completing Sunset Review. |
| *D | 5321039 | PRIT | 06/23/2016 | Updated Truth Table . Updated to new template. |



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