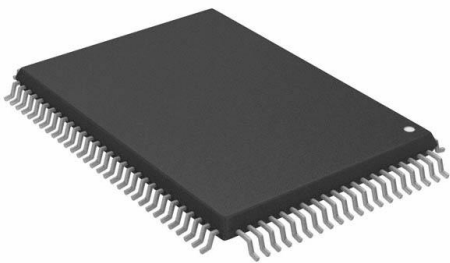


CY7C1353G-100AXCT Datasheet

www.digi-electronics.com



<https://www.DiGi-Electronics.com>

DiGi Electronics Part Number	CY7C1353G-100AXCT-DG
Manufacturer	Infineon Technologies
Manufacturer Product Number	CY7C1353G-100AXCT
Description	IC SRAM 4.5MBIT PAR 100TQFP
Detailed Description	SRAM - Synchronous, SDR Memory IC 4.5Mbit Parallel 100 MHz 8 ns 100-TQFP (14x20)

This model CY7C1353G-100AXCT is available at DiGi Electronics.

DiGi Electronics offers a global database of semiconductor and electronic component datasheets.

We welcome your inquiries regarding pricing, lead time, or other product-related questions.

 [Request a Quote](#)

 [Datasheet Search](#)



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.

Purchase and inquiry

Manufacturer Product Number:

CY7C1353G-100AXCT

Series:

NoBL™

DiGi-Electronics Programmable:

Not Verified

Memory Format:

SRAM

Memory Size:

4.5Mbit

Memory Interface:

Parallel

Write Cycle Time - Word, Page:

-

Voltage - Supply:

3.135V ~ 3.465V

Mounting Type:

Surface Mount

Supplier Device Package:

100-TQFP (14x20)

Manufacturer:

Infineon Technologies

Product Status:

Active

Memory Type:

Volatile

Technology:

SRAM - Synchronous, SDR

Memory Organization:

256K x 18

Clock Frequency:

100 MHz

Access Time:

8 ns

Operating Temperature:

0°C ~ 70°C (TA)

Package / Case:

100-LQFP

Base Product Number:

CY7C1353

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.32.0041

Moisture Sensitivity Level (MSL):

3 (168 Hours)

ECCN:

3A991B2A



Please note that Cypress is an Infineon Technologies Company.

The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content

The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.



CY7C1353G

4-Mbit (256K × 18) Flow-Through SRAM with NoBL™ Architecture

Features

- Supports up to 100-MHz bus operations with zero wait states
 - Data is transferred on every clock
- Pin compatible and functionally equivalent to ZBT™ devices
- Internally self timed output buffer control to eliminate the need to use OE
- Registered inputs for flow-through operation
- Byte write capability
- 256K × 18 common I/O architecture
- 2.5 V/3.3 V I/O power supply (V_{DDQ})
- Fast clock-to-output times
 - 8.0 ns (for 100 MHz device)
- Clock enable ($\overline{\text{CEN}}$) pin to suspend operation
- Synchronous self timed writes
- Asynchronous output enable
- Available in Pb-free 100-pin TQFP package
- Burst capability – linear or interleaved burst order
- Low standby power

Functional Description

The CY7C1353G is a 3.3 V, 256K × 18 synchronous flow-through burst SRAM designed specifically to support unlimited true back-to-back read/write operations without the insertion of wait states. The CY7C1353G is equipped with the advanced No Bus Latency™ (NoBL™) logic required to enable consecutive read/write operations with data being transferred on every clock cycle. This feature dramatically improves the throughput of data through the SRAM, especially in systems that require frequent write-read transitions.

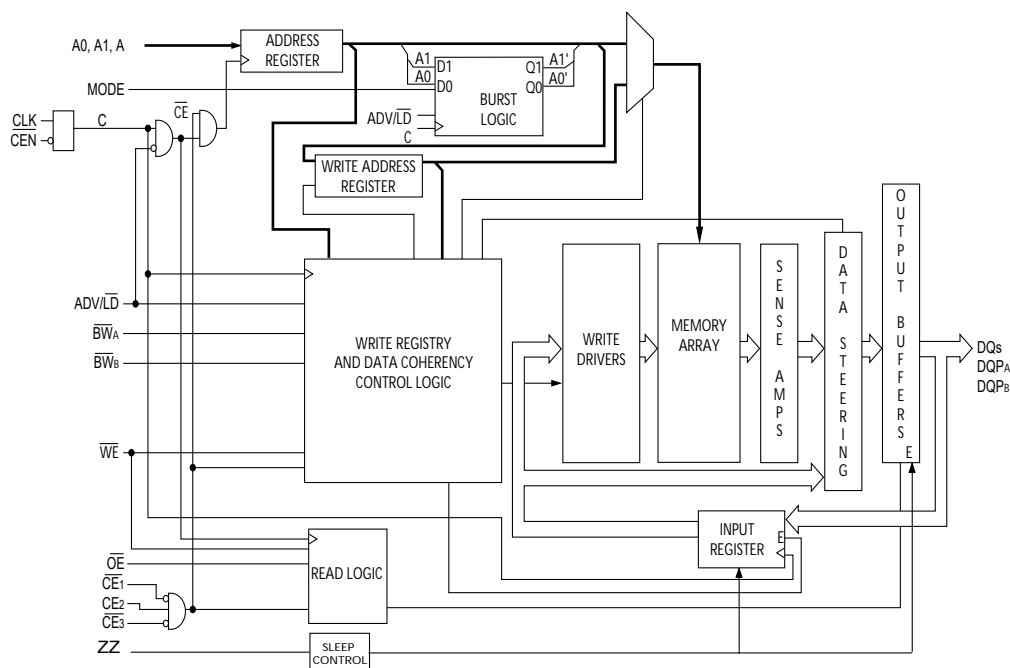
All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock input is qualified by the clock enable (CEN) signal, which when deasserted suspends operation and extends the previous clock cycle. Maximum access delay from the clock rise is 8.0 ns (100 MHz device).

Write operations are controlled by the two byte write select ($\overline{\text{BW}}_{[A:B]}$) and a write enable ($\overline{\text{WE}}$) input. All writes are conducted with on-chip synchronous self timed write circuitry.

Three synchronous chip enables ($\overline{\text{CE}}_1, \overline{\text{CE}}_2, \overline{\text{CE}}_3$) and an asynchronous output enable (OE) provide for easy bank selection and output tri-state control. To avoid bus contention, the output drivers are synchronously tri-stated during the data portion of a write sequence.

For a complete list of related documentation, click [here](#).

Logic Block Diagram



Errata: For information on silicon errata, see [Errata](#) on page 16. Details include trigger conditions, devices affected, and proposed workaround.



Contents

Selection Guide	3	Switching Characteristics	10
Pin Configuration	3	Switching Waveforms	11
Pin Definitions	4	Ordering Information	13
Functional Overview	5	Ordering Code Definitions	13
Single Read Accesses	5	Package Diagram	14
Burst Read Accesses	5	Acronyms	15
Single Write Accesses	5	Document Conventions	15
Burst Write Accesses	6	Units of Measure	15
Sleep Mode	6	Errata	16
Linear Burst Address Table	6	Part Numbers Affected	16
Interleaved Burst Address Table	6	Product Status	16
ZZ Mode Electrical Characteristics	6	Ram9 NoBL ZZ Pin Issues Errata Summary	16
Truth Table	7	Document History Page	17
Partial Truth Table for Read/Write	7	Sales, Solutions, and Legal Information	19
Maximum Ratings	8	Worldwide Sales and Design Support	19
Operating Range	8	Products	19
Electrical Characteristics	8	PSoC® Solutions	19
Capacitance	9	Cypress Developer Community	19
Thermal Resistance	9	Technical Support	19
AC Test Loads and Waveforms	9		

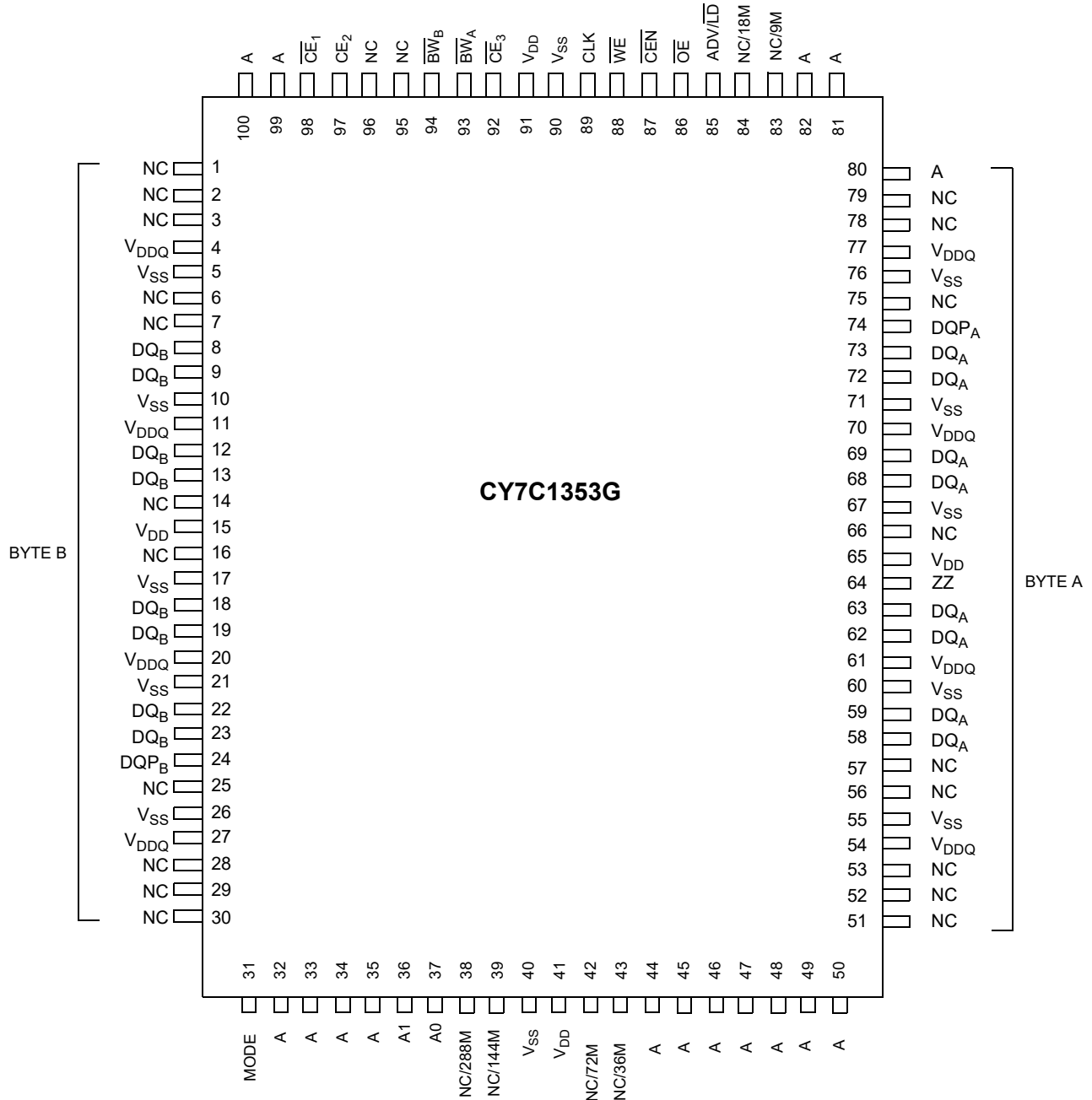


Selection Guide

Description	100 MHz	Unit
Maximum access time	8.0	ns
Maximum operating current	205	mA
Maximum CMOS standby current	40	mA

Pin Configuration

Figure 1. 100-pin TQFP (14 × 20 × 1.4 mm) pinout ^[1]



Note

1. **Errata:** The ZZ pin (Pin 64) needs to be externally connected to ground. For more information, see [Errata on page 16](#).



Pin Definitions

Name	I/O	Description
A ₀ , A ₁ , A	Input-synchronous	Address inputs used to select one of the 256K address locations. Sampled at the rising edge of the CLK. A _[1:0] are fed to the two-bit burst counter.
BW _[A:B]	Input-synchronous	Byte write inputs, active LOW. Qualified with \overline{WE} to conduct writes to the SRAM. Sampled on the rising edge of CLK.
\overline{WE}	Input-synchronous	Write enable input, active LOW. Sampled on the rising edge of CLK if \overline{CEN} is active LOW. This signal must be asserted LOW to initiate a write sequence.
ADV/LD	Input-synchronous	Advance/load input. Used to advance the on-chip address counter or load a new address. When HIGH (and CEN is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After being deselected, ADV/LD must be driven LOW to load a new address.
CLK	Input-clock	Clock input. Used to capture all synchronous inputs to the device. CLK is qualified with \overline{CEN} . CLK is only recognized if \overline{CEN} is active LOW.
\overline{CE}_1	Input-synchronous	Chip enable 1 input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with \overline{CE}_2 , and \overline{CE}_3 to select/deselect the device.
\overline{CE}_2	Input-synchronous	Chip enable 2 input, active HIGH. Sampled on the rising edge of CLK. Used in conjunction with \overline{CE}_1 and \overline{CE}_3 to select/deselect the device.
\overline{CE}_3	Input-synchronous	Chip enable 3 input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with \overline{CE}_1 and \overline{CE}_2 to select/deselect the device.
\overline{OE}	Input-asynchronous	Output enable, asynchronous input, active LOW. Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins. \overline{OE} is masked during the data portion of a write sequence, during the first clock when emerging from a deselected state, when the device has been deselected.
\overline{CEN}	Input-synchronous	Clock enable input, active LOW. When asserted LOW the clock signal is recognized by the SRAM. When deasserted HIGH the clock signal is masked. While deasserting \overline{CEN} does not deselect the device, \overline{CEN} can be used to extend the previous cycle when required.
ZZ ^[2]	Input-asynchronous	ZZ "sleep" Input. This active HIGH input places the device in a non-time critical "sleep" condition with data integrity preserved. During normal operation, this pin has to be low or left floating. ZZ pin has an internal pull-down.
DQ _s	I/O-synchronous	Bidirectional data I/O lines. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by address during the clock rise of the read cycle. The direction of the pins is controlled by \overline{OE} and the internal control logic. When \overline{OE} is asserted LOW, the pins can behave as outputs. When HIGH, DQ _s and DQP _[A:B] are placed in a tri-state condition. The outputs are automatically tri-stated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of \overline{OE} .

Note

- Errata:** The ZZ pin (Pin 64) needs to be externally connected to ground. For more information, see [Errata on page 16](#).



Pin Definitions *(continued)*

Name	I/O	Description
DQP _[A:B]	I/O-synchronous	Bidirectional data parity I/O lines. Functionally, these signals are identical to DQ _s . During write sequences, DQP _[A:B] is controlled by BW _x correspondingly.
MODE	Input strap pin	MODE input. Selects the burst order of the device. When tied to GND selects linear burst sequence. When tied to V _{DD} or left floating selects interleaved burst sequence.
V _{DD}	Power supply	Power supply inputs to the core of the device.
V _{DDQ}	I/O power supply	Power supply for the I/O circuitry.
V _{SS}	Ground	Ground for the device.
NC, NC/9M, NC/18M, NC/36M, NC/72M, NC/144M, NC/288M	–	No Connects. Not internally connected to the die. NC/9M, NC/18M, NC/72M, NC/144M, NC/288M are address expansion pins are not internally connected to the die.

Functional Overview

The CY7C1353G is a synchronous flow-through burst SRAM designed specifically to eliminate wait states during write-read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the clock enable input signal (\overline{CEN}). If \overline{CEN} is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with \overline{CEN} . Maximum access delay from the clock rise (t_{CDV}) is 8.0 ns (100-MHz device).

Accesses can be initiated by asserting all three chip enables (\overline{CE}_1 , \overline{CE}_2 , \overline{CE}_3) active at the rising edge of the clock. If clock enable (\overline{CEN}) is active LOW and $\overline{ADV/LD}$ is asserted LOW, the address presented to the device is latched. The access can either be a read or write operation, depending on the status of the write enable (\overline{WE}). $BW_{[A:B]}$ can be used to conduct byte write operations.

Write operations are qualified by the write enable (\overline{WE}). All writes are simplified with on-chip synchronous self timed write circuitry.

Three synchronous chip enables (\overline{CE}_1 , \overline{CE}_2 , \overline{CE}_3) and an asynchronous output enable (\overline{OE}) simplify depth expansion. All operations (reads, writes, and deselections) are pipe lined. $\overline{ADV/LD}$ must be driven LOW after the device has been deselected to load a new address for the next operation.

Single Read Accesses

A read access is initiated when the following conditions are satisfied at clock rise: (1) \overline{CEN} is asserted LOW, (2) \overline{CE}_1 , \overline{CE}_2 , and \overline{CE}_3 are all asserted active, (3) the write enable input signal \overline{WE} is deasserted HIGH, and (4) $\overline{ADV/LD}$ is asserted LOW. The address presented to the address inputs is latched into the address register and presented to the memory array and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the output buffers. The data is available within 8.0 ns (100-MHz device) provided \overline{OE} is active LOW. After the first clock of the read access, the output buffers are controlled by \overline{OE} and the internal control logic. \overline{OE} must be driven LOW in order for the

device to drive out the requested data. On the subsequent clock, another operation (read/write/deselect) can be initiated. When the SRAM is deselected at clock rise by one of the chip enable signals, its output is tri-stated immediately.

Burst Read Accesses

The CY7C1353G has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four reads without reasserting the address inputs. $\overline{ADV/LD}$ must be driven LOW to load a new address into the SRAM, as described in the [Single Read Accesses](#). The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence, and wraps around when incremented sufficiently. A HIGH input on $\overline{ADV/LD}$ increments the internal burst counter regardless of the state of chip enable inputs or \overline{WE} . \overline{WE} is latched at the beginning of a burst cycle. Therefore, the type of access (read or write) is maintained throughout the burst sequence.

Single Write Accesses

Write access are initiated when these conditions are satisfied at clock rise:

- \overline{CEN} is asserted LOW
- \overline{CE}_1 , \overline{CE}_2 , and \overline{CE}_3 are all asserted active
- The write signal \overline{WE} is asserted LOW.

The address presented to the address bus is loaded into the address register. The write signals are latched into the control logic block. The data lines are automatically tri-stated regardless of the state of the \overline{OE} input signal. This allows the external logic to present the data on DQs and DQP_[A:B].

On the next clock rise the data presented to DQs and DQP_[A:B] (or a subset for byte write operations, see truth table for details) inputs is latched into the device and the write is complete. Additional accesses (read/write/deselect) can be initiated on this cycle.



The data written during the write operation is controlled by $BW_{[A:B]}$ signals. The CY7C1353G provides byte write capability that is described in the truth table. Asserting the write enable input (\overline{WE}) with the selected byte write select input selectively writes to only the desired bytes. Bytes not selected during a byte write operation remains unaltered. A synchronous self timed write mechanism has been provided to simplify the write operations. Byte write capability has been included to greatly simplify read/modify/write sequences, which can be reduced to simple byte write operations.

Because the CY7C1353G is a common I/O device, data must not be driven into the device while the outputs are active. The output enable (\overline{OE}) can be deasserted HIGH before presenting data to the DQs and $DQP_{[A:B]}$ inputs. Doing so tri-states the output drivers. As a safety precaution, DQs and $DQP_{[A:B]}$ are automatically tri-stated during the data portion of a write cycle, regardless of the state of \overline{OE} .

Burst Write Accesses

The CY7C1353G has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four write operations without reasserting the address inputs. ADV/LD must be driven LOW to load the initial address, as described in the [Single Write Accesses on page 5](#). When ADV/LD is driven HIGH on the subsequent clock rise, the chip enables (CE_1 , CE_2 , and CE_3) and WE inputs are ignored and the burst counter is incremented. The correct $BW_{[A:B]}$ inputs must be driven in each cycle of the burst write, to write the correct bytes of data.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode.

While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. \overline{CE}_1 , CE_2 , and CE_3 , must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Linear Burst Address Table

(MODE = GND)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Interleaved Burst Address Table

(MODE = Floating or V_{DD})

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	$ZZ \geq V_{DD} - 0.2 V$	–	40	mA
t_{ZZS}	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2 V$	–	$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	$ZZ \leq 0.2 V$	$2t_{CYC}$	–	ns
t_{ZZI}	ZZ active to sleep current	This parameter is sampled	–	$2t_{CYC}$	ns
t_{RZZI}	ZZ inactive to exit sleep current	This parameter is sampled	0	–	ns



Truth Table

The truth table for CY7C1353G follows. [3, 4, 5, 6, 7, 8, 9]

Operation	Address Used	\overline{CE}_1	CE_2	\overline{CE}_3	ZZ	ADV/LD	\overline{WE}	\overline{BW}_x	\overline{OE}	\overline{CEN}	CLK	DQ
Deselect cycle	None	H	X	X	L	L	X	X	X	L	L->H	Tri-state
Deselect cycle	None	X	X	H	L	L	X	X	X	L	L->H	Tri-state
Deselect cycle	None	X	L	X	L	L	X	X	X	L	L->H	Tri-state
Continue deselect cycle	None	X	X	X	L	H	X	X	X	L	L->H	Tri-state
READ cycle (begin burst)	External	L	H	L	L	L	H	X	L	L	L->H	Data out (Q)
READ cycle (continue burst)	Next	X	X	X	L	H	X	X	L	L	L->H	Data out (Q)
NOP/DUMMY READ (begin burst)	External	L	H	L	L	L	H	X	H	L	L->H	Tri-state
DUMMY READ (continue burst)	Next	X	X	X	L	H	X	X	H	L	L->H	Tri-state
WRITE cycle (begin burst)	External	L	H	L	L	L	L	L	X	L	L->H	Data in (D)
WRITE cycle (continue burst)	Next	X	X	X	L	H	X	L	X	L	L->H	Data in (D)
NOP/WRITE ABORT (begin burst)	None	L	H	L	L	L	L	H	X	L	L->H	Tri-state
WRITE ABORT (continue burst)	Next	X	X	X	L	H	X	H	X	L	L->H	Tri-state
IGNORE CLOCK EDGE (stall)	Current	X	X	X	L	X	X	X	X	H	L->H	-
SLEEP MODE	None	X	X	X	H	X	X	X	X	X	X	Tri-state

Partial Truth Table for Read/Write

The partial truth table for Read/Write for CY7C1353G follows. [3, 4, 10]

Function	\overline{WE}	\overline{BW}_A	\overline{BW}_B
Read	H	X	X
Write – no bytes written	L	H	H
Write byte A – (DQ _A and DQP _A)	L	L	H
Write byte B – (DQ _B and DQP _B)	L	H	L
Write all bytes	L	L	L

Notes

- X = "Don't Care." H = Logic HIGH, L = Logic LOW. \overline{BW}_x = L signifies at least one byte write select is active, \overline{BW}_x = valid signifies that the desired byte write selects are asserted, see truth table for details.
- Write is defined by \overline{BW}_x , and \overline{WE} . See truth table for read/write.
- When a write cycle is detected, all IOs are tri-stated, even during byte writes.
- The DQs and DQP_[A:B] pins are controlled by the current cycle and the \overline{OE} signal. \overline{OE} is asynchronous and is not sampled with the clock.
- \overline{CEN} = H, inserts wait states.
- Device powers up deselected and the IOs in a tri-state condition, regardless of \overline{OE} .
- \overline{OE} is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle DQs and DQP_[A:B] = tri-state when \overline{OE} is inactive or when the device is deselected, and DQs and DQP_[A:B] = data when \overline{OE} is active.
- Table only lists a partial listing of the byte write combinations. Any combination of BW[A:D] is valid. Appropriate write is based on which byte write is active.



Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature -65 °C to +150 °C

Ambient temperature with power applied -55 °C to +125 °C

Supply voltage on V_{DD} relative to GND -0.5 V to +4.6 V

Supply voltage on V_{DDQ} relative to GND -0.5 V to V_{DD}

DC voltage applied to outputs in tri-state -0.5 V to $V_{DDQ} + 0.5$ V

DC input voltage -0.5 V to $V_{DD} + 0.5$ V

Current into outputs (LOW) 20 mA

Static discharge voltage (MIL-STD-883, method 3015) > 2001 V

Latch-up current > 200 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{DD}	V_{DDQ}
Commercial	0 °C to +70 °C	3.3 V - 5% / + 10%	2.5 V - 5% to V_{DD}

Electrical Characteristics

Over the Operating Range

Parameter ^[11, 12]	Description	Test Conditions	Min	Max	Unit
V_{DD}	Power supply voltage		3.135	3.6	V
V_{DDQ}	I/O supply voltage		2.375	V_{DD}	V
V_{OH}	Output HIGH voltage	for 3.3 V I/O, $I_{OH} = -4.0$ mA	2.4	-	V
		for 2.5 V I/O, $I_{OH} = -1.0$ mA	2.0	-	V
V_{OL}	Output LOW voltage	for 3.3 V I/O, $I_{OH} = 8.0$ mA	-	0.4	V
		for 2.5 V I/O, $I_{OH} = 1.0$ mA	-	0.4	V
V_{IH}	Input HIGH voltage	for 3.3 V I/O	2.0	$V_{DD} + 0.3$	V
	Input HIGH voltage	for 2.5 V I/O	1.7	$V_{DD} + 0.3$	V
V_{IL}	Input LOW voltage ^[11]	for 3.3 V I/O	-0.3	0.8	V
	Input LOW voltage ^[11]	for 2.5 V I/O	-0.3	0.7	V
I_X	Input leakage current except ZZ and MODE	$GND \leq V_I \leq V_{DDQ}$	-5	5	μ A
	Input current of MODE	Input = V_{SS}	-30	-	μ A
		Input = V_{DD}	-	5	μ A
	Input current of ZZ	Input = V_{SS}	-5	-	μ A
Input = V_{DD}		-	30	μ A	
I_{OZ}	Output leakage current	$GND \leq V_I \leq V_{DDQ}$, output disabled	-5	5	μ A
I_{DD}	V_{DD} operating supply current	$V_{DD} = \text{Max.}$, $I_{OUT} = 0$ mA, $f = f_{MAX} = 1/t_{CYC}$	-	205	mA
I_{SB1}	Automatic CE power-down current – TTL inputs	$V_{DD} = \text{Max.}$, device deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$, inputs switching	-	80	mA
I_{SB2}	Automatic CE power-down current – CMOS inputs	$V_{DD} = \text{Max.}$, device deselected, $V_{IN} \geq V_{DD} - 0.3$ V or $V_{IN} \leq 0.3$ V, $f = 0$, inputs static	-	40	mA
I_{SB3}	Automatic CE power-down current – CMOS inputs	$V_{DD} = \text{Max.}$, device deselected, $V_{IN} \geq V_{DDQ} - 0.3$ V or $V_{IN} \leq 0.3$ V, $f = f_{MAX}$, inputs switching	-	65	mA
I_{SB4}	Automatic CE power-down current – TTL inputs	$V_{DD} = \text{Max.}$, device deselected, $V_{IN} \geq V_{DD} - 0.3$ V or $V_{IN} \leq 0.3$ V, $f = 0$, inputs static	-	45	mA

Notes

11. Overshoot: $V_{IH(AC)} < V_{DD} + 1.5$ V (Pulse width less than $t_{CYC}/2$), undershoot: $V_{IL(AC)} > -2$ V (Pulse width less than $t_{CYC}/2$).

12. $T_{Power-up}$: Assumes a linear ramp from 0 V to $V_{DD(min)}$ within 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \leq V_{DD}$.

Capacitance

Parameter ^[13]	Description	Test Conditions	100-pin TQFP Max	Unit
C_{IN}	Input capacitance	$T_A = 25\text{ }^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{DD} = 3.3\text{ V}$, $V_{DDQ} = 3.3\text{ V}$	5	pF
C_{CLOCK}	Clock input capacitance		5	pF
C_{IO}	I/O capacitance		5	pF

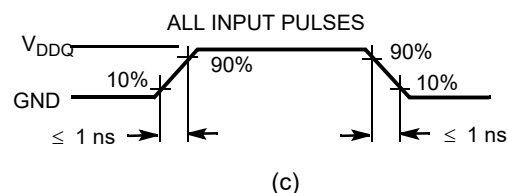
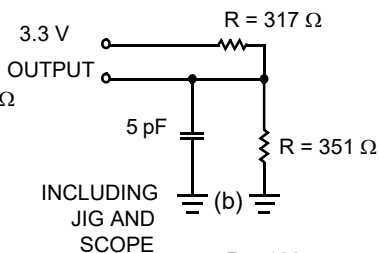
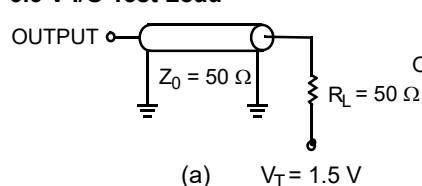
Thermal Resistance

Parameter ^[13]	Description	Test Conditions	100-pin TQFP Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, according to EIA/JESD51.	30.32	$^\circ\text{C/W}$
Θ_{JC}	Thermal resistance (junction to case)		6.85	$^\circ\text{C/W}$

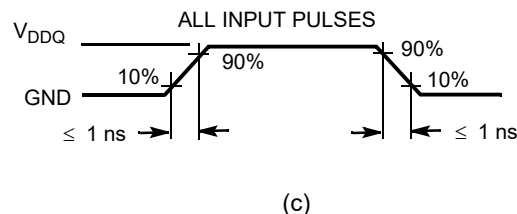
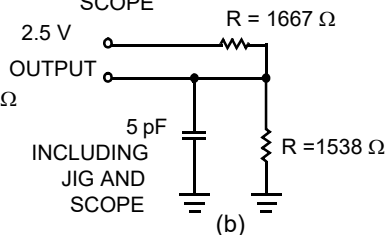
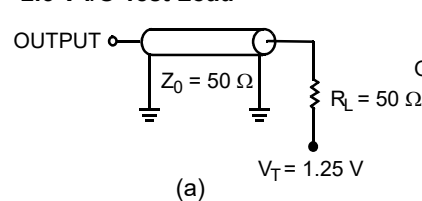
AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms

3.3 V I/O Test Load



2.5 V I/O Test Load



Note

13. Tested initially and after any design or process changes that may affect these parameters.



Switching Characteristics

Over the Operating Range

Parameter ^[14, 15]	Description	-100		Unit
		Min	Max	
t _{POWER}	V _{DD} (typical) to the first access ^[16]	1	–	ms
Clock				
t _{CYC}	Clock cycle time	10	–	ns
t _{CH}	Clock HIGH	4.0	–	ns
t _{CL}	Clock LOW	4.0	–	ns
Output Times				
t _{CDV}	Data output valid after CLK rise	–	8.0	ns
t _{DOH}	Data output hold after CLK rise	2.0	–	ns
t _{CLZ}	Clock to low Z ^[17, 18, 19]	0	–	ns
t _{CHZ}	Clock to high Z ^[17, 18, 19]	–	3.5	ns
t _{OEV}	$\overline{\text{OE}}$ LOW to output valid	–	3.5	ns
t _{OELZ}	$\overline{\text{OE}}$ LOW to output low Z ^[17, 18, 19]	0	–	ns
t _{OEHZ}	$\overline{\text{OE}}$ HIGH to output high Z ^[17, 18, 19]	–	3.5	ns
Setup Times				
t _{AS}	Address setup before CLK rise	2.0	–	ns
t _{ALS}	ADV/LD setup before CLK rise	2.0	–	ns
t _{WES}	$\overline{\text{WE}}$, $\overline{\text{BW}}_X$ setup before CLK rise	2.0	–	ns
t _{CENS}	$\overline{\text{CEN}}$ setup before CLK rise	2.0	–	ns
t _{DS}	Data input setup before CLK rise	2.0	–	ns
t _{CES}	Chip enable setup before CLK rise	2.0	–	ns
Hold Times				
t _{AH}	Address hold after CLK rise	0.5	–	ns
t _{ALH}	ADV/LD hold after CLK rise	0.5	–	ns
t _{WEH}	$\overline{\text{WE}}$, $\overline{\text{BW}}_X$ hold after CLK rise	0.5	–	ns
t _{CENH}	$\overline{\text{CEN}}$ hold after CLK rise	0.5	–	ns
t _{DH}	Data input hold after CLK rise	0.5	–	ns
t _{CEH}	Chip enable hold after CLK rise	0.5	–	ns

Notes

14. Timing reference level is 1.5 V when V_{DDQ} = 3.3 V and is 1.25 V when V_{DDQ} = 2.5 V.

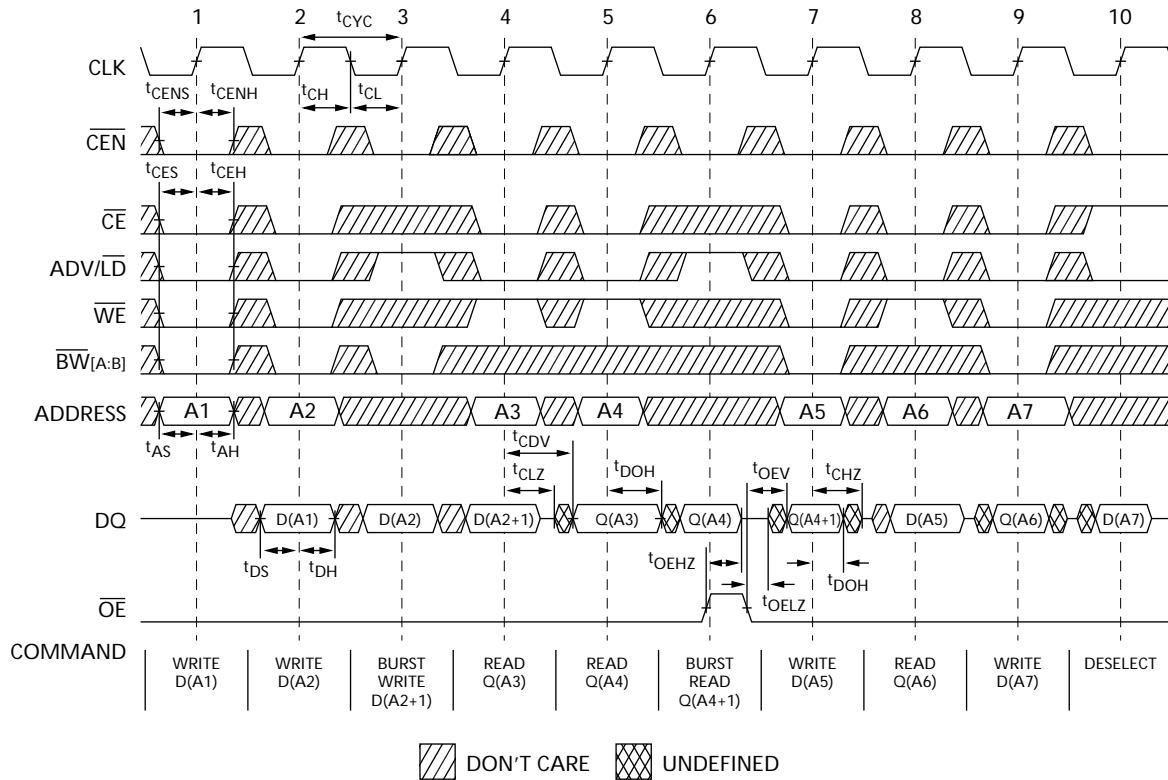
15. Test conditions shown in (a) of [Figure 2 on page 9](#), unless otherwise noted.

16. This part has a voltage regulator internally; t_{POWER} is the time that the power needs to be supplied above V_{DD(minimum)} initially before a read or write operation can be initiated.

17. t_{CHZ}, t_{CLZ}, t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of [Figure 2 on page 9](#). Transition is measured ± 200 mV from steady-state voltage.

18. At any voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve tri-state prior to low Z under the same system conditions.

19. This parameter is sampled and not 100% tested.

Switching Waveforms**Figure 3. Read/Write Waveforms** [20, 21, 22]**Notes**

20. For this waveform ZZ is tied low.

21. When \overline{CE} is LOW, \overline{CE}_1 is LOW, \overline{CE}_2 is HIGH and \overline{CE}_3 is LOW. When \overline{CE} is HIGH, \overline{CE}_1 is HIGH or \overline{CE}_2 is LOW or \overline{CE}_3 is HIGH.

22. Order of the Burst sequence is determined by the status of the MODE (0 = Linear, 1 = Interleaved). Burst operations are optional.

Switching Waveforms (continued)

Figure 4. NOP, STALL and DESELECT Cycles [23, 24, 25]

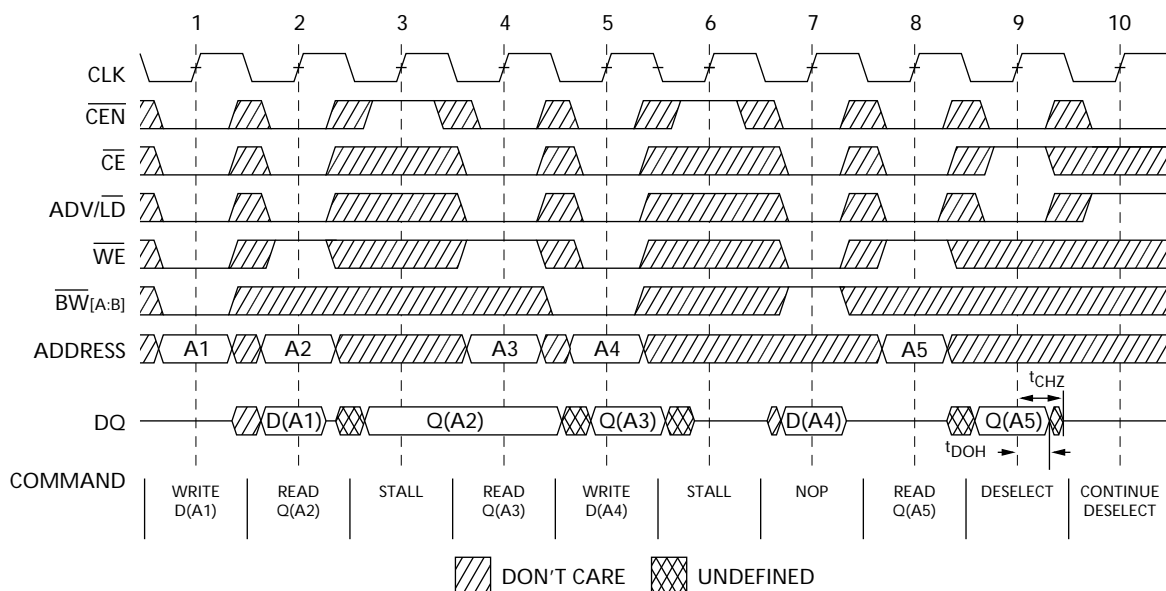
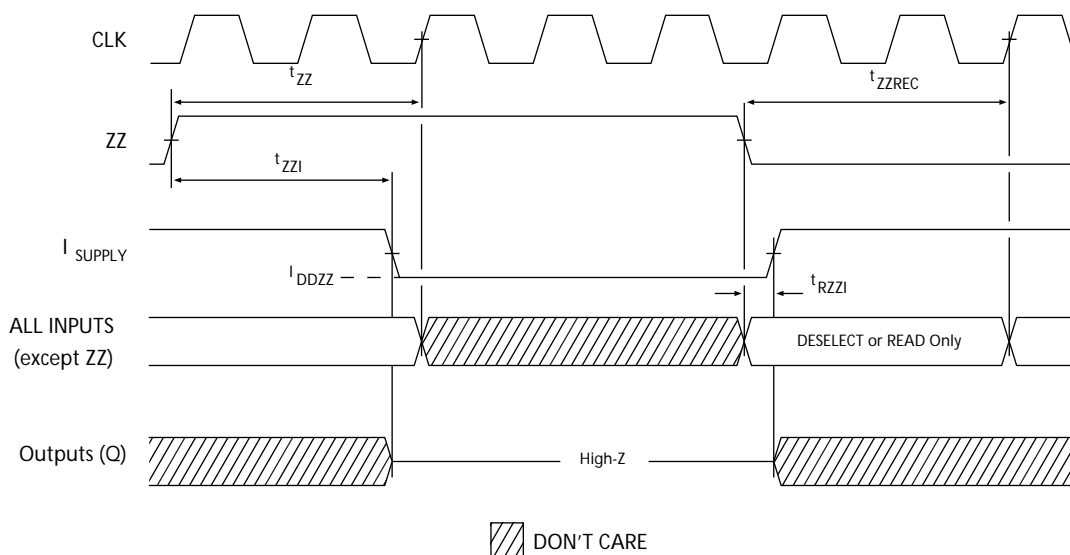


Figure 5. ZZ Mode Timing [26, 27]



Notes

- 23. For this waveform ZZ is tied low.
- 24. When \overline{CE} is LOW, \overline{CE}_1 is LOW, CE_2 is HIGH and \overline{CE}_3 is LOW. When \overline{CE} is HIGH, \overline{CE}_1 is HIGH or CE_2 is LOW or \overline{CE}_3 is HIGH.
- 25. The IGNORE CLOCK EDGE or STALL cycle (Clock 3) illustrates \overline{CEN} being used to create a pause. A write is not performed during this cycle.
- 26. Device must be deselected when entering ZZ mode. See truth table for all possible signal conditions to deselect the device.
- 27. DQs are in high Z when exiting ZZ sleep mode.



Ordering Information

Cypress offers other versions of this type of product in many different configurations and features. The following table contains only the list of parts that are currently available.

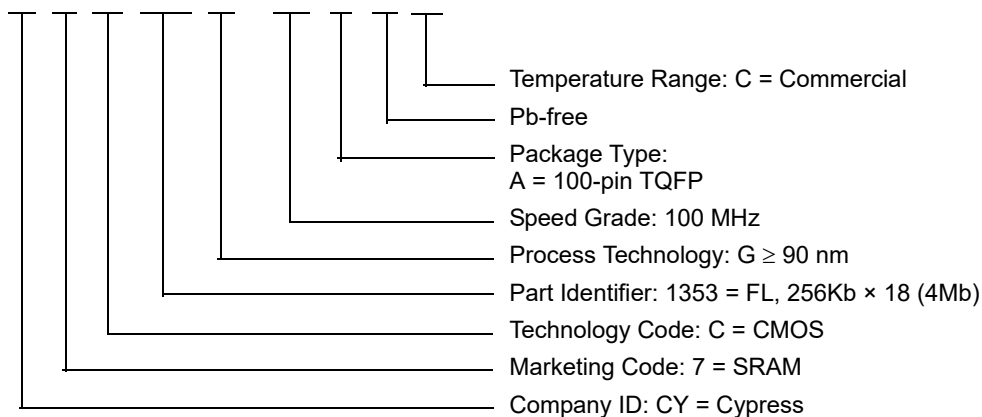
For a complete listing of all options, visit the Cypress website at www.cypress.com and refer to the product summary page at <http://www.cypress.com/products> or contact your local sales representative.

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives and distributors. To find the office closest to you, visit us at <http://www.cypress.com/go/datasheet/offices>.

Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
100	CY7C1353G-100AXC	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Commercial

Ordering Code Definitions

CY 7 C 1353 G - 100 A X C





Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
$\overline{\text{CE}}$	Chip Enable
CEN	Clock Enable
EIA	Electronic Industries Alliance
I/O	Input/Output
JEDEC	Joint Electron Devices Engineering Council
NoBL	No Bus Latency
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TQFP	Thin Quad Flat Pack
TTL	Transistor-Transistor Logic
$\overline{\text{WE}}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
mA	milliampere
ms	millisecond
mV	millivolt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt



Errata

This section describes the Ram9 NoBL ZZ pin issue. Details include trigger conditions, the devices affected, proposed workaround and silicon revision applicability. Please contact your local Cypress sales representative if you have further questions.

Part Numbers Affected

Density & Revision	Package Type	Operating Range
4Mb-Ram9 NoBL™ SRAMs: CY7C135*G	100-pin TQFP	Commercial

Product Status

All of the devices in the Ram9 4Mb NoBL family are qualified and available in production quantities.

Ram9 NoBL ZZ Pin Issues Errata Summary

The following table defines the errata applicable to available Ram9 4Mb NoBL family devices.

Item	Issues	Description	Device	Fix Status
1.	ZZ Pin	When asserted HIGH, the ZZ pin places device in a “sleep” condition with data integrity preserved. The ZZ pin currently does not have an internal pull-down resistor and hence cannot be left floating externally by the user during normal mode of operation.	4M-Ram9 (90 nm)	For the 4M Ram9 (90 nm) devices, there is no plan to fix this issue.

1. ZZ Pin Issue

■ Problem Definition

The problem occurs only when the device is operated in the normal mode with ZZ pin left floating. The ZZ pin on the SRAM device does not have an internal pull-down resistor. Switching noise in the system may cause the SRAM to recognize a HIGH on the ZZ input, which may cause the SRAM to enter sleep mode. This could result in incorrect or undesirable operation of the SRAM.

■ Trigger Conditions

Device operated with ZZ pin left floating.

■ Scope of Impact

When the ZZ pin is left floating, the device delivers incorrect data.

■ Workaround

Tie the ZZ pin externally to ground.

■ Fix Status

For the 4M Ram9 (90 nm) devices, there is no plan to fix this issue.

Document History Page

Document Title: CY7C1353G, 4-Mbit (256K × 18) Flow-Through SRAM with NoBL™ Architecture				
Document Number: 38-05515				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	224363	RKF	05/17/2004	New data sheet.
*A	288431	VBL	11/10/2004	Updated Features (Removed 66 MHz frequency related information). Updated Selection Guide (Removed 66 MHz frequency related information). Updated Electrical Characteristics (Removed 66 MHz frequency related information). Updated Switching Characteristics (Removed 66 MHz frequency related information). Updated Ordering Information (Updated part numbers (Removed 66 MHz frequency related information; changed TQFP package in Ordering Information section to Pb-free TQFP)).
*B	333626	SYT	03/15/2005	Updated Features (Removed 117 MHz frequency related information). Updated Selection Guide (Removed 117 MHz frequency related information). Updated Pin Configuration (Modified Address Expansion balls in the pinouts for 100-pin TQFP Packages according to JEDEC standards). Updated Pin Definitions . Updated Functional Overview (Updated ZZ Mode Electrical Characteristics (Replaced “Snooze” with “Sleep”)). Updated Truth Table (Replaced “Snooze” with “Sleep”). Updated Electrical Characteristics (Updated Test Conditions of V_{OL} , V_{OH} parameters; removed 117 MHz frequency related information). Updated Thermal Resistance (Replaced values of θ_{JA} and θ_{JC} parameters from TBD to their respective values). Updated Switching Characteristics (Removed 117 MHz frequency related information). Updated Ordering Information (Updated part numbers (By shading and unshading MPNs according to availability)).
*C	418633	R XU	01/06/2006	Changed status from Preliminary to Final. Changed address of Cypress Semiconductor Corporation from “3901 North First Street” to “198 Champion Court”. Updated Electrical Characteristics (Updated Note 12 (Modified test condition from $V_{DDQ} < V_{DD}$ to $V_{DDQ} \leq V_{DD}$); changed “Input Load Current except ZZ and MODE” to “Input Leakage Current except ZZ and MODE”). Updated Ordering Information (Updated part numbers; removed Package Name column; added Package Diagram column). Updated Package Diagram (spec 51-85050 (changed revision from *A to *B)).
*D	480124	VKN	07/14/2006	Updated Maximum Ratings (Added the Maximum Rating for Supply Voltage on V_{DDQ} Relative to GND). Updated Ordering Information (Updated part numbers).
*E	1274724	VKN / AESA	07/17/2007	Updated Ordering Information (Updated part numbers (Corrected typo only)).
*F	2896584	NJY	03/20/2010	Updated Ordering Information (Updated part numbers). Updated Package Diagram : spec 51-85050 – Changed revision from *B to *C.
*G	3033272	NJY	09/19/2010	Updated Ordering Information : No change in part numbers. Added Ordering Code Definitions . Added Acronyms and Units of Measure Minor edits. Updated to new template. Completing Sunset Review.



Document History Page *(continued)*

Document Title: CY7C1353G, 4-Mbit (256K × 18) Flow-Through SRAM with NoBL™ Architecture Document Number: 38-05515				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*H	3357006	PRIT	08/29/2011	Updated Package Diagram : spec 51-85050 – Changed revision from *C to *D. Updated to new template. Completing Sunset Review.
*I	3619154	PRIT	05/16/2012	Updated Features (Removed 133 MHz frequency related information). Updated Functional Description (Removed the Note “For best-practices recommendations, please refer to the Cypress application note <i>System Design Guidelines</i> on www.cypress.com .” and its reference; removed 133 MHz frequency related information). Updated Selection Guide (Removed 133 MHz frequency related information). Updated Operating Range (Removed Industrial Temperature Range). Updated Electrical Characteristics (Removed 133 MHz frequency related information). Updated Switching Characteristics (Removed 133 MHz frequency related information). Replaced all instances of IO with I/O across the document.
*J	3754982	PRIT	09/25/2012	No technical updates. Completing Sunset Review.
*K	3980362	PRIT	04/24/2013	Added Errata .
*L	4038283	PRIT	06/24/2013	Added Errata Footnotes. Updated to new template.
*M	4149033	PRIT	10/07/2013	Updated Errata .
*N	4539104	PRIT	10/15/2014	Updated Package Diagram : spec 51-85050 – Changed revision from *D to *E. Completing Sunset Review.
*O	4572829	PRIT	11/18/2014	Updated Functional Description : Added “For a complete list of related documentation, click here .” at the end.
*P	5512557	PRIT	11/07/2016	Updated Package Diagram : spec 51-85050 – Changed revision from *E to *F. Updated to new template. Completing Sunset Review.
*Q	6041206	RMES	01/22/2018	Updated Package Diagram : spec 51-85050 – Changed revision from *F to *G. Updated to new template. Completing Sunset Review.
*R	6520144	RMES	03/25/2019	Updated to new template.



Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Arm® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6 MCU](#)

Cypress Developer Community

[Community](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2004–2019. This document is the property of Cypress Semiconductor Corporation and its subsidiaries ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress shall have no liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. CYPRESS DOES NOT REPRESENT, WARRANT, OR GUARANTEE THAT CYPRESS PRODUCTS, OR SYSTEMS CREATED USING CYPRESS PRODUCTS, WILL BE FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (collectively, "Security Breach"). Cypress disclaims any liability relating to any Security Breach, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any Security Breach. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. "High-Risk Device" means any device or system whose failure could cause personal injury, death, or property damage. Examples of High-Risk Devices are weapons, nuclear installations, surgical implants, and other medical devices. "Critical Component" means any component of a High-Risk Device whose failure to perform can be reasonably expected to cause, directly or indirectly, the failure of the High-Risk Device, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any use of a Cypress product as a Critical Component in a High-Risk Device. You shall indemnify and hold Cypress, its directors, officers, employees, agents, affiliates, distributors, and assigns harmless from and against all claims, costs, damages, and expenses, arising out of any claim, including claims for product liability, personal injury or death, or property damage arising from any use of a Cypress product as a Critical Component in a High-Risk Device. Cypress products are not intended or authorized for use as a Critical Component in any High-Risk Device except to the limited extent that (i) Cypress's published data sheet for the product explicitly states Cypress has qualified the product for use in a specific High-Risk Device, or (ii) Cypress has given you advance written authorization to use the product as a Critical Component in the specific High-Risk Device and you have signed a separate indemnification agreement.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.

OUR CERTIFICATE

DiGi provide top-quality products and perfect service for customer worldwide through standardization, technological innovation and continuous improvement. DiGi through third-party certification, we stricly control the quality of products and services. Welcome your RFQ to

Email: Info@DiGi-Electronics.com



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.