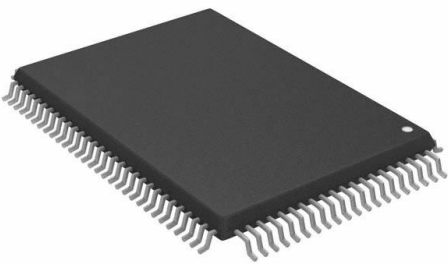


CY7C1370KVE33-167AXM Datasheet

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DiGi Electronics Part Number	CY7C1370KVE33-167AXM-DG
Manufacturer	Infineon Technologies
Manufacturer Product Number	CY7C1370KVE33-167AXM
Description	IC SRAM 18MBIT PAR 100TQFP
Detailed Description	SRAM - Synchronous, SDR Memory IC 18Mbit Parallel 167 MHz 3.4 ns 100-TQFP (14x20)

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Manufacturer Product Number:

CY7C1370KVE33-167AXM

Series:

NoBL™

DiGi-Electronics Programmable:

Not Verified

Memory Format:

SRAM

Memory Size:

18Mbit

Memory Interface:

Parallel

Write Cycle Time - Word, Page:

-

Voltage - Supply:

3.135V ~ 3.6V

Mounting Type:

Surface Mount

Supplier Device Package:

100-TQFP (14x20)

Manufacturer:

Infineon Technologies

Product Status:

Active

Memory Type:

Volatile

Technology:

SRAM - Synchronous, SDR

Memory Organization:

512K x 36

Clock Frequency:

167 MHz

Access Time:

3.4 ns

Operating Temperature:

-55°C ~ 125°C (TC)

Package / Case:

100-LQFP

Base Product Number:

CY7C1370

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.32.0041

Moisture Sensitivity Level (MSL):

3 (168 Hours)

ECCN:

3A001A2C



CY7C1370KVE33

Military Temperature, 18-Mbit (512K × 36) Pipelined SRAM with NoBL™ Architecture (With ECC)

Features

- Pin-compatible and functionally equivalent to ZBT™
- Supports 167-MHz bus operations with zero wait states
- Internally self-timed output buffer control to eliminate the need to use asynchronous OE
- Fully registered (inputs and outputs) for pipelined operation
- Byte write capability
- 3.3 V core power supply (V_{DD})
- 3.3 V/2.5 V I/O power supply (V_{DDQ})
- Fast clock-to-output times
 - 3.4 ns (for 167 MHz device)
- Clock enable (\overline{CEN}) pin to suspend operation
- Synchronous self-timed writes
- Available in JEDEC-standard Pb-free 100-pin TQFP
- Burst capability – linear or interleaved burst order
- “ZZ” sleep mode option and stop clock option
- On chip Error Correction Code (ECC) to reduce Soft Error Rate (SER)
- Available in Military Temperature Range

Functional Description

The CY7C1370KVE33 is a 3.3 V, 512K × 36 synchronous pipelined burst SRAMs with No Bus Latency™ (NoBL™) logic, respectively. They are designed to support unlimited true back-to-back read/write operations with no wait states. The CY7C1370KVE33 is equipped with the advanced (NoBL) logic required to enable consecutive read/write operations with data being transferred on every clock cycle. This feature dramatically improves the throughput of data in systems that require frequent write/read transitions. The CY7C1370KVE33 is pin compatible and functionally equivalent to ZBT devices.

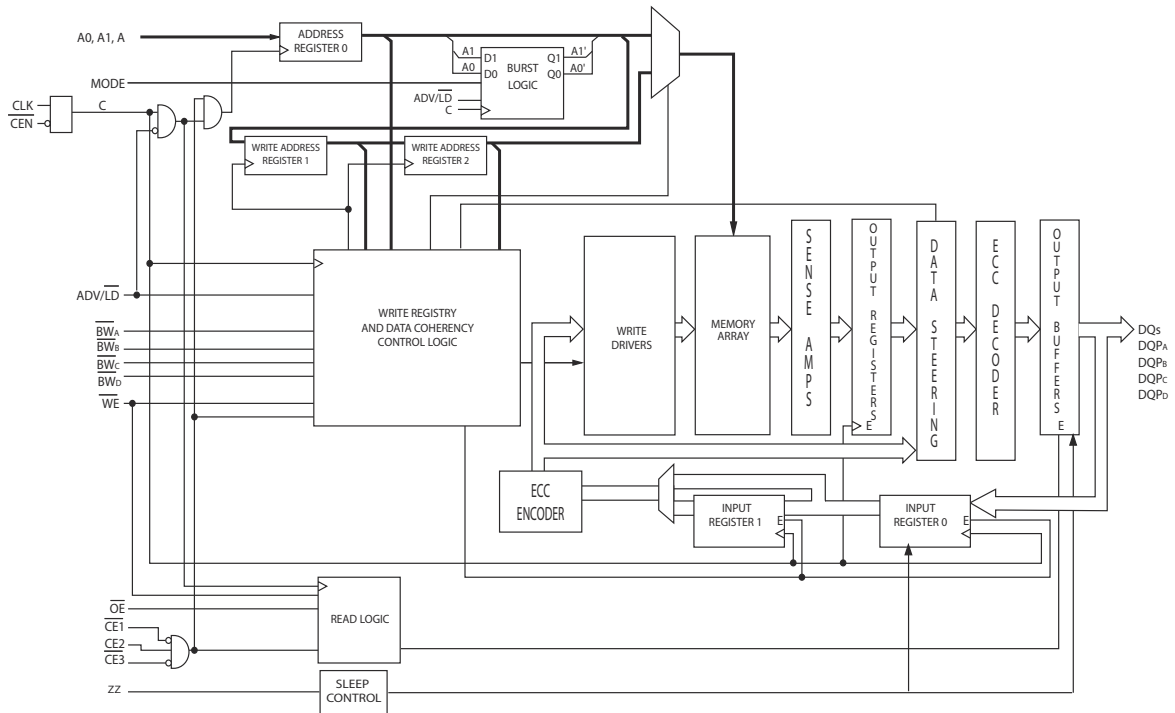
All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. The clock input is qualified by the clock enable (\overline{CEN}) signal, which when deasserted suspends operation and extends the previous clock cycle.

Write operations are controlled by the byte write selects (\overline{BW}_a – \overline{BW}_d for CY7C1370KVE33) and a write enable (\overline{WE}) input. All writes are conducted with on-chip synchronous self-timed write circuitry.

Three synchronous chip enables (\overline{CE}_1 , \overline{CE}_2 , \overline{CE}_3) and an asynchronous output enable (\overline{OE}) provide for easy bank selection and output tri-state control. In order to avoid bus contention, the output drivers are synchronously tristated during the data portion of a write sequence.

Selection Guide

Description		167 MHz	Unit
Maximum access time		3.4	ns
Maximum operating current		190	mA

Logic Block Diagram – CY7C1370KVE33



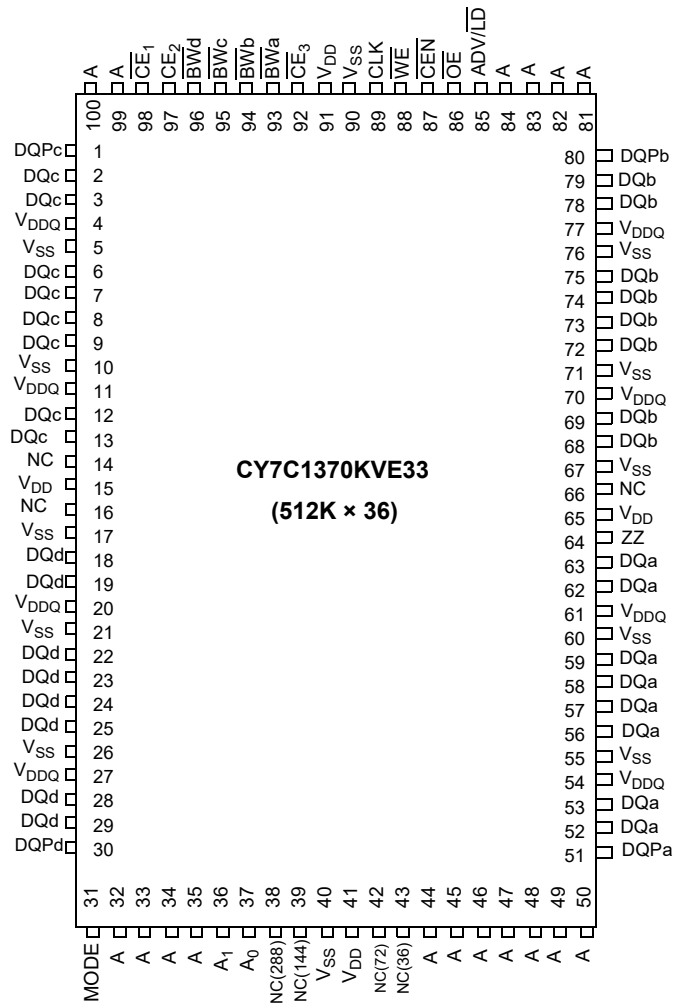
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Pin Configurations

Figure 1. 100-pin TQFP (14 × 20 × 1.4 mm) pinout





Pin Definitions

Pin Name	I/O Type	Pin Description
A ₀ , A ₁ , A	Input-synchronous	Address inputs used to select one of the address locations. Sampled at the rising edge of the CLK.
\overline{BW}_a , \overline{BW}_b , \overline{BW}_c , \overline{BW}_d	Input-synchronous	Byte write select inputs, active LOW. Qualified with \overline{WE} to conduct writes to the SRAM. Sampled on the rising edge of CLK. \overline{BW}_a controls DQ _a and DQP _a , \overline{BW}_b controls DQ _b and DQP _b , \overline{BW}_c controls DQ _c and DQP _c , \overline{BW}_d controls DQ _d and DQP _d .
\overline{WE}	Input-synchronous	Write enable input, active LOW. Sampled on the rising edge of CLK if \overline{CEN} is active LOW. This signal must be asserted LOW to initiate a write sequence.
ADV/LD	Input-synchronous	Advance/load input used to advance the on-chip address counter or load a new address. When HIGH (and \overline{CEN} is asserted LOW) the internal burst counter is advanced. When LOW, a new address can be loaded into the device for an access. After being deselected, ADV/LD should be driven LOW in order to load a new address.
CLK	Input-clock	Clock input. Used to capture all synchronous inputs to the device. CLK is qualified with \overline{CEN} . CLK is only recognized if \overline{CEN} is active LOW.
\overline{CE}_1	Input-synchronous	Chip enable 1 input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with \overline{CE}_2 and \overline{CE}_3 to select/deselect the device.
\overline{CE}_2	Input-synchronous	Chip enable 2 input, active HIGH. Sampled on the rising edge of CLK. Used in conjunction with \overline{CE}_1 and \overline{CE}_3 to select/deselect the device.
\overline{CE}_3	Input-synchronous	Chip enable 3 input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with \overline{CE}_1 and \overline{CE}_2 to select/deselect the device.
\overline{OE}	Input-asynchronous	Output enable, active LOW. Combined with the synchronous logic block inside the device to control the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pins. \overline{OE} is masked during the data portion of a write sequence, during the first clock when emerging from a deselected state and when the device has been deselected.
\overline{CEN}	Input-synchronous	Clock enable input, active LOW. When asserted LOW the clock signal is recognized by the SRAM. When deasserted HIGH the clock signal is masked. Since deasserting \overline{CEN} does not deselect the device, \overline{CEN} can be used to extend the previous cycle when required.
DQ _s	I/O-synchronous	Bidirectional data I/O lines. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by A _[17:0] during the previous clock rise of the read cycle. The direction of the pins is controlled by \overline{OE} and the internal control logic. When \overline{OE} is asserted LOW, the pins can behave as outputs. When HIGH, DQ _a –DQ _d are placed in a tristate condition. The outputs are automatically tristated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of \overline{OE} .
DQP _x	I/O-synchronous	Bidirectional data parity I/O lines. Functionally, these signals are identical to DQ _s . During write sequences, DQP _a is controlled by \overline{BW}_a , DQP _b is controlled by \overline{BW}_b , DQP _c is controlled by \overline{BW}_c , and DQP _d is controlled by \overline{BW}_d .
MODE	Input strap pin	Mode input. Selects the burst order of the device. Tied HIGH selects the interleaved burst order. Pulled LOW selects the linear burst order. MODE should not change states during operation. When left floating MODE will default HIGH, to an interleaved burst order.
V _{DD}	Power supply	Power supply inputs to the core of the device.
V _{DDQ}	I/O power supply	Power supply for the I/O circuitry.
V _{SS}	Ground	Ground for the device. Should be connected to ground of the system.
NC	–	No connects. This pin is not connected to the die.



Pin Definitions (continued)

Pin Name	I/O Type	Pin Description
NC/(36M, 72M, 144M, 288M, 576M, 1G)	–	These pins are not connected. They will be used for expansion to the 36M, 72M, 144M, 288M, 576M and 1G densities.
ZZ	Input-asynchronous	ZZ “sleep” input. This active HIGH input places the device in a non-time critical “sleep” condition with data integrity preserved. During normal operation, this pin can be connected to V_{SS} or left floating. ZZ pin has an internal pull down.

Functional Overview

The CY7C1370KVE33 is synchronous-pipelined burst NoBL SRAMs designed specifically to eliminate wait states during write/read transitions. All synchronous inputs pass through input registers controlled by the rising edge of the clock. The clock signal is qualified with the clock enable input signal (\overline{CEN}). If \overline{CEN} is HIGH, the clock signal is not recognized and all internal states are maintained. All synchronous operations are qualified with \overline{CEN} . All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CO}) is 3.4 ns (167-MHz device).

Accesses can be initiated by asserting all three chip enables (CE_1 , CE_2 , CE_3) active at the rising edge of the clock. If clock enable (\overline{CEN}) is active LOW and $\overline{ADV/LD}$ is asserted LOW, the address presented to the device will be latched. The access can either be a read or write operation, depending on the status of the write enable (\overline{WE}). \overline{BW}_X can be used to conduct byte write operations.

Write operations are qualified by the write enable (\overline{WE}). All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous chip enables (\overline{CE}_1 , CE_2 , \overline{CE}_3) and an asynchronous output enable (\overline{OE}) simplify depth expansion. All operations (reads, writes, and deselected) are pipelined. $\overline{ADV/LD}$ should be driven LOW once the device has been deselected in order to load a new address for the next operation.

Single Read Accesses

A read access is initiated when the following conditions are satisfied at clock rise: (1) \overline{CEN} is asserted LOW, (2) \overline{CE}_1 , CE_2 , and CE_3 are all asserted active, (3) the write enable input signal \overline{WE} is deasserted HIGH, and (4) $\overline{ADV/LD}$ is asserted LOW. The address presented to the address inputs is latched into the address register and presented to the memory core and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the input of the output register. At the rising edge of the next clock the requested data is allowed to propagate through the output register and onto the data bus within 3.4 ns (167-MHz device) provided \overline{OE} is active LOW. After the first clock of the read access the output buffers are controlled by \overline{OE} and the internal control logic. \overline{OE} must be driven LOW in order for the device to drive out the requested data. During the second clock, a subsequent operation (read/write/deselect) can be initiated. Deselecting the device is also pipelined. Therefore, when the SRAM is deselected at clock rise by one of the chip enable signals, its output will tristate following the next clock rise.

Burst Read Accesses

The CY7C1370KVE33 have an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four reads without reasserting the address inputs. $\overline{ADV/LD}$ must be driven LOW in order to load a new address into the SRAM, as described in the [Single Read Accesses](#). The sequence of the burst counter is determined by the MODE input signal. A LOW input on MODE selects a linear burst mode, a HIGH selects an interleaved burst sequence. Both burst counters use A0 and A1 in the burst sequence, and will wrap-around when incremented sufficiently. A HIGH input on $\overline{ADV/LD}$ will increment the internal burst counter regardless of the state of chip enables inputs or \overline{WE} . \overline{WE} is latched at the beginning of a burst cycle. Therefore, the type of access (read or write) is maintained throughout the burst sequence.

Single Write Accesses

Write access are initiated when the following conditions are satisfied at clock rise: (1) \overline{CEN} is asserted LOW, (2) \overline{CE}_1 , CE_2 , and CE_3 are all asserted active, and (3) the write signal \overline{WE} is asserted LOW. The address presented is loaded into the address register. The write signals are latched into the control logic block.

On the subsequent clock rise the data lines are automatically tristated regardless of the state of the \overline{OE} input signal. This allows the external logic to present the data on DQ and DQP ($DQ_{a,b,c,d}$ / $DQP_{a,b,c,d}$ for CY7C1370KVE33). In addition, the address for the subsequent access (read/write/deselect) is latched into the address register (provided the appropriate control signals are asserted).

On the next clock rise the data presented to DQ and DQP ($DQ_{a,b,c,d}$ / $DQP_{a,b,c,d}$ for CY7C1370KVE33) (or a subset for byte write operations, see Write Cycle Description table for details) inputs is latched into the device and the write is complete.

The data written during the write operation is controlled by \overline{BW} ($\overline{BW}_{a,b,c,d}$ for CY7C1370KVE33) signals.

The CY7C1370KVE33 provides byte write capability that is described in the [Write Cycle Description](#) table. Asserting the write enable input (\overline{WE}) with the selected byte write select (\overline{BW}) input will selectively write to only the desired bytes. Bytes not selected during a byte write operation will remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations. Byte write capability has been included in order to greatly simplify read/modify/write sequences, which can be reduced to simple byte write operations.



Because the CY7C1370KVE33 is common I/O devices, data should not be driven into the device while the outputs are active. The output enable (OE) can be deasserted HIGH before presenting data to the DQ and DQP ($DQ_{a,b,c,d}/DQP_{a,b,c,d}$ for CY7C1370KVE33) inputs. Doing so will tri-state the output drivers. As a safety precaution, DQ and DQP ($DQ_{a,b,c,d}/DQP_{a,b,c,d}$ for CY7C1370KVE33) are automatically tristated during the data portion of a write cycle, regardless of the state of OE.

Burst Write Accesses

The CY7C1370KVE33 has an on-chip burst counter that allows the user the ability to supply a single address and conduct up to four write operations without reasserting the address inputs. $\overline{ADV/LD}$ must be driven LOW in order to load the initial address, as described in the [Single Write Accesses](#) section above. When $\overline{ADV/LD}$ is driven HIGH on the subsequent clock rise, the chip enables (\overline{CE}_1 , \overline{CE}_2 , and \overline{CE}_3) and \overline{WE} inputs are ignored and the burst counter is incremented. The correct BW ($BW_{a,b,c,d}$ for CY7C1370KVE33) inputs must be driven in each cycle of the burst write in order to write the correct bytes of data.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. \overline{CE}_1 , \overline{CE}_2 , and \overline{CE}_3 , must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	$ZZ \geq V_{DD} - 0.2 V$	–	90	mA
t_{ZZS}	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2 V$	–	$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	$ZZ \leq 0.2 V$	$2t_{CYC}$	–	ns
t_{ZZI}	ZZ active to sleep current	This parameter is sampled	–	$2t_{CYC}$	ns
t_{RZZI}	ZZ Inactive to exit sleep current	This parameter is sampled	0	–	ns

Interleaved Burst Address Table

(MODE = Floating or V_{DD})

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table

(MODE = GND)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10



Truth Table

The Truth Table for CY7C1370KVE33 follows. [1, 2, 3, 4, 5, 6, 7]

Operation	Address Used	$\overline{\text{CE}}$	ZZ	$\overline{\text{ADV/LD}}$	$\overline{\text{WE}}$	$\overline{\text{BW}}_x$	$\overline{\text{OE}}$	$\overline{\text{CEN}}$	CLK	DQ
Deselect cycle	None	H	L	L	X	X	X	L	L-H	Tri-state
Continue deselect cycle	None	X	L	H	X	X	X	L	L-H	Tri-state
Read cycle (begin burst)	External	L	L	L	H	X	L	L	L-H	Data out (Q)
Read cycle (continue burst)	Next	X	L	H	X	X	L	L	L-H	Data out (Q)
NOP/dummy read (begin burst)	External	L	L	L	H	X	H	L	L-H	Tri-state
Dummy read (continue burst)	Next	X	L	H	X	X	H	L	L-H	Tri-state
Write cycle (begin burst)	External	L	L	L	L	L	X	L	L-H	Data in (D)
Write cycle (continue burst)	Next	X	L	H	X	L	X	L	L-H	Data in (D)
NOP/write abort (begin burst)	None	L	L	L	L	H	X	L	L-H	Tri-state
Write abort (continue burst)	Next	X	L	H	X	H	X	L	L-H	Tri-state
Ignore clock edge (stall)	Current	X	L	X	X	X	X	H	L-H	-
Sleep mode	None	X	H	X	X	X	X	X	X	Tri-state

Notes

1. X = "Don't Care", H = Logic HIGH, L = Logic LOW, $\overline{\text{CE}}$ stands for ALL Chip Enables active. $\overline{\text{BW}}_x = \text{L}$ signifies at least one Byte Write Select is active, $\overline{\text{BW}}_x = \text{Valid}$ signifies that the desired byte write selects are asserted, see Write Cycle Description table for details.
2. Write is defined by $\overline{\text{WE}}$ and $\overline{\text{BW}}_x$. See Write Cycle Description table for details.
3. When a write cycle is detected, all I/Os are tristated, even during byte writes.
4. The DQ and DQP pins are controlled by the current cycle and the $\overline{\text{OE}}$ signal.
5. $\overline{\text{CEN}} = \text{H}$ inserts wait states.
6. Device will power-up deselected and the I/Os in a tristate condition, regardless of $\overline{\text{OE}}$.
7. $\overline{\text{OE}}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle DQ_s and $\text{DQP}_x = \text{Tri-state}$ when $\overline{\text{OE}}$ is inactive or when the device is deselected, and $\text{DQ}_s = \text{data}$ when OE is active.



Partial Write Cycle Description

The Partial Write Cycle Description for CY7C1370KVE33 follows. [8, 9, 10, 11]

Function (CY7C1370KVE33)	\overline{WE}	\overline{BW}_d	\overline{BW}_c	\overline{BW}_b	\overline{BW}_a
Read	H	X	X	X	X
Write – No bytes written	L	H	H	H	H
Write Byte a – (DQ _a and DQP _a)	L	H	H	H	L
Write Byte b – (DQ _b and DQP _b)	L	H	H	L	H
Write Bytes b, a	L	H	H	L	L
Write Byte c – (DQ _c and DQP _c)	L	H	L	H	H
Write Bytes c, a	L	H	L	H	L
Write Bytes c, b	L	H	L	L	H
Write Bytes c, b, a	L	H	L	L	L
Write Byte d – (DQ _d and DQP _d)	L	L	H	H	H
Write Bytes d, a	L	L	H	H	L
Write Bytes d, b	L	L	H	L	H
Write Bytes d, b, a	L	L	H	L	L
Write Bytes d, c	L	L	L	H	H
Write Bytes d, c, a	L	L	L	H	L
Write Bytes d, c, b	L	L	L	L	H
Write All Bytes	L	L	L	L	L

Notes

8. X = "Don't Care", H = Logic HIGH, L = Logic LOW, \overline{CE} stands for ALL Chip Enables active. $\overline{BW}_x = L$ signifies at least one Byte Write Select is active, $\overline{BW}_x = \text{Valid}$ signifies that the desired byte write selects are asserted, see [Truth Table on page 8](#) for details.
9. Write is defined by \overline{WE} and \overline{BW}_x . See Write Cycle Description table for details.
10. When a write cycle is detected, all I/Os are tristated, even during byte writes.
11. Table only lists a partial listing of the byte write combinations. Any Combination of \overline{BW}_x is valid Appropriate write will be done based on which byte write is active.



Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature -65 °C to +150 °C

Case Temperature
with Power Applied -55 °C to +125 °C

Supply Voltage on V_{DD} Relative to GND -0.5 V to +4.6 V

Supply Voltage on V_{DDQ} Relative to GND -0.5 V to + V_{DD}

DC to Outputs in Tristate -0.5 V to $V_{DDQ} + 0.5$ V

DC Input Voltage -0.5 V to $V_{DD} + 0.5$ V

Current into Outputs (LOW) 20 mA

Static Discharge Voltage
(per MIL-STD-883, Method 3015) > 2001V

Latch-up Current > 200 mA

Operating Range

Range	Case Temperature	V_{DD}	V_{DDQ}
Military	-55 °C to +125 °C	3.3 V - 5% / +10%	2.5 V - 5% to V_{DD}

Neutron Soft Error Immunity

Parameter	Description	Test Conditions	Typ	Max*	Unit
LSBU (Device with ECC)	Logical Single-Bit Upsets	25 °C	0	0.01	FIT/Mb
LMBU	Logical Multi-Bit Upsets	25 °C	0	0.01	FIT/Mb
SEL	Single Event Latch up	85 °C	0	0.1	FIT/Dev

* No LMBU or SEL events occurred during testing; this column represents a statistical χ^2 , 95% confidence limit calculation. For more details refer to Application Note AN54908 "Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates".

Electrical Characteristics

Over the Operating Range

Parameter ^[12, 13]	Description	Test Conditions	Min	Max	Unit
V_{DD}	Power Supply Voltage		3.135	3.6	V
V_{DDQ}	I/O Supply Voltage	for 3.3 V I/O	3.135	V_{DD}	V
		for 2.5 V I/O	2.375	2.625	V
V_{OH}	Output HIGH Voltage	for 3.3 V I/O, $I_{OH} = -4.0$ mA	2.4	-	V
		for 2.5 V I/O, $I_{OH} = -1.0$ mA	2.0	-	V
V_{OL}	Output LOW Voltage	for 3.3 V I/O, $I_{OL} = 8.0$ mA	-	0.4	V
		for 2.5 V I/O, $I_{OL} = 1.0$ mA	-	0.4	V
V_{IH}	Input HIGH Voltage ^[12]	for 3.3 V I/O	2.0	$V_{DD} + 0.3$ V	V
		for 2.5 V I/O	1.7	$V_{DD} + 0.3$ V	V
V_{IL}	Input LOW Voltage ^[12]	for 3.3 V I/O	-0.3	0.8	V
		for 2.5 V I/O	-0.3	0.7	V
I_X	Input Leakage Current except ZZ and MODE	$GND \leq V_I \leq V_{DDQ}$	-5	5	μ A
		Input Current of MODE	Input = V_{SS}	-30	
	Input Current of ZZ	Input = V_{SS}	-5	-	
		Input = V_{DD}	-	30	

Notes

- Overshoot: $V_{IH(AC)} < V_{DD} + 1.5$ V (Pulse width less than $t_{CYC}/2$), undershoot: $V_{IL(AC)} > -2$ V (Pulse width less than $t_{CYC}/2$).
- $T_{Power-up}$: Assumes a linear ramp from 0 V to $V_{DD(min)}$ of at least 200 ms. During this time $V_{IH} < V_{DD}$ and $V_{DDQ} \leq V_{DD}$.



Electrical Characteristics (continued)

Over the Operating Range

Parameter ^[12, 13]	Description	Test Conditions	Min	Max	Unit
I_{OZ}	Output Leakage Current	$GND \leq V_I \leq V_{DDQ}$, Output Disabled	-5	5	μA
I_{DD}	V_{DD} Operating Supply	$V_{DD} = \text{Max.}$, $I_{OUT} = 0 \text{ mA}$, $f = f_{MAX} = 1/t_{CYC}$	–	190	mA
I_{SB1}	Automatic CE Power-down Current – TTL Inputs	Max. V_{DD} , Device Deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX} = 1/t_{CYC}$	–	105	mA
I_{SB2}	Automatic CE Power-down Current – CMOS Inputs	Max. V_{DD} , Device Deselected, $V_{IN} \leq 0.3 \text{ V}$ or $V_{IN} \geq V_{DDQ} - 0.3 \text{ V}$, $f = 0$	–	90	mA
I_{SB3}	Automatic CE Power-down Current – CMOS Inputs	Max. V_{DD} , Device Deselected, $V_{IN} \leq 0.3 \text{ V}$ or $V_{IN} \geq V_{DDQ} - 0.3 \text{ V}$, $f = f_{MAX} = 1/t_{CYC}$	–	105	mA
I_{SB4}	Automatic CE Power-down Current – TTL Inputs	Max. V_{DD} , Device Deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = 0$	–	90	mA



Capacitance

Parameter	Description	Test Conditions	100-pin TQFP Max	Unit
C_{IN}	Input capacitance	$T_A = 25\text{ }^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{DD} = 3.3\text{ V}$, $V_{DDQ} = 2.5\text{ V}$	5	pF
C_{CLK}	Clock input capacitance		5	pF
$C_{I/O}$	Input/Output capacitance		5	pF

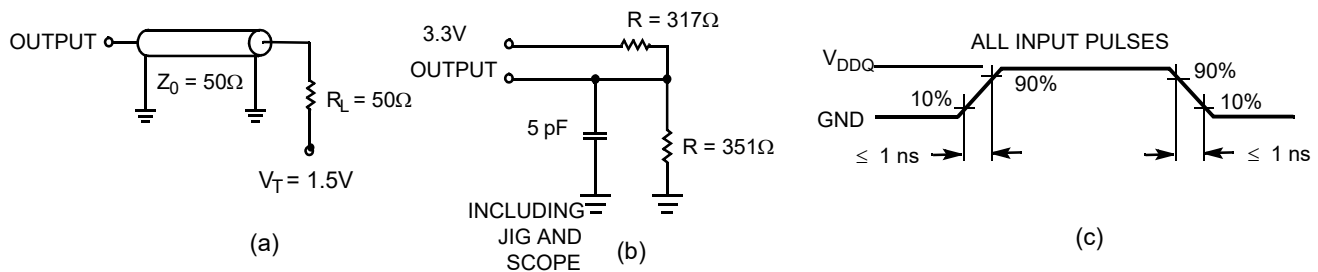
Thermal Resistance

Parameter	Description	Test Conditions	100-pin TQFP Package	Unit
Θ_{JC}	Thermal resistance (junction to case)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	8.36	$^\circ\text{C/W}$

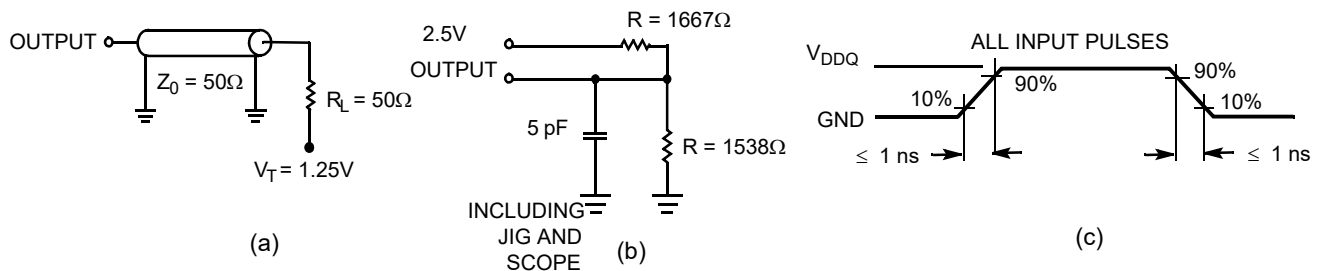
AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms

3.3V I/O Test Load



2.5V I/O Test Load





Switching Characteristics

Over the Operating Range

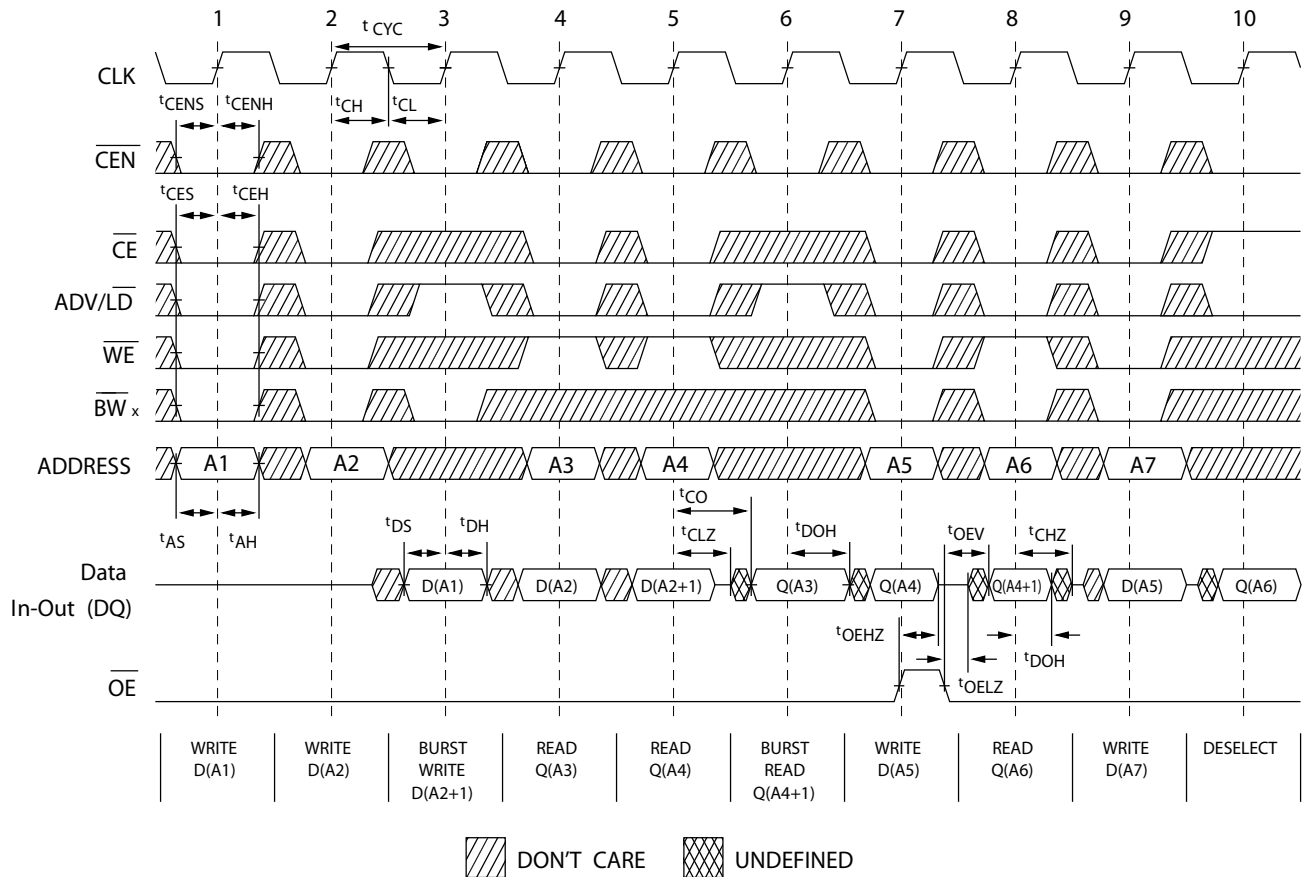
Parameter ^[14, 15]	Description	-167		Unit
		Min	Max	
$t_{Power}^{[16]}$	$V_{CC}(\text{typical})$ to the first access read or write	1	–	ms
Clock				
t_{CYC}	Clock cycle time	6.0	–	ns
F_{MAX}	Maximum operating frequency	–	167	MHz
t_{CH}	Clock HIGH	2.2	–	ns
t_{CL}	Clock LOW	2.2	–	ns
Output Times				
t_{CO}	Data output valid after CLK rise	–	3.4	ns
t_{EOV}	\overline{OE} LOW to output valid	–	3.4	ns
t_{DOH}	Data output hold after CLK rise	1.5	–	ns
t_{CHZ}	Clock to high Z ^[17, 18, 19]	–	3.4	ns
t_{CLZ}	Clock to low Z ^[17, 18, 19]	1.5	–	ns
t_{EOHZ}	\overline{OE} HIGH to output high Z ^[17, 18, 19]	–	3.4	ns
t_{EOLZ}	\overline{OE} LOW to output low Z ^[17, 18, 19]	0	–	ns
Setup Times				
t_{AS}	Address setup before CLK rise	1.5	–	ns
t_{DS}	Data input setup before CLK rise	1.5	–	ns
t_{CENS}	\overline{CEN} setup before CLK rise	1.5	–	ns
t_{WES}	\overline{WE} , \overline{BW}_x setup before CLK rise	1.5	–	ns
t_{ALS}	ADV/LD setup before CLK rise	1.5	–	ns
t_{CES}	Chip select setup	1.5	–	ns
Hold Times				
t_{AH}	Address hold after CLK rise	0.5	–	ns
t_{DH}	Data input hold after CLK rise	0.5	–	ns
t_{CENH}	\overline{CEN} hold after CLK rise	0.5	–	ns
t_{WEH}	\overline{WE} , \overline{BW}_x hold after CLK rise	0.5	–	ns
t_{ALH}	ADV/LD hold after CLK rise	0.5	–	ns
t_{CEH}	Chip select hold after CLK rise	0.5	–	ns

Notes

14. Timing reference is 1.5 V when $V_{DDQ} = 3.3$ V and is 1.25 V when $V_{DDQ} = 2.5$ V.
15. Test conditions shown in (a) of [Figure 2 on page 12](#) unless otherwise noted.
16. This part has a voltage regulator internally; t_{Power} is the time power needs to be supplied above V_{DD} minimum initially, before a Read or Write operation can be initiated.
17. t_{CHZ} , t_{CLZ} , t_{EOLZ} , and t_{EOHZ} are specified with AC test conditions shown in (b) of [Figure 2 on page 12](#). Transition is measured ± 200 mV from steady-state voltage.
18. At any given voltage and temperature, t_{EOHZ} is less than t_{EOLZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve High Z prior to Low Z under the same system conditions.
19. This parameter is sampled and not 100% tested.

Switching Waveforms

Figure 3. Read/Write/Timing [20, 21, 22]



Notes

20. For this waveform ZZ is tied LOW.

21. When \overline{CE} is LOW, \overline{CE}_1 is LOW, \overline{CE}_2 is HIGH and \overline{CE}_3 is LOW. When \overline{CE} is HIGH, \overline{CE}_1 is HIGH or \overline{CE}_2 is LOW or \overline{CE}_3 is HIGH.

22. Order of the Burst sequence is determined by the status of the MODE (0 = Linear, 1 = Interleaved). Burst operations are optional.



Switching Waveforms (continued)

Figure 4. NOP, STALL, and DESELECT Cycles [23, 24, 25]

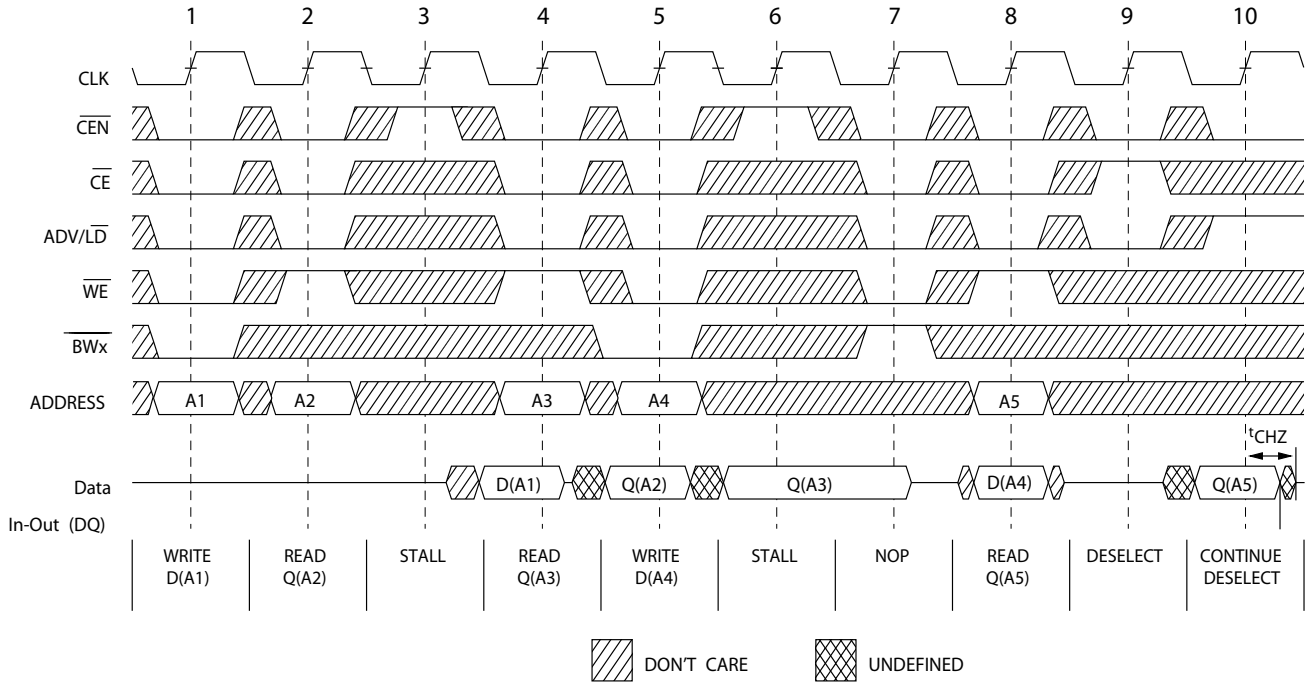
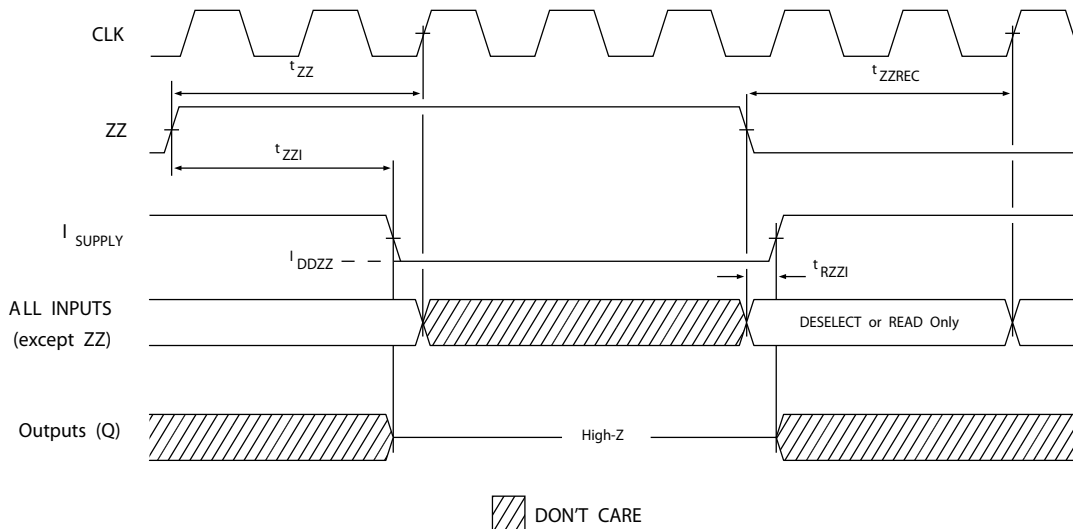


Figure 5. ZZ Mode Timing [26, 27]



Notes

- 23. For this waveform ZZ is tied LOW.
- 24. When \overline{CE} is LOW, \overline{CE}_1 is LOW, CE_2 is HIGH and \overline{CE}_3 is LOW. When \overline{CE} is HIGH, \overline{CE}_1 is HIGH or CE_2 is LOW or \overline{CE}_3 is HIGH.
- 25. The Ignore Clock Edge or Stall cycle (Clock 3) illustrated CEN being used to create a pause. A write is not performed during this cycle.
- 26. Device must be deselected when entering ZZ mode. See cycle description table for all possible signal conditions to deselect the device.
- 27. I/Os are in High Z when exiting ZZ sleep mode.



Ordering Information

Cypress offers other versions of this type of product in many different configurations and features. The following table contains only the list of parts that are currently available.

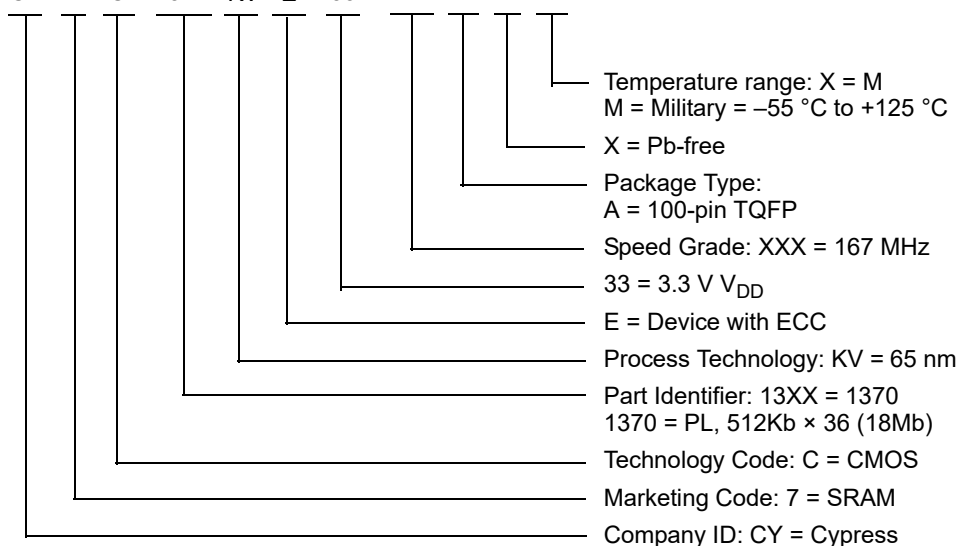
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Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
167	CY7C1370KVE33-167AXM	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Military

Ordering Code Definitions

CY 7 C 13XX KV E 33 - XXX A X X





Acronyms

Acronym	Description
\overline{CE}	Chip Enable
\overline{CEN}	Clock Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
LMBU	Logical Multi-Bit Upsets
LSB	Least Significant Bit
LSBU	Logical Single-Bit Upsets
MSB	Most Significant Bit
NoBL	No Bus Latency
\overline{OE}	Output Enable
SEL	Single Event Latch-up
SRAM	Static Random Access Memory
TQFP	Thin Quad Flat Pack
TTL	Transistor-Transistor Logic
\overline{WE}	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
$^{\circ}\text{C}$	degree Celsius
$\text{k}\Omega$	kilohm
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mV	millivolt
mm	millimeter
ms	millisecond
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ps	picosecond
V	volt
W	watt



Document History Page

Document Title: CY7C1370KVE33 Military Temperature, 18-Mbit (512K × 36) Pipelined SRAM with NoBL™ Architecture (With ECC)				
Document Number: 002-13841				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	5407552	PRIT	08/24/2016	New data sheet.
*A	6013501	CNX	01/04/2018	Updated Package Diagrams : spec 51-85050 – Changed revision from *E to *G. Updated to new template.



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