

CY8C4024FNI-S412T Datasheet

www.digi-electronics.com



<https://www.DiGi-Electronics.com>

| | |
|------------------------------|--|
| DiGi Electronics Part Number | CY8C4024FNI-S412T-DG |
| Manufacturer | Infineon Technologies |
| Manufacturer Product Number | CY8C4024FNI-S412T |
| Description | IC MCU 32BIT 16KB FLASH 25WLCSP |
| Detailed Description | ARM® Cortex®-M0+ PSOC® 4 CY8C4000S Microcontroller IC 32-Bit Single-Core 24MHz 16KB (16K x 8) FLASH 25-WLCSP (2.02x1.93) |

This model CY8C4024FNI-S412T is available at DiGi Electronics.

DiGi Electronics offers a global database of semiconductor and electronic component datasheets.

We welcome your inquiries regarding pricing, lead time, or other product-related questions.

 [Request a Quote](#)

 [Datasheet Search](#)



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.

Purchase and inquiry

Manufacturer Product Number:

CY8C4024FNI-S412T

Series:

PSOC® 4 CY8C4000S

DiGi-Electronics Programmable:

Not Verified

Core Size:

32-Bit Single-Core

Connectivity:

I2C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART

Number of I/O:

21

Program Memory Type:

FLASH

RAM Size:

2K x 8

Data Converters:

A/D 1x10b

Operating Temperature:

-40°C ~ 85°C (TA)

Package / Case:

25-XFBGA, WLCSP

Base Product Number:

CY8C4024

Manufacturer:

Infineon Technologies

Product Status:

Active

Core Processor:

ARM® Cortex®-M0+

Speed:

24MHz

Peripherals:

Brown-out Detect/Reset, CapSense, LCD, LVD, POR, PWM, WDT

Program Memory Size:

16KB (16K x 8)

EEPROM Size:

-

Voltage - Supply (Vcc/Vdd):

1.71V ~ 5.5V

Oscillator Type:

Internal

Mounting Type:

Surface Mount

Supplier Device Package:

25-WLCSP (2.02x1.93)

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.31.0001

Moisture Sensitivity Level (MSL):

3 (168 Hours)

ECCN:

3A991A2

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

General description

PSoC™ 4 is a scalable and reconfigurable platform architecture for a family of programmable embedded system controllers with an Arm® Cortex®-M0+ CPU. It combines programmable and reconfigurable analog and digital blocks with flexible automatic routing. The PSoC™ 4000S product family is a member of the PSoC™ 4 platform architecture. It is a combination of a microcontroller with standard communication and timing peripherals, a capacitive touch-sensing system (CAPSENSE™) with best-in-class performance, programmable general-purpose continuous-time and switched-capacitor analog blocks, and programmable connectivity. PSoC™ 4000S products are upward compatible with members of the PSoC™ 4 platform for new applications and design needs.

Features

- 32-bit MCU subsystem
 - 48-MHz Arm® Cortex®-M0+ CPU with single-cycle multiply
 - Up to 32 KB of flash with read accelerator
 - Up to 4 KB of SRAM
- Programmable analog
 - Single-slope 10-bit ADC function provided by Capacitance sensing block
 - Two current DACs (IDACs) for general-purpose or capacitive sensing applications on any pin
 - Two low-power comparators that operate in Deep Sleep low-power mode
- Programmable digital
 - Programmable logic blocks allowing boolean operations to be performed on port inputs and outputs
- Low-power 1.71-V to 5.5-V operation
 - Deep Sleep mode with operational analog and 2.5 µA digital system current
- Capacitive sensing
 - Capacitive sigma-delta provides best-in-class signal-to-noise ratio (SNR) (>5:1) and water tolerance
 - Infineon-supplied software component makes capacitive sensing design easy
 - Automatic hardware tuning (SmartSense)
- LCD drive capability
 - LCD segment drive capability on GPIOs
- Serial communication
 - Two independent run-time reconfigurable serial communication blocks (SCBs) with re-configurable I²C, SPI, or UART functionality
- Timing and pulse-width modulation
 - Five 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
 - Center-aligned, edge, and pseudo-random modes
 - Comparator-based triggering of kill signals for motor drive and other high-reliability digital logic applications
- Up to 36 programmable GPIO pins
 - 48-pin TQFP, 40-pin QFN, 32-pin QFN, 24-pin QFN, 32-pin TQFP, and 25-ball WLCSP packages
 - Any GPIO pin can be CAPSENSE™, analog, or digital
 - Drive modes, strengths, and slew rates are programmable



PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Features

- Clock sources
 - 32 kHz watch crystal oscillator (WCO)
 - $\pm 2\%$ internal main oscillator (IMO)
 - 32 kHz internal low-power oscillator (ILO)
- ModusToolbox™ software
 - Comprehensive collection of multi-platform tools and software libraries
 - Includes board support packages (BSPs), peripheral driver library (PDL), and middleware such as CAPSENSE™
- PSoC™ Creator design environment
 - Integrated development environment (IDE) provides schematic design entry and build, with analog and digital automatic routing
 - Application programming interface (API) components for all fixed-function and programmable peripherals
- Industry-standard tool compatibility
 - After schematic entry, development can be done with Arm®-based industry-standard development tools

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Table of contents

Table of contents

| | |
|--|-----------|
| General description | 1 |
| Features | 1 |
| Table of contents | 3 |
| 1 Development ecosystem | 4 |
| 1.1 PSoC™ 4 MCU resources | 4 |
| 1.2 ModusToolbox™ software | 5 |
| 1.3 PSoC™ Creator | 6 |
| Block diagram | 7 |
| 2 Functional description | 9 |
| 3 Functional definition | 10 |
| 3.1 CPU and memory subsystem | 10 |
| 3.2 System resources | 10 |
| 3.3 Analog blocks | 12 |
| 3.4 Programmable digital blocks | 12 |
| 3.5 Fixed function digital | 13 |
| 3.6 GPIO | 14 |
| 3.7 Special function peripherals | 14 |
| 4 Pinouts | 15 |
| 4.1 Alternate pin functions | 17 |
| 5 Power | 19 |
| 5.1 Mode 1: 1.8 V to 5.5 V external supply | 19 |
| 5.2 Mode 2: 1.8 V ± 5% external supply | 20 |
| 6 Electrical specifications | 21 |
| 6.1 Absolute maximum ratings | 21 |
| 6.2 Device level specifications | 22 |
| 6.3 Analog peripherals | 27 |
| 6.4 Digital peripherals | 32 |
| 6.5 Memory | 36 |
| 6.6 System resources | 37 |
| 7 Ordering information | 41 |
| 8 Packaging | 43 |
| 8.1 Package diagrams | 44 |
| 9 Acronyms | 49 |
| 10 Document conventions | 53 |
| 10.1 Units of measure | 53 |
| Revision history | 54 |

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Development ecosystem

1 Development ecosystem

1.1 PSoC™ 4 MCU resources

Infineon provides a wealth of data at www.infineon.com to help you select the right PSoC™ device and quickly and effectively integrate it into your design. The following is an abbreviated, hyperlinked list of resources for PSoC™ 4 MCU:

- **Overview: PSoC™ Portfolio**
- **Product selectors: PSoC™ 4 MCU**
- **Application notes** cover a broad range of topics, from basic to advanced level, and include the following:
 - **AN79953:** Getting started With PSoC™ 4 MCU. This application note has a convenient flow chart to help decide which IDE to use: **ModusToolbox™ software** or **PSoC™ Creator**.
 - **AN91184:** PSoC™ 4 Bluetooth® Low Energy - Designing Bluetooth® LE applications
 - **AN88619:** PSoC™ 4 Hardware design considerations
 - **AN73854:** PSoC™ - Introduction to bootloaders
 - **AN89610:** PSoC™ Arm® Cortex® code optimization
 - **AN86233:** PSoC™ 4 MCU low-power modes and power reduction techniques
 - **AN57821:** PSoC™ 3, PSoC™ 4, and PSoC™ 5LP mixed-signal circuit board layout considerations
 - **AN85951:** PSoC™ 4 and PSoC™ 6 MCU CAPSENSE™ design guide
- **Code examples** demonstrate product features and usage, and are also available on **Infineon GitHub repositories**.
- **Reference manuals** provide detailed descriptions of PSoC™ 4 MCU architecture and registers.
- **PSoC™ 4 MCU programming specification** provides the information necessary to program PSoC™ 4 MCU non-volatile memory.
- **Development tools**
 - **ModusToolbox™ software** enables cross platform code development with a robust suite of tools and software libraries.
 - **PSoC™ Creator** is a free Windows-based IDE. It enables concurrent hardware and firmware design of PSoC™ 3, PSoC™ 4, PSoC™ 5LP, and PSoC™ 6 MCU based systems. Applications are created using schematic capture and over 150 pre-verified, production-ready peripheral components.
 - **CY8CKIT-145-40XX** PSoC™ 4000S CAPSENSE™ prototyping kit, is a low-cost and easy-to-use evaluation platform. This kit provides easy access to all the device I/Os in a breadboard-compatible format.
 - **MiniProg4** and **MiniProg3** all-in-one development programmers and debuggers.
 - **PSoC™ 4 MCU CAD libraries** provide footprint and schematic support for common tools. **IBIS models** are also available.
- **Training Videos** are available on a wide range of topics including the **PSoC™ 101 series**.
- **Infineon developer community** enables connection with fellow PSoC™ developers around the world, 24 hours a day, 7 days a week, and hosts a dedicated **PSoC™ 4 MCU community**.

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Development ecosystem

1.2 ModusToolbox™ software

ModusToolbox™ software is Infineon's comprehensive collection of multi-platform tools and software libraries that enable an immersive development experience for creating converged MCU and wireless systems. It is:

- Comprehensive - it has the resources you need
- Flexible - you can use the resources in your own workflow
- Atomic - you can get just the resources you want

Infineon provides a large collection of code **repositories on GitHub**, including:

- Board support packages (BSPs) aligned with Infineon kits
- Low-level resources, including a peripheral driver library (PDL)
- Middleware enabling industry-leading features such as CAPSENSE™
- An extensive set of thoroughly tested **code example applications**

ModusToolbox™ software is IDE-neutral and easily adaptable to your workflow and preferred development environment. It includes a project creator, peripheral and library configurators, a library manager, as well as the optional Eclipse IDE for ModusToolbox™, as **Figure 1** shows. For information on using Infineon tools, refer to the documentation delivered with ModusToolbox™ software, and **AN79953: Getting Started with PSoc™ 4**.

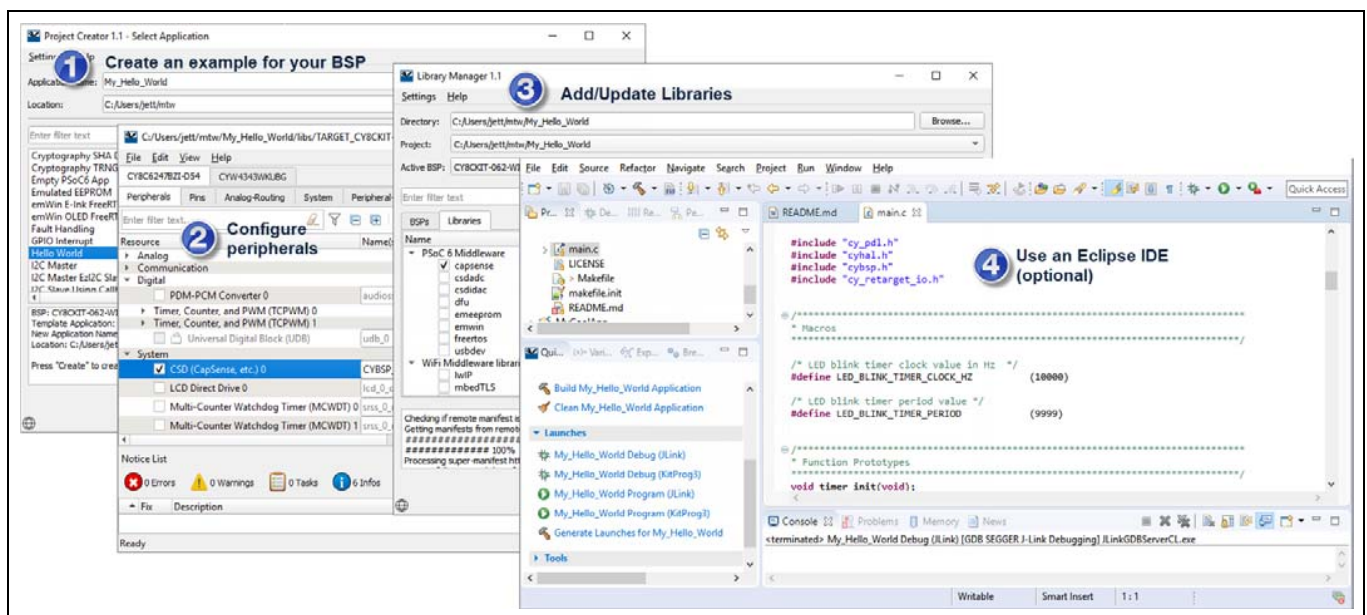


Figure 1 ModusToolbox™ software tools

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Development ecosystem

1.3 PSoC™ Creator

PSoC™ Creator is a free Windows-based IDE. It enables you to design hardware and firmware systems concurrently, based on PSoC™ 4 MCU. As **Figure 2** shows, with PSoC™ Creator you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Co-design your application firmware with the PSoC™ hardware, using the PSoC™ Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets
6. Prototype your solution with the PSoC™ 4 Pioneer kits. If a design change is needed, PSoC™ Creator and components enable you to make changes on-the-fly without the need for hardware revisions.

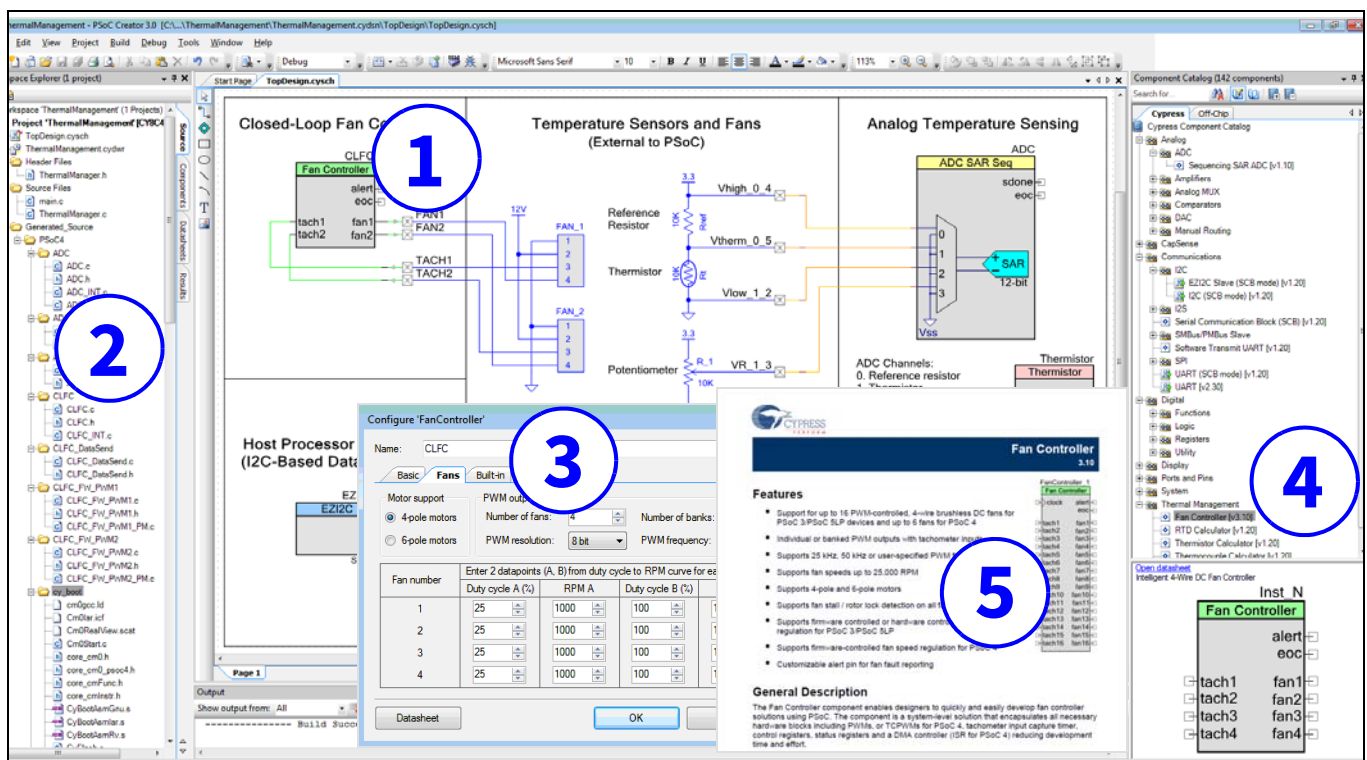


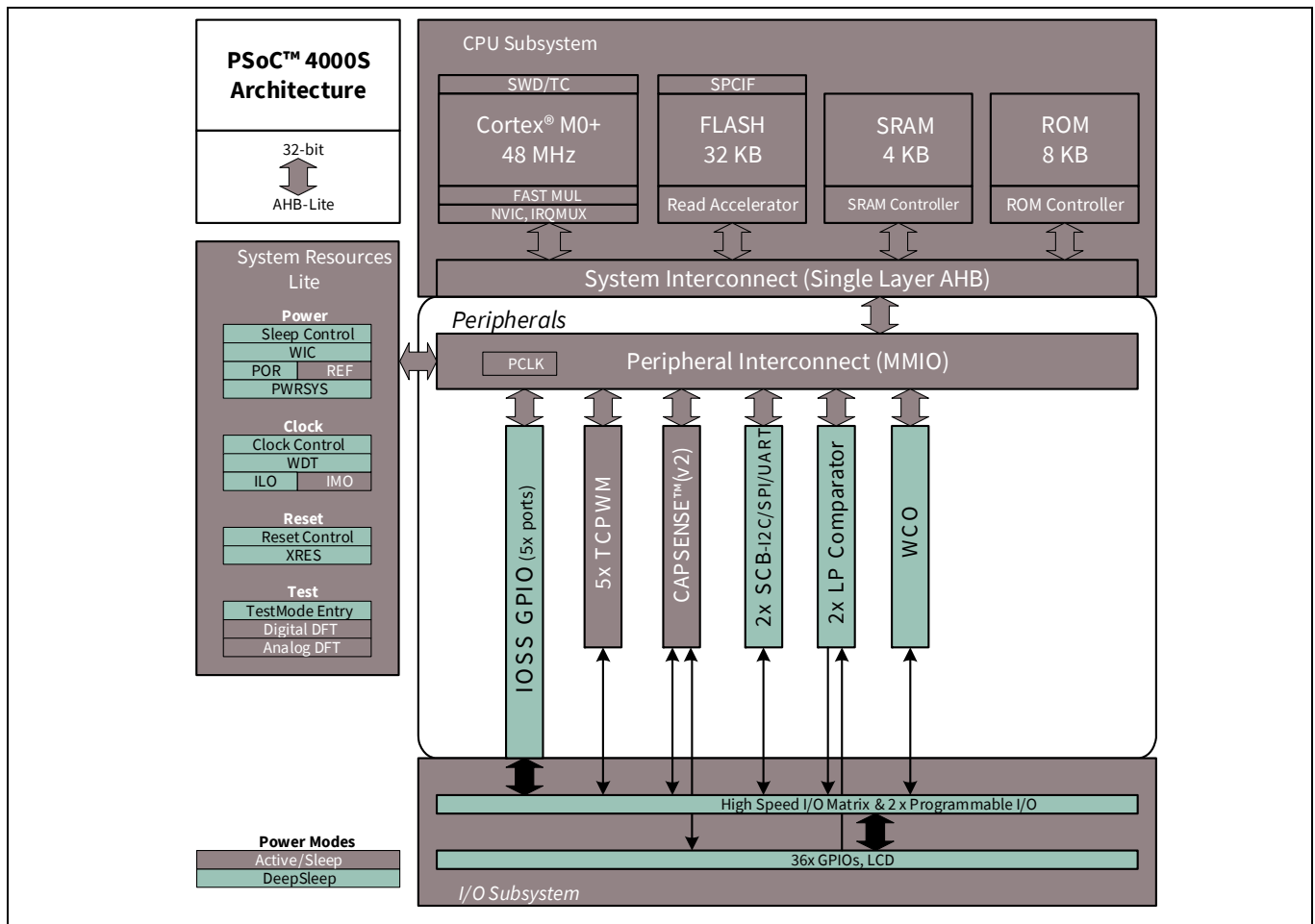
Figure 2 Multiple-sensor example project in PSoC™ Creator

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Block diagram

Block diagram



PSoC™ 4000S devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The Arm® serial-wire debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC™ Creator IDE provides fully integrated programming and debug support for the PSoC™ 4000S devices. The SWD interface is fully compatible with industry-standard third-party tools. The PSoC™ 4000S provides a level of security not possible with multi-chip application solutions or with microcontrollers.

It has the following advantages:

- Allows disabling of debug features
- Robust flash protection
- Allows customer-proprietary functionality to be implemented in on-chip programmable blocks



PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Block diagram

The debug circuits are enabled by default and can be disabled in firmware. If they are not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging. Thus firmware control of debugging cannot be over-ridden without erasing the firmware thus providing security.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. Therefore, PSoC™ 4000S, with device security enabled, may not be returned for failure analysis. This is a trade-off the PSoC™ 4000S allows the customer to make.



PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Functional description

2 Functional description

PSoC™ 4000S devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The Arm® serial-wire debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full-device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC™ Creator IDE provides fully integrated programming and debug support for the PSoC™ 4000S devices. The SWD interface is fully compatible with industry-standard third-party tools. The PSoC™ 4000S family provides a level of security not possible with multi-chip application solutions or with microcontrollers. It has the following advantages:

- Allows disabling of debug features
- Robust flash protection
- Allows customer-proprietary functionality to be implemented in on-chip programmable blocks

The debug circuits are enabled by default and can be disabled in firmware. If they are not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging. Thus firmware control of debugging cannot be over-ridden without erasing the firmware thus providing security.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. Therefore, PSoC™ 4000S, with device security enabled, may not be returned for failure analysis. This is a trade-off the PSoC™ 4000S allows the customer to make.

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Functional definition

3 Functional definition

3.1 CPU and memory subsystem

3.1.1 CPU

The Cortex®-M0+ CPU in the PSoC™ 4000S is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and the CPU executes a subset of the thumb-2 instruction set. It includes a nested vectored interrupt controller (NVIC) block with eight interrupt inputs and also includes a wakeup interrupt controller (WIC). The WIC can wake the processor from Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in Deep Sleep mode.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a two-wire form of JTAG. The debug configuration used for PSoC™ 4000S has four breakpoint (address) comparators and two watchpoint (data) comparators.

3.1.2 Flash

The PSoC™ 4000S device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The low-power flash block is designed to deliver two wait-state (WS) access time at 48 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average.

3.1.3 SRAM

Four KB of SRAM are provided with zero wait-state access at 48 MHz.

3.1.4 SRAM

A supervisory ROM that contains boot and configuration routines is provided.

3.2 System resources

3.2.1 Power system

The power system is described in detail in the section **“Power”** on page 19. It provides assurance that voltage levels are as required for each respective mode and either delays mode entry (for example, on power-on reset (POR)) until voltage levels are as required for proper functionality, or generates resets (for example, on brown-out detection). The PSoC™ 4000S operates with a single external supply over the range of either 1.8 V \pm 5% (externally regulated) or 1.8 to 5.5 V (internally regulated) and has three different power modes, transitions between which are managed by the power system. The PSoC™ 4000S provides Active, Sleep, and Deep Sleep low-power modes.

All subsystems are operational in Active mode. The CPU subsystem (CPU, flash, and SRAM) is clock-gated off in Sleep mode, while all peripherals and interrupts are active with instantaneous wake-up on a wake-up event. In Deep Sleep mode, the high-speed clock and associated circuitry is switched off; wake-up from this mode takes 35 μ s.

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Functional definition

3.2.2 Clock system

The PSoC™ 4000S clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that there are no metastable conditions.

The clock system for the PSoC™ 4000S consists of the internal main oscillator (IMO), internal low-frequency oscillator (ILO), a 32 kHz watch crystal oscillator (WCO) and provision for an external clock. Clock dividers are provided to generate clocks for peripherals on a fine-grained basis. Fractional dividers are also provided to enable clocking of higher data rates for UARTs.

The HFCLK signal can be divided down to generate synchronous clocks for the analog and digital peripherals. There are eight clock dividers for the PSoC™ 4000S, two of those are fractional dividers. The 16-bit capability allows flexible generation of fine-grained frequency values, and is fully supported in PSoC™ Creator.

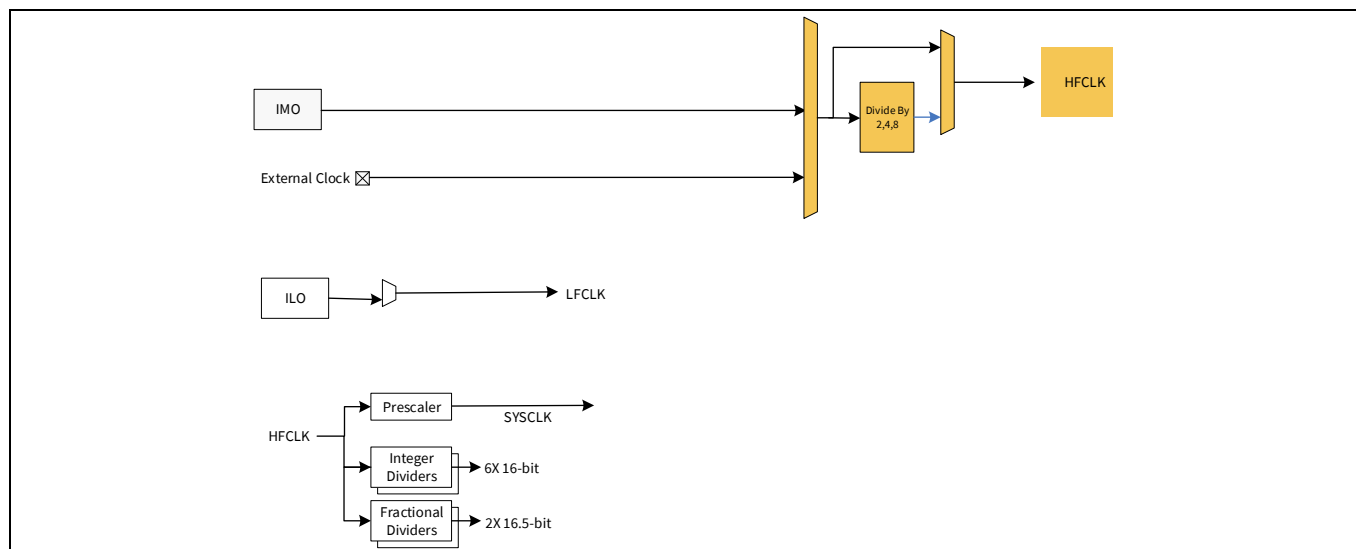


Figure 3 PSoC™ 4000S MCU clocking architecture

3.2.3 IMO clock source

The IMO is the primary source of internal clocking in the PSoC™ 4000S. It is trimmed during testing to achieve the specified accuracy. The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The IMO tolerance with Infineon-provided calibration settings is $\pm 2\%$.

3.2.4 ILO clock source

The ILO is a very low power, nominally 40-kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Infineon provides a software component, which does the calibration.

3.2.5 Watch crystal oscillator (WCO)

The PSoC™ 4000S clock subsystem also implements a low-frequency (32-kHz watch crystal) oscillator that can be used for precision timing applications. The WCO block allows locking the IMO to the 32-kHz oscillator. The WCO on PSoC™ 4000S series devices does not connect to the LFCLK or WDT. Due to this, RTC functionality is not supported.

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Functional definition

3.2.6 Watchdog timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a Reset Cause Register, which is firmware readable.

3.2.7 Reset

The PSoC™ 4000S can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset by asserting it active low. The XRES pin has an internal pull-up resistor that is always enabled.

3.2.8 Voltage reference

The PSoC™ 4000S reference system generates all internally required references. A 1.2-V voltage reference is provided for the comparator. The IDACs are based on a $\pm 5\%$ reference.

3.3 Analog blocks

3.3.1 Low-power comparators (LPC)

The PSoC™ 4000S has a pair of low-power comparators, which can also operate in Deep Sleep modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode where the system wake-up circuit is activated by a comparator switch event. The LPC outputs can be routed to pins.

3.3.2 Current DACs

The PSoC™ 4000S has two IDACs, which can drive any of the pins on the chip. These IDACs have programmable current ranges.

3.3.3 Analog multiplexed buses

The PSoC™ 4000S has two concentric independent buses that go around the periphery of the chip. These buses (called amux buses) are connected to firmware-programmable analog switches that allow the chip's internal resources (IDACs, comparator) to connect to any pin on the I/O Ports.

3.4 Programmable digital blocks

The programmable I/O (Smart I/O) block is a fabric of switches and LUTs that allows boolean functions to be performed in signals being routed to the pins of a GPIO port. The Smart I/O can perform logical operations on input pins to the chip and on signals going out as outputs.

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Functional definition

3.5 Fixed function digital

3.5.1 Timer/Counter/PWM (TCPWM) block

The TCPWM block consists of a 16-bit counter with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register that is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals that are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as dead-band programmable complementary PWM outputs. It also has a kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an over-current state is indicated and the PWM driving the FETs needs to be shut off immediately with no time for software intervention. There are five TCPWM blocks in the PSoC™ 4000S.

3.5.2 Serial communication block (SCB)

The PSoC™ 4000S has two serial communication blocks, which can be programmed to have SPI, I2C, or UART functionality.

I²C Mode: The hardware I²C block implements a full multi-master and slave interface (it is capable of multi-master arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. It also supports EZI2C that creates a mailbox address range in the memory of the PSoC™ 4000S and effectively reduces I²C communication to reading from and writing to an array in memory. In addition, the block supports an 8-deep FIFO for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduces the need for clock stretching caused by the CPU not having read data on time.

The I²C peripheral is compatible with the I²C Standard-mode and Fast-mode devices as defined in the NXP I²C-bus specification and user manual (UM10204). The I²C bus I/O is implemented with GPIO in open-drain modes.

The PSoC™ 4000S is not completely compliant with the I²C spec in the following respect:

- GPIO cells are not over-voltage tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I²C system.

UART Mode: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

SPI Mode: The SPI mode supports full Motorola SPI, TI SSP (adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO.

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Functional definition

3.6 GPIO

The PSoC™ 4000S has up to 36 GPIOs. The GPIO block implements the following:

- Eight drive modes:
 - Analog input mode (input and output buffers disabled)
 - Input only
 - Weak pull-up with strong pull-down
 - Strong pull-up with weak pull-down
 - Open drain with strong pull-down
 - Open drain with strong pull-up
 - Strong pull-up with strong pull-down
 - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width (less for ports 2 and 3). During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (5 for PSoC™ 4000S).

3.7 Special function peripherals

3.7.1 CAPSENSE™

CAPSENSE™ is supported in the PSoC™ 4000S through a CAPSENSE™ Sigma-Delta (CSD) block that can be connected to any pins through an analog multiplex bus via analog switches. CAPSENSE™ function can thus be provided on any available pin or group of pins in a system under software control. A PSoC™ Creator component is provided for the CAPSENSE™ block to make it easy for the user.

Shield voltage can be driven on another analog multiplex bus to provide water-tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input. Proximity sensing can also be implemented.

The CAPSENSE™ block has two IDACs, which can be used for general purposes if CAPSENSE™ is not being used (both IDACs are available in that case) or if CAPSENSE™ is used without water tolerance (one IDAC is available). The CAPSENSE™ block also provides a 10-bit slope ADC function, which can be used in conjunction with the CAPSENSE™ function.

The CAPSENSE™ block is an advanced, low-noise, programmable block with programmable voltage references and current source ranges for improved sensitivity and flexibility. It can also use an external reference voltage. It has a full-wave CSD mode that alternates sensing to VDDA and Ground to null out power-supply related noise.

3.7.2 LCD segment drive

The PSoC™ 4000S has an LCD controller, which can drive up to 8 commons and up to 28 segments. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as digital correlation and PWM. Digital correlation pertains to modulating the frequency and drive levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal to zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays. PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays.

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Pinouts

4 Pinouts

The following table provides the pin list for PSoC™ 4000S for the 48-pin TQFP, 40-pin QFN, 32-pin QFN, 24-pin QFN, 32-pin TQFP, and 25-ball CSP packages. All port pins support GPIO. Pin 11 is a No-Connect in the 48-TQFP.

Table 1 PSoC™ 4000S pin list

| 48-pin TQFP | | 32-pin QFN | | 24-pin QFN | | 25-ball CSP | | 40-pin QFN | | 32-pin TQFP | |
|-------------|------|------------|------|------------|------|-------------|------|------------|------|-------------|------|
| Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name |
| 28 | P0.0 | 17 | P0.0 | 13 | P0.0 | D1 | P0.0 | 22 | P0.0 | 17 | P0.0 |
| 29 | P0.1 | 18 | P0.1 | 14 | P0.1 | C3 | P0.1 | 23 | P0.1 | 18 | P0.1 |
| 30 | P0.2 | 19 | P0.2 | – | – | – | – | 24 | P0.2 | 19 | P0.2 |
| 31 | P0.3 | 20 | P0.3 | – | – | – | – | 25 | P0.3 | 20 | P0.3 |
| 32 | P0.4 | 21 | P0.4 | 15 | P0.4 | C2 | P0.4 | 26 | P0.4 | 21 | P0.4 |
| 33 | P0.5 | 22 | P0.5 | 16 | P0.5 | C1 | P0.5 | 27 | P0.5 | 22 | P0.5 |
| 34 | P0.6 | 23 | P0.6 | 17 | P0.6 | B1 | P0.6 | 28 | P0.6 | 23 | P0.6 |
| 35 | P0.7 | – | – | – | – | B2 | P0.7 | 29 | P0.7 | – | – |
| 36 | XRES | 24 | XRES | 18 | XRES | B3 | XRES | 30 | XRES | 24 | XRES |
| 37 | VCCD | 25 | VCCD | 19 | VCCD | A1 | VCCD | 31 | VCCD | 25 | VCCD |
| 38 | VSSD | 26 | VSSD | 20 | VSSD | A2 | VSS | – | – | 26 | VSSD |
| 39 | VDDD | 27 | VDD | 21 | VDD | A3 | VDD | 32 | VDDD | 27 | VDD |
| 40 | VDDA | 27 | VDD | 21 | VDD | A3 | VDD | 33 | VDDA | 27 | VDD |
| 41 | VSSA | 28 | VSSA | 22 | VSSA | A2 | VSS | 34 | VSSA | 28 | VSSA |
| 42 | P1.0 | 29 | P1.0 | – | – | – | – | 35 | P1.0 | 29 | P1.0 |
| 43 | P1.1 | 30 | P1.1 | – | – | – | – | 36 | P1.1 | 30 | P1.1 |
| 44 | P1.2 | 31 | P1.2 | 23 | P1.2 | A4 | P1.2 | 37 | P1.2 | 31 | P1.2 |
| 45 | P1.3 | 32 | P1.3 | 24 | P1.3 | B4 | P1.3 | 38 | P1.3 | 32 | P1.3 |
| 46 | P1.4 | – | – | – | – | – | – | 39 | P1.4 | – | – |
| 47 | P1.5 | – | – | – | – | – | – | – | – | – | – |
| 48 | P1.6 | – | – | – | – | – | – | – | – | – | – |
| 1 | P1.7 | 1 | P1.7 | 1 | P1.7 | A5 | P1.7 | 40 | P1.7 | 1 | P1.7 |
| 2 | P2.0 | 2 | P2.0 | 2 | P2.0 | B5 | P2.0 | 1 | P2.0 | 2 | P2.0 |
| 3 | P2.1 | 3 | P2.1 | 3 | P2.1 | C5 | P2.1 | 2 | P2.1 | 3 | P2.1 |
| 4 | P2.2 | 4 | P2.2 | – | – | – | – | 3 | P2.2 | 4 | P2.2 |
| 5 | P2.3 | 5 | P2.3 | – | – | – | – | 4 | P2.3 | 5 | P2.3 |
| 6 | P2.4 | – | – | – | – | – | – | 5 | P2.4 | – | – |
| 7 | P2.5 | 6 | P2.5 | – | – | – | – | 6 | P2.5 | 6 | P2.5 |
| 8 | P2.6 | 7 | P2.6 | 4 | P2.6 | D5 | P2.6 | 7 | P2.6 | 7 | P2.6 |
| 9 | P2.7 | 8 | P2.7 | 5 | P2.7 | C4 | P2.7 | 8 | P2.7 | 8 | P2.7 |
| 10 | VSSD | – | – | – | – | A2 | VSS | 9 | VSSD | – | – |
| 12 | P3.0 | 9 | P3.0 | 6 | P3.0 | E5 | P3.0 | 10 | P3.0 | 9 | P3.0 |
| 13 | P3.1 | 10 | P3.1 | – | – | D4 | P3.1 | 11 | P3.1 | 10 | P3.1 |

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Pinouts

Table 1 PSoC™ 4000S pin list (continued)

| 48-pin TQFP | | 32-pin QFN | | 24-pin QFN | | 25-ball CSP | | 40-pin QFN | | 32-pin TQFP | |
|-------------|------|------------|------|------------|------|-------------|------|------------|------|-------------|------|
| Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name |
| 14 | P3.2 | 11 | P3.2 | 7 | P3.2 | E4 | P3.2 | 12 | P3.2 | 11 | P3.2 |
| 16 | P3.3 | 12 | P3.3 | 8 | P3.3 | D3 | P3.3 | 13 | P3.3 | 12 | P3.3 |
| 17 | P3.4 | – | – | – | – | – | – | 14 | P3.4 | – | – |
| 18 | P3.5 | – | – | – | – | – | – | 15 | P3.5 | – | – |
| 19 | P3.6 | – | – | – | – | – | – | 16 | P3.6 | – | – |
| 20 | P3.7 | – | – | – | – | – | – | 17 | P3.7 | – | – |
| 21 | VDDD | – | – | – | – | – | – | – | – | – | – |
| 22 | P4.0 | 13 | P4.0 | 9 | P4.0 | E3 | P4.0 | 18 | P4.0 | 13 | P4.0 |
| 23 | P4.1 | 14 | P4.1 | 10 | P4.1 | D2 | P4.1 | 19 | P4.1 | 14 | P4.1 |
| 24 | P4.2 | 15 | P4.2 | 11 | P4.2 | E2 | P4.2 | 20 | P4.2 | 15 | P4.2 |
| 25 | P4.3 | 16 | P4.3 | 12 | P4.3 | E1 | P4.3 | 21 | P4.3 | 16 | P4.3 |

Note: Pins 11, 15, 26, and 27 are No connects (NC) on the 48-pin TQFP.

Descriptions of the pin functions are as follows:

VDDD: Power supply for the digital section.

VDDA: Power supply for the analog section.

VSSD, VSSA: Ground pins for the digital and analog sections respectively.

VCCD: Regulated digital supply (1.8 V ± 5%)

VDD: Power supply to all sections of the chip

VSS: Ground for all sections of the chip



4.1 Alternate pin functions

Each port pin can be assigned to one of multiple functions; it can, for instance, be an analog I/O, a digital peripheral function, an LCD pin, or a CAPSENSE™ pin. The pin assignments are shown in the following table.

Table 2 Pin assignments

| Port/ Pin | Analog | Smart I/O | Alternate Function 1 | Alternate Function 2 | Alternate Function 3 | Deep Sleep 1 | Deep Sleep 2 |
|--------------|----------------|----------------|-----------------------|----------------------|----------------------|------------------|----------------------|
| P0.0 | lpcomp.in_p[0] | - | - | - | tcpwm.tr_in[0] | - | scb[0].spi_select1:0 |
| P0.1 | lpcomp.in_n[0] | - | - | - | tcpwm.tr_in[1] | - | scb[0].spi_select2:0 |
| P0.2 | lpcomp.in_p[1] | - | - | - | - | - | scb[0].spi_select3:0 |
| P0.3 | lpcomp.in_n[1] | - | - | - | - | - | - |
| P0.4 | wco.wco_in | - | - | scb[1].uart_rx:0 | - | scb[1].i2c_scl:0 | scb[1].spi_mosi:1 |
| P0.5 | wco.wco_out | - | - | scb[1].uart_tx:0 | - | scb[1].i2c_sda:0 | scb[1].spi_miso:1 |
| P0.6 | - | - | srss.ext_clk | scb[1].uart_cts:0 | - | - | scb[1].spi_clk:1 |
| P0.7 | - | - | - | scb[1].uart_rts:0 | - | - | scb[1].spi_select0:1 |
| P1.0 | - | - | tcpwm.line[2]:1 | scb[0].uart_rx:1 | - | scb[0].i2c_scl:0 | scb[0].spi_mosi:1 |
| P1.1 | - | - | tcpwm.line_compl[2]:1 | scb[0].uart_tx:1 | - | scb[0].i2c_sda:0 | scb[0].spi_miso:1 |
| P1.2 | - | - | tcpwm.line[3]:1 | scb[0].uart_cts:1 | tcpwm.tr_in[2] | - | scb[0].spi_clk:1 |
| P1.3 | - | - | tcpwm.line_compl[3]:1 | scb[0].uart_rts:1 | tcpwm.tr_in[3] | - | scb[0].spi_select0:1 |
| P1.4 | - | - | - | - | - | - | scb[0].spi_select1:1 |
| P1.5 | - | - | - | - | - | - | scb[0].spi_select2:1 |
| P1.6 | - | - | - | - | - | - | scb[0].spi_select3:1 |
| P1.7 | - | - | - | - | - | - | - |
| P2.0 | - | prgio[0].io[0] | tcpwm.line[4]:0 | csd.comp | tcpwm.tr_in[4] | scb[1].i2c_scl:1 | scb[1].spi_mosi:2 |
| P2.1 | - | prgio[0].io[1] | tcpwm.line_compl[4]:0 | - | tcpwm.tr_in[5] | scb[1].i2c_sda:1 | scb[1].spi_miso:2 |
| P2.2 | - | prgio[0].io[2] | - | - | - | - | scb[1].spi_clk:2 |

Table 2 Pin assignments (continued)

| Port/ Pin | Analog | Smart I/O | Alternate Function 1 | Alternate Function 2 | Alternate Function 3 | Deep Sleep 1 | Deep Sleep 2 |
|--------------|-----------------|----------------|-----------------------|----------------------|----------------------|------------------|----------------------|
| P2.3 | – | prgio[0].io[3] | – | – | – | – | scb[1].spi_select0:2 |
| P2.4 | – | prgio[0].io[4] | tcpwm.line[0]:1 | – | – | – | scb[1].spi_select1:1 |
| P2.5 | – | prgio[0].io[5] | tcpwm.line_compl[0]:1 | – | – | – | scb[1].spi_select2:1 |
| P2.6 | – | prgio[0].io[6] | tcpwm.line[1]:1 | – | – | – | scb[1].spi_select3:1 |
| P2.7 | – | prgio[0].io[7] | tcpwm.line_compl[1]:1 | – | – | lpcomp.comp[0]:1 | – |
| P3.0 | – | prgio[1].io[0] | tcpwm.line[0]:0 | scb[1].uart_rx:1 | – | scb[1].i2c_scl:2 | scb[1].spi_mosi:0 |
| P3.1 | – | prgio[1].io[1] | tcpwm.line_compl[0]:0 | scb[1].uart_tx:1 | – | scb[1].i2c_sda:2 | scb[1].spi_miso:0 |
| P3.2 | – | prgio[1].io[2] | tcpwm.line[1]:0 | scb[1].uart_cts:1 | – | cpuss.swd_data | scb[1].spi_clk:0 |
| P3.3 | – | prgio[1].io[3] | tcpwm.line_compl[1]:0 | scb[1].uart_rts:1 | – | cpuss.swd_clk | scb[1].spi_select0:0 |
| P3.4 | – | prgio[1].io[4] | tcpwm.line[2]:0 | – | tcpwm.tr_in[6] | – | scb[1].spi_select1:0 |
| P3.5 | – | prgio[1].io[5] | tcpwm.line_compl[2]:0 | – | tcpwm.tr_in[7] | – | scb[1].spi_select2:0 |
| P3.6 | – | prgio[1].io[6] | tcpwm.line[3]:0 | – | tcpwm.tr_in[8] | – | scb[1].spi_select3:0 |
| P3.7 | – | prgio[1].io[7] | tcpwm.line_compl[3]:0 | – | tcpwm.tr_in[9] | lpcomp.comp[1]:1 | – |
| P4.0 | csd.vref_ext | – | – | scb[0].uart_rx:0 | tcpwm.tr_in[10] | scb[0].i2c_scl:1 | scb[0].spi_mosi:0 |
| P4.1 | csd.cshieldpads | – | – | scb[0].uart_tx:0 | tcpwm.tr_in[11] | scb[0].i2c_sda:1 | scb[0].spi_miso:0 |
| P4.2 | csd.cmodpad | – | – | scb[0].uart_cts:0 | – | lpcomp.comp[0]:0 | scb[0].spi_clk:0 |
| P4.3 | csd.csh_tank | – | – | scb[0].uart_rts:0 | – | lpcomp.comp[1]:0 | scb[0].spi_select0:0 |

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Power

5 Power

The following power system diagram shows the set of power supply pins as implemented for the PSoC™ 4000S. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the V_{DD} input.

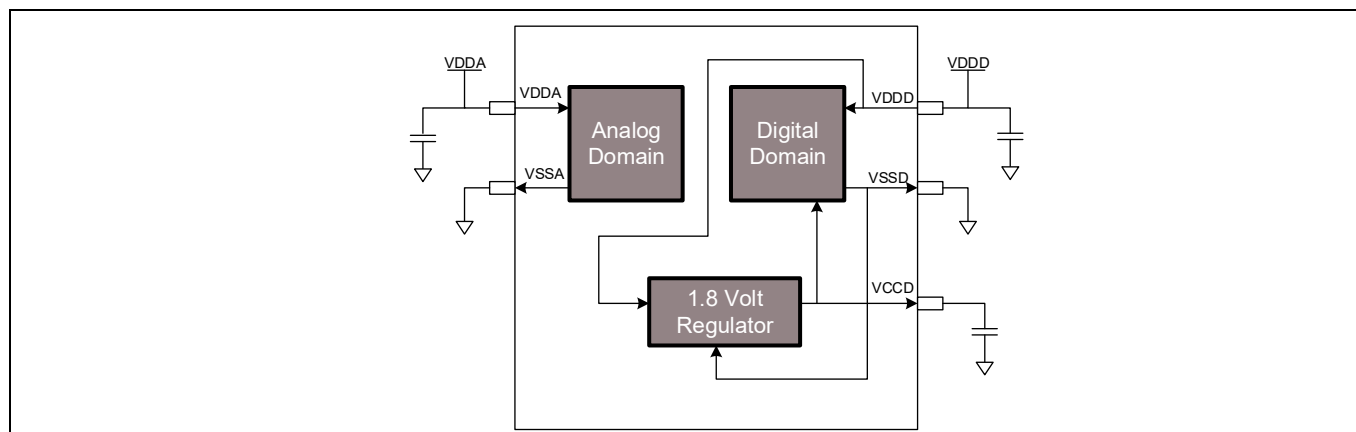


Figure 4 Power supply connections

There are two distinct modes of operation. In Mode 1, the supply voltage range is 1.8 V to 5.5 V (unregulated externally; internal regulator operational). In Mode 2, the supply range is $1.8 \text{ V} \pm 5\%$ (externally regulated; 1.71 V to 1.89 V, internal regulator bypassed).

5.1 Mode 1: 1.8 V to 5.5 V external supply

In this mode, the PSoC™ 4000S is powered by an external power supply that can be anywhere in the range of 1.8 V to 5.5 V. This range is also designed for battery-powered operation. For example, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of the PSoC™ 4000S supplies the internal logic and its output is connected to the V_{CCD} pin. The V_{CCD} pin must be bypassed to ground via an external capacitor (0.1 μF ; X5R ceramic or better) and must not be connected to anything else.

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Power

5.2 Mode 2: 1.8 V ± 5% external supply

In this mode, the PSoC™ 4000S is powered by an external power supply that must be within the range of 1.71 V to 1.89 V; note that this range needs to include the power supply ripple too. In this mode, the VDD and VCCD pins are shorted together and bypassed. The internal regulator can be disabled in the firmware.

Bypass capacitors must be used from VDDD to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1- μ F range, in parallel with a smaller capacitor (0.1 μ F, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

An example of a bypass scheme is shown in the following diagram.

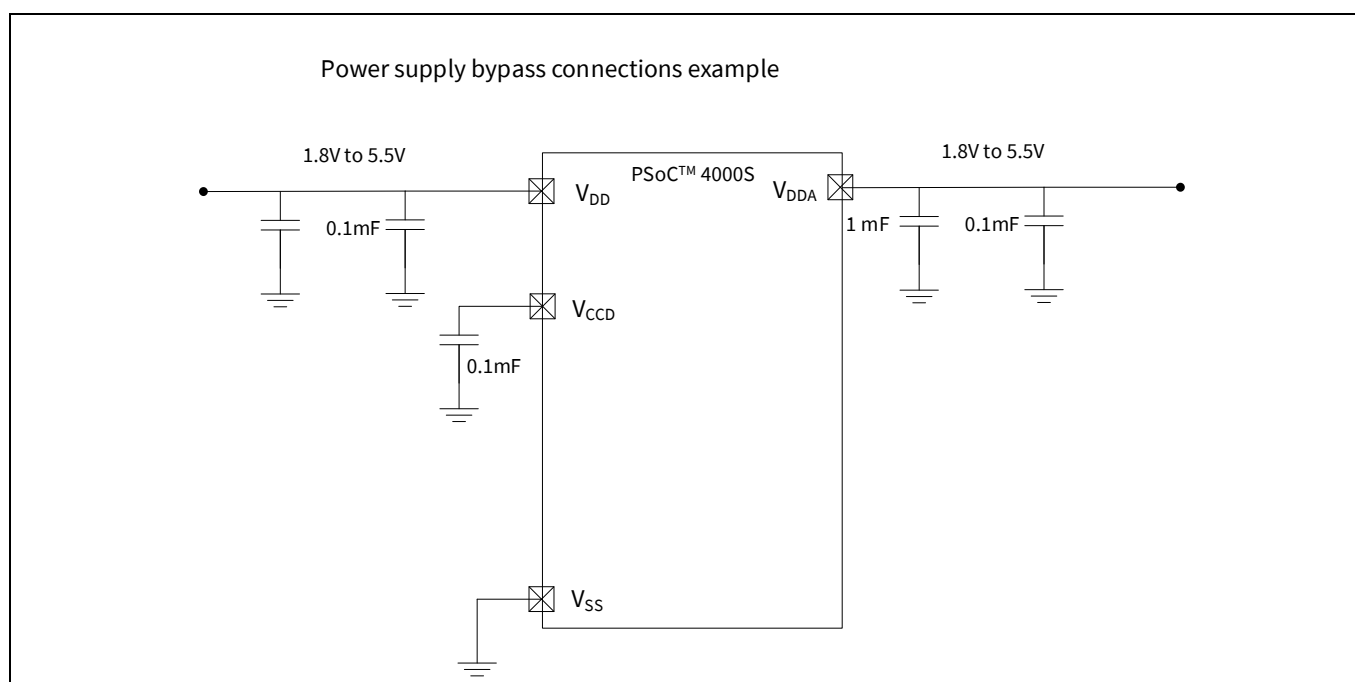


Figure 5 External supply range from 1.8 V to 5.5 V with internal regulator active

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Electrical specifications

6 Electrical specifications

6.1 Absolute maximum ratings

Table 3 Absolute maximum ratings^[1]

| Spec ID# | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|----------|-----------------------------|--|------|-----|-----------------------|------|--------------------------|
| SID1 | V _{DDD_ABS} | Digital supply relative to V _{SS} | -0.5 | - | 6 | V | - |
| SID2 | V _{CCD_ABS} | Direct digital core voltage input relative to V _{SS} | -0.5 | - | 1.95 | | - |
| SID3 | V _{GPIO_ABS} | GPIO voltage | -0.5 | - | V _{DD} + 0.5 | | - |
| SID4 | I _{GPIO_ABS} | Maximum current per GPIO | -25 | - | 25 | mA | - |
| SID5 | I _{GPIO_injection} | GPIO injection current, Max for V _{IH} > V _{DDD} , and Min for V _{IL} < V _{SS} | -0.5 | - | 0.5 | | Current injected per pin |
| BID44 | ESD_HBM | Electrostatic discharge human body model | 2200 | - | - | V | - |
| BID45 | ESD_CDM | Electrostatic discharge charged device model | 500 | - | - | | - |
| BID46 | LU | Pin current for latch-up | -140 | - | 140 | mA | - |

Note

- Usage above the absolute maximum conditions listed in [Table 3](#) may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150°C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.



PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Electrical specifications

6.2 Device level specifications

All specifications are valid for $-40^{\circ}\text{C} \leq T_A \leq 105^{\circ}\text{C}$ and $T_J \leq 125^{\circ}\text{C}$, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 4 DC specifications

Typical values measured at $V_{DD} = 3.3\text{ V}$ and 25°C .

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---------|-----------|---|------|-----|------|---------------|-------------------------------|
| SID53 | V_{DD} | Power supply input voltage | 1.8 | – | 5.5 | V | Internally regulated supply |
| SID255 | V_{DD} | Power supply input voltage ($V_{CCD} = V_{DD} = V_{DDA}$) | 1.71 | – | 1.89 | | Internally unregulated supply |
| SID54 | V_{CCD} | Output voltage (for core logic) | – | 1.8 | – | | – |
| SID55 | C_{EFC} | External regulator voltage bypass | – | 0.1 | – | μF | X5R ceramic or better |
| SID56 | C_{EXC} | Power supply bypass capacitor | – | 1 | – | | X5R ceramic or better |

Active mode, $V_{DD} = 1.8\text{ V}$ to 5.5 V . Typical values measured at $V_{DD} = 3.3\text{ V}$ and 25°C .

| | | | | | | | |
|-------|------------|-----------------------------------|---|-----|-----|----|---|
| SID10 | I_{DD5} | Execute from flash; CPU at 6 MHz | – | 1.2 | 2.0 | mA | – |
| SID16 | I_{DD8} | Execute from flash; CPU at 24 MHz | – | 2.4 | 4.0 | | – |
| SID19 | I_{DD11} | Execute from flash; CPU at 48 MHz | – | 4.6 | 5.9 | | – |

Sleep mode, $V_{DDD} = 1.8\text{ V}$ to 5.5 V (Regulator on)

| | | | | | | | |
|-------|------------|--|---|-----|-----|----|--------|
| SID22 | I_{DD17} | I ² C wakeup WDT, and comparators on | – | 1.1 | 1.6 | mA | 6 MHz |
| SID25 | I_{DD20} | I ² C wakeup, WDT, and comparators on | – | 1.4 | 1.9 | | 12 MHz |

Sleep mode, $V_{DDD} = 1.71\text{ V}$ to 1.89 V (Regulator bypassed)

| | | | | | | | |
|--------|-------------|--|---|-----|-----|----|--------|
| SID28 | I_{DD23} | I ² C wakeup, WDT, and Comparators on | – | 0.7 | 0.9 | mA | 6 MHz |
| SID28A | I_{DD23A} | I ² C wakeup, WDT, and Comparators on | – | 0.9 | 1.1 | mA | 12 MHz |

Deep Sleep mode, $V_{DD} = 1.8\text{ V}$ to 3.6 V (Regulator on)

| | | | | | | | |
|-------|------------|------------------------------------|---|-----|----|---------------|---|
| SID31 | I_{DD26} | I ² C wakeup and WDT on | – | 2.5 | 60 | μA | – |
|-------|------------|------------------------------------|---|-----|----|---------------|---|

Deep Sleep mode, $V_{DD} = 3.6\text{ V}$ to 5.5 V (Regulator on)

| | | | | | | | |
|-------|------------|------------------------------------|---|-----|----|---------------|---|
| SID34 | I_{DD29} | I ² C wakeup and WDT on | – | 2.5 | 60 | μA | – |
|-------|------------|------------------------------------|---|-----|----|---------------|---|

Deep Sleep mode, $V_{DD} = V_{CCD} = 1.71\text{ V}$ to 1.89 V (Regulator bypassed)

| | | | | | | | |
|-------|------------|------------------------------------|---|-----|----|---------------|---|
| SID37 | I_{DD32} | I ² C wakeup and WDT on | – | 2.5 | 60 | μA | – |
|-------|------------|------------------------------------|---|-----|----|---------------|---|

XRES current

| | | | | | | | |
|--------|--------------|------------------------------------|---|---|---|----|---|
| SID307 | I_{DD_XR} | Supply current while XRES asserted | – | 2 | 5 | mA | – |
|--------|--------------|------------------------------------|---|---|---|----|---|

PSoC™ 4000S MCU**Based on Arm® Cortex®-M0+ CPU**

Electrical specifications

Table 5 AC specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|----------------------|------------------------|-----------------------------|-----|-----|-----|------|----------------------------------|
| SID48 | F _{CPU} | CPU frequency | DC | – | 48 | MHz | 1.71 V ≤ V _{DD} ≤ 5.5 V |
| SID49 ^[2] | T _{SLEEP} | Wakeup from Sleep mode | – | 0 | – | μs | – |
| SID50 ^[2] | T _{DEEPSLEEP} | Wakeup from Deep Sleep mode | – | 35 | – | | – |

Note

2. Guaranteed by characterization.

PSoC™ 4000S MCU**Based on Arm® Cortex®-M0+ CPU**

Electrical specifications

6.2.1 GPIO**Table 6 GPIO DC specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|-----------------------|------------------|---|-----------------------|-----|----------------------|--|--|
| SID57 | $V_{IH}^{[3]}$ | Input voltage high threshold | $0.7 \times V_{DDD}$ | - | - | V | CMOS input |
| SID58 | V_{IL} | Input voltage low threshold | - | - | $0.3 \times V_{DDD}$ | | CMOS input |
| SID241 | $V_{IH}^{[3]}$ | LVTTL input, $V_{DDD} < 2.7\text{ V}$ | $0.7 \times V_{DDD}$ | - | - | | - |
| SID242 | V_{IL} | LVTTL input, $V_{DDD} < 2.7\text{ V}$ | - | - | $0.3 \times V_{DDD}$ | | - |
| SID243 | $V_{IH}^{[3]}$ | LVTTL input, $V_{DDD} \geq 2.7\text{ V}$ | 2.0 | - | - | | - |
| SID244 | V_{IL} | LVTTL input, $V_{DDD} \geq 2.7\text{ V}$ | - | - | 0.8 | | - |
| SID59 | V_{OH} | Output voltage high level | $V_{DDD} - 0.6$ | - | - | | $I_{OH} = 4\text{ mA}$ at $3\text{ V } V_{DDD}$ |
| SID60 | V_{OH} | Output voltage high level | $V_{DDD} - 0.5$ | - | - | | $I_{OH} = 1\text{ mA}$ at $3\text{ V } V_{DDD}$ |
| SID61 | V_{OL} | Output voltage low level | - | - | 0.6 | | $I_{OL} = 4\text{ mA}$ at $1.8\text{ V } V_{DDD}$ |
| SID62 | V_{OL} | Output voltage low level | - | - | 0.6 | | $I_{OL} = 10\text{ mA}$ at $3\text{ V } V_{DDD}$ |
| SID62A | V_{OL} | Output voltage low level | - | - | 0.4 | $I_{OL} = 3\text{ mA}$ at $3\text{ V } V_{DDD}$ | |
| SID63 | R_{PULLUP} | Pull-up resistor | 3.5 | 5.6 | 8.5 | k Ω | - |
| SID64 | $R_{PULLDOWN}$ | Pull-down resistor | 3.5 | 5.6 | 8.5 | | - |
| SID65 | I_{IL} | Input leakage current (absolute value) | - | - | 2 | nA | 25°C , $V_{DDD} = 3.0\text{ V}$ |
| SID66 | C_{IN} | Input capacitance | - | - | 7 | pF | - |
| SID67 ^[4] | V_{HYSTTL} | Input hysteresis LVTTL | 25 | 40 | - | mV | $V_{DDD} \geq 2.7\text{ V}$ |
| SID68 ^[4] | $V_{HYSCMOS}$ | Input hysteresis CMOS | $0.05 \times V_{DDD}$ | - | - | | $V_{DD} < 4.5\text{ V}$ |
| SID68A ^[4] | $V_{HYSCMOS5V5}$ | Input hysteresis CMOS | 200 | - | - | | $V_{DD} > 4.5\text{ V}$ |
| SID69 ^[4] | I_{DIODE} | Current through protection diode to V_{DD}/V_{SS} | - | - | 100 | μA | - |
| SID69A ^[4] | I_{TOT_GPIO} | Maximum total source or sink chip current | - | - | 200 | mA | - |

Notes

3. V_{IH} must not exceed $V_{DDD} + 0.2\text{ V}$.
4. Guaranteed by characterization.

PSoC™ 4000S MCU**Based on Arm® Cortex®-M0+ CPU**

Electrical specifications

Table 7 GPIO AC Specifications

(Guaranteed by characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|---------|----------------------|---|-----|-----|------|------|--|
| SID70 | T _{RISEF} | Rise time in fast strong mode | 2 | – | 12 | ns | 3.3 V V _{DDD} , Load = 25 pF |
| SID71 | T _{FALLF} | Fall time in fast strong mode | 2 | – | 12 | | 3.3 V V _{DDD} , Load = 25 pF |
| SID72 | T _{RISES} | Rise time in slow strong mode | 10 | – | 60 | – | 3.3 V V _{DDD} , Load = 25 pF |
| SID73 | T _{FALLS} | Fall time in slow strong mode | 10 | – | 60 | – | 3.3 V V _{DDD} , Load = 25 pF |
| SID74 | F _{GPIOUT1} | GPIO F _{OUT} ; 3.3 V ≤ V _{DDD} ≤ 5.5 V; fast strong mode | – | – | 33 | MHz | 90/10%, 25 pF load, 60/40 duty cycle |
| SID75 | F _{GPIOUT2} | GPIO F _{OUT} ; 1.71 V ≤ V _{DDD} ≤ 3.3 V; fast strong mode | – | – | 16.7 | | 90/10%, 25 pF load, 60/40 duty cycle |
| SID76 | F _{GPIOUT3} | GPIO F _{OUT} ; 3.3 V ≤ V _{DDD} ≤ 5.5 V; slow strong mode | – | – | 7 | | 90/10%, 25 pF load, 60/40 duty cycle |
| SID245 | F _{GPIOUT4} | GPIO F _{OUT} ; 1.71 V ≤ V _{DDD} ≤ 3.3 V; slow strong mode | – | – | 3.5 | | 90/10%, 25 pF load, 60/40 duty cycle |
| SID246 | F _{GPIOIN} | GPIO input operating frequency; 1.71 V ≤ V _{DDD} ≤ 5.5 V | – | – | 48 | | 90/10% V _{IO} |

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Electrical specifications

6.2.2 XRES

Table 8 XRES DC specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|----------------------|---------------|---|----------------------|-----|----------------------|------------|---|
| SID77 | V_{IH} | Input voltage high threshold | $0.7 \times V_{DDD}$ | – | – | V | CMOS Input |
| SID78 | V_{IL} | Input voltage low threshold | – | – | $0.3 \times V_{DDD}$ | | |
| SID79 | R_{PULLUP} | Pull-up resistor | – | 60 | – | k Ω | – |
| SID80 | C_{IN} | Input capacitance | – | – | 7 | pF | – |
| SID81 ^[5] | $V_{HYSXRES}$ | Input voltage hysteresis | – | 100 | – | mV | Typical hysteresis is 200 mV for $V_{DD} > 4.5$ V |
| SID82 | I_{DIODE} | Current through protection diode to V_{DD}/V_{SS} | – | – | 100 | μ A | – |

Table 9 XRES AC specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|-----------------------|------------------|---------------------------------|-----|-----|-----|---------|------------------------|
| SID83 ^[5] | $T_{RESETWIDTH}$ | Reset pulse width | 1 | – | – | μ s | – |
| BID194 ^[5] | $T_{RESETWAKE}$ | Wake-up time from reset release | – | – | 2.7 | ms | – |

Note

5. Guaranteed by characterization.

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Electrical specifications

6.3 Analog peripherals

6.3.1 Comparator

Table 10 Comparator DC specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|---------|----------------------|---|-----|-----|-------------------------|------|-----------------------------------|
| SID84 | V _{OFFSET1} | Input offset voltage, factory trim | - | - | ±10 | mV | - |
| SID85 | V _{OFFSET2} | Input offset voltage, custom trim | - | - | ±4 | | - |
| SID86 | V _{HYST} | Hysteresis when enabled | - | 10 | 35 | | - |
| SID87 | V _{ICM1} | Input common mode voltage in normal mode | 0 | - | V _{DDD} - 0.1 | V | Modes 1 and 2 |
| SID247 | V _{ICM2} | Input common mode voltage in low power mode | 0 | - | V _{DDD} | | - |
| SID247A | V _{ICM3} | Input common mode voltage in ultra low power mode | 0 | - | V _{DDD} - 1.15 | | V _{DDD} ≥ 2.2 V at -40°C |
| SID88 | C _{MRR} | Common mode rejection ratio | 50 | - | - | dB | V _{DDD} ≥ 2.7V |
| SID88A | C _{MRR} | Common mode rejection ratio | 42 | - | - | | V _{DDD} ≤ 2.7V |
| SID89 | I _{CMP1} | Block current, normal mode | - | - | 400 | μA | - |
| SID248 | I _{CMP2} | Block current, low power mode | - | - | 100 | | - |
| SID259 | I _{CMP3} | Block current in ultra low-power mode | - | 6 | 28 | | V _{DDD} ≥ 2.2 V at -40°C |
| SID90 | Z _{CMP} | DC Input impedance of comparator | 35 | - | - | MΩ | - |

Table 11 Comparator AC specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|---------|-----------|---|-----|-----|-----|------|-----------------------------------|
| SID91 | TRESP1 | Response time, Normal mode, 50 mV overdrive | - | 38 | 110 | ns | - |
| SID258 | TRESP2 | Response time, Low-power mode, 50 mV overdrive | - | 70 | 200 | | - |
| SID92 | TRESP3 | Response time, Ultra-low power mode, 200 mV overdrive | - | 2.3 | 15 | μs | V _{DDD} ≥ 2.2 V at -40°C |

PSoC™ 4000S MCU**Based on Arm® Cortex®-M0+ CPU**

Electrical specifications

6.3.2 CSD and IDAC**Table 12 CSD and IDAC specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|-------------|----------------|--|------|-----|-----------------|-------|--|
| SYS.PER#3 | VDD_RIPPLE | Max allowed ripple on power supply, DC to 10 MHz | – | – | ±50 | mV | $V_{DD} > 2\text{ V}$ (with ripple), 25°C T_A , Sensitivity = 0.1 pF |
| SYS.PER#16 | VDD_RIPPLE_1.8 | Max allowed ripple on power supply, DC to 10 MHz | – | – | ±25 | mV | $V_{DD} > 1.75\text{ V}$ (with ripple), 25°C T_A , Parasitic Capacitance (C_p) < 20 pF, Sensitivity ≥ 0.4 pF |
| SID.CSD.BLK | ICSD | Maximum block current | – | – | 4000 | μA | Maximum block current for both IDACs in dynamic (switching) mode including comparators, buffer, and reference generator. |
| SID.CSD#15 | V_{REF} | Voltage reference for CSD and comparator | 0.6 | 1.2 | $V_{DDA} - 0.6$ | V | $V_{DDA} - 0.6$ or 4.4 V, whichever is lower |
| SID.CSD#15A | V_{REF_EXT} | External Voltage reference for CSD and comparator | 0.6 | – | $V_{DDA} - 0.6$ | V | $V_{DDA} - 0.6$ or 4.4 V, whichever is lower |
| SID.CSD#16 | IDAC1IDD | IDAC1 (7-bits) block current | – | – | 1750 | μA | – |
| SID.CSD#17 | IDAC2IDD | IDAC2 (7-bits) block current | – | – | 1750 | μA | – |
| SID308 | VCSD | Voltage range of operation | 1.71 | – | 5.5 | V | 1.8 V ± 5% or 1.8 V to 5.5 V |
| SID308A | $V_{COMPIDAC}$ | Voltage compliance range of IDAC | 0.6 | – | $V_{DDA} - 0.6$ | V | $V_{DDA} - 0.6$ or 4.4 V, whichever is lower |
| SID309 | IDAC1DNL | DNL | –1 | – | 1 | LSB | – |
| SID310 | IDAC1INL | INL | –2 | – | 2 | LSB | INL is ±5.5 LSB for $V_{DDA} < 2\text{ V}$ |
| SID311 | IDAC2DNL | DNL | –1 | – | 1 | LSB | – |
| SID312 | IDAC2INL | INL | –2 | – | 2 | LSB | INL is ±5.5 LSB for $V_{DDA} < 2\text{ V}$ |
| SID313 | SNR | Ratio of counts of finger to noise. Guaranteed by characterization | 5 | – | – | Ratio | Capacitance range of 5 pF to 35 pF, 0.1 pF sensitivity. All use cases. $V_{DDA} > 2\text{ V}$. |
| SID314 | IDAC1CRT1 | Output current of IDAC1 (7 bits) in low range | 4.2 | – | 5.4 | μA | LSB = 37.5 nA typ. |
| SID314A | IDAC1CRT2 | Output current of IDAC1 (7 bits) in medium range | 34 | – | 41 | μA | LSB = 300 nA typ. |

PSoC™ 4000S MCU**Based on Arm® Cortex®-M0+ CPU**

Electrical specifications

Table 12 CSD and IDAC specifications (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---------|------------|---|-----|-----|------|------|---|
| SID314B | IDAC1CRT3 | Output current of IDAC1 (7 bits) in high range | 275 | – | 330 | μA | LSB = 2.4 μA typ |
| SID314C | IDAC1CRT12 | Output current of IDAC1 (7 bits) in low range, 2X mode | 8 | – | 10.5 | μA | LSB = 75 nA typ |
| SID314D | IDAC1CRT22 | Output current of IDAC1 (7 bits) in medium range, 2X mode | 69 | – | 82 | μA | LSB = 600 nA typ |
| SID314E | IDAC1CRT32 | Output current of IDAC1 (7 bits) in high range, 2X mode | 540 | – | 660 | μA | LSB = 4.8 μA typ |
| SID315 | IDAC2CRT1 | Output current of IDAC2 (7 bits) in low range | 4.2 | – | 5.4 | μA | LSB = 37.5 nA typ |
| SID315A | IDAC2CRT2 | Output current of IDAC2 (7 bits) in medium range | 34 | – | 41 | μA | LSB = 300 nA typ |
| SID315B | IDAC2CRT3 | Output current of IDAC2 (7 bits) in high range | 275 | – | 330 | μA | LSB = 2.4 μA typ |
| SID315C | IDAC2CRT12 | Output current of IDAC2 (7 bits) in low range, 2X mode | 8 | – | 10.5 | μA | LSB = 75 nA typ |
| SID315D | IDAC2CRT22 | Output current of IDAC2 (7 bits) in medium range, 2X mode | 69 | – | 82 | μA | LSB = 600 nA typ |
| SID315E | IDAC2CRT32 | Output current of IDAC2 (7 bits) in high range, 2X mode | 540 | – | 660 | μA | LSB = 4.8 μA typ |
| SID315F | IDAC3CRT13 | Output current of IDAC in 8-bit mode in low range | 8 | – | 10.5 | μA | LSB = 37.5 nA typ |
| SID315G | IDAC3CRT23 | Output current of IDAC in 8-bit mode in medium range | 69 | – | 82 | μA | LSB = 300 nA typ |
| SID315H | IDAC3CRT33 | Output current of IDAC in 8-bit mode in high range | 540 | – | 660 | μA | LSB = 2.4 μA typ |
| SID320 | IDACOFFSET | All zeroes input | – | – | 1 | LSB | Polarity set by Source or Sink. Offset is 2 LSBs for 37.5 nA/LSB mode |
| SID321 | IDACGAIN | Full-scale error less offset | – | – | ±10 | % | – |

PSoC™ 4000S MCU**Based on Arm® Cortex®-M0+ CPU**

Electrical specifications

Table 12 CSD and IDAC specifications (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---------|---------------|---|-----|-----|-----|------|---|
| SID322 | IDACMISMATCH1 | Mismatch between IDAC1 and IDAC2 in Low mode | – | – | 9.2 | LSB | LSB = 37.5 nA typ |
| SID322A | IDACMISMATCH2 | Mismatch between IDAC1 and IDAC2 in Medium mode | – | – | 5.6 | LSB | LSB = 300 nA typ |
| SID322B | IDACMISMATCH3 | Mismatch between IDAC1 and IDAC2 in High mode | – | – | 6.8 | LSB | LSB = 2.4 μA typ |
| SID323 | IDACSET8 | Settling time to 0.5 LSB for 8-bit IDAC | – | – | 10 | μs | Full-scale transition. No external load |
| SID324 | IDACSET7 | Settling time to 0.5 LSB for 7-bit IDAC | – | – | 10 | μs | Full-scale transition. No external load |
| SID325 | CMOD | External modulator capacitor | – | 2.2 | – | nF | 5-V rating, X7R or NP0 cap |

PSoC™ 4000S MCU**Based on Arm® Cortex®-M0+ CPU**

Electrical specifications

6.3.3 10-bit CAPSENSE™ ADC**Table 13 10-bit CAPSENSE™ ADC specifications**

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|----------|-----------|---|------------------|-----|------------------|------|---|
| SIDA94 | A_RES | Resolution | – | – | 10 | bits | Auto-zeroing is required every millisecond |
| SIDA95 | A_CHNLS_S | Number of channels - single ended | – | – | 16 | | Defined by AMUX Bus |
| SIDA97 | A-MONO | Monotonicity | – | – | – | Yes | – |
| SIDA98 | A_GAINERR | Gain error | – | – | ±2 | % | In V _{REF} (2.4 V) mode with V _{DDA} bypass capacitance of 10 μF |
| SIDA99 | A_OFFSET | Input offset voltage | – | – | 3 | mV | In V _{REF} (2.4 V) mode with V _{DDA} bypass capacitance of 10 μF |
| SIDA100 | A_ISAR | Current consumption | – | – | 0.25 | mA | – |
| SIDA101 | A_VINS | Input voltage range - single ended | V _{SSA} | – | V _{DDA} | V | – |
| SIDA103 | A_INRES | Input resistance | – | 2.2 | – | KΩ | – |
| SIDA104 | A_INCAP | Input capacitance | – | 20 | – | pF | – |
| SIDA106 | A_PSRR | Power supply rejection ratio | – | 60 | – | dB | In V _{REF} (2.4 V) mode with V _{DDA} bypass capacitance of 10 μF |
| SIDA107 | A_TACQ | Sample acquisition time | – | 1 | – | μs | – |
| SIDA108 | A_CONV8 | Conversion time for 8-bit resolution at conversion rate = Fhclk/(2 ^{N+2}). Clock frequency = 48 MHz. | – | – | 21.3 | μs | Does not include acquisition time. Equivalent to 44.8 ksp/s including acquisition time. |
| SIDA108A | A_CONV10 | Conversion time for 10-bit resolution at conversion rate = Fhclk/(2 ^{N+2}). Clock frequency = 48 MHz. | – | – | 85.3 | μs | Does not include acquisition time. Equivalent to 11.6 ksp/s including acquisition time. |
| SIDA109 | A_SND | Signal-to-noise and Distortion ratio (SINAD) | – | 61 | – | dB | With 10-Hz input sine wave, external 2.4-V reference, V _{REF} (2.4 V) mode |
| SIDA110 | A_BW | Input bandwidth without aliasing | – | – | 22.4 | kHz | 8-bit resolution |

PSoC™ 4000S MCU**Based on Arm® Cortex®-M0+ CPU**

Electrical specifications

Table 13 10-bit CAPSENSE™ ADC specifications (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|---------|-----------|---------------------------------------|-----|-----|-----|------|--|
| SIDA111 | A_INL | Integral Non Linearity. 1 ksps | – | – | 2 | LSB | V _{REF} = 2.4 V or greater |
| SIDA112 | A_DNL | Differential Non Linearity. 1 ksps | – | – | 1 | LSB | – |

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Electrical specifications

6.4 Digital peripherals

6.4.1 Timer counter pulse-width modulator (TCPWM)

Table 14 TCPWM specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|--------------|-----------------------|-------------------------------------|------------------|-----|----------------|------|--|
| SID.TCPWM.1 | ITCPWM1 | Block current consumption at 3 MHz | – | – | 45 | μA | All modes (TCPWM) |
| SID.TCPWM.2 | ITCPWM2 | Block current consumption at 12 MHz | – | – | 155 | | All modes (TCPWM) |
| SID.TCPWM.2A | ITCPWM3 | Block current consumption at 48 MHz | – | – | 650 | | All modes (TCPWM) |
| SID.TCPWM.3 | TCPWM _{FREQ} | Operating frequency | – | – | F _c | MHz | F _c max = CLK_SYS Maximum = 48 MHz |
| SID.TCPWM.4 | TPWM _{ENEXT} | Input trigger pulse width | 2/F _c | – | – | ns | For all trigger events ^[6] |
| SID.TCPWM.5 | TPWM _{EXT} | Output trigger pulse widths | 2/F _c | – | – | | Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs |
| SID.TCPWM.5A | TC _{RES} | Resolution of counter | 1/F _c | – | – | | Minimum time between successive counts |
| SID.TCPWM.5B | PWM _{RES} | PWM resolution | 1/F _c | – | – | | Minimum pulse width of PWM Output |
| SID.TCPWM.5C | Q _{RES} | Quadrature inputs resolution | 1/F _c | – | – | | Minimum pulse width between Quadrature phase inputs |

Note

6. Trigger events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Electrical specifications

6.4.2 I²C

Table 15 Fixed I²C DC specifications^[7]

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|---------|-------------------|---|-----|-----|-----|------|------------------------|
| SID149 | I _{I2C1} | Block current consumption at 100 kHz | – | – | 50 | μA | – |
| SID150 | I _{I2C2} | Block current consumption at 400 kHz | – | – | 135 | | – |
| SID151 | I _{I2C3} | Block current consumption at 1 Mbps | – | – | 310 | | – |
| SID152 | I _{I2C4} | I ² C enabled in Deep Sleep mode | – | – | 1.4 | | – |

Table 16 Fixed I²C AC specifications^[7]

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|---------|-------------------|-------------|-----|-----|-----|-------|------------------------|
| SID153 | F _{I2C1} | Bit rate | – | – | 1 | Msp/s | – |

Note

7. Guaranteed by characterization.

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Electrical specifications

6.4.3 SPI

Table 17 SPI DC specifications^[7]

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|---------|-----------|-------------------------------------|-----|-----|-----|------|------------------------|
| SID163 | ISPI1 | Block current consumption at 1 Mbps | - | - | 360 | μA | - |
| SID164 | ISPI2 | Block current consumption at 4 Mbps | - | - | 560 | | - |
| SID165 | ISPI3 | Block current consumption at 8 Mbps | - | - | 600 | | - |

Table 18 SPI AC specifications^[7]

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|---------|-----------|---|-----|-----|-----|------|------------------------|
| SID166 | FSPI | SPI operating frequency (Master; 6X Oversampling) | - | - | 8 | MHz | - |

Fixed SPI Master mode AC specifications

| | | | | | | | |
|--------|------|---|----|---|----|----|----------------------------------|
| SID167 | TDMO | MOSI valid after SClOCK driving edge | - | - | 15 | ns | - |
| SID168 | TDSI | MISO valid before SClOCK capturing edge | 20 | - | - | | Full clock, late MISO sampling |
| SID169 | THMO | Previous MOSI data hold time | 0 | - | - | | Referred to Slave capturing edge |

Fixed SPI Slave mode AC specifications

| | | | | | | | |
|---------|-----------|---|-----|---|---------------------------|----|-----------------------|
| SID170 | TDMI | MOSI valid before SClOCK capturing edge | 40 | - | - | ns | - |
| SID171 | TDSO | MISO valid after SClOCK driving edge | - | - | $42 + (3 \times T_{cpu})$ | | $T_{CPU} = 1/F_{CPU}$ |
| SID171A | TDSO_EXT | MISO valid after SClOCK driving edge in External Clock mode | - | - | 48 | | - |
| SID172 | THSO | Previous MISO data hold time | 0 | - | - | | - |
| SID172A | TSSELSSCK | SSEL valid to first SCK valid edge | 100 | - | - | ns | - |

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Electrical specifications

6.4.4 UART

Table 19 UART DC specifications^[8]

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|---------|-------------|--|-----|-----|-----|------|------------------------|
| SID160 | I_{UART1} | Block current consumption at 100 Kbps | - | - | 55 | μA | - |
| SID161 | I_{UART2} | Block current consumption at 1000 Kbps | - | - | 312 | μA | - |

Table 20 UART AC specifications^[8]

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|---------|------------|-------------|-----|-----|-----|------|------------------------|
| SID162 | F_{UART} | Bit rate | - | - | 1 | Mbps | - |

6.4.5 LCD direct drive

Table 21 LCD direct drive DC specifications^[8]

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|---------|----------------|---|-----|-----|------|------|-------------------------------------|
| SID154 | I_{LCDLOW} | Operating current in low power mode | - | 5 | - | μA | 16 × 4 small segment disp. at 50 Hz |
| SID155 | C_{LCDCAP} | LCD capacitance per segment/common driver | - | 500 | 5000 | pF | - |
| SID156 | LCD_{OFFSET} | Long-term segment offset | - | 20 | - | mV | - |
| SID157 | I_{LCDOP1} | LCD system operating current $V_{bias} = 5 V$ | - | 2 | - | mA | 32 × 4 segments. 50 Hz. 25°C |
| SID158 | I_{LCDOP2} | LCD system operating current $V_{bias} = 3.3 V$ | - | 2 | - | | 32 × 4 segments. 50 Hz. 25°C |

Table 22 LCD direct drive AC specifications^[8]

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|---------|-----------|----------------|-----|-----|-----|------|------------------------|
| SID159 | F_{LCD} | LCD frame rate | 10 | 50 | 150 | Hz | - |

Note

8. Guaranteed by characterization.

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Electrical specifications

6.5 Memory

6.5.1 Flash

Table 23 Flash DC specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|---------|-----------------|---------------------------|------|-----|-----|------|--------------------|
| SID173 | V _{PE} | Erase and program voltage | 1.71 | – | 5.5 | V | – |

Table 24 Flash AC specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/conditions |
|-------------------------|--|--|-------|-----|-----|---------|--------------------------------|
| SID174 | T _{ROWWRITE} ^[9] | Row (block) write time (erase and program) | – | – | 20 | ms | Row (block) = 128 bytes |
| SID175 | T _{ROWERASE} ^[9] | Row erase time | – | – | 16 | | – |
| SID176 | T _{ROWPROGRAM} ^[9] | Row program time after erase | – | – | 4 | | – |
| SID178 | T _{BULKERASE} ^[9] | Bulk erase time (32 KB) | – | – | 35 | | – |
| SID180 ^[10] | T _{DEVPROG} ^[9] | Total device program time | – | – | 7 | Seconds | – |
| SID181 ^[10] | F _{END} | Flash endurance | 100 K | – | – | Cycles | – |
| SID182 ^[10] | F _{RET} | Flash retention. T _A ≤ 55°C, 100 K P/E cycles. | 20 | – | – | Years | – |
| SID182A ^[10] | – | Flash retention. T _A ≤ 85°C, 10 K P/E cycles. | 10 | – | – | | – |
| SID182B ^[10] | F _{RETQ} | Flash retention. T _A ≤ 105°C, 10 K P/E cycles, ≤ three years at T _A ≥ 85 °C. | 10 | – | 20 | | Guaranteed by Characterization |
| SID256 | TWS48 | Number of Wait states at 48 MHz | 2 | – | – | – | CPU execution from Flash |
| SID257 | TWS24 | Number of Wait states at 24 MHz | 1 | – | – | – | CPU execution from Flash |

Notes

9. It can take as much as 20 milliseconds to write to flash. During this time the device should not be Reset, or Flash operations may be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

10. Guaranteed by characterization.

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Electrical specifications

6.6 System resources

6.6.1 Power-on reset (POR)

Table 25 Power-on reset (PRES)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|------------------------|-----------------------|------------------------|------|-----|-----|------|----------------------------|
| SID.CLK#6 | SR_POWER_UP | Power supply slew rate | 1 | – | 67 | V/ms | At power-up and power-down |
| SID185 ^[11] | V _{RISEIPOR} | Rising trip voltage | 0.80 | – | 1.5 | V | – |
| SID186 ^[11] | V _{FALLIPOR} | Falling trip voltage | 0.70 | – | 1.4 | | – |

Table 26 Brown-out detect (BOD) for V_{CCD}

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|------------------------|------------------------|--|------|-----|------|------|------------------------|
| SID190 ^[11] | V _{FALLPPOR} | BOD trip voltage in active and sleep modes | 1.48 | – | 1.62 | V | – |
| SID192 ^[11] | V _{FALLDPSLP} | BOD trip voltage in Deep Sleep | 1.11 | – | 1.5 | | – |

6.6.2 SWD interface

Table 27 SWD interface specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|-------------------------|--------------|---|-----------------|-----|----------------|------|--|
| SID213 | F_SWDCCLK1 | $3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ | – | – | 14 | MHz | SWDCCLK \leq 1/3 CPU clock frequency |
| SID214 | F_SWDCCLK2 | $1.71\text{ V} \leq V_{DD} \leq 3.3\text{ V}$ | – | – | 7 | | SWDCCLK \leq 1/3 CPU clock frequency |
| SID215 ^[11] | T_SWDI_SETUP | $T = 1/f\text{ SWDCCLK}$ | $0.25 \times T$ | – | – | ns | – |
| SID216 ^[11] | T_SWDI_HOLD | $T = 1/f\text{ SWDCCLK}$ | $0.25 \times T$ | – | – | | – |
| SID217 ^[11] | T_SWDO_VALID | $T = 1/f\text{ SWDCCLK}$ | – | – | $0.5 \times T$ | | – |
| SID217A ^[11] | T_SWDO_HOLD | $T = 1/f\text{ SWDCCLK}$ | 1 | – | – | | – |

Notes

11.Guaranteed by characterization.

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Electrical specifications

6.6.3 Internal main oscillator (IMO)

Table 28 IMO DC specifications

(Guaranteed by design)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|---------|------------|---------------------------------|-----|-----|-----|------|------------------------|
| SID218 | I_{IMO1} | IMO operating current at 48 MHz | – | – | 250 | μA | – |
| SID219 | I_{IMO2} | IMO operating current at 24 MHz | – | – | 180 | μA | – |

Table 29 IMO AC specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|-----------------------------|------------------|---|-----|-----|-------|------|---|
| SID223 ^[13] | $F_{IMOTOL1}$ | Frequency variation at 24, 32, and 48 MHz (trimmed) | – | – | ±2.0 | % | At –40°C to 85°C, for industrial temperature range and original extended industrial range parts |
| SID223A ^[12, 13] | | | – | – | ±2.5 | % | At –40°C to 105°C, for all extended industrial temperature range parts |
| SID223B ^[12, 13] | | | – | – | ±2.0 | % | At –30°C to 105°C, for enhanced IMO extended industrial temperature range parts |
| SID223C ^[12, 13] | | | – | – | ±1.5 | % | At –20°C to 105°C, for enhanced IMO extended industrial temperature range parts |
| SID223D ^[12, 13] | | | – | – | ±1.25 | % | At 0°C to 85°C, for enhanced IMO extended industrial temperature range parts |
| SID226 | $T_{STARTIMO}$ | IMO startup time | – | – | 7 | μs | – |
| SID228 | $T_{JITRMSIMO2}$ | RMS jitter at 24 MHz | – | 145 | – | ps | – |

Notes

12. The enhanced IMO extended temperature range parts replace the original extended industrial temperature range parts. For details on how to identify enhanced IMO extended temperature range parts, please refer to [KBA235887](#).

13. Evaluated by characterization. Does not take into account soldering or board-level effects.

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Electrical specifications

6.6.4 Internal low-speed oscillator (ILO)

Table 30 ILO DC specifications

(Guaranteed by design)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|------------------------|-------------------|-----------------------|-----|-----|------|------|------------------------|
| SID231 ^[14] | I _{ILO1} | ILO operating current | – | 0.3 | 1.05 | μA | – |

Table 31 ILO AC specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|------------------------|------------------------|---------------------|-----|-----|-----|------|------------------------|
| SID234 ^[14] | T _{STARTILO1} | ILO startup time | – | – | 2 | ms | – |
| SID236 ^[14] | T _{ILODUTY} | ILO duty cycle | 40 | 50 | 60 | % | – |
| SID237 | F _{ILOTRIM1} | ILO frequency range | 20 | 40 | 80 | kHz | – |

6.6.5 Watch crystal oscillator (WCO)

Table 32 Watch crystal oscillator (WCO) specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|---------|-----------|-------------------------------------|-----|--------|------|------|------------------------|
| SID398 | FWCO | Crystal frequency | – | 32.768 | – | kHz | – |
| SID399 | FTOL | Frequency tolerance | – | 50 | 250 | ppm | With 20-ppm crystal |
| SID400 | ESR | Equivalent series resistance | – | 50 | – | kΩ | – |
| SID401 | PD | Drive level | – | – | 1 | μW | – |
| SID402 | TSTART | Startup time | – | – | 500 | ms | – |
| SID403 | CL | Crystal load capacitance | 6 | – | 12.5 | pF | – |
| SID404 | C0 | Crystal shunt capacitance | – | 1.35 | – | pF | – |
| SID405 | IWCO1 | Operating current (high power mode) | – | – | 8 | μA | – |
| SID406 | IWCO2 | Operating current (low power mode) | – | – | 1 | μA | – |

Notes

14. Guaranteed by characterization.

15. For industrial temperature range parts, the maximum temperature is 85°C.

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Electrical specifications

6.6.6 External clock

Table 33 External clock specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|------------------------|------------|------------------------------------|-----|-----|-----|------|------------------------|
| SID305 ^[16] | ExtClkFreq | External clock input frequency | 0 | – | 48 | MHz | – |
| SID306 ^[16] | ExtClkDuty | Duty cycle; measured at $V_{DD/2}$ | 45 | – | 55 | % | – |

6.6.7 Clock

Table 34 Clock specs

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|------------------------|-----------------|------------------------------------|-----|-----|-----|---------|------------------------|
| SID262 ^[16] | $T_{CLKSWITCH}$ | System clock source switching time | 3 | – | 4 | Periods | – |

6.6.8 Smart I/O Pass-through Time

Table 35 Smart I/O pass-through time (Delay in Bypass Mode)

| Spec ID | Parameter | Description | Min | Typ | Max | Unit | Details/ conditions |
|---------|------------|---|-----|-----|-----|------|------------------------|
| SID252 | PRG_BYPASS | Max delay added by Smart I/O in Bypass Mode | – | – | 1.6 | ns | – |

Note

16. Guaranteed by characterization.

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Ordering information

7 Ordering information

The PSoC™ 4000S part numbers and features are listed in [Table 36](#).

Table 36 PSoC™ 4000S ordering information

| Category | Product | Features | | | | | | | | | | | Package | | | | | Temperature range | | | |
|------------------|-------------------|---------------------|------------|-----------|--------------|-----------|----------------|----------------|----------------|--------------|------------|------------|---------|-----------------------|------------|------------|-------------|-------------------|----------------|---------------|----------------|
| | | Max CPU speed (MHz) | Flash (KB) | SRAM (KB) | Opamp (CTBm) | CAPSENSE™ | 10-bit CSD ADC | 12-bit SAR ADC | LP Comparators | TCPWM Blocks | SCB Blocks | Smart I/Os | GPIO | WLCSP (0.35-mm pitch) | 24-pin QFN | 32-pin QFN | 32-pin TQFP | | 40-pin QFN | 48-pin TQFP | |
| 4024 | CY8C4024FNI-S402T | 24 | 16 | 2 | 0 | 0 | 1 | 0 | 2 | 5 | 2 | 8 | 21 | ✓ | - | - | - | - | - | -40°C to 85°C | |
| | CY8C4024LQI-S401 | 24 | 16 | 2 | 0 | 0 | 1 | 0 | 2 | 5 | 2 | 8 | 19 | - | ✓ | - | - | - | - | | |
| | CY8C4024LQI-S402 | 24 | 16 | 2 | 0 | 0 | 1 | 0 | 2 | 5 | 2 | 16 | 27 | - | - | ✓ | - | - | - | | |
| | CY8C4024AXI-S402 | 24 | 16 | 2 | 0 | 0 | 1 | 0 | 2 | 5 | 2 | 16 | 27 | - | - | - | ✓ | - | - | | |
| | CY8C4024LQI-S403 | 24 | 16 | 2 | 0 | 0 | 1 | 0 | 2 | 5 | 2 | 16 | 34 | - | - | - | - | ✓ | - | | |
| | CY8C4024AZI-S403 | 24 | 16 | 2 | 0 | 0 | 1 | 0 | 2 | 5 | 2 | 16 | 36 | - | - | - | - | - | ✓ | | |
| | CY8C4024FNI-S412T | 24 | 16 | 2 | 0 | 1 | 1 | 0 | 2 | 5 | 2 | 8 | 21 | ✓ | - | - | - | - | - | | |
| | CY8C4024LQI-S411 | 24 | 16 | 2 | 0 | 1 | 1 | 0 | 2 | 5 | 2 | 8 | 19 | - | ✓ | - | - | - | - | | |
| | CY8C4024LQI-S412 | 24 | 16 | 2 | 0 | 1 | 1 | 0 | 2 | 5 | 2 | 16 | 27 | - | - | ✓ | - | - | - | | |
| | CY8C4024AXI-S412 | 24 | 16 | 2 | 0 | 1 | 1 | 0 | 2 | 5 | 2 | 16 | 27 | - | - | - | ✓ | - | - | | |
| | CY8C4024LQI-S413 | 24 | 16 | 2 | 0 | 1 | 1 | 0 | 2 | 5 | 2 | 16 | 34 | - | - | - | - | ✓ | - | | |
| | CY8C4024AZI-S413 | 24 | 16 | 2 | 0 | 1 | 1 | 0 | 2 | 5 | 2 | 16 | 36 | - | - | - | - | - | ✓ | | |
| CY8C4024AZQ-S413 | 24 | 16 | 2 | 0 | 1 | 1 | 0 | 2 | 5 | 2 | 16 | 36 | - | - | - | - | - | ✓ | -40°C to 105°C | | |
| 4025 | CY8C4025FNI-S402T | 24 | 32 | 4 | 0 | 0 | 1 | 0 | 2 | 5 | 2 | 8 | 21 | ✓ | - | - | - | - | - | -40°C to 85°C | |
| | CY8C4025LQI-S401 | 24 | 32 | 4 | 0 | 0 | 1 | 0 | 2 | 5 | 2 | 8 | 19 | - | ✓ | - | - | - | - | | |
| | CY8C4025LQI-S402 | 24 | 32 | 4 | 0 | 0 | 1 | 0 | 2 | 5 | 2 | 16 | 27 | - | - | ✓ | - | - | - | | |
| | CY8C4025AXI-S402 | 24 | 32 | 4 | 0 | 0 | 1 | 0 | 2 | 5 | 2 | 16 | 27 | - | - | - | ✓ | - | - | | |
| | CY8C4025LQI-S403 | 24 | 32 | 4 | 0 | 0 | 1 | 0 | 2 | 5 | 2 | 16 | 34 | - | - | - | - | ✓ | - | | |
| | CY8C4025AZI-S403 | 24 | 32 | 4 | 0 | 0 | 1 | 0 | 2 | 5 | 2 | 16 | 36 | - | - | - | - | - | ✓ | | |
| | CY8C4025AZQ-S403 | 24 | 32 | 4 | 0 | 0 | 1 | 0 | 2 | 5 | 2 | 16 | 36 | - | - | - | - | - | ✓ | | -40°C to 105°C |
| | CY8C4025FNI-S412T | 24 | 32 | 4 | 0 | 1 | 1 | 0 | 2 | 5 | 2 | 8 | 21 | ✓ | - | - | - | - | - | | |
| | CY8C4025LQI-S411 | 24 | 32 | 4 | 0 | 1 | 1 | 0 | 2 | 5 | 2 | 8 | 19 | - | ✓ | - | - | - | - | | |
| | CY8C4025LQI-S412 | 24 | 32 | 4 | 0 | 1 | 1 | 0 | 2 | 5 | 2 | 16 | 27 | - | - | ✓ | - | - | - | | |
| | CY8C4025AXI-S412 | 24 | 32 | 4 | 0 | 1 | 1 | 0 | 2 | 5 | 2 | 16 | 27 | - | - | - | ✓ | - | - | | |
| | CY8C4025LQI-S413 | 24 | 32 | 4 | 0 | 1 | 1 | 0 | 2 | 5 | 2 | 16 | 34 | - | - | - | - | ✓ | - | | |
| CY8C4025AZI-S413 | 24 | 32 | 4 | 0 | 1 | 1 | 0 | 2 | 5 | 2 | 16 | 36 | - | - | - | - | - | ✓ | | | |
| CY8C4025AZQ-S413 | 24 | 32 | 4 | 0 | 1 | 1 | 0 | 2 | 5 | 2 | 16 | 36 | - | - | - | - | - | ✓ | -40°C to 105°C | | |
| 4045 | CY8C4045FNI-S412T | 48 | 32 | 4 | 0 | 1 | 1 | 0 | 2 | 5 | 2 | 8 | 21 | ✓ | - | - | - | - | - | -40°C to 85°C | |
| | CY8C4045LQI-S411 | 48 | 32 | 4 | 0 | 1 | 1 | 0 | 2 | 5 | 2 | 8 | 19 | - | ✓ | - | - | - | - | | |
| | CY8C4045LQI-S412 | 48 | 32 | 4 | 0 | 1 | 1 | 0 | 2 | 5 | 2 | 16 | 27 | - | - | ✓ | - | - | - | | |
| | CY8C4045AXI-S412 | 48 | 32 | 4 | 0 | 1 | 1 | 0 | 2 | 5 | 2 | 16 | 27 | - | - | - | ✓ | - | - | | |
| | CY8C4045LQI-S413 | 48 | 32 | 4 | 0 | 1 | 1 | 0 | 2 | 5 | 2 | 16 | 34 | - | - | - | - | ✓ | - | | |
| | CY8C4045AZI-S413 | 48 | 32 | 4 | 0 | 1 | 1 | 0 | 2 | 5 | 2 | 16 | 36 | - | - | - | - | - | ✓ | | |
| CY8C4045AZQ-S413 | 48 | 32 | 4 | 0 | 1 | 1 | 0 | 2 | 5 | 2 | 16 | 36 | - | - | - | - | - | ✓ | -40°C to 105°C | | |

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

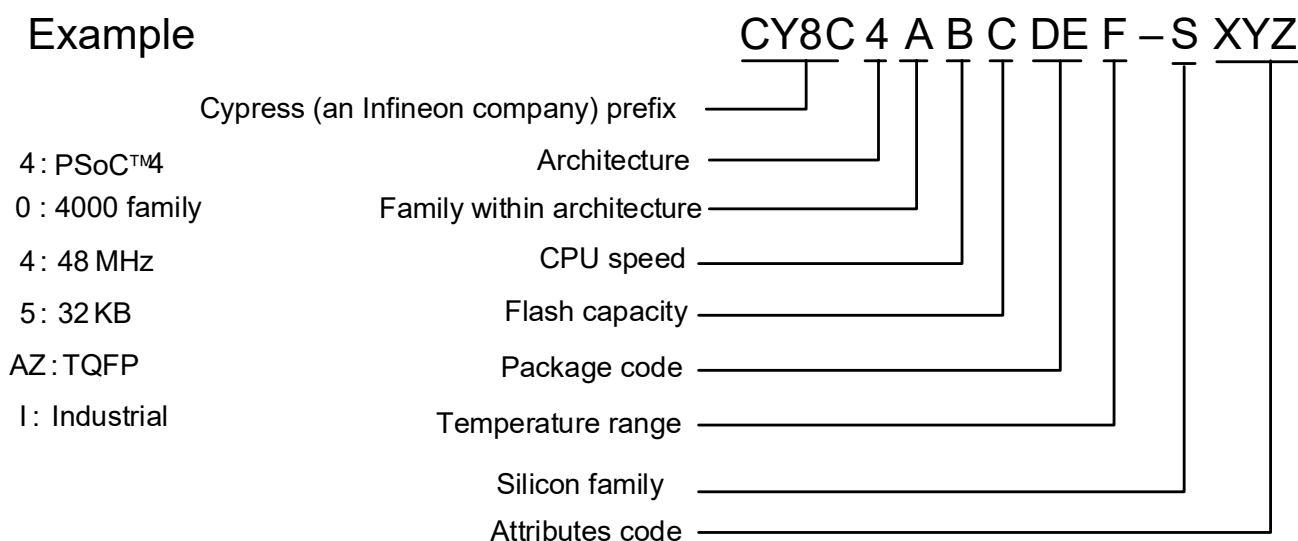
Ordering information

The nomenclature used in the preceding table is based on the following part numbering convention:

| Field | Description | Values | Meaning |
|-------|-------------------|---------|--|
| CY8C | Prefix | – | – |
| 4 | Architecture | 4 | PSoC™ 4 |
| A | Family | 0 | 4000 Family |
| B | CPU speed | 2 | 24 MHz |
| | | 4 | 48 MHz |
| C | Flash capacity | 4 | 16 KB |
| | | 5 | 32 KB |
| | | 6 | 64 KB |
| | | 7 | 128 KB |
| DE | Package code | AX | TQFP (0.8-mm pitch) |
| | | AZ | TQFP (0.5-mm pitch) |
| | | LQ | QFN |
| | | PV | SSOP |
| | | FN | CSP |
| F | Temperature range | I | Industrial |
| | | Q | Extended Industrial |
| S | Series designator | S | PSoC™ 4 S-Series |
| | | M | PSoC™ 4 M-Series |
| | | L | PSoC™ 4 L-Series |
| | | BL | PSoC™ 4 BLE-Series |
| XYZ | Attributes code | 000-999 | Code of feature set in the specific family |

The following is an example of a part number:

Example



PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Packaging

8 Packaging

The PSoC™ 4000S is offered in 48LD TQFP, 40L QFN, 32 LEAD QFN, 24L QFN, 32LD TQFP, and 25-ball WLCSP packages.

Package dimensions and Infineon drawing numbers are in the following table.

Table 37 Package list

| Spec ID | Package | Description | Package drawing |
|---------|---------------|---|-----------------|
| BID20 | 48LD TQFP | 7 × 7 × 1.4 mm height with 0.5-mm pitch | 51-85135 |
| BID27 | 40L QFN | 6 × 6 × 0.6 mm height with 0.5-mm pitch | 001-80659 |
| BID34A | 32 LEAD QFN | 5 × 5 × 0.6 mm height with 0.5-mm pitch | 001-42168 |
| BID34 | 24L QFN | 4 × 4 × 0.6 mm height with 0.5-mm pitch | 001-13937 |
| BID34G | 32LD TQFP | 7 × 7 × 1.4 mm height with 0.8-mm pitch | 51-85088 |
| BID34F | 25-ball WLCSP | 2.02 × 1.93 × 0.48 mm height with 0.35-mm pitch | 002-09957 |

Table 38 Package thermal characteristics

| Parameter | Description | Package | Min | Typ | Max | Unit |
|-----------------|--------------------------------|---------------|-----|------|-----|------|
| T _A | Operating ambient temperature | – | –40 | 25 | 105 | °C |
| T _J | Operating junction temperature | – | –40 | – | 125 | °C |
| T _{JA} | Package θ _{JA} | 48LD TQFP | – | 73.5 | – | °C/W |
| T _{JC} | Package θ _{JC} | 48LD TQFP | – | 33.5 | – | °C/W |
| T _{JA} | Package θ _{JA} | 40L QFN | – | 17.8 | – | °C/W |
| T _{JC} | Package θ _{JC} | 40L QFN | – | 2.8 | – | °C/W |
| T _{JA} | Package θ _{JA} | 32 LEAD QFN | – | 20.8 | – | °C/W |
| T _{JC} | Package θ _{JC} | 32 LEAD QFN | – | 5.9 | – | °C/W |
| T _{JA} | Package θ _{JA} | 24L QFN | – | 21.7 | – | °C/W |
| T _{JC} | Package θ _{JC} | 24L QFN | – | 5.6 | – | °C/W |
| T _{JA} | Package θ _{JA} | 32LD TQFP | – | 29.4 | – | °C/W |
| T _{JC} | Package θ _{JC} | 32LD TQFP | – | 3.5 | – | °C/W |
| T _{JA} | Package θ _{JA} | 25-ball WLCSP | – | 40 | – | °C/W |
| T _{JC} | Package θ _{JC} | 25-ball WLCSP | – | 0.5 | – | °C/W |

Table 39 Solder reflow peak temperature

| Package | Maximum peak temperature | Maximum time at peak temperature |
|---------|--------------------------|----------------------------------|
| All | 260 °C | 30 s |

Table 40 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-020

| Package | MSL |
|------------------|-------|
| All except WLCSP | MSL 3 |
| 25-ball WLCSP | MSL 1 |

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Packaging

8.1 Package diagrams

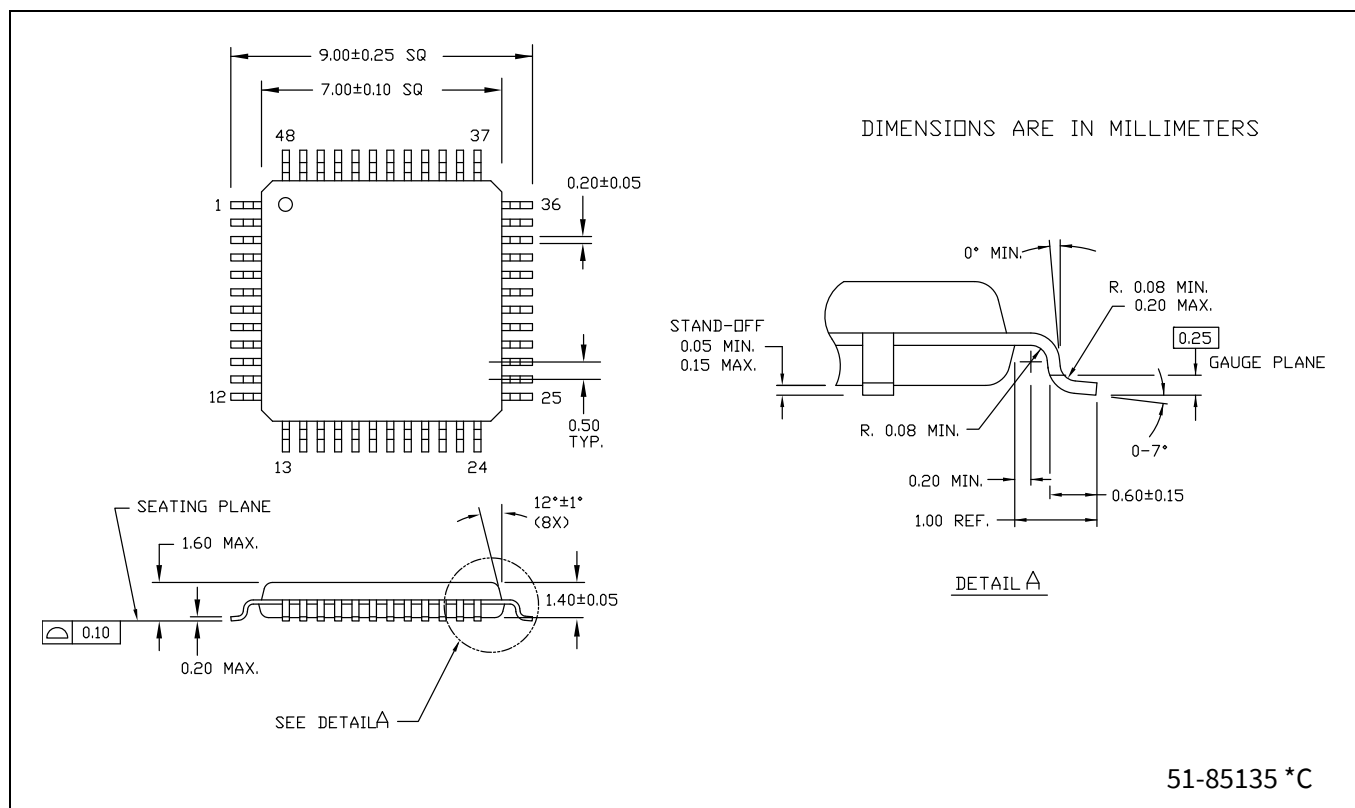


Figure 6 48LD TQFP 7×7×1.4 MM A48, PACKAGE OUTLINE, (PG-TQFP-48)

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Packaging

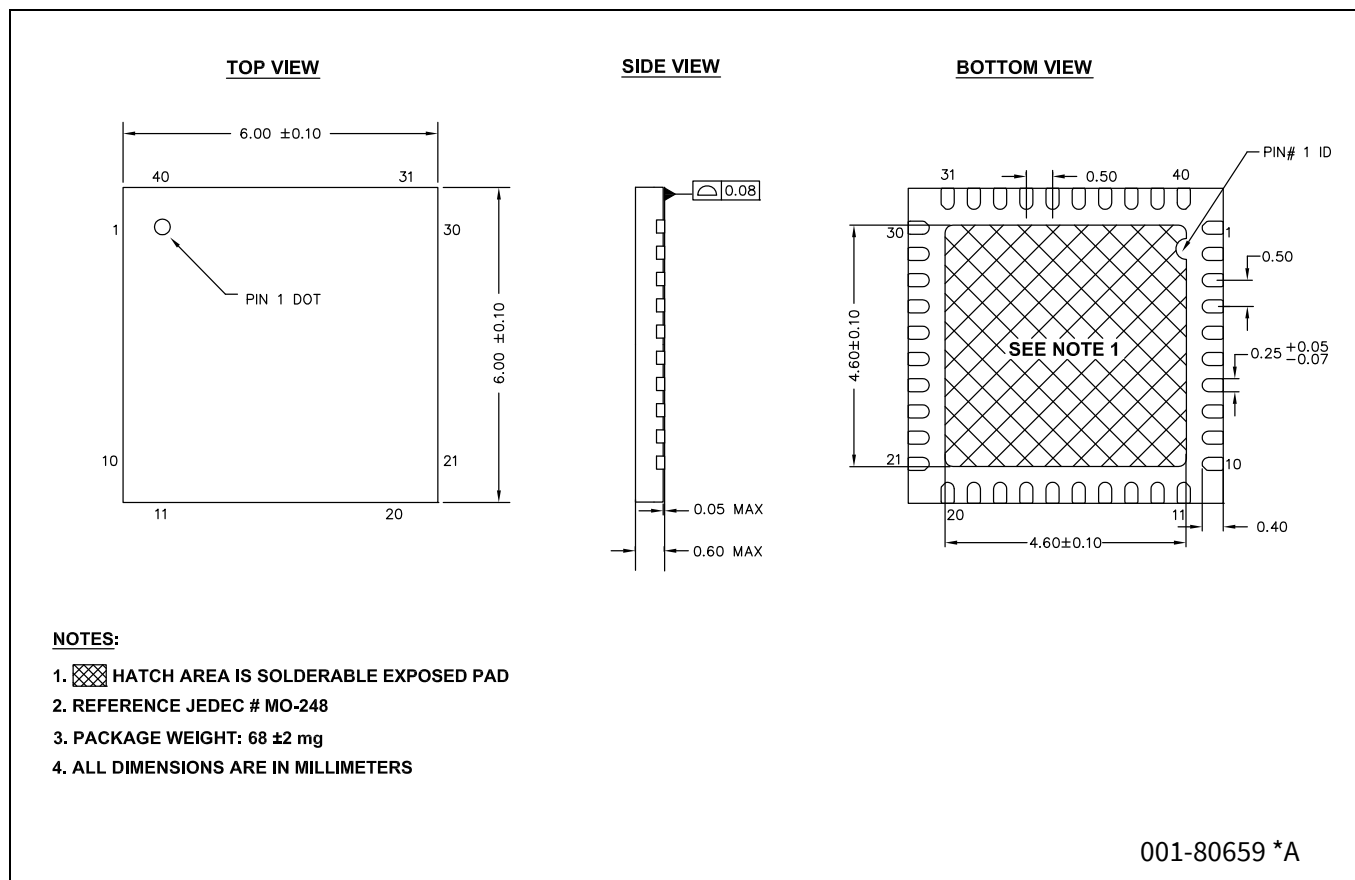


Figure 7 40L QFN 6×6×0.6 MM LR40A/LQ40A 4.6×4.6 E-PAD (SAWN), PACKAGE OUTLINE, (PG-VQFN-40)

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Packaging

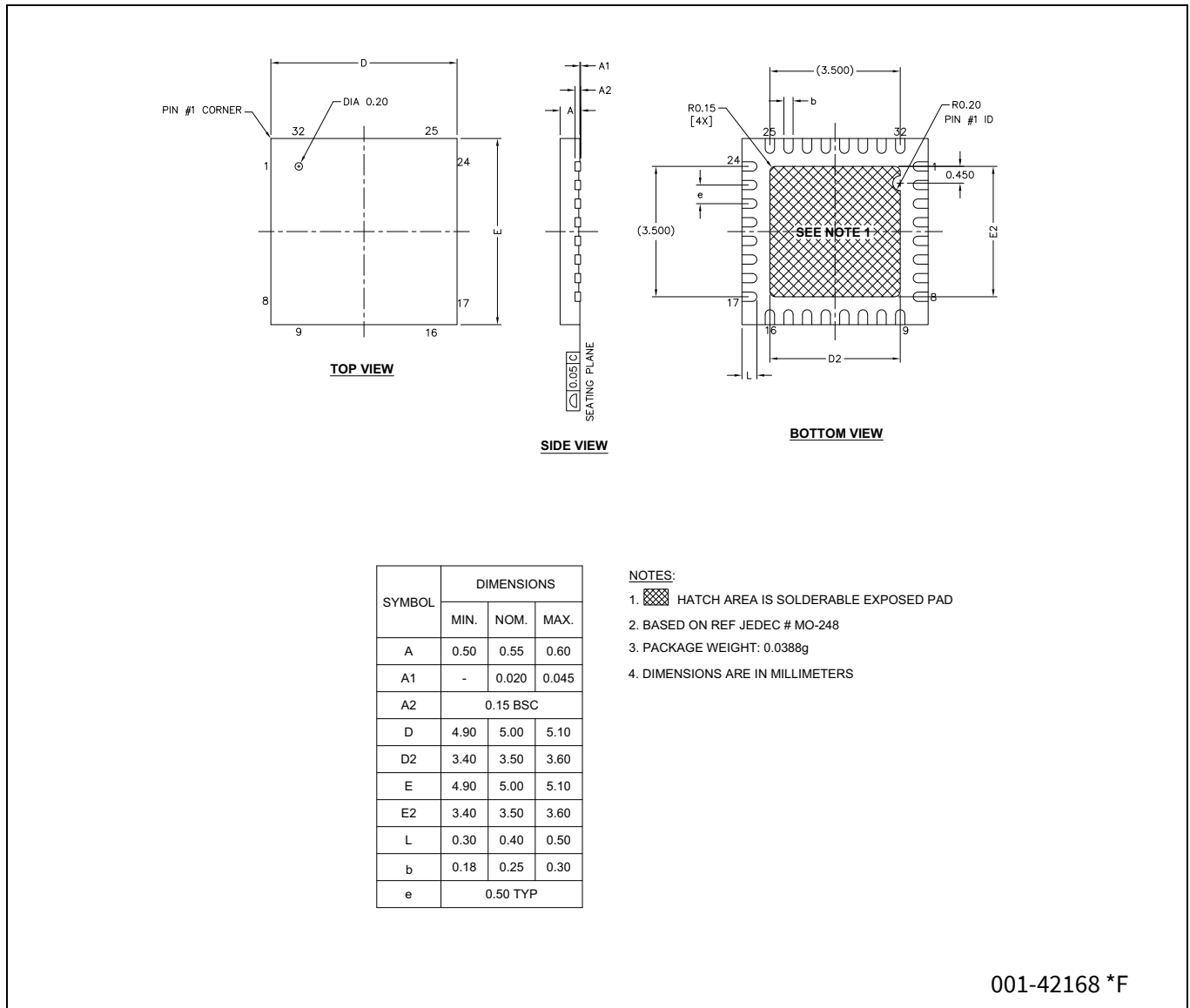


Figure 8 32 LEAD QFN 5.0×5.0×0.55 MM LQ32/LQ32B 3.5×3.5 MM EPAD (SAWN), PACKAGE OUTLINE, (PG-VQFN-32)

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Acronyms

9 Acronyms

Table 41 Acronyms used in this document

| Acronym | Description |
|---------|--|
| abus | analog local bus |
| ADC | analog-to-digital converter |
| AG | analog global |
| AHB | AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm® data transfer bus |
| ALU | arithmetic logic unit |
| AMUXBUS | analog multiplexer bus |
| API | application programming interface |
| APSR | application program status register |
| Arm® | advanced RISC machine, a CPU architecture |
| ATM | automatic thump mode |
| BW | bandwidth |
| CAN | Controller Area Network, a communications protocol |
| CMRR | common-mode rejection ratio |
| CPU | central processing unit |
| CRC | cyclic redundancy check, an error-checking protocol |
| DAC | digital-to-analog converter, see also IDAC, VDAC |
| DFB | digital filter block |
| DIO | digital input/output, GPIO with only digital capabilities, no analog. See GPIO. |
| DMIPS | Dhrystone million instructions per second |
| DMA | direct memory access, see also TD |
| DNL | differential nonlinearity, see also INL |
| DNU | do not use |
| DR | port write data registers |
| DSI | digital system interconnect |
| DWT | data watchpoint and trace |
| ECC | error correcting code |
| ECO | external crystal oscillator |
| EEPROM | electrically erasable programmable read-only memory |
| EMI | electromagnetic interference |
| EMIF | external memory interface |
| EOC | end of conversion |
| EOF | end of frame |
| EPSR | Execution Program Status register |
| ESD | electrostatic discharge |
| ETM | embedded trace macrocell |
| FIR | finite impulse response, see also IIR |

PSoC™ 4000S MCU**Based on Arm® Cortex®-M0+ CPU**

Acronyms

Table 41 Acronyms used in this document (continued)

| Acronym | Description |
|--------------------------|--|
| FPB | flash patch and breakpoint |
| FS | full-speed |
| GPIO | general-purpose input/output, applies to a PSoC™ pin |
| HVI | high-voltage interrupt, see also LVI, LVD |
| IC | integrated circuit |
| IDAC | current DAC, see also DAC, VDAC |
| IDE | integrated development environment |
| I ² C, or IIC | Inter-Integrated Circuit, a communications protocol |
| IIR | infinite impulse response, see also FIR |
| ILO | internal low-speed oscillator, see also IMO |
| IMO | internal main oscillator, see also ILO |
| INL | integral nonlinearity, see also DNL |
| I/O | input/output, see also GPIO, DIO, SIO, USBIO |
| IPOR | initial power-on reset |
| IPSR | interrupt program status register |
| IRQ | interrupt request |
| ITM | instrumentation trace macrocell |
| LCD | liquid crystal display |
| LIN | Local Interconnect Network, a communications protocol. |
| LR | link register |
| LUT | lookup table |
| LVD | low-voltage detect, see also LVI |
| LVI | low-voltage interrupt, see also HVI |
| LVTTL | low-voltage transistor-transistor logic |
| MAC | multiply-accumulate |
| MCU | microcontroller unit |
| MISO | master-in slave-out |
| NC | no connect |
| NMI | nonmaskable interrupt |
| NRZ | non-return-to-zero |
| NVIC | nested vectored interrupt controller |
| NVL | nonvolatile latch, see also WOL |
| opamp | operational amplifier |
| PAL | programmable array logic, see also PLD |
| PC | program counter |
| PCB | printed circuit board |
| PGA | programmable gain amplifier |
| PHUB | peripheral hub |
| PHY | physical layer |
| PICU | port interrupt control unit |

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Acronyms

Table 41 Acronyms used in this document (continued)

| Acronym | Description |
|---------|--|
| PLA | programmable logic array |
| PLD | programmable logic device, see also PAL |
| PLL | phase-locked loop |
| PMDD | package material declaration datasheet |
| POR | power-on reset |
| PRES | precise power-on reset |
| PRS | pseudo random sequence |
| PS | port read data register |
| PSoC™ | Programmable System-on-Chip™ |
| PSRR | power supply rejection ratio |
| PWM | pulse-width modulator |
| RAM | random-access memory |
| RISC | reduced-instruction-set computing |
| RMS | root-mean-square |
| RTC | real-time clock |
| RTL | register transfer language |
| RTR | remote transmission request |
| RX | receive |
| SAR | successive approximation register |
| SC/CT | switched capacitor/continuous time |
| SCL | I ² C serial clock |
| SDA | I ² C serial data |
| S/H | sample and hold |
| SINAD | signal to noise and distortion ratio |
| SIO | special input/output, GPIO with advanced features. See GPIO. |
| SOC | start of conversion |
| SOF | start of frame |
| SPI | Serial Peripheral Interface, a communications protocol |
| SR | slew rate |
| SRAM | static random access memory |
| SRES | software reset |
| SWD | serial wire debug, a test protocol |
| SWV | single-wire viewer |
| TD | transaction descriptor, see also DMA |
| THD | total harmonic distortion |
| TIA | transimpedance amplifier |
| TRM | technical reference manual |
| TTL | transistor-transistor logic |
| TX | transmit |
| UART | Universal Asynchronous Transmitter Receiver, a communications protocol |

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Acronyms

Table 41 Acronyms used in this document *(continued)*

| Acronym | Description |
|---------|---|
| UDB | universal digital block |
| USB | Universal Serial Bus |
| USBIO | USB input/output, PSoC pins used to connect to a USB port |
| VDAC | voltage DAC, see also DAC, IDAC |
| WDT | watchdog timer |
| WOL | write once latch, see also NVL |
| WRES | watchdog timer reset |
| XRES | external reset I/O pin |
| XTAL | crystal |

PSoC™ 4000S MCU

Based on Arm® Cortex®-M0+ CPU

Document conventions

10 Document conventions

10.1 Units of measure

Table 42 Units of measure

| Symbol | Unit of measure |
|--------|------------------------|
| °C | degrees celsius |
| dB | decibel |
| fF | femto farad |
| Hz | hertz |
| KB | 1024 bytes |
| kbps | kilobits per second |
| Khr | kilohour |
| kHz | kilohertz |
| kΩ | kilo ohm |
| ksps | kilosamples per second |
| LSB | least significant bit |
| Mbps | megabits per second |
| MHz | megahertz |
| MΩ | mega-ohm |
| MspS | megasamples per second |
| μA | microampere |
| μF | microfarad |
| μH | microhenry |
| μs | microsecond |
| μV | microvolt |
| μW | microwatt |
| mA | milliampere |
| ms | millisecond |
| mV | millivolt |
| nA | nanoampere |
| ns | nanosecond |
| nV | nanovolt |
| Ω | ohm |
| pF | picofarad |
| ppm | parts per million |
| ps | picosecond |
| s | second |
| sps | samples per second |
| sqrtHz | square root of hertz |
| V | volt |

PSoC™ 4000S MCU**Based on Arm® Cortex®-M0+ CPU**

Revision history

Revision history

| Document version | Date of release | Description of changes |
|------------------|-----------------|--|
| *G | 2016-07-27 | <p>Changed status from Preliminary to Final.</p> <p>Updated Functional definition:</p> <p>Updated Special function peripherals:</p> <p>Updated LCD segment drive:</p> <p>Updated description.</p> <p>Updated Electrical specifications:</p> <p>Updated Device level specifications:</p> <p>Updated Table 4 (Updated details corresponding to I_{DD5}, I_{DD8}, I_{DD11}, I_{DD17}, I_{DD20}, I_{DD23}, I_{DD23A}, I_{DD26}, I_{DD29}, I_{DD32}, I_{DD_XR} parameters).</p> <p>Updated GPIO:</p> <p>Updated Table 6 (Updated details in “Details/Conditions” column corresponding to V_{OH} parameter and spec ID SID60).</p> <p>Updated Packaging:</p> <p>Updated Table 37 (Updated details in “Description” column corresponding to 25-Ball WLCSP package (Updated package dimensions)).</p> <p>Updated Table 40 (Added 25-ball WLCSP package and its corresponding details).</p> <p>Completing Sunset Review.</p> |
| *H | 2016-09-14 | <p>Added 40-pin QFN package related information in all instances across the document.</p> <p>Updated Electrical specifications:</p> <p>Updated Device level specifications:</p> <p>Updated Table 4 (Updated details corresponding to I_{DD5}, I_{DD8}, I_{DD11}, I_{DD17}, I_{DD20}, I_{DD23}, I_{DD23A}, I_{DD26}, I_{DD29}, I_{DD32}, I_{DD_XR} parameters).</p> <p>Updated Packaging:</p> <p>Updated Package diagrams:</p> <p>Added spec 001-80659 *A.</p> |
| *I | 2017-01-09 | <p>Updated Electrical specifications:</p> <p>Replaced PRGIO with Smart I/O in all instances.</p> |
| *J | 2017-04-26 | Updated Cypress Logo and Copyright. |
| *K | 2017-11-17 | <p>Updated Document Title to read as “PSoC® 4: PSoC 4000S Datasheet Programmable System-on-Chip (PSoC®)”.</p> <p>Added 32-pin TQFP Package related information in all instance across the document.</p> <p>Updated Ordering information:</p> <p>Updated part numbers.</p> <p>Updated Packaging:</p> <p>Updated Package diagrams:</p> <p>spec 001-42168 – Changed revision from *E to *F.</p> <p>Added spec 51-85088 *E.</p> |

PSoC™ 4000S MCU**Based on Arm® Cortex®-M0+ CPU**

Revision history

| Document version | Date of release | Description of changes |
|------------------|-----------------|--|
| *L | 2019-07-31 | <p>Updated Features: Updated 32-bit MCU subsystem: Updated description. Added Development ecosystem. Added PSoC™ Creator. Updated Functional definition: Updated System resources: Updated Power system: Updated description. Updated Watch crystal oscillator (WCO): Updated description. Updated Fixed function digital: Updated Serial communication block (SCB): Updated description. Updated Special function peripherals: Updated LCD segment drive: Updated description. Updated Pinouts: Added Note below Table 1. Updated Electrical specifications: Updated Analog peripherals: Updated CSD and IDAC: Updated Table 12 (Updated details in “Details/Conditions” column corresponding to V_{REF}, V_{REF_EXT} and $V_{COMPIDAC}$ parameters). Updated Digital peripherals: Updated SPI: Updated Table 18 (Updated all values corresponding to TSELSSCK parameter). Updated Ordering information: Updated part numbers. Updated Packaging: Updated Package diagrams: spec 001-13937 – Changed revision from *F to *G. Updated to new template. Completing Sunset Review.</p> |
| *M | 2020-11-20 | <p>Updated Features: Added “Clock sources”. Added “ModusToolbox™ software”. Updated Development ecosystem: Replaced “More Information” with “Development ecosystem” in heading. Updated description. Added ModusToolbox™ software. Updated Electrical specifications: Updated Device level specifications: Updated temperature range in description below heading. Updated System resources: Updated Power-on reset (POR): Updated Table 25. Updated Ordering information: Updated Table 36: Added Q-temp MPNs for the 48-pin TQFP package. Updated Packaging: Updated Table 38. Updated to new template.</p> |

PSoC™ 4000S MCU**Based on Arm® Cortex®-M0+ CPU**

Revision history

| Document version | Date of release | Description of changes |
|------------------|-----------------|--|
| *N | 2020-12-23 | Updated Ordering information : Updated Nomenclature: Updated details under Temperature Range to show “Extended Industrial”. |
| *O | 2022-07-28 | Updated Table 29 : Updated spec SID223 and SID223A. Added specs SID223B through SID223D. Migrated to Infineon template. |
| *P | 2023-01-23 | Updated the footnotes in IMO AC specifications . |
| *Q | 2024-03-14 | Fixed broken links. Updated Development ecosystem . Updated product from CY8C4024FNI-S402 to CY8C4024FNI-S402T, CY8C4024FNI-S412 to CY8C4024FNI-S412T, CY8C4025FNI-S402 to CY8C4025FNI-S402T, CY8C4025FNI-S412 to CY8C4025FNI-S412T, and CY8C4045FNI-S412 to CY8C4045FNI-S412T in Table 36 Updated packing diagram titles with IFX package code for Figure 6 , Figure 7 , Figure 8 , Figure 9 , Figure 10 and Figure 11 Updated Packaging . |

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Edition 2024-03-14

Published by

**Infineon Technologies AG
81726 Munich, Germany**

**© 2024 Infineon Technologies AG.
All Rights Reserved.**

Do you have a question about this document?

Email:

erratum@infineon.com

Document reference

002-00123 Rev. *Q

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.

OUR CERTIFICATE

DiGi provide top-quality products and perfect service for customer worldwide through standardization, technological innovation and continuous improvement. DiGi through third-party certification, we stricly control the quality of products and services. Welcome your RFQ to

Email: Info@DiGi-Electronics.com



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.