

IPD10N03LA Datasheet



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DiGi Electronics Part Number	IPD10N03LA-DG
Manufacturer	Infineon Technologies
Manufacturer Product Number	IPD10N03LA
Description	MOSFET N-CH 25V 30A TO252-3
Detailed Description	N-Channel 25 V 30A (Tc) 52W (Tc) Surface Mount PG -TO252-3-11



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Purchase and inquiry

Manufacturer Product Number:

IPD10N03LA

Series:

OptiMOS™

Part Status:

Obsolete

Technology:

MOSFET (Metal Oxide)

Current - Continuous Drain (Id) @ 25°C:

30A (Tc)

Rds On (Max) @ Id, Vgs:

10.4mOhm @ 30A, 10V

Gate Charge (Qg) (Max) @ Vgs:

11 nC @ 5 V

Input Capacitance (Ciss) (Max) @ Vds:

1358 pF @ 15 V

Power Dissipation (Max):

52W (Tc)

Mounting Type:

Surface Mount

Package / Case:

TO-252-3, DPAK (2 Leads + Tab), SC-63

Manufacturer:

Infineon Technologies

Packaging:

Tape & Reel (TR)

FET Type:

N-Channel

Drain to Source Voltage (Vdss):

25 V

Drive Voltage (Max Rds On, Min Rds On):

4.5V, 10V

Vgs(th) (Max) @ Id:

2V @ 20µA

Vgs (Max):

±20V

FET Feature:

-

Operating Temperature:

-55°C ~ 175°C (TJ)

Supplier Device Package:

PG-T0252-3-11

Base Product Number:

IPD10N

Environmental & Export classification

RoHS Status:

RoHS non-compliant

REACH Status:

REACH Unaffected

HTSUS:

8541.29.0095

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99



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 IPS10N03LA G IPU10N03LA G

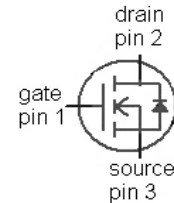
OptiMOS[®] 2 Power-Transistor

Features

- Ideal for high-frequency dc/dc converters
- Qualified according to JEDEC¹⁾ for target application
- N-channel, logic level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Superior thermal resistance
- 175 °C operating temperature
- Pb-free lead plating; RoHS compliant

Product Summary

V_{DS}	25	V
$R_{DS(on),max}$	10.4	m Ω
I_D	30	A



Type	IPD10N03LA	IPF10N03LA	IPS10N03LA	IPU10N03LA
Package	P-TO252-3-11	P-TO252-3-23	P-TO251-3-11	P-TO251-3-1
Marking	10N03LA	10N03LA	10N03LA	10N03LA

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25\text{ °C}^{2)}$	30	A
		$T_C=100\text{ °C}$	30	
Pulsed drain current	$I_{D,pulse}$	$T_C=25\text{ °C}^{3)}$	210	
Avalanche energy, single pulse	E_{AS}	$I_D=30\text{ A}$, $R_{GS}=25\ \Omega$	80	mJ
Reverse diode dv/dt	dv/dt	$I_D=30\text{ A}$, $V_{DS}=20\text{ V}$, $di/dt=200\text{ A}/\mu\text{s}$, $T_{j,max}=175\text{ °C}$	6	kV/ μs
Gate source voltage ⁴⁾	V_{GS}		± 20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	52	W
Operating and storage temperature	T_j , T_{stg}		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	



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Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - case	R_{thJC}		-	-	2.9	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	75	
		6 cm ² cooling area ⁵⁾	-	-	50	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	25	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=20\text{ }\mu\text{A}$	1.2	1.6	2	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=25\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$	-	0.1	1	μA
		$V_{DS}=25\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ °C}$	-	10	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5\text{ V}, I_D=20\text{ A}$	-	13.9	17.4	m Ω
		$V_{GS}=10\text{ V}, I_D=30\text{ A}$	-	8.7	10.4	
Gate resistance	R_G		-	1	-	Ω
Transconductance	g_{fs}	$ V_{DS} >2 I_D R_{DS(on)max}, I_D=30\text{ A}$	20	41	-	S

¹⁾ J-STD20 and JESD22

²⁾ Current is limited by bondwire; with an $R_{thJC}=2.9\text{ K/W}$ the chip is able to carry 53 A.

³⁾ See figure 3

⁴⁾ $T_{j,max}=150\text{ °C}$ and duty cycle $D<0.25$ for $V_{GS}<-5\text{ V}$

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.



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Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=15\text{ V},$ $f=1\text{ MHz}$	-	1021	1358	pF
Output capacitance	C_{oss}		-	393	522	
Reverse transfer capacitance	C_{rss}		-	52	78	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=15\text{ V}, V_{GS}=10\text{ V},$ $I_D=15\text{ A}, R_G=2.7\ \Omega$	-	6.3	9.4	ns
Rise time	t_r		-	4.8	7.2	
Turn-off delay time	$t_{d(off)}$		-	18	27	
Fall time	t_f		-	2.8	4.2	

Gate Charge Characteristics+A40⁶⁾

Gate to source charge	Q_{gs}	$V_{DD}=15\text{ V}, I_D=15\text{ A},$ $V_{GS}=0\text{ to }5\text{ V}$	-	3.4	4.5	nC
Gate charge at threshold	$Q_{g(th)}$		-	1.6	2.2	
Gate to drain charge	Q_{gd}		-	2.3	3.5	
Switching charge	Q_{sw}		-	4.1	5.8	
Gate charge total	Q_g		-	8.2	11	
Gate plateau voltage	$V_{plateau}$		-	3.3	-	
Gate charge total, sync. FET	$Q_{g(sync)}$	$V_{DS}=0.1\text{ V},$ $V_{GS}=0\text{ to }5\text{ V}$	-	7.2	9.6	nC
Output charge	Q_{oss}	$V_{DD}=15\text{ V}, V_{GS}=0\text{ V}$	-	8.5	11	

Reverse Diode

Diode continuous forward current	I_S	$T_C=25\text{ }^\circ\text{C}$	-	-	30	A
Diode pulse current	$I_{S,pulse}$		-	-	210	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=30\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	0.93	1.2	V
Reverse recovery charge	Q_{rr}	$V_R=15\text{ V}, I_F=I_S,$ $di_F/dt=400\text{ A}/\mu\text{s}$	-	-	10	nC

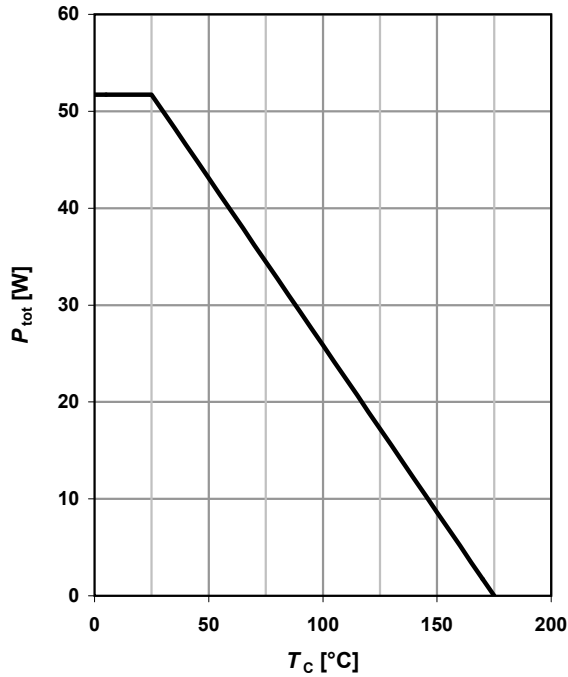
⁶⁾ See figure 16 for gate charge parameter definition



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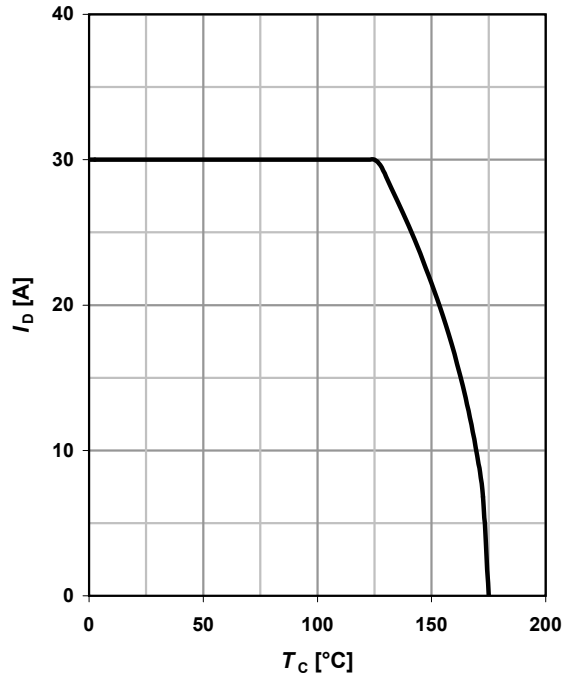
1 Power dissipation

$P_{tot}=f(T_C)$



2 Drain current

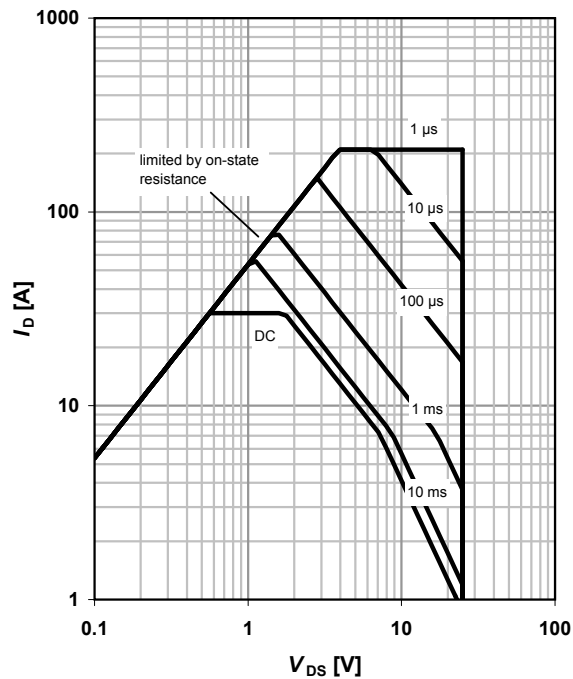
$I_D=f(T_C); V_{GS} \geq 10V$



3 Safe operating area

$I_D=f(V_{DS}); T_C=25^\circ C; D=0$

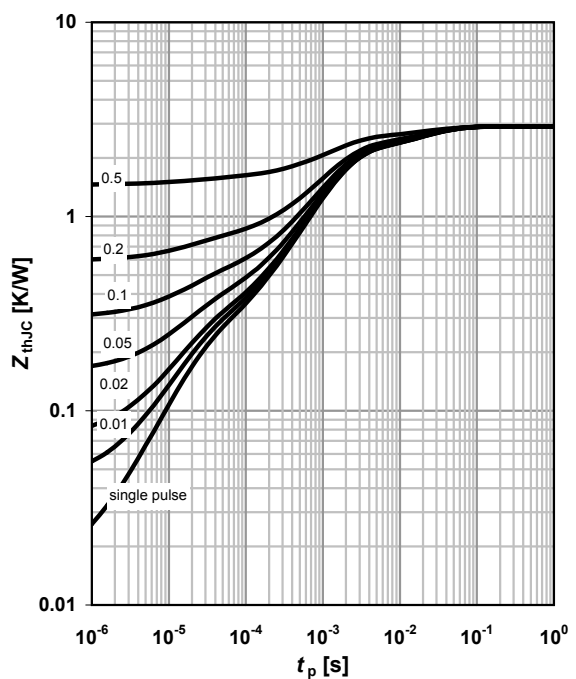
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

parameter: $D=t_p/T$



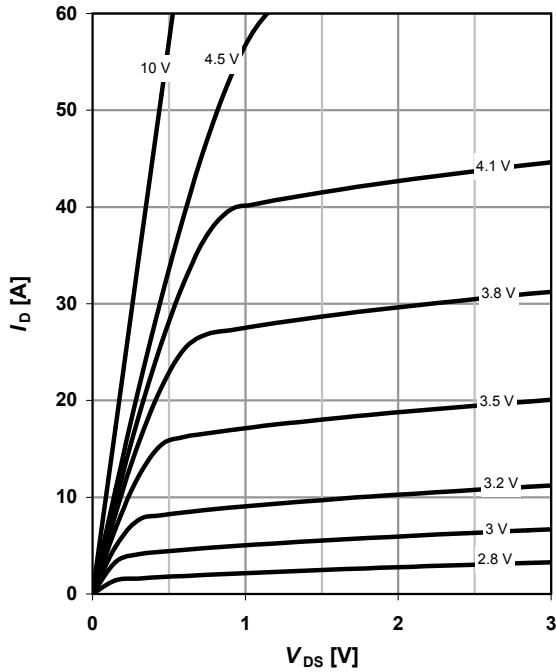


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5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

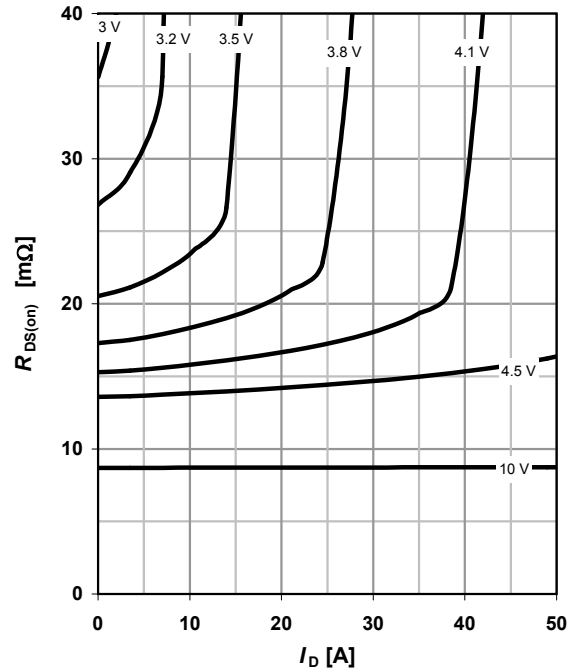
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

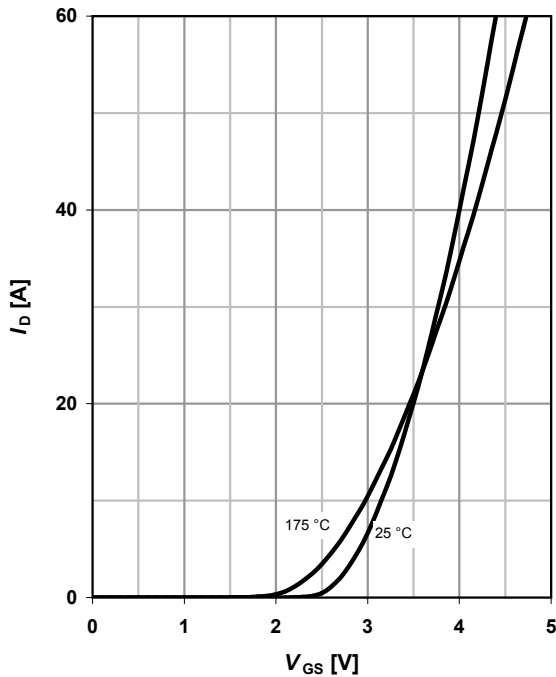
parameter: V_{GS}



7 Typ. transfer characteristics

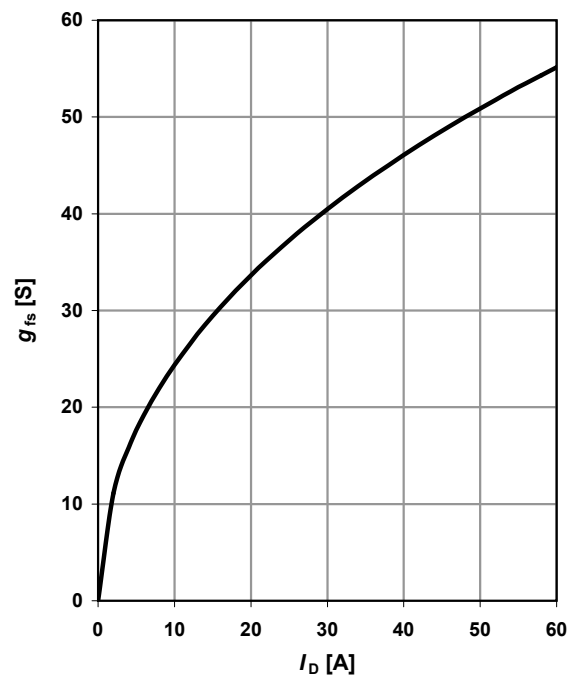
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

parameter: T_j



8 Typ. forward transconductance

$g_{fs} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

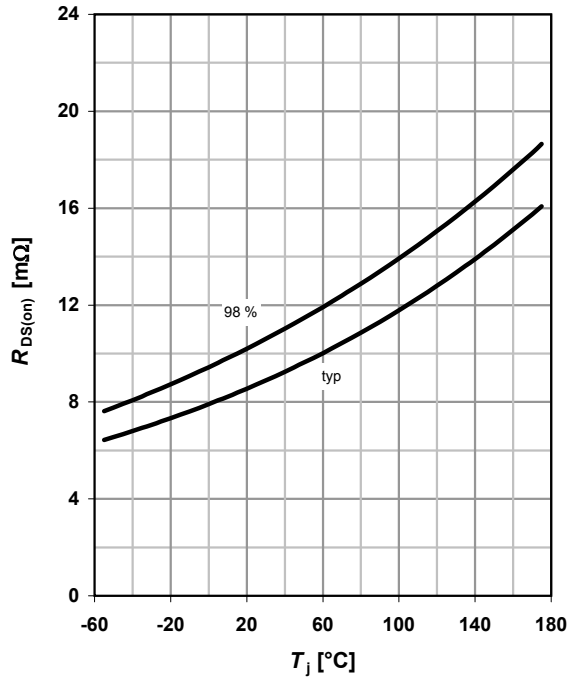




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9 Drain-source on-state resistance

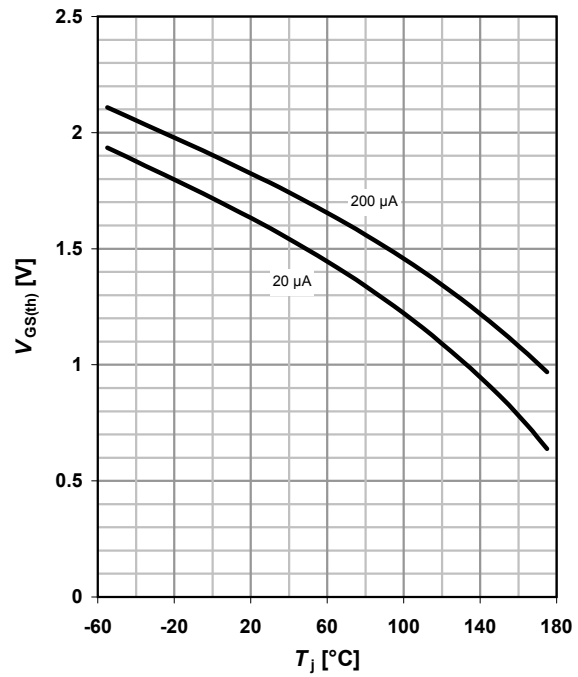
$R_{DS(on)} = f(T_j); I_D = 30 \text{ A}; V_{GS} = 10 \text{ V}$



10 Typ. gate threshold voltage

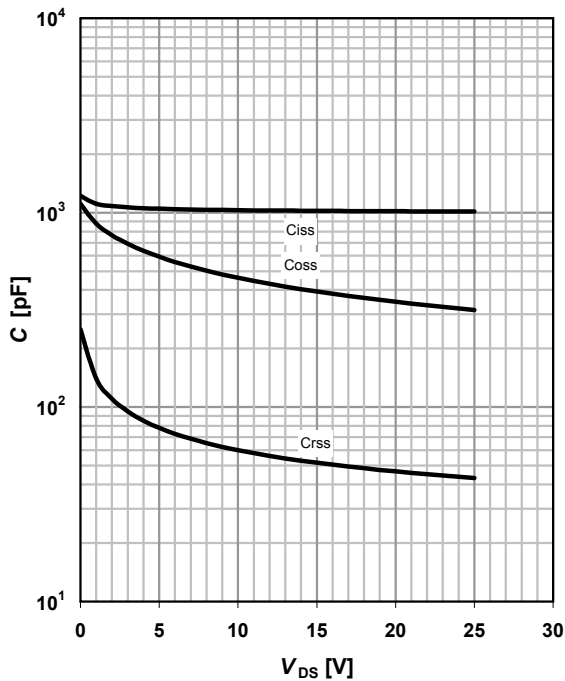
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter: I_D



11 Typ. capacitances

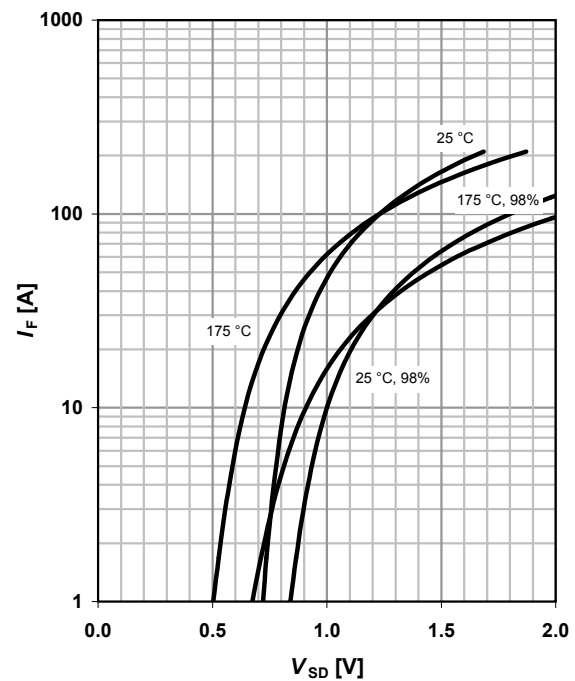
$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$



12 Forward characteristics of reverse diode

$I_F = f(V_{SD})$

parameter: T_j



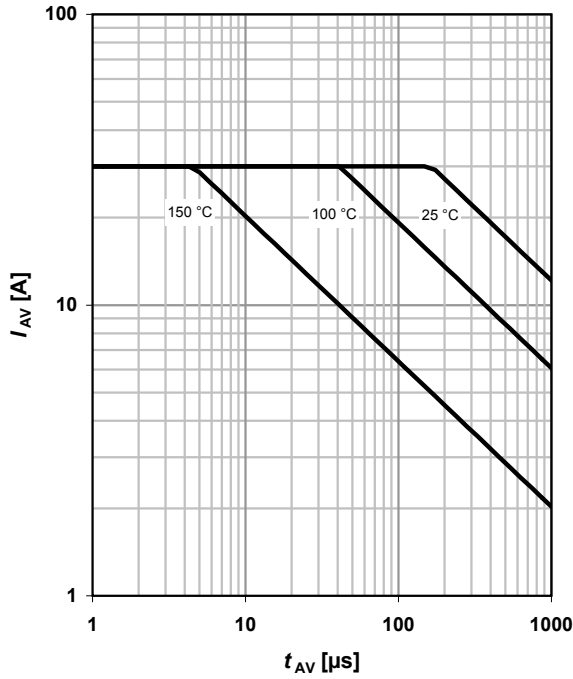


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13 Avalanche characteristics

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

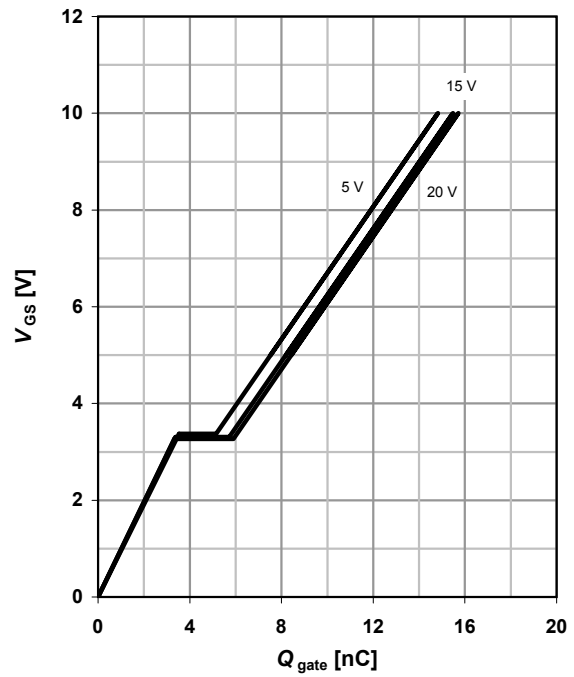
parameter: $T_{j(start)}$



14 Typ. gate charge

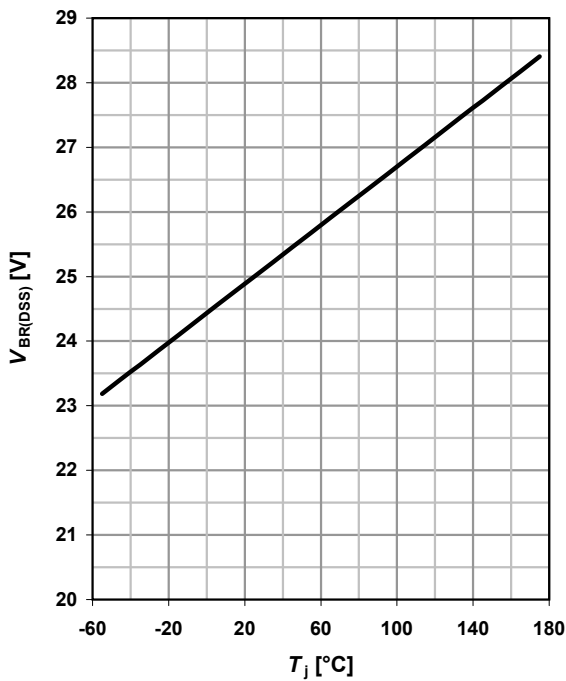
$V_{GS}=f(Q_{gate}); I_D=15 \text{ A pulsed}$

parameter: V_{DD}

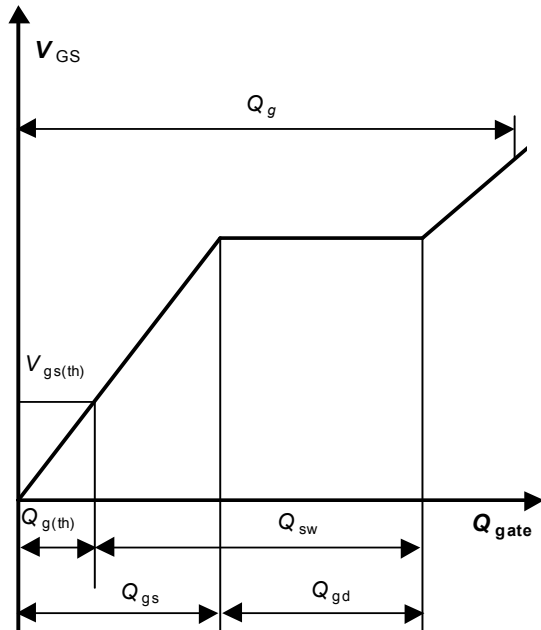


15 Drain-source breakdown voltage

$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$



16 Gate charge waveforms

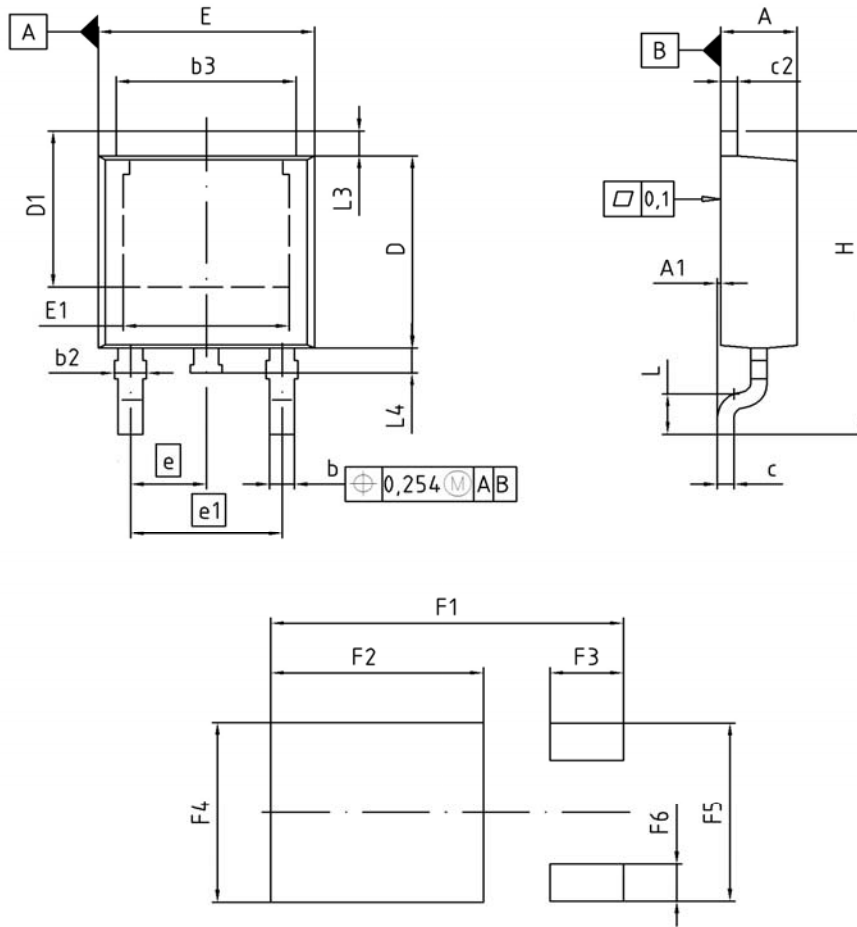




IPD10N03LA G IPF10N03LA G
 IPS10N03LA G IPU10N03LA G

Package Outline

PG-TO252-3-11



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.16	2.41	0.085	0.095
A1	0.00	0.15	0.000	0.006
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b3	5.00	5.50	0.197	0.217
c	0.46	0.60	0.018	0.024
c2	0.46	0.98	0.018	0.039
D	5.97	6.22	0.235	0.245
D1	5.02	5.84	0.198	0.230
E	6.40	6.73	0.252	0.265
E1	4.70	5.21	0.185	0.205
e	2.29		0.090	
e1	4.57		0.180	
N	3		3	
H	9.40	10.48	0.370	0.413
L	1.18	1.70	0.046	0.067
L3	0.90	1.25	0.035	0.049
L4	0.51	1.00	0.020	0.039
F1	10.50	10.70	0.413	0.421
F2	6.30	6.50	0.248	0.256
F3	2.10	2.30	0.083	0.091
F4	5.70	5.90	0.224	0.232
F5	5.66	5.86	0.223	0.231
F6	1.10	1.30	0.043	0.051

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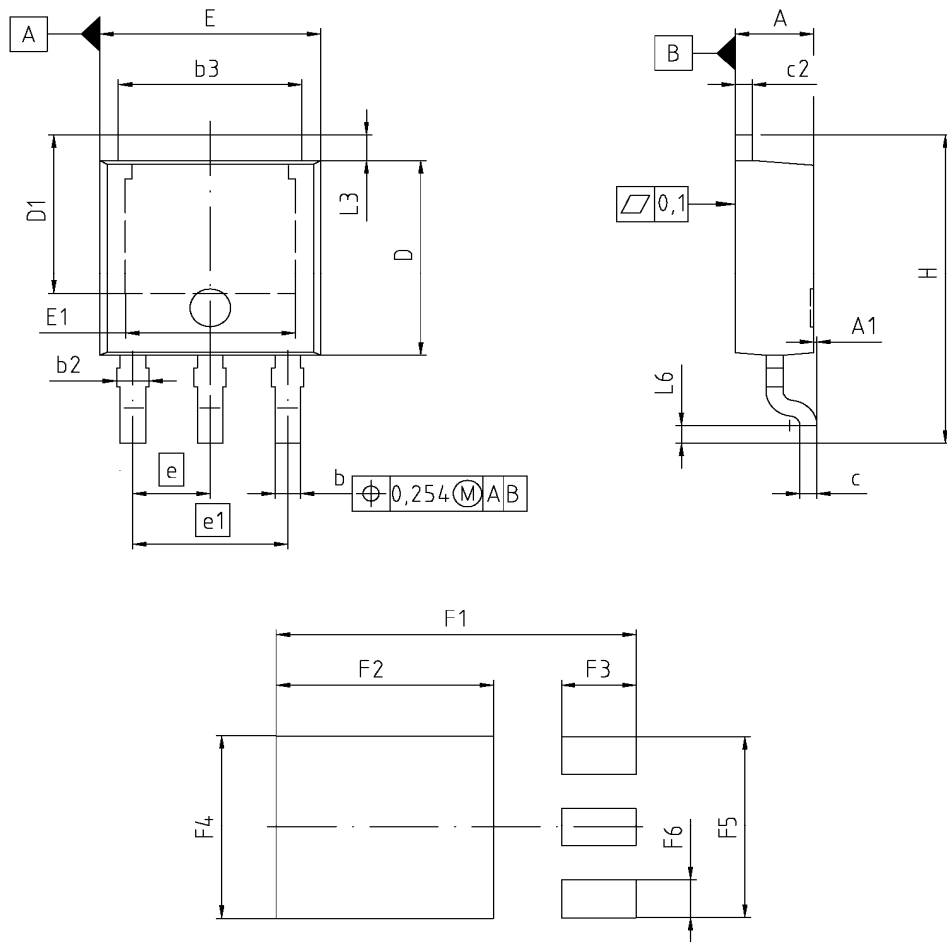
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IPD10N03LA G IPF10N03LA G
 IPS10N03LA G IPU10N03LA G

Package Outline

PG-TO252-3-23



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.159	2.413	0.085	0.095
A1	0.000	0.150	0.000	0.006
b	0.635	0.889	0.025	0.035
b2	0.650	1.150	0.026	0.045
b3	5.004	5.500	0.197	0.217
c	0.457	0.580	0.018	0.023
c2	0.460	0.980	0.018	0.039
D	5.969	6.223	0.235	0.245
D1	5.020	5.842	0.198	0.230
E	6.400	6.731	0.252	0.265
E1	4.850	5.207	0.191	0.205
e	2.286		0.090	
e1	4.572		0.180	
N	3		3	
H	9.400	10.480	0.370	0.413
L3	0.900	1.143	0.035	0.045
L4	0.584	0.950	0.023	0.037
L6	0.510	0.686	0.020	0.027
F1	10.500	10.700	0.413	0.421
F2	6.300	6.500	0.248	0.256
F3	2.100	2.300	0.083	0.091
F4	5.700	5.900	0.224	0.232
F5	5.660	5.860	0.222	0.231
F6	1.100	1.300	0.043	0.051

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0 2.0 4mm

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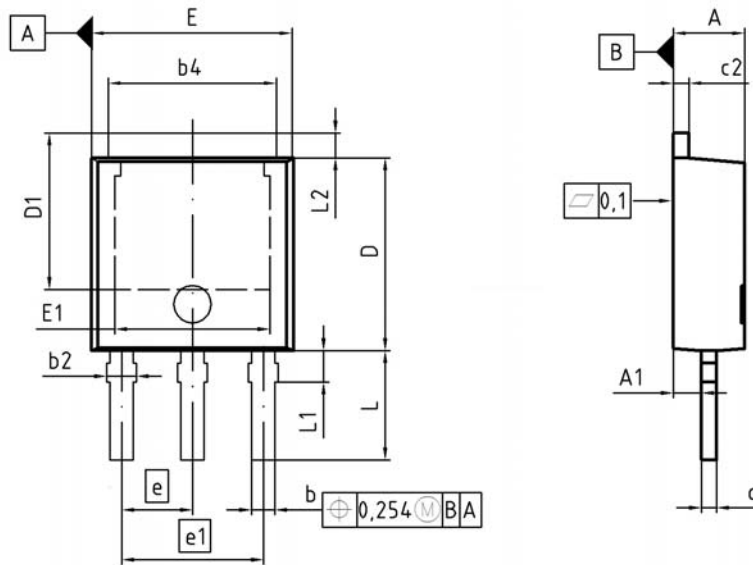
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IPD10N03LA G IPF10N03LA G
 IPS10N03LA G IPU10N03LA G

Package Outline

PG-TO251-3-11



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.18	2.39	0.086	0.094
A1	0.80	1.14	0.031	0.045
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b4	4.95	5.50	0.195	0.217
c	0.46	0.58	0.018	0.023
c2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.04	5.44	0.198	0.214
E	6.35	6.73	0.250	0.265
E1	4.90	5.10	0.193	0.201
e	2.29		0.090	
e1	4.57		0.180	
N	3		3	
L	3.40	3.60	0.134	0.142
L1	0.90	1.10	0.035	0.043
L2	0.90	1.10	0.035	0.043

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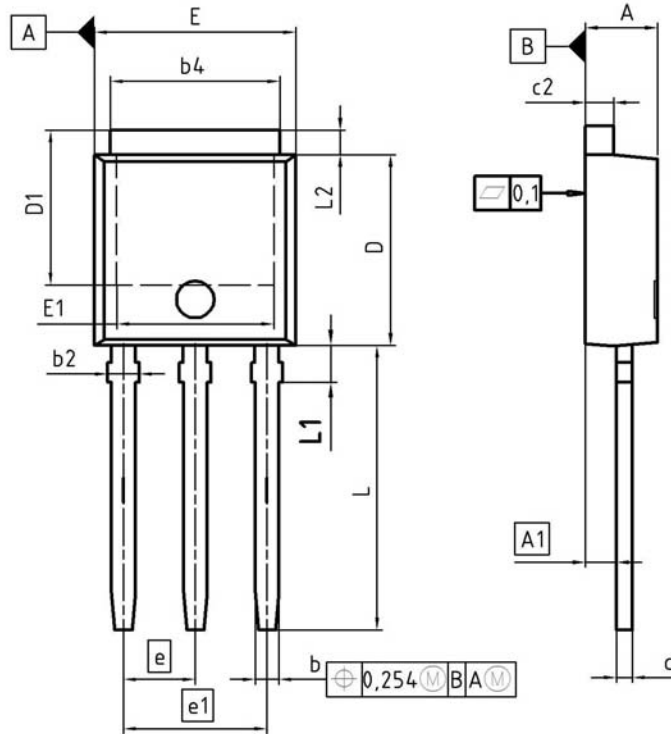
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IPD10N03LA G IPF10N03LA G
 IPS10N03LA G IPU10N03LA G

Package Outline

PG-TO251-3-21



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.16	2.41	0.085	0.095
A1	0.90	1.14	0.035	0.045
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b4	4.95	5.50	0.195	0.217
c	0.46	0.60	0.018	0.024
c2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.04	5.77	0.198	0.227
E	6.35	6.73	0.250	0.265
E1	4.70	5.21	0.185	0.205
e	2.29		0.090	
e1	4.57		0.180	
N	3		3	
L	8.89	9.65	0.350	0.380
L1	1.90	2.29	0.075	0.090
L2	0.89	1.37	0.035	0.054

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IPD10N03LA G IPF10N03LA G
IPS10N03LA G IPU10N03LA G

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