

IPD110N12N3GBUMA1 Datasheet



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DiGi Electronics Part Number	IPD110N12N3GBUMA1-DG
Manufacturer	Infineon Technologies
Manufacturer Product Number	IPD110N12N3GBUMA1
Description	MOSFET N-CH 120V 75A TO252-3
Detailed Description	N-Channel 120 V 75A (Tc) 136W (Tc) Surface Mount PG-TO252-3



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Purchase and inquiry

Manufacturer Product Number:

IPD110N12N3GBUMA1

Series:

OptiMOS™

FET Type:

N-Channel

Drain to Source Voltage (Vdss):

120 V

Drive Voltage (Max Rds On, Min Rds On):

10V

Vgs(th) (Max) @ Id:

4V @ 83µA

Vgs (Max):

±20V

FET Feature:

-

Operating Temperature:

-55°C ~ 175°C (Tj)

Supplier Device Package:

PG-T0252-3

Base Product Number:

IPD110N

Manufacturer:

Infineon Technologies

Product Status:

Obsolete

Technology:

MOSFET (Metal Oxide)

Current - Continuous Drain (Id) @ 25°C:

75A (Tc)

Rds On (Max) @ Id, Vgs:

11mOhm @ 75A, 10V

Gate Charge (Qg) (Max) @ Vgs:

65 nC @ 10 V

Input Capacitance (Ciss) (Max) @ Vds:

4310 pF @ 60 V

Power Dissipation (Max):

136W (Tc)

Mounting Type:

Surface Mount

Package / Case:

TO-252-3, DPAK (2 Leads + Tab), SC-63

Environmental & Export classification

Moisture Sensitivity Level (MSL):

3 (168 Hours)

ECCN:

EAR99

REACH Status:

REACH Unaffected

HTSUS:

8541.29.0095



MOSFET

Metal Oxide Semiconductor Field Effect Transistor

OptiMOS™ Power-Transistor, 120V

OptiMOS™ 3 Power-Transistor
IPD_S110N12N3 G

Data Sheet

Rev. 2.4
Final

Industrial & Multimarket



IPD110N12N3 G

IPS110N12N3 G

OptiMOS™3 Power-Transistor

Features

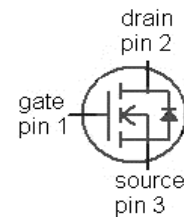
- N-channel, normal level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC¹⁾ for target application
- Halogen free according to IEC61249-2-21 *
- Ideal for high-frequency switching and synchronous rectification

Product Summary

V_{DS}	120	V
$R_{DS(on),max}$	11	m Ω
I_D	75	A



Type	IPS110N12N3 G	IPD110N12N3 G
Package	PG-TO251-3	PG-TO252-3
Marking	110N12N	110N12N



Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25\text{ °C}$	75	A
		$T_C=100\text{ °C}$	54	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	300	
Avalanche energy, single pulse	E_{AS}	$I_D=75\text{ A}$, $R_{GS}=25\text{ }\Omega$	120	mJ
Gate source voltage ³⁾	V_{GS}		± 20	V
	P_{tot}	$T_C=25\text{ °C}$	136	W
Operating and storage temperature	T_j , T_{stg}		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

¹⁾J-STD20 and JESD22

²⁾ see figure 3

³⁾ $T_{jmax}=150\text{ °C}$ and duty cycle $D=0.01$ for $V_{gs}<-5V$

* Except package TO251-3



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Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - case	R_{thJC}		-	-	1.1	K/W
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint	-	-	75	
		6 cm ² cooling area ⁴⁾	-	-	50	

Electrical characteristics, at $T_j=25\text{ }^\circ\text{C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	120	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=83\text{ }\mu\text{A}$	2	3	4	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=100\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ }^\circ\text{C}$	-	0.1	1	μA
		$V_{DS}=100\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ }^\circ\text{C}$	-	10	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	1	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{ V}, I_D=75\text{ A}$	-	9.2	11	m Ω
Gate resistance	R_G		-	1.5	-	Ω
Transconductance	g_{fs}	$ V_{DS} >2 I_D R_{DS(on)max}, I_D=75\text{ A}$	42	83	-	S

⁴⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.



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Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics⁶⁾

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=60\text{ V},$ $f=1\text{ MHz}$	-	3240	4310	pF
Output capacitance	C_{oss}		-	408	543	
Reverse transfer capacitance	C_{rss}		-	22	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=60\text{ V}, V_{GS}=10\text{ V},$ $I_D=75\text{ A}, R_{G,ext}=1.6\ \Omega$	-	16	-	ns
Rise time	t_r		-	16	-	
Turn-off delay time	$t_{d(off)}$		-	24	-	
Fall time	t_f		-	8	-	

Gate Charge Characteristics⁵⁾

Gate to source charge	Q_{gs}	$V_{DD}=60\text{ V}, I_D=75\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	18	-	nC
Gate to drain charge	Q_{gd}		-	12	-	
Switching charge	Q_{sw}		-	20	-	
Gate charge total ⁶⁾	Q_g		-	49	65	
Gate plateau voltage	$V_{plateau}$		-	5.6	-	V
Output charge ⁶⁾	Q_{oss}	$V_{DD}=60\text{ V}, V_{GS}=0\text{ V}$	-	56	75	nC

Reverse Diode

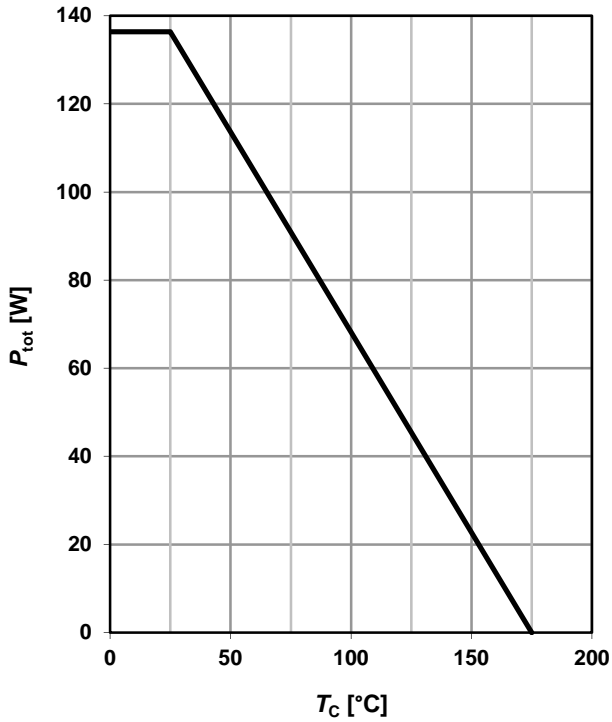
Diode continuous forward current	I_S	$T_C=25\text{ }^\circ\text{C}$	-	-	75	A
Diode pulse current	$I_{S,pulse}$		-	-	300	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=75\text{ A},$ $T_J=25\text{ }^\circ\text{C}$	-	1	1.2	V
Reverse recovery charge	t_{rr}	$V_R=60\text{ V}, I_F=I_S,$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	90		ns
	Q_{rr}		-	249		nC

⁵⁾ See figure 16 for gate charge parameter definition⁶⁾ Defined by design. Not subject to production test



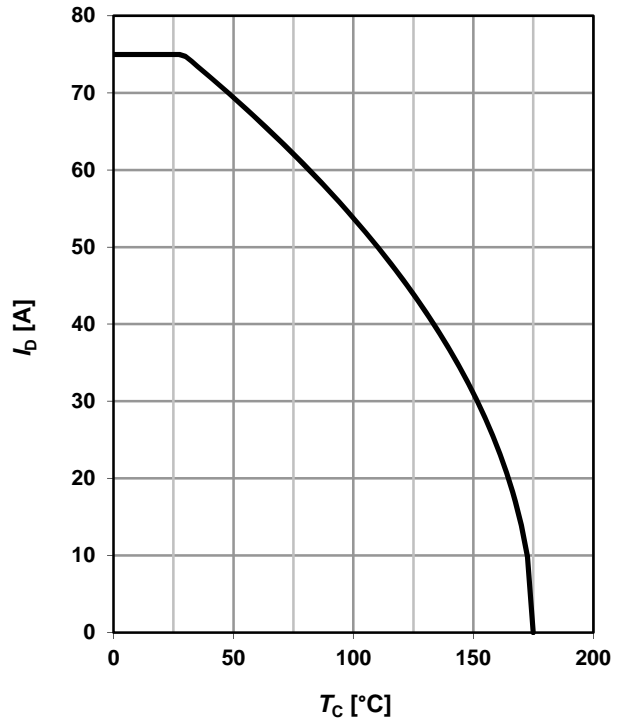
1 Power dissipation

$P_{tot}=f(T_C)$



2 Drain current

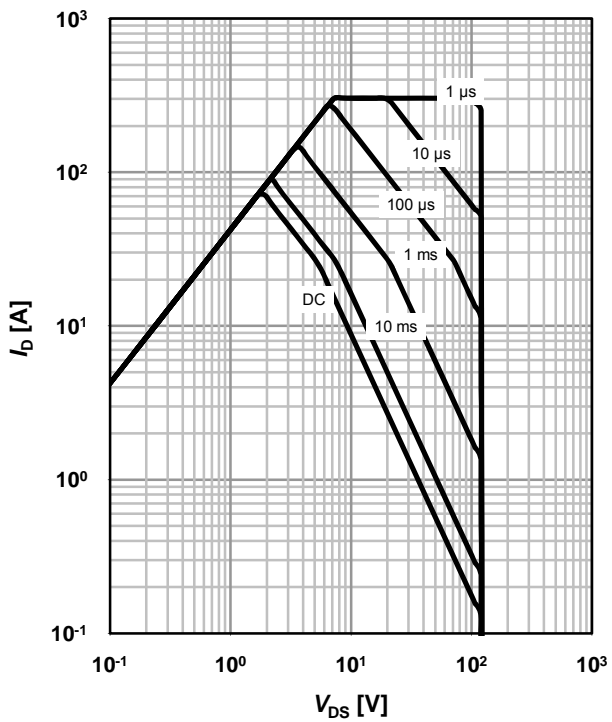
$I_D=f(T_C); V_{GS} \geq 10\text{ V}$



3 Safe operating area

$I_D=f(V_{DS}); T_C=25\text{ °C}; D=0$

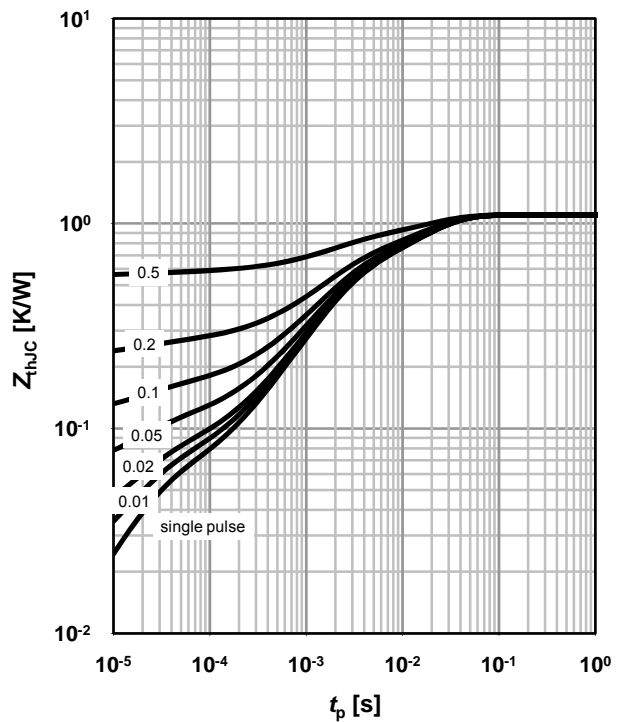
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

parameter: $D=t_p/T$

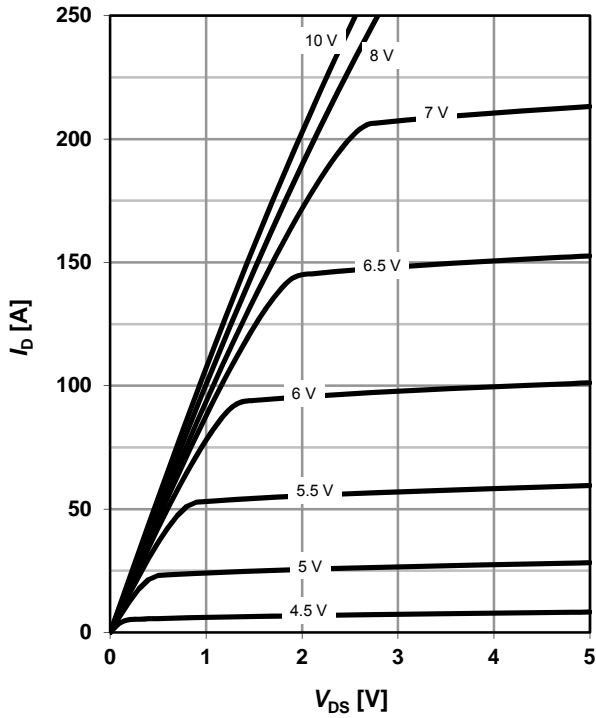




5 Typ. output characteristics

$I_D=f(V_{DS}); T_j=25\text{ }^\circ\text{C}$

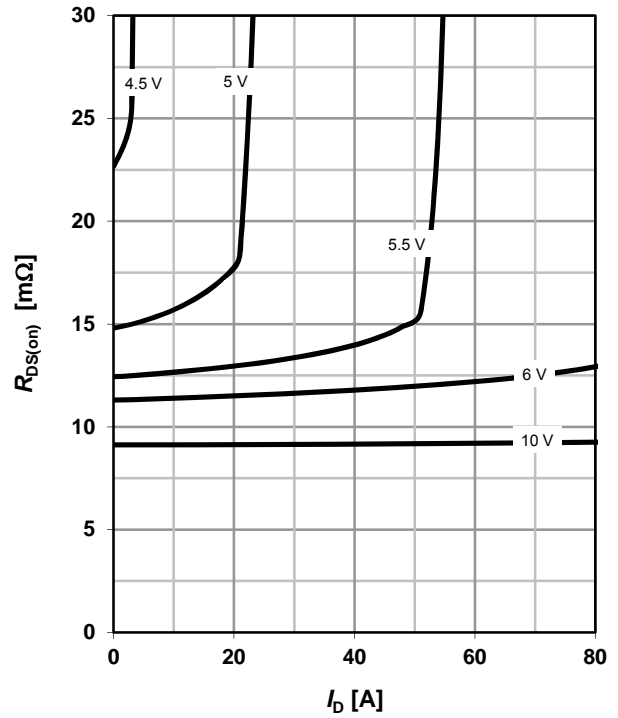
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}=f(I_D); T_j=25\text{ }^\circ\text{C}$

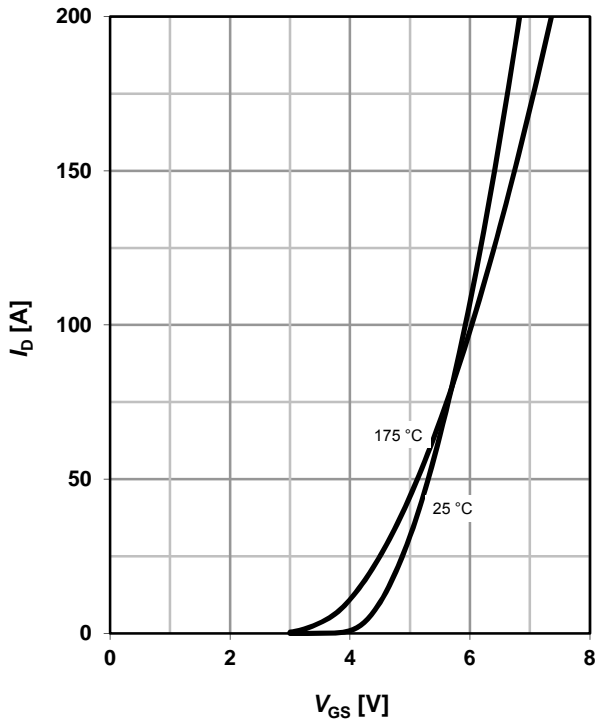
parameter: V_{GS}



7 Typ. transfer characteristics

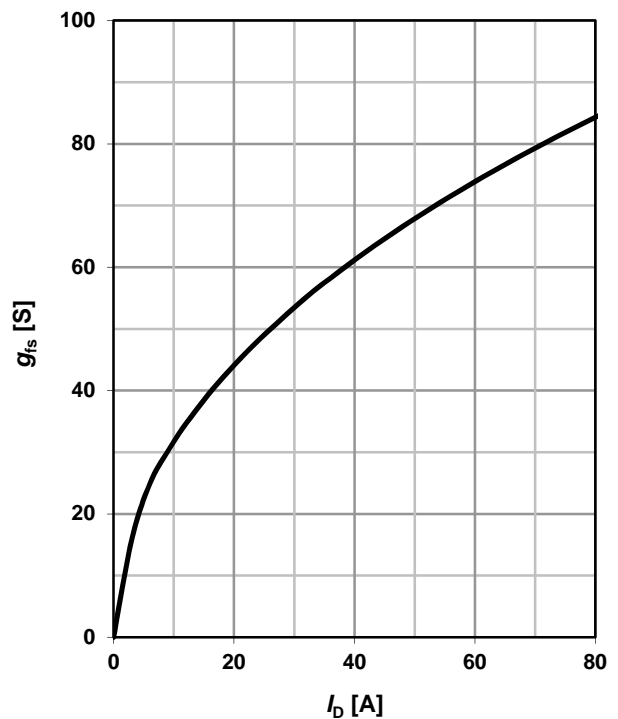
$I_D=f(V_{GS}); |V_{DS}|>2|I_D|R_{DS(on)max}$

parameter: T_j



8 Typ. forward transconductance

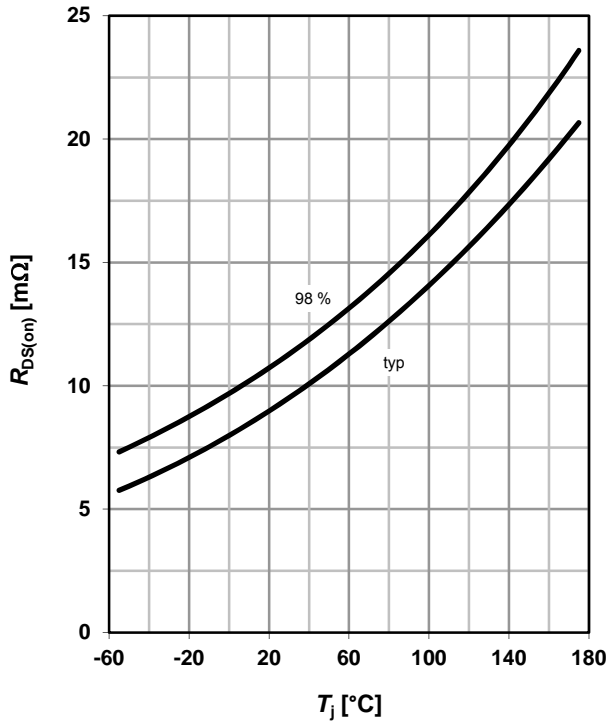
$g_{fs}=f(I_D); T_j=25\text{ }^\circ\text{C}$





9 Drain-source on-state resistance

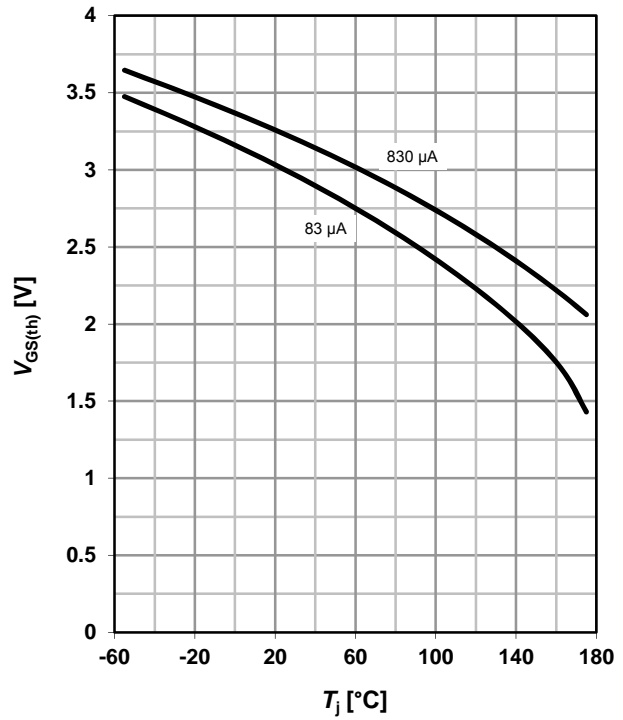
$R_{DS(on)}=f(T_j)$; $I_D=75\text{ A}$; $V_{GS}=10\text{ V}$



10 Typ. gate threshold voltage

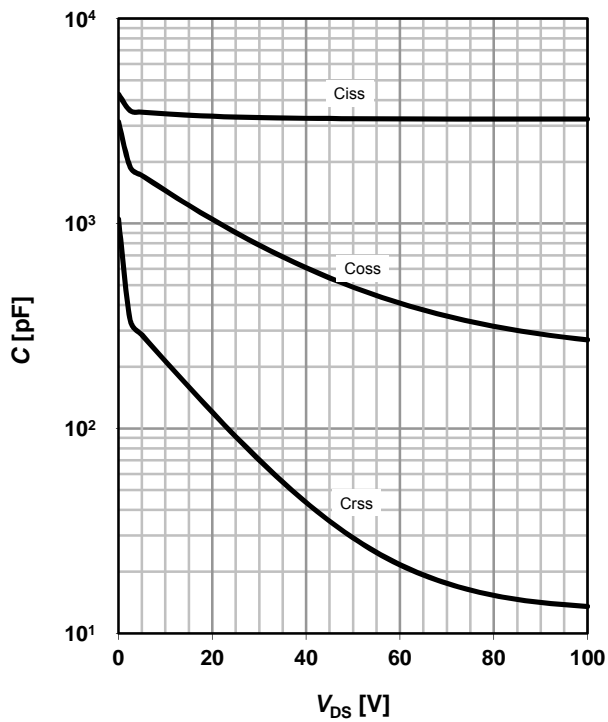
$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$

parameter: I_D



11 Typ. capacitances

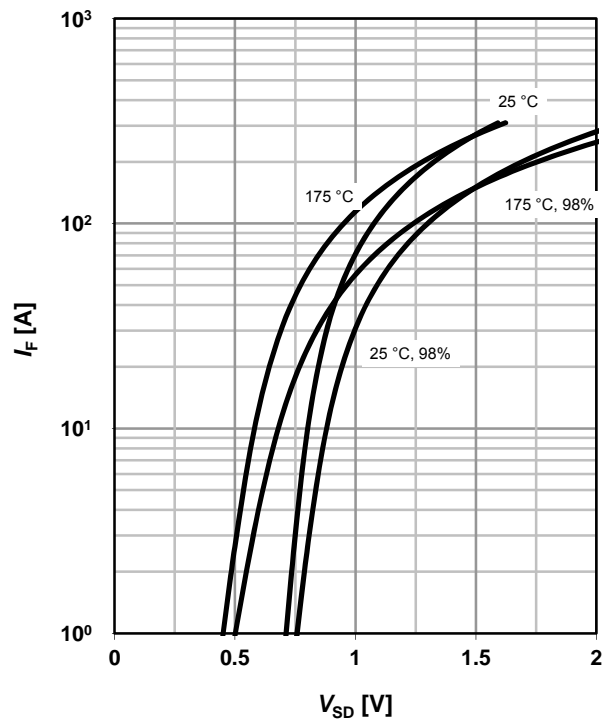
$C=f(V_{DS})$; $V_{GS}=0\text{ V}$; $f=1\text{ MHz}$



12 Forward characteristics of reverse diode

$I_F=f(V_{SD})$

parameter: T_j

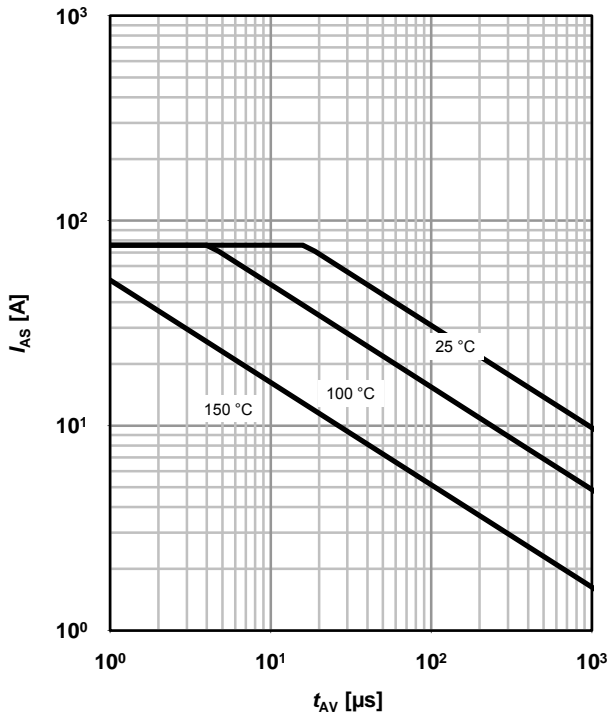




13 Avalanche characteristics

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

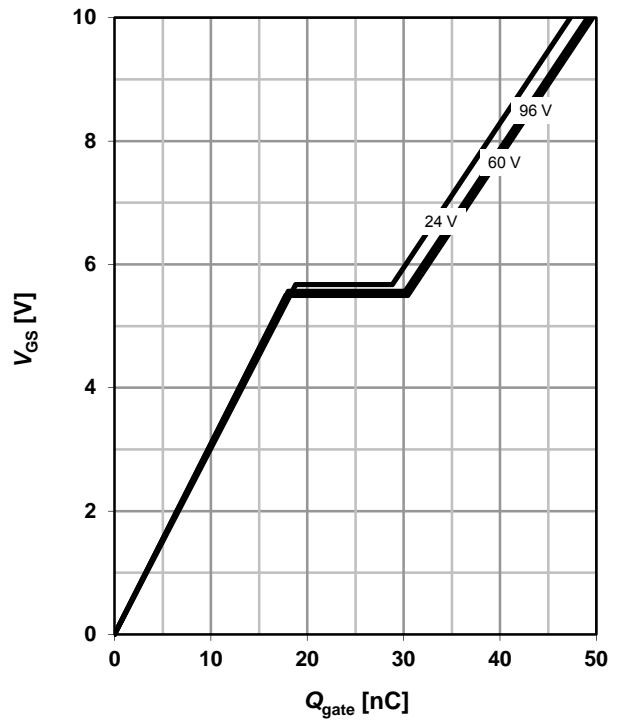
parameter: $T_{j(start)}$



14 Typ. gate charge

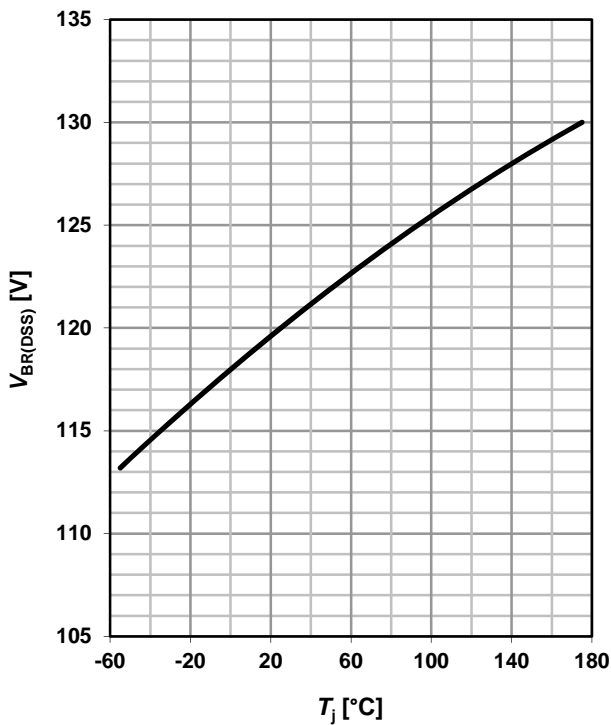
$V_{GS}=f(Q_{gate}); I_D=67 \text{ A pulsed}$

parameter: V_{DD}

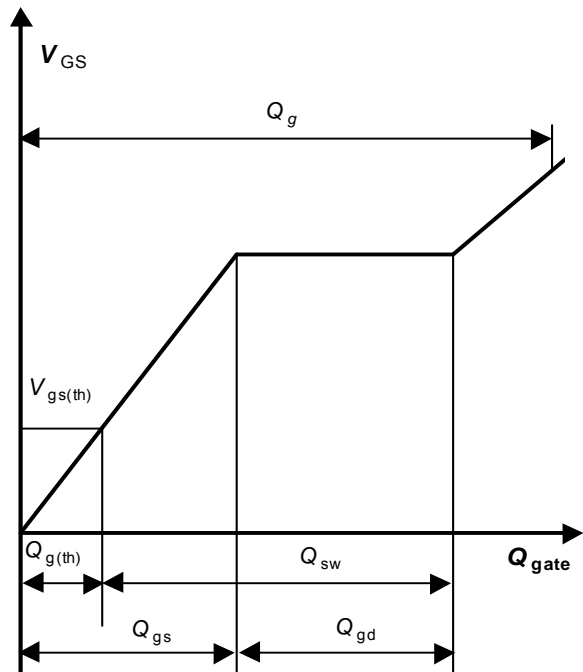


15 Drain-source breakdown voltage

$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$



16 Gate charge waveforms

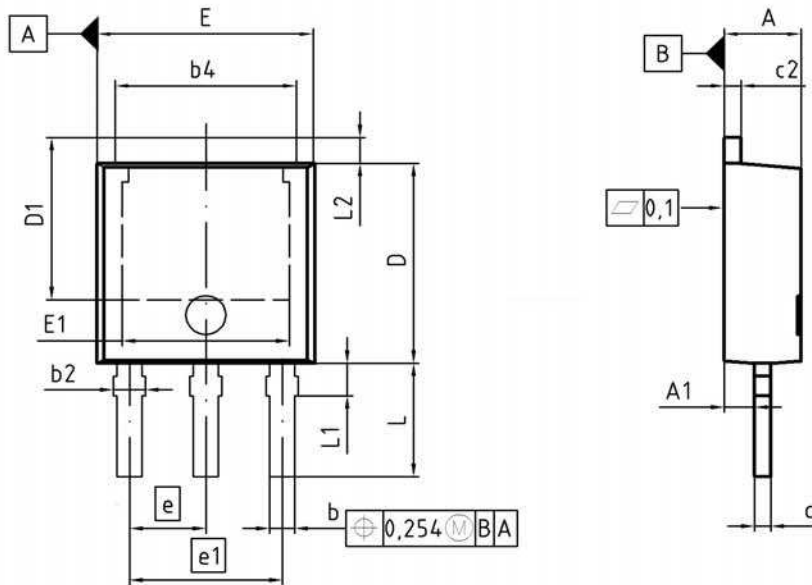




IPD110N12N3 G

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PG-TO-251SL : Outline



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.18	2.39	0.086	0.094
A1	0.80	1.14	0.031	0.045
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b4	4.95	5.50	0.195	0.217
c	0.46	0.58	0.018	0.023
c2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.04	5.44	0.198	0.214
E	6.35	6.73	0.250	0.265
E1	4.90	5.10	0.193	0.201
e	2.29		0.090	
e1	4.57		0.180	
N	3		3	
L	3.40	3.60	0.134	0.142
L1	0.90	1.10	0.035	0.043
L2	0.90	1.10	0.035	0.043

DOCUMENT NO.
Z8B00003329

SCALE

EUROPEAN PROJECTION

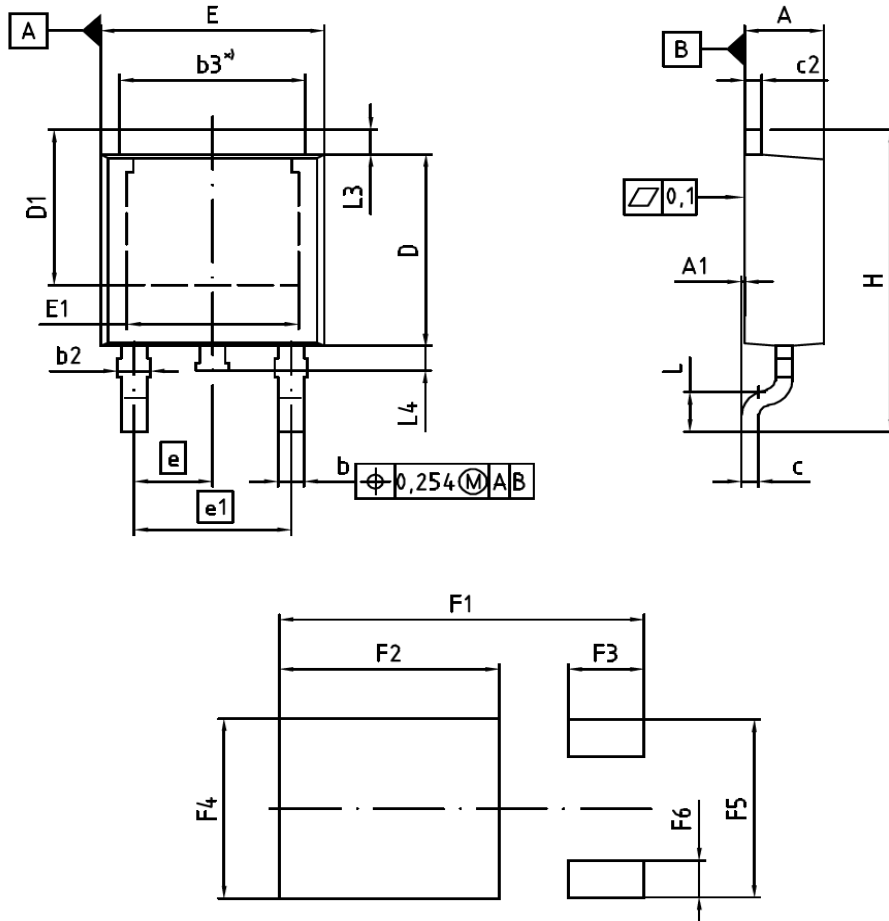
ISSUE DATE
17-01-2008

REVISION
03



IPD110N12N3 G
IPS110N12N3 G

PG-TO252-3: Outline



*) mold flash not included

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.16	2.41	0.085	0.095
A1	0.00	0.15	0.000	0.006
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b3	5.00	5.50	0.197	0.217
c	0.46	0.60	0.018	0.024
c2	0.46	0.98	0.018	0.039
D	5.97	6.22	0.235	0.245
D1	5.02	5.84	0.198	0.230
E	6.40	6.73	0.252	0.265
E1	4.70	5.21	0.185	0.205
e	2.29 (BSC)		0.090 (BSC)	
e1	4.57		0.180	
N	3		3	
H	9.40	10.48	0.370	0.413
L	1.18	1.70	0.046	0.067
L3	0.90	1.25	0.035	0.049
L4	0.51	1.00	0.020	0.039
F1	10.60		0.417	
F2	6.40		0.252	
F3	2.20		0.087	
F4	5.80		0.228	
F5	5.76		0.227	
F6	1.20		0.047	

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SCALE 0 2.0 4mm
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REVISION 04



Revision History

IPD_S110N12N3 G

Revision: 2015-07-16, Rev. 2.4

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.4	2015-07-16	Update VGS(th) and package outline TO252-3

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