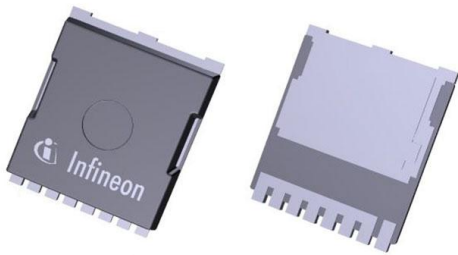


IPT012N08NF2SATMA1 Datasheet

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DiGi Electronics Part Number	IPT012N08NF2SATMA1-DG
Manufacturer	Infineon Technologies
Manufacturer Product Number	IPT012N08NF2SATMA1
Description	MOSFET
Detailed Description	N-Channel 80 V 39A (Ta), 351A (Tc) 3.8W (Ta), 300W (Tc) Surface Mount PG-HSOF-8

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Manufacturer Product Number:

IPT012N08NF2SATMA1

Series:

StrongIRFET™ 2

FET Type:

N-Channel

Drain to Source Voltage (Vdss):

80 V

Drive Voltage (Max Rds On, Min Rds On):

6V, 10V

Vgs(th) (Max) @ Id:

3.8V @ 267µA

Vgs (Max):

±20V

FET Feature:

-

Operating Temperature:

-55°C ~ 175°C (Tj)

Supplier Device Package:

PG-HSOF-8

Manufacturer:

Infineon Technologies

Product Status:

Active

Technology:

MOSFET (Metal Oxide)

Current - Continuous Drain (Id) @ 25°C:

39A (Ta), 351A (Tc)

Rds On (Max) @ Id, Vgs:

1.23mOhm @ 150A, 10V

Gate Charge (Qg) (Max) @ Vgs:

255 nC @ 10 V

Input Capacitance (Ciss) (Max) @ Vds:

12000 pF @ 40 V

Power Dissipation (Max):

3.8W (Ta), 300W (Tc)

Mounting Type:

Surface Mount

Package / Case:

8-PowerSFN

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8541.29.0095

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

MOSFET

StrongIRFET™ 2 Power-Transistor

Features

- Optimized for a wide range of applications
- N-Channel, normal level
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Qualified according to JEDEC Standard

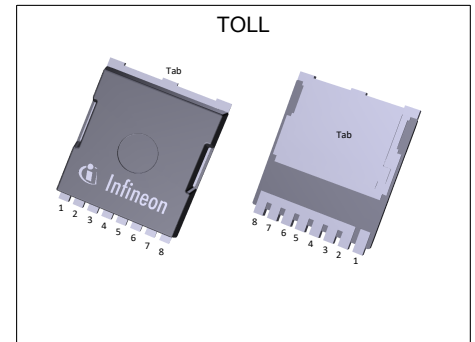
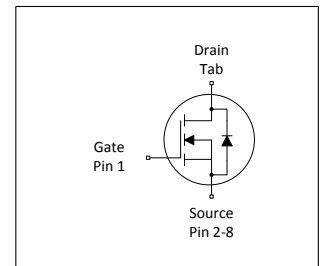


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	80	V
$R_{DS(on),max}$	1.23	m Ω
I_D	351	A
Q_{oss}	199	nC
Q_G	170	nC



RoHS

Type / Ordering Code	Package	Marking	Related Links
IPT012N08NF2S	PG-HSOF-8	012N08NS	-



StrongIRFET™ 2 Power-Transistor

IPT012N08NF2S

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StrongIRFET™ 2 Power-Transistor

IPT012N08NF2S

1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	351 248 211 39	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=6\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=40\text{ °C/W}^2)$
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	1404	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	374	mJ	$I_D=150\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	300 3.8	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{thJA}=40\text{ °C/W}^2)$
Operating and storage temperature	T_j , T_{stg}	-55	-	175	°C	-

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.5	°C/W	-
Thermal resistance, junction - ambient, 6 cm ² cooling area ²⁾	R_{thJA}	-	-	40	°C/W	-
Thermal resistance, junction - ambient, minimal footprint	R_{thJA}	-	-	62	°C/W	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

StrongIRFET™ 2 Power-Transistor

IPT012N08NF2S

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	80	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.2	3.0	3.8	V	$V_{DS}=V_{GS}$, $I_D=267\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	μA	$V_{DS}=80\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=80\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	1.1 1.3	1.23 1.8	m Ω	$V_{GS}=10\text{ V}$, $I_D=150\text{ A}$ $V_{GS}=6\text{ V}$, $I_D=75\text{ A}$
Gate resistance	R_G	-	1.4	-	Ω	-
Transconductance ¹⁾	g_{fs}	135	-	-	S	$ V_{DS} \geq 2 I_D R_{DS(on)max}$, $I_D=100\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	12000	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=40\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}	-	1900	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=40\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance	C_{rss}	-	83	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=40\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	25	-	ns	$V_{DD}=40\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	72	-	ns	$V_{DD}=40\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	72	-	ns	$V_{DD}=40\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Fall time	t_f	-	44	-	ns	$V_{DD}=40\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$

Table 6 Gate charge characteristics²⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	53	-	nC	$V_{DD}=40\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	36	-	nC	$V_{DD}=40\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	Q_{gd}	-	35	-	nC	$V_{DD}=40\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	Q_{sw}	-	53	-	nC	$V_{DD}=40\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total ¹⁾	Q_g	-	170	255	nC	$V_{DD}=40\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	4.4	-	V	$V_{DD}=40\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge	Q_{oss}	-	199	-	nC	$V_{DS}=40\text{ V}$, $V_{GS}=0\text{ V}$

¹⁾ Defined by design. Not subject to production test.

²⁾ See "Gate charge waveforms" for parameter definition

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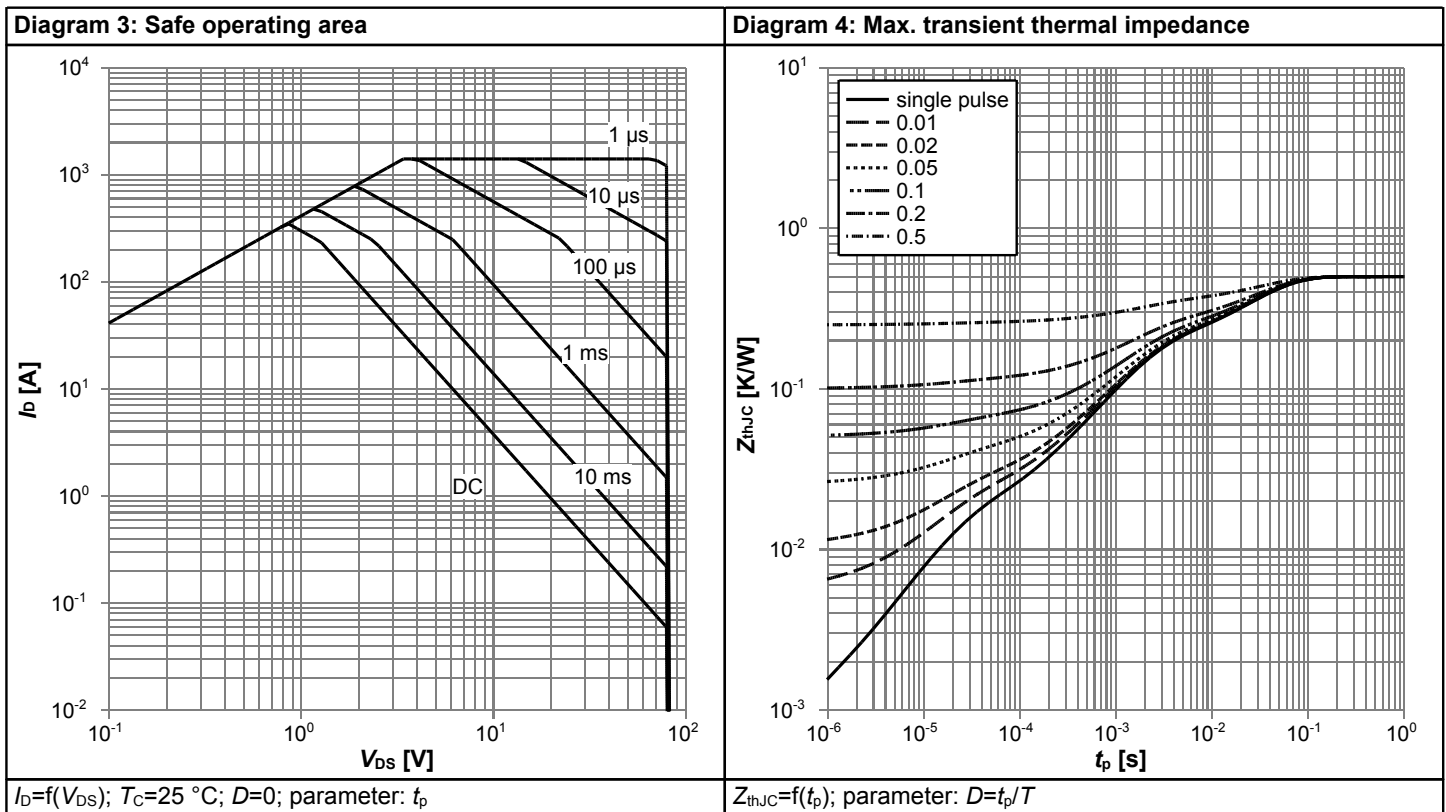
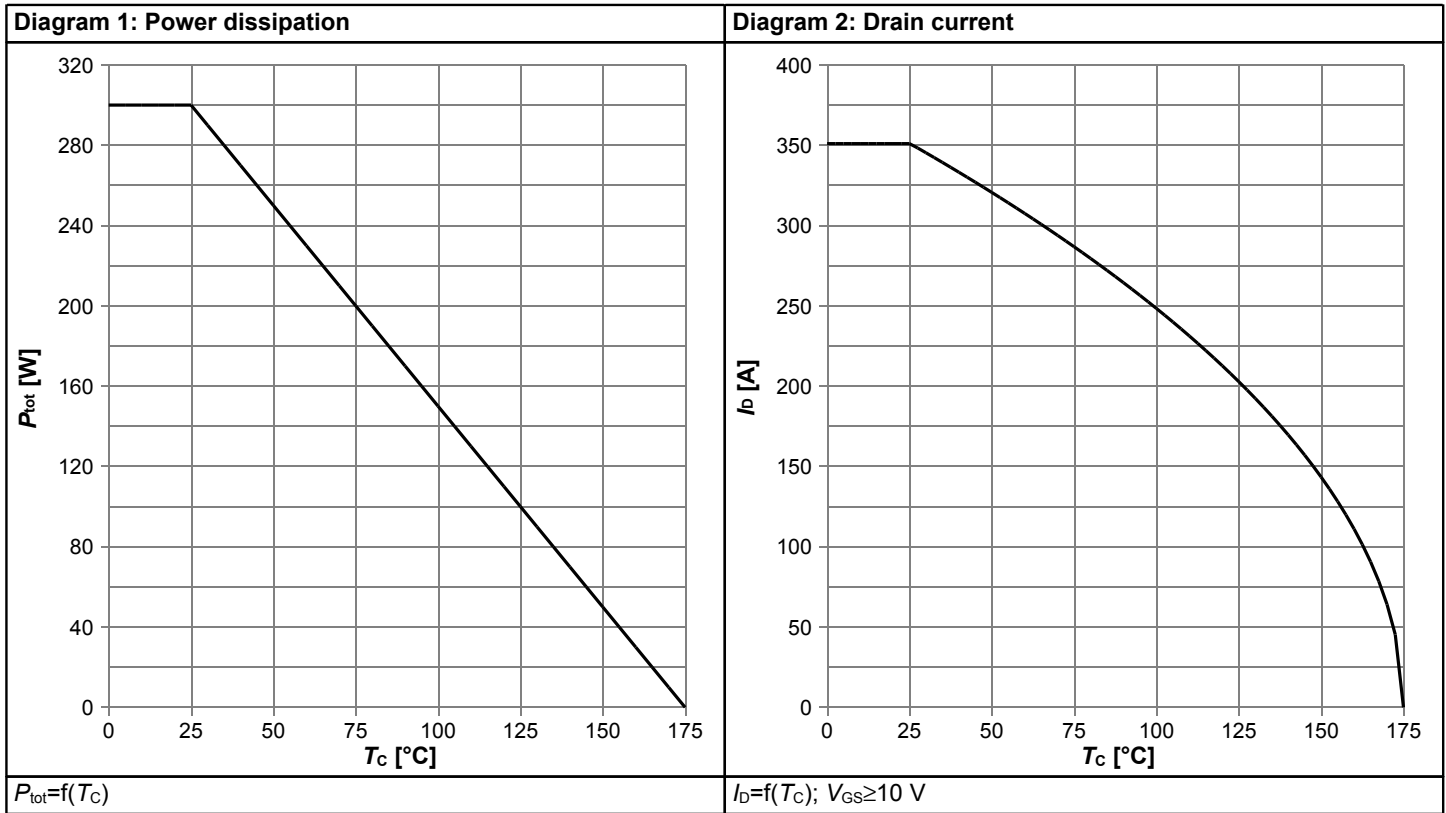
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	214	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	1404	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.85	1.2	V	$V_{GS}=0\text{ V}, I_F=100\text{ A}, T_j=25\text{ °C}$
Reverse recovery time	t_{rr}	-	48	-	ns	$V_R=40\text{ V}, I_F=100\text{ A}, di_F/dt=500\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}	-	383	-	nC	$V_R=40\text{ V}, I_F=100\text{ A}, di_F/dt=500\text{ A}/\mu\text{s}$



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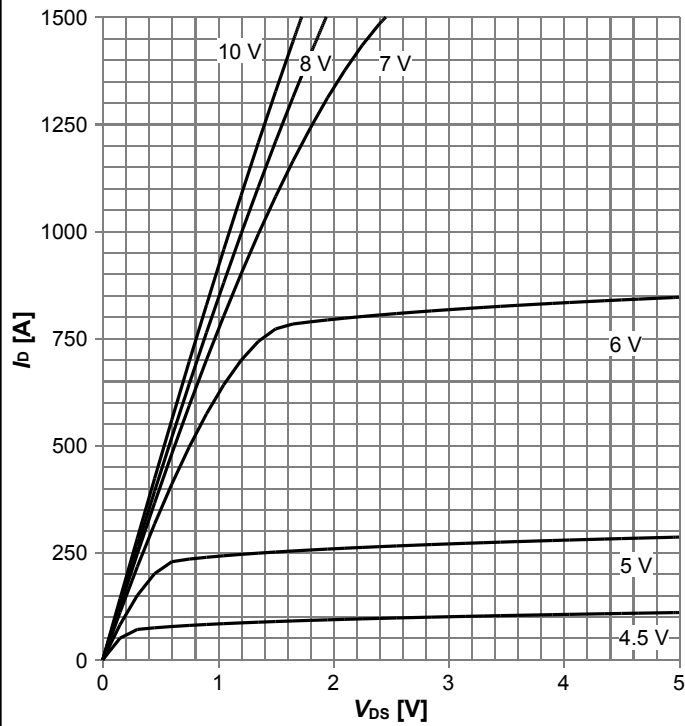
4 Electrical characteristics diagrams





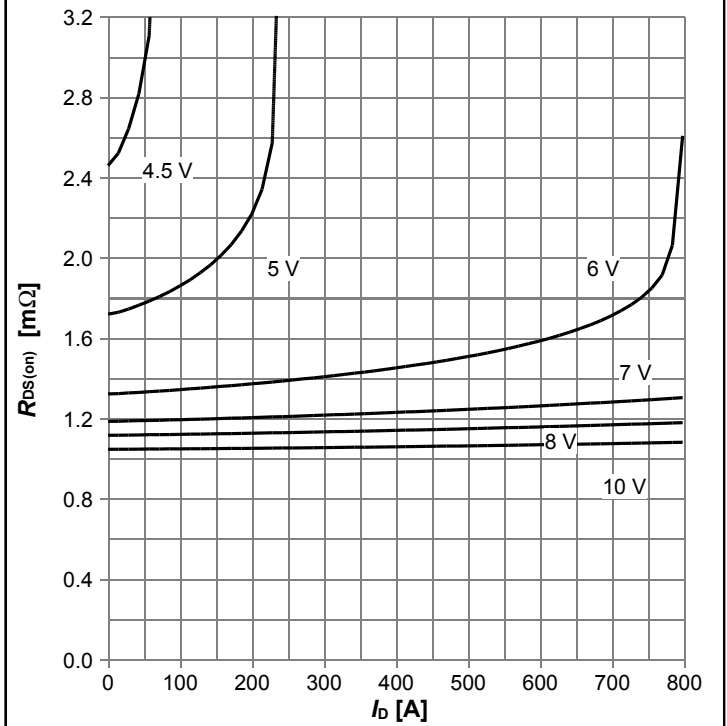
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Diagram 5: Typ. output characteristics



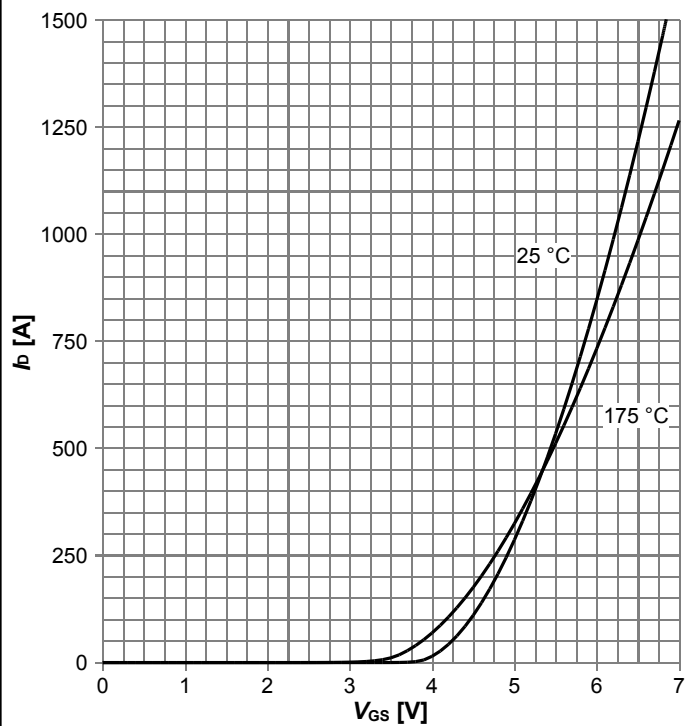
$I_D = f(V_{DS})$, $T_j = 25\text{ °C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



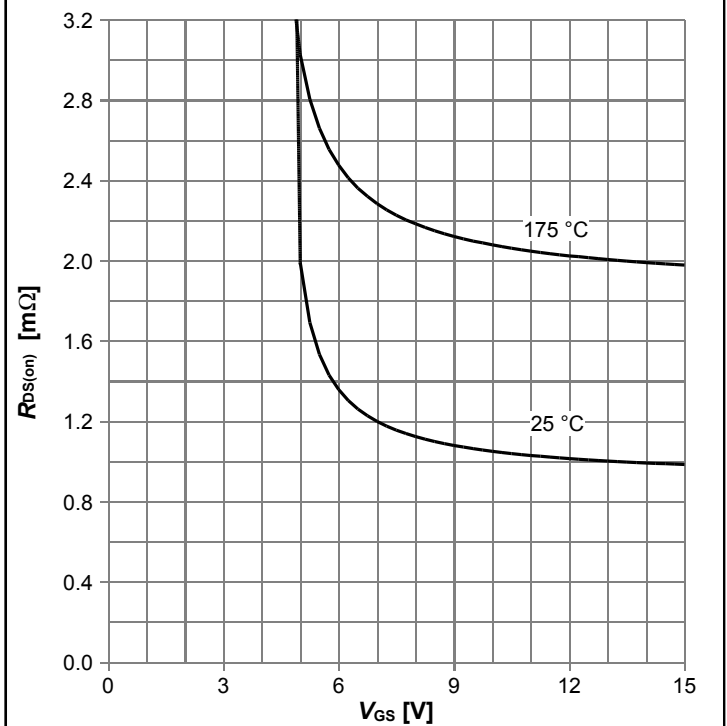
$R_{DS(on)} = f(I_D)$, $T_j = 25\text{ °C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



$I_D = f(V_{GS})$, $|V_{DS}| > 2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance

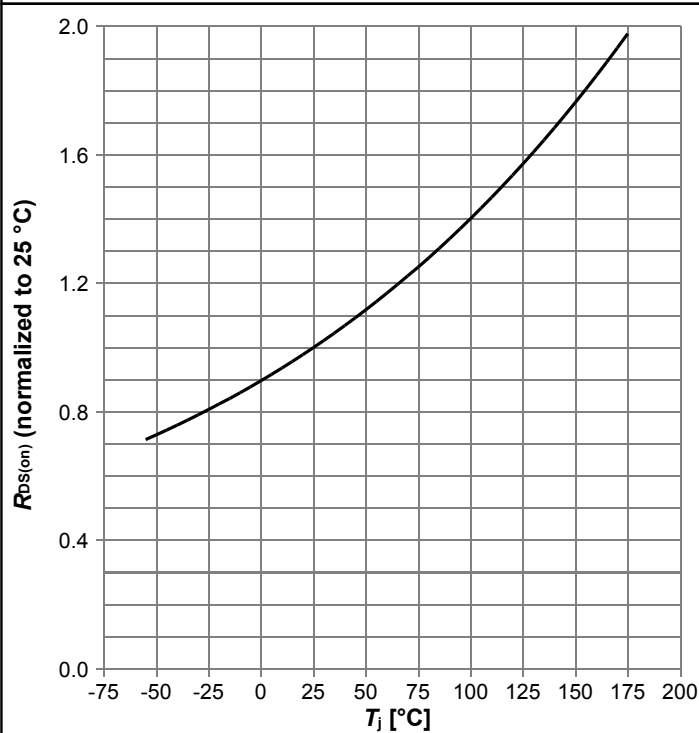


$R_{DS(on)} = f(V_{GS})$, $I_D = 150\text{ A}$; parameter: T_j



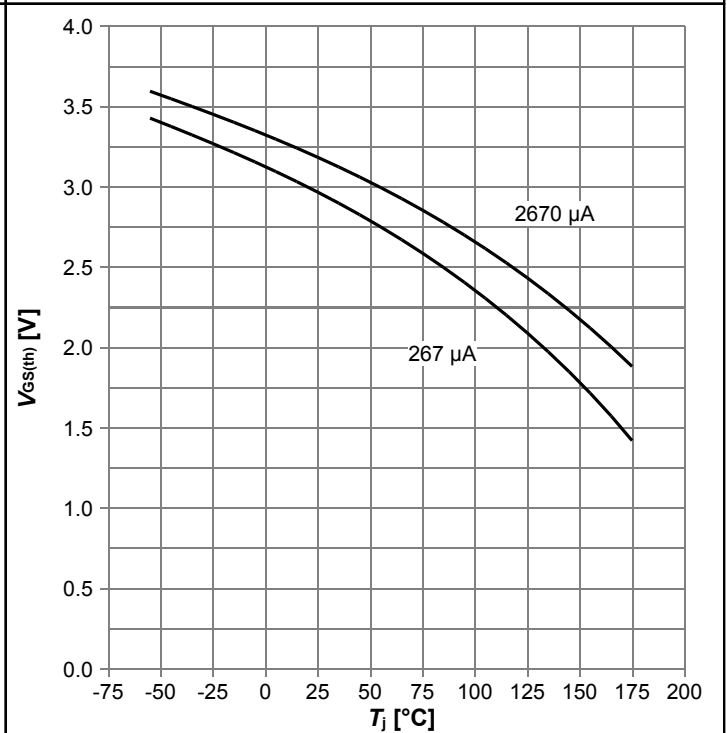
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Diagram 9: Normalized drain-source on resistance



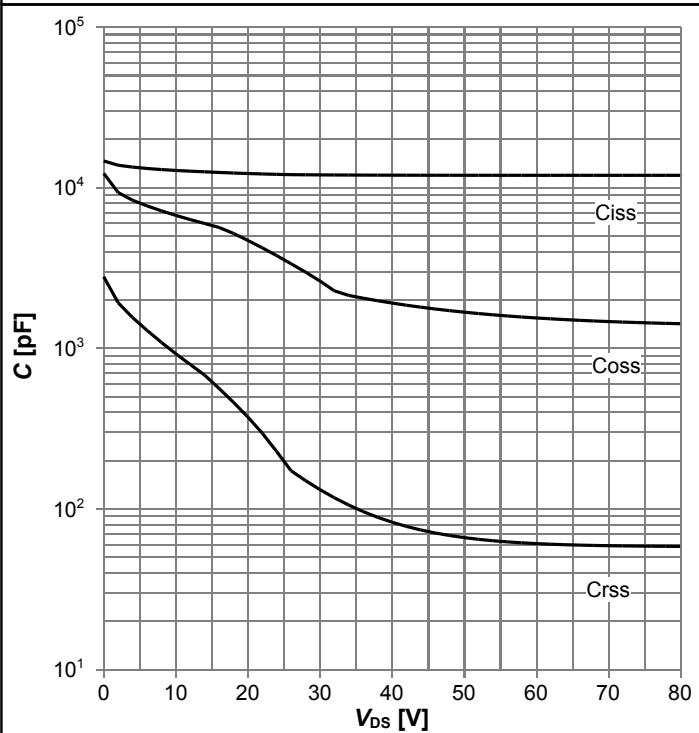
$R_{DS(on)}=f(T_j)$, $I_D=150$ A, $V_{GS}=10$ V

Diagram 10: Typ. gate threshold voltage



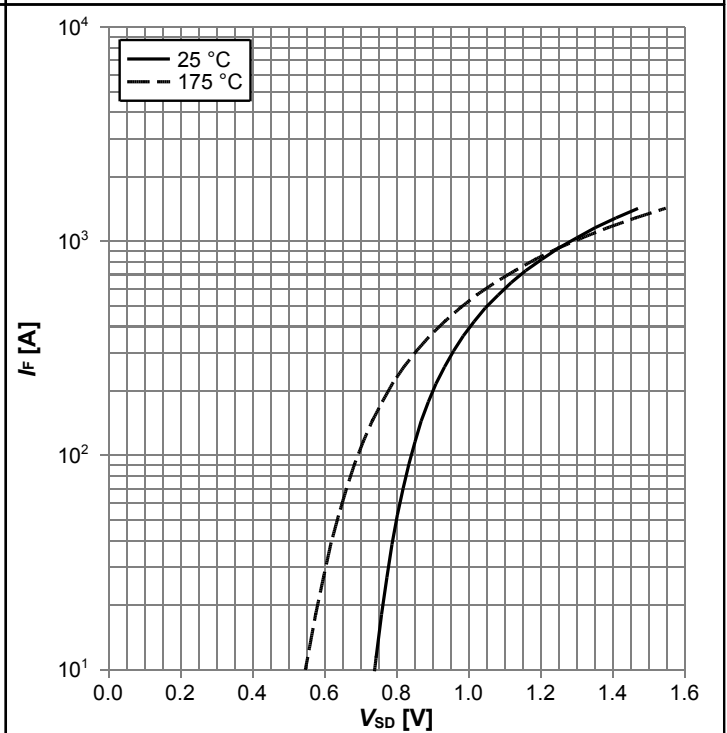
$V_{GS(th)}=f(T_j)$, $V_{GS}=V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz

Diagram 12: Typ. forward characteristics of reverse diode

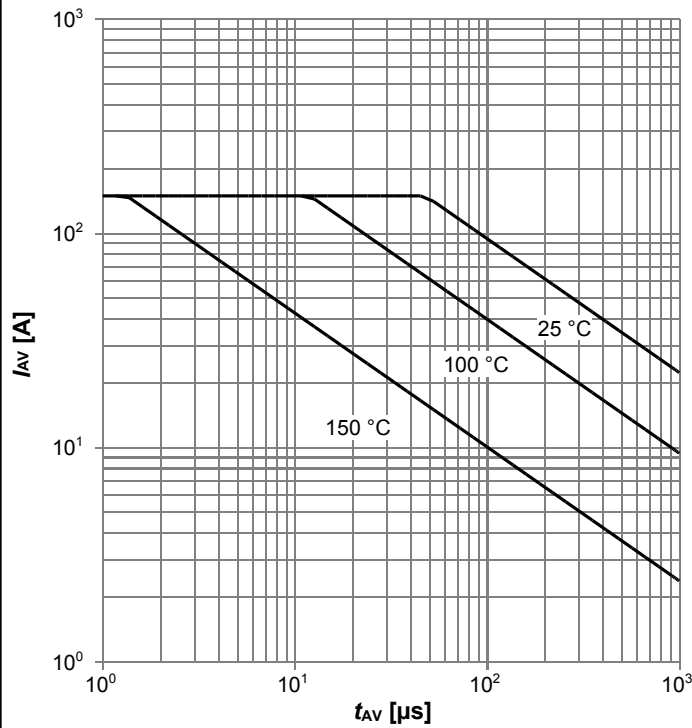


$I_F=f(V_{SD})$; parameter: T_j



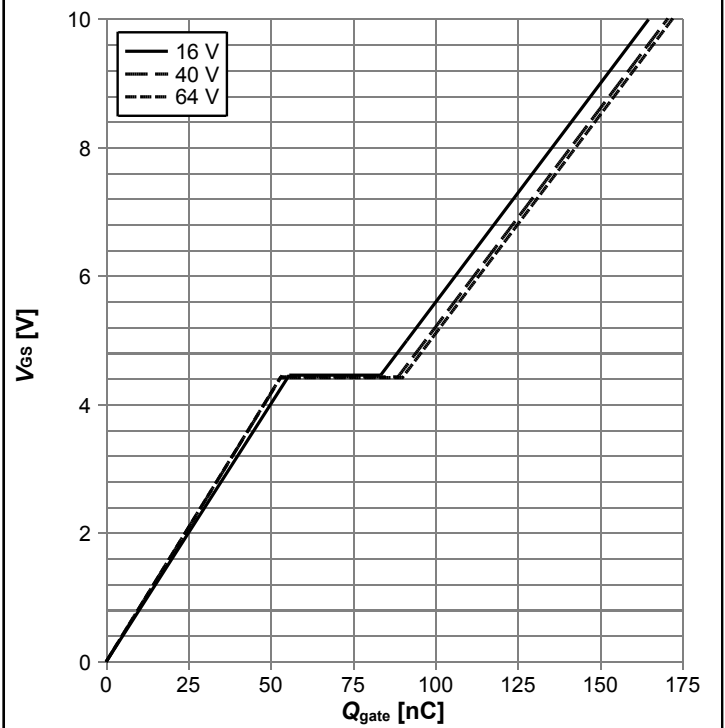
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Diagram 13: Avalanche characteristics



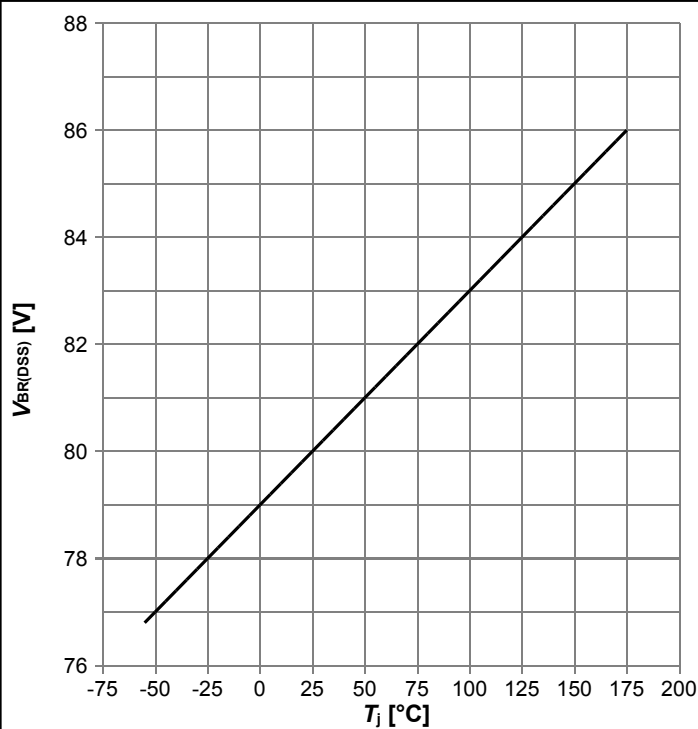
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



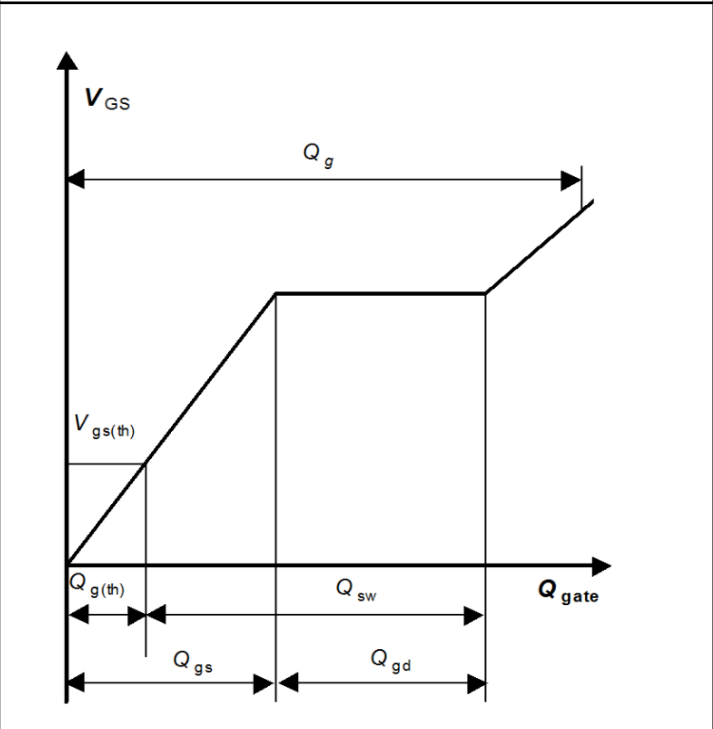
$V_{GS}=f(Q_{gate}), I_D=100$ A pulsed, $T_j=25$ °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j); I_D=1$ mA

Diagram Gate charge waveforms



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5 Package Outlines

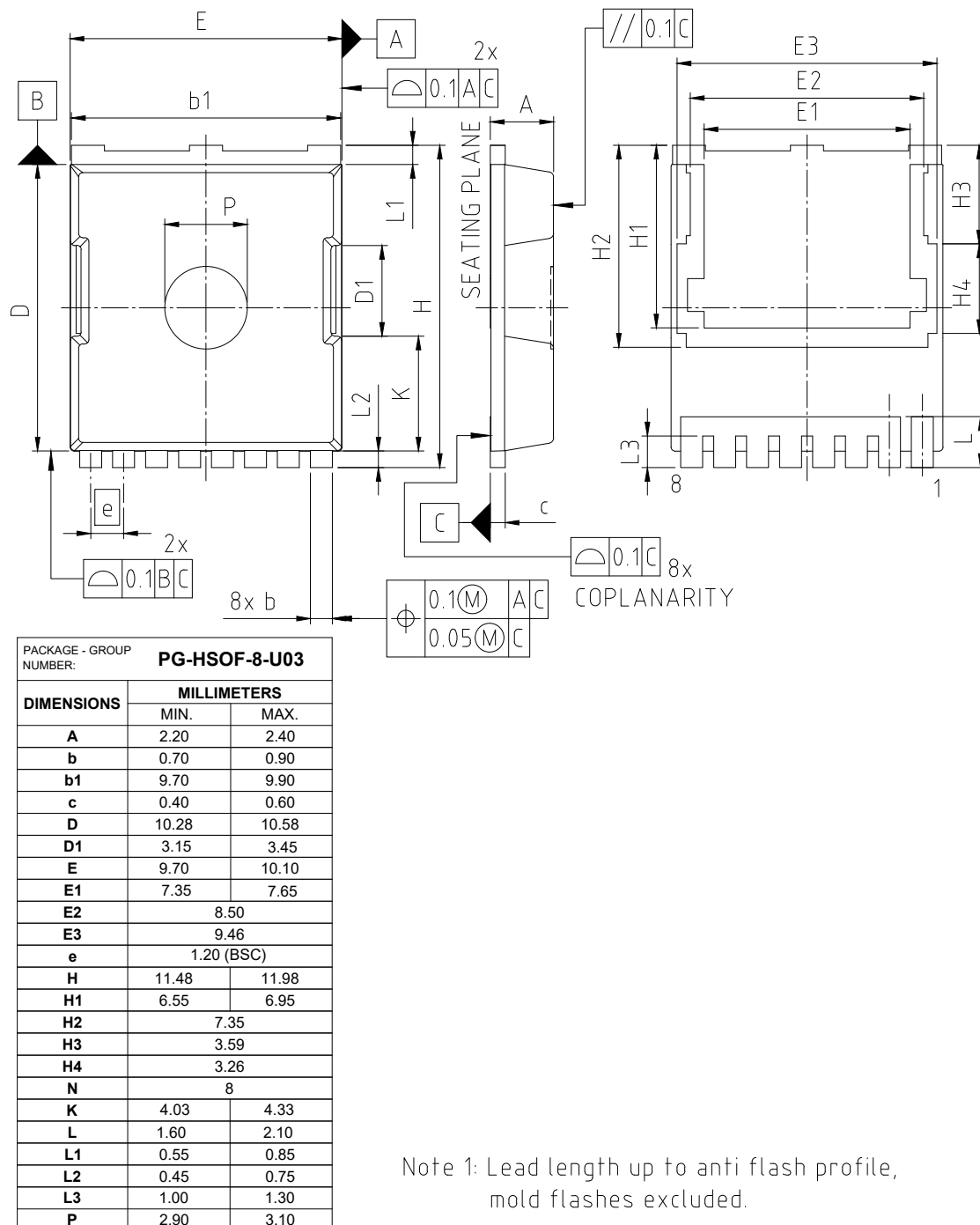


Figure 1 Outline PG-HSOF-8, dimensions in mm



StrongIRFET™ 2 Power-Transistor

IPT012N08NF2S

Revision History

IPT012N08NF2S

Revision: 2022-08-08, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2022-07-20	Release of final version
2.1	2022-08-08	Update current for Rds(on)

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