

IPT65R105G7XTMA1 Datasheet

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DiGi Electronics Part Number	IPT65R105G7XTMA1-DG
Manufacturer	Infineon Technologies
Manufacturer Product Number	IPT65R105G7XTMA1
Description	MOSFET N-CH 650V 24A 8HSOF
Detailed Description	N-Channel 650 V 24A (Tc) 156W (Tc) Surface Mount PG-HSOF-8-2



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Purchase and inquiry

Manufacturer Product Number:

IPT65R105G7XTMA1

Series:

CoolMOS™ C7

FET Type:

N-Channel

Drain to Source Voltage (Vdss):

650 V

Drive Voltage (Max Rds On, Min Rds On):

10V

Vgs(th) (Max) @ Id:

4V @ 440µA

Vgs (Max):

±20V

FET Feature:

-

Operating Temperature:

-55°C ~ 150°C (Tj)

Supplier Device Package:

PG-HSOF-8-2

Base Product Number:

IPT65R105

Manufacturer:

Infineon Technologies

Product Status:

Obsolete

Technology:

MOSFET (Metal Oxide)

Current - Continuous Drain (Id) @ 25°C:

24A (Tc)

Rds On (Max) @ Id, Vgs:

105mOhm @ 8.9A, 10V

Gate Charge (Qg) (Max) @ Vgs:

35 nC @ 10 V

Input Capacitance (Ciss) (Max) @ Vds:

1670 pF @ 400 V

Power Dissipation (Max):

156W (Tc)

Mounting Type:

Surface Mount

Package / Case:

8-PowerSFN

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8541.29.0095

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

MOSFET

650V CoolMOS™ C7 Gold series (G7) SJ Power Device

The C7 GOLD series (G7) for the first time brings together the benefits of the C7 GOLD CoolMOS™ technology, 4 pin Kelvin Source capability and the improved thermal properties of the TOLL package to enable a possible SMD solution for high current topologies such as PFC up to 3kW

Features

- C7 Gold gives best in class FOM $R_{DS(on)} * E_{oss}$ and $R_{DS(on)} * Q_g$.
- C7 Gold technology enables best in class $R_{DS(on)}$ in smallest footprint.
- TOLL package has inbuilt 4th pin Kelvin Source configuration and low parasitic source inductance (~1nH).
- TOLL package is MSL1 compliant, total Pb-free and has easy visual inspection grooved leads.
- TOLL SMD package combined with lead free die attach process enables improved thermal performance R_{th} .

Benefits

- C7 Gold FOM $R_{DS(on)} * Q_g$ is 14% better than previous C7 650V enabling faster switching leading to higher efficiency.
- C7 Gold can reach $33m\Omega$ in in TOLL $115mm^2$ footprint, whereas previous BIC C7 650V was $45m\Omega$ in $150mm^2$ D²PAK footprint.
- Reducing parasitic source inductance by Kelvin Source improves efficiency by faster switching and ease of use due to less ringing.
- TOLL package is easy to use and has the highest quality standards.
- Improved thermals enable SMD TOLL package to be used in higher current designs than has been previously possible.

Potential applications

PFC stages and hard switching PWM stages for e.g. Computing, Server, Telecom, UPS and Solar.

Product validation

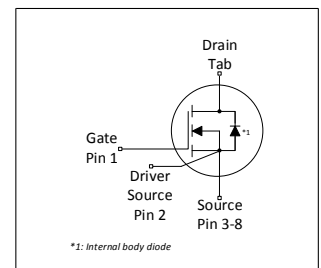
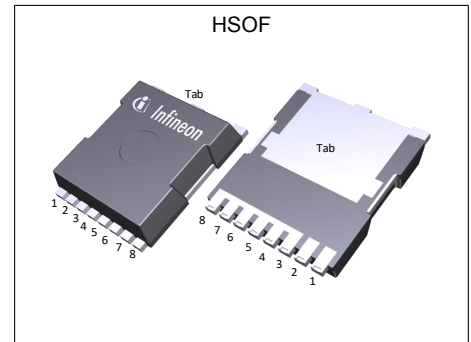
Fully qualified according to JEDEC for Industrial Applications

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	700	V
$R_{DS(on),max}$	105	$m\Omega$
$Q_{g,typ}$	35	nC
$I_{D,pulse}$	75	A
$I_{D,continuous} @ T_j < 150^\circ C$	32	A
$E_{oss}@400V$	4.2	μJ
Body diode di/dt	55	$A/\mu s$

Type / Ordering Code	Package	Marking	Related Links
IPT65R105G7	PG-HSOF-8	65R105G7	see Appendix A



RoHS



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650V CoolMOS™ C7 Gold series (G7) SJ Power Device

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1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	24 16	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	75	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	89	mJ	$I_D=7.1\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.44	mJ	$I_D=7.1\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche current, single pulse	I_{AS}	-	-	7.1	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	100	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC ($f>1\text{ Hz}$)
Power dissipation	P_{tot}	-	-	156	W	$T_C=25^\circ\text{C}$
Storage temperature	T_{stg}	-55	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_j	-55	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	n.a.	Ncm	-
Continuous diode forward current	I_S	-	-	24	A	$T_C=25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	75	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	1	V/ns	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di/dt	-	-	55	A/ μs	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$ see table 8
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms} , $T_C=25^\circ\text{C}$, $t=1\text{ min}$

¹⁾ Limited by $T_{j,max}$.

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Identical low side and high side switch



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2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.8	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	35	45	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm ² (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Soldering temperature, wave- & reflow soldering allowed	T_{sold}	-	-	260	°C	reflow MSL1

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3 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	$V_{GS}=0\text{V}$, $I_D=1\text{mA}$
Gate threshold voltage	$V_{(GS)th}$	3	3.5	4	V	$V_{DS}=V_{GS}$, $I_D=0.44\text{mA}$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=650$, $V_{GS}=0\text{V}$, $T_j=25^\circ\text{C}$ $V_{DS}=650$, $V_{GS}=0\text{V}$, $T_j=150^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20\text{V}$, $V_{DS}=0\text{V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.091	0.105	Ω	$V_{GS}=10\text{V}$, $I_D=8.9\text{A}$, $T_j=25^\circ\text{C}$ $V_{GS}=10\text{V}$, $I_D=8.9\text{A}$, $T_j=150^\circ\text{C}$
Gate resistance	R_G	-	1	-	Ω	$f=1\text{MHz}$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1670	-	pF	$V_{GS}=0\text{V}$, $V_{DS}=400\text{V}$, $f=250\text{kHz}$
Output capacitance	C_{oss}	-	26	-	pF	$V_{GS}=0\text{V}$, $V_{DS}=400\text{V}$, $f=250\text{kHz}$
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	53	-	pF	$V_{GS}=0\text{V}$, $V_{DS}=0\dots400\text{V}$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	579	-	pF	$I_D=\text{constant}$, $V_{GS}=0\text{V}$, $V_{DS}=0\dots400\text{V}$
Turn-on delay time	$t_{d(on)}$	-	13	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=8.9\text{A}$, $R_G=10\Omega$; see table 9
Rise time	t_r	-	7	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=8.9\text{A}$, $R_G=10\Omega$; see table 9
Turn-off delay time	$t_{d(off)}$	-	68	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=8.9\text{A}$, $R_G=10\Omega$; see table 9
Fall time	t_f	-	7	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=8.9\text{A}$, $R_G=10\Omega$; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{GS}	-	9	-	nC	$V_{DD}=400\text{V}$, $I_D=8.9\text{A}$, $V_{GS}=0$ to 10V
Gate to drain charge	Q_{gd}	-	11	-	nC	$V_{DD}=400\text{V}$, $I_D=8.9\text{A}$, $V_{GS}=0$ to 10V
Gate charge total	Q_g	-	35	-	nC	$V_{DD}=400\text{V}$, $I_D=8.9\text{A}$, $V_{GS}=0$ to 10V
Gate plateau voltage	$V_{plateau}$	-	5.4	-	V	$V_{DD}=400\text{V}$, $I_D=8.9\text{A}$, $V_{GS}=0$ to 10V

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V



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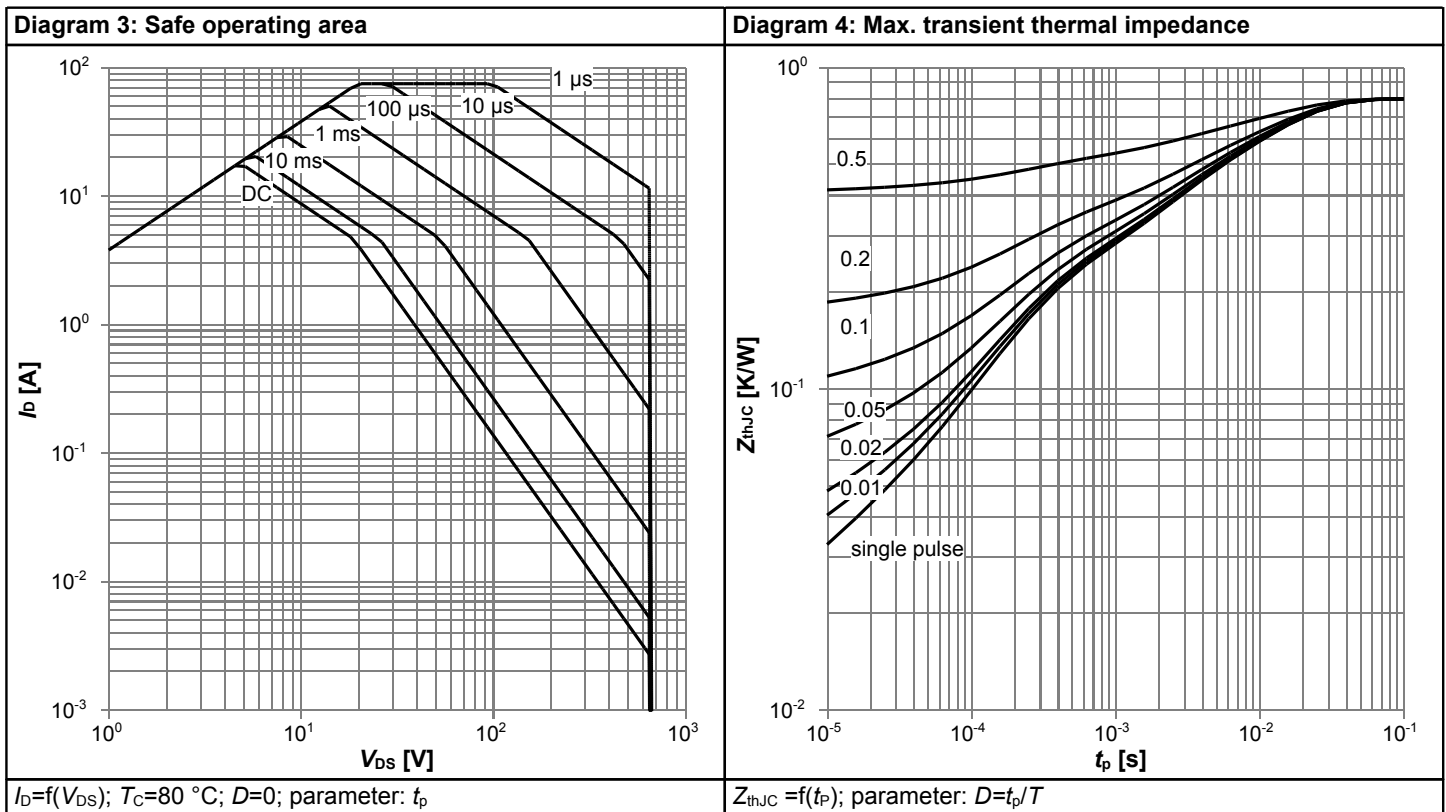
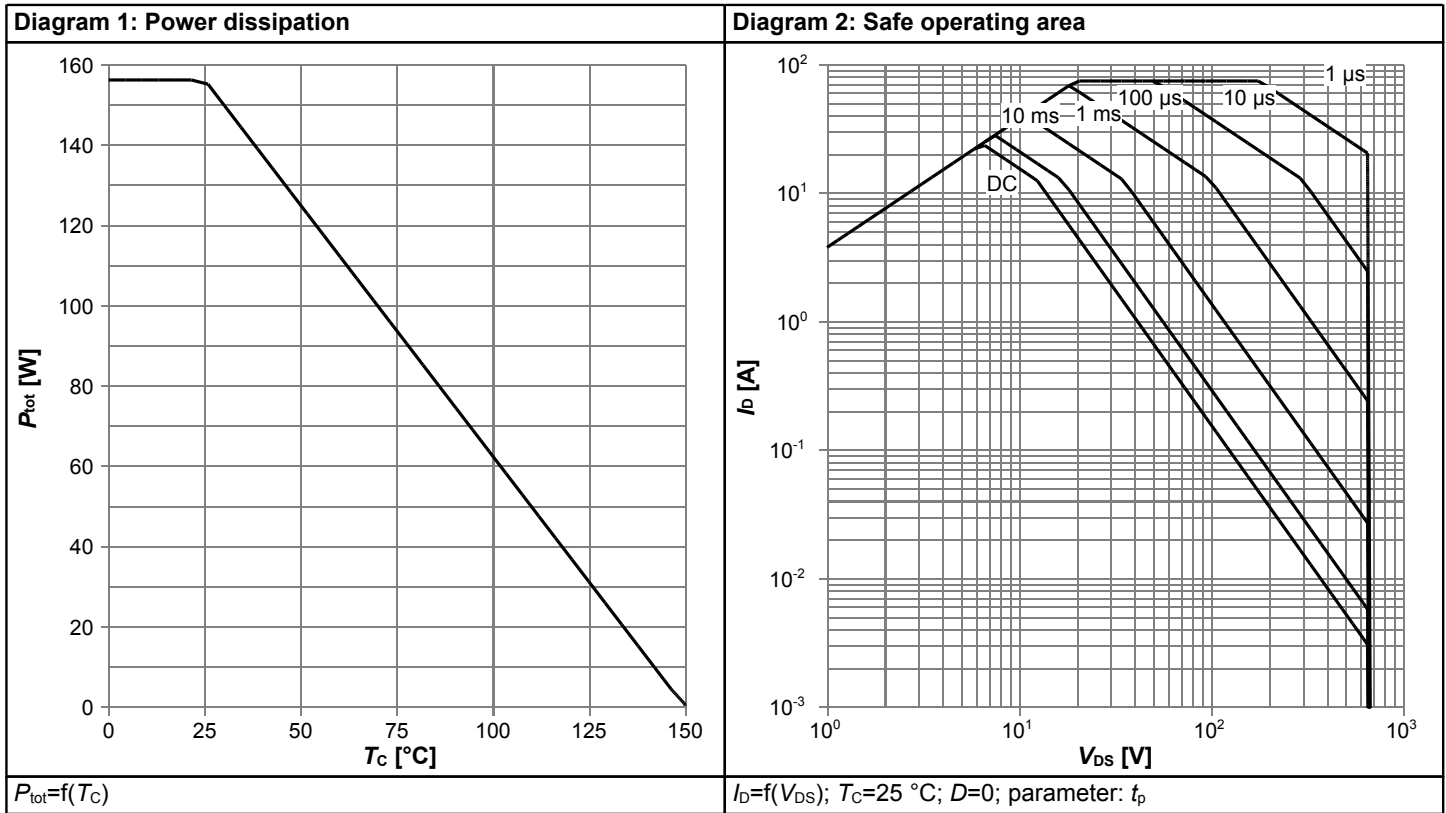
Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	$V_{GS}=0V, I_F=8.9A, T_j=25^\circ C$
Reverse recovery time	t_{rr}	-	460	-	ns	$V_R=400V, I_F=8.9A, di_F/dt=55A/\mu s$; see table 8
Reverse recovery charge	Q_{rr}	-	3.7	-	μC	$V_R=400V, I_F=8.9A, di_F/dt=55A/\mu s$; see table 8
Peak reverse recovery current	I_{rrm}	-	17	-	A	$V_R=400V, I_F=8.9A, di_F/dt=55A/\mu s$; see table 8



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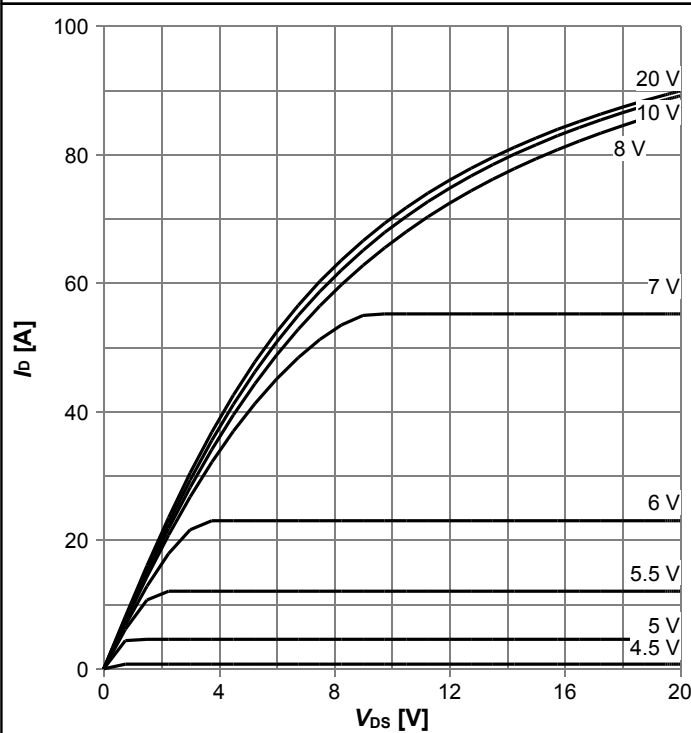
4 Electrical characteristics diagrams





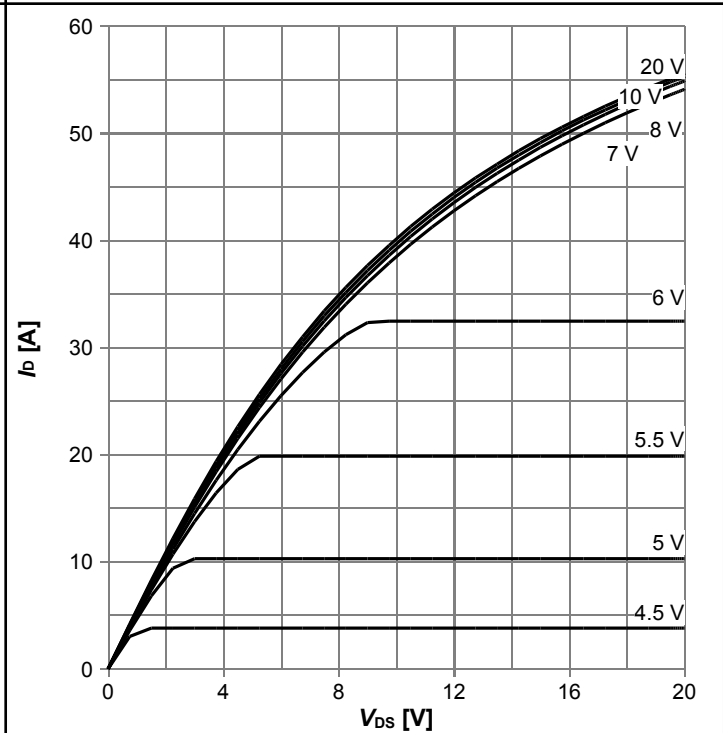
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Diagram 5: Typ. output characteristics



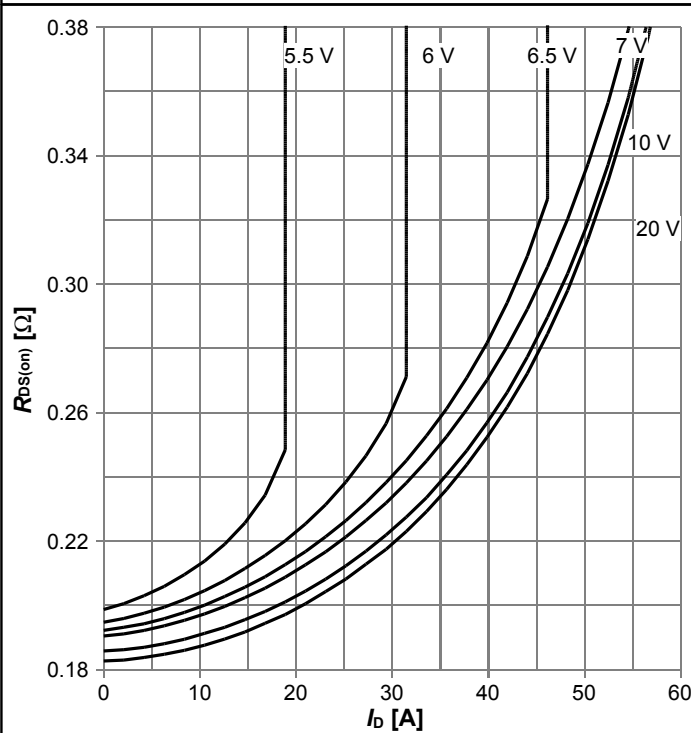
$I_D = f(V_{DS})$; $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. output characteristics



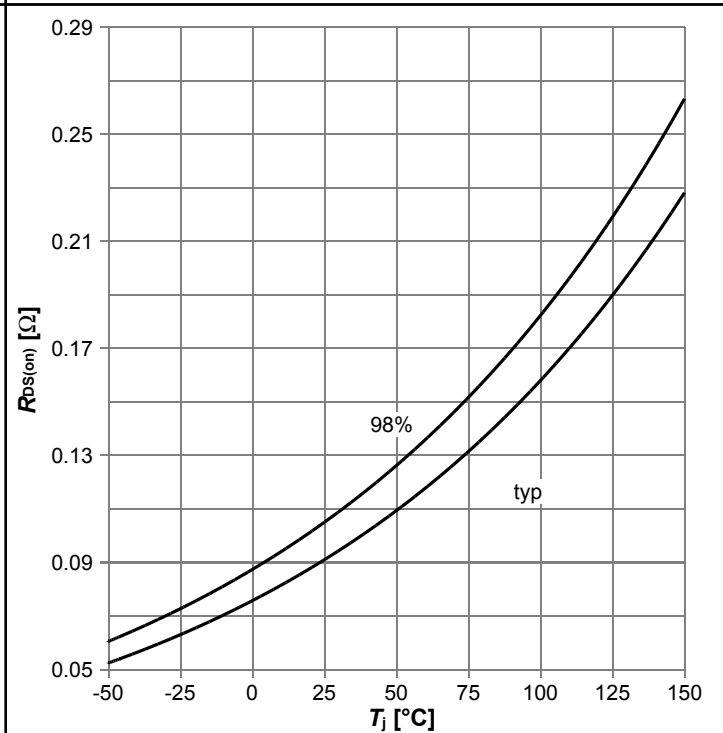
$I_D = f(V_{DS})$; $T_j = 125^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



$R_{DS(on)} = f(I_D)$; $T_j = 125^\circ\text{C}$; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance

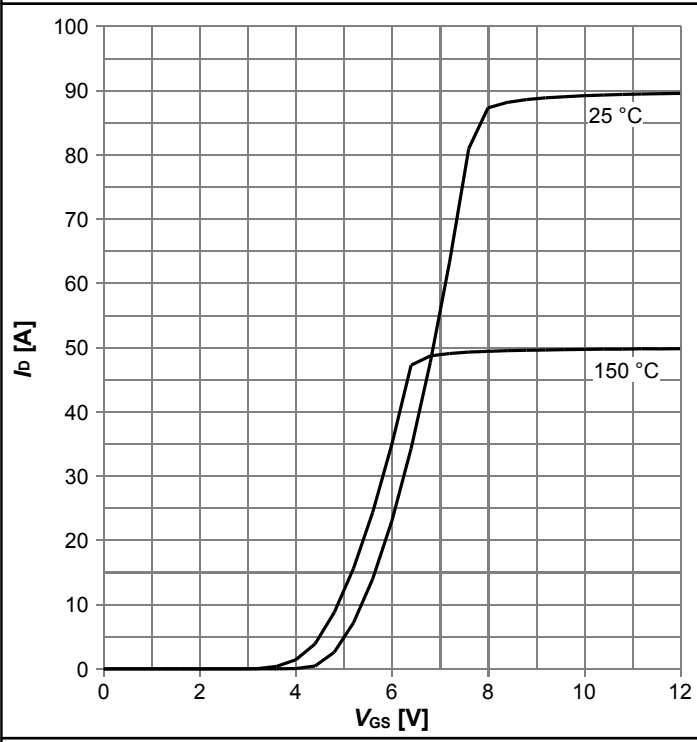


$R_{DS(on)} = f(T_j)$; $I_D = 8.9\text{ A}$; $V_{GS} = 10\text{ V}$



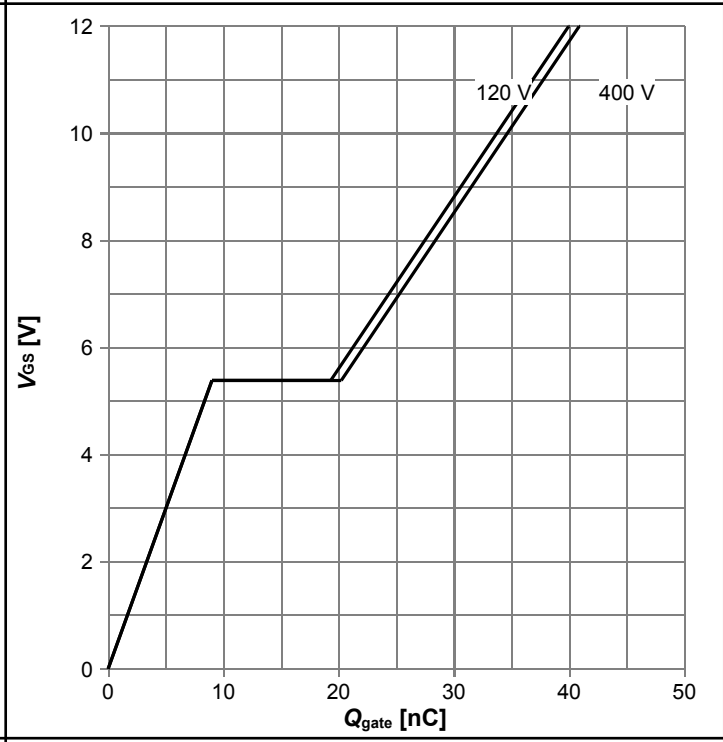
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Diagram 9: Typ. transfer characteristics



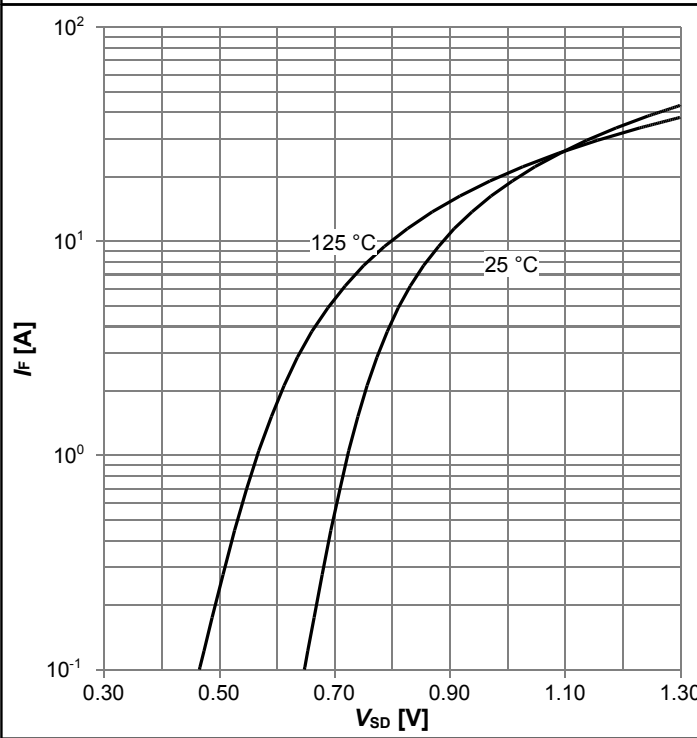
$I_D=f(V_{GS}); V_{DS}=20V; \text{parameter: } T_j$

Diagram 10: Typ. gate charge



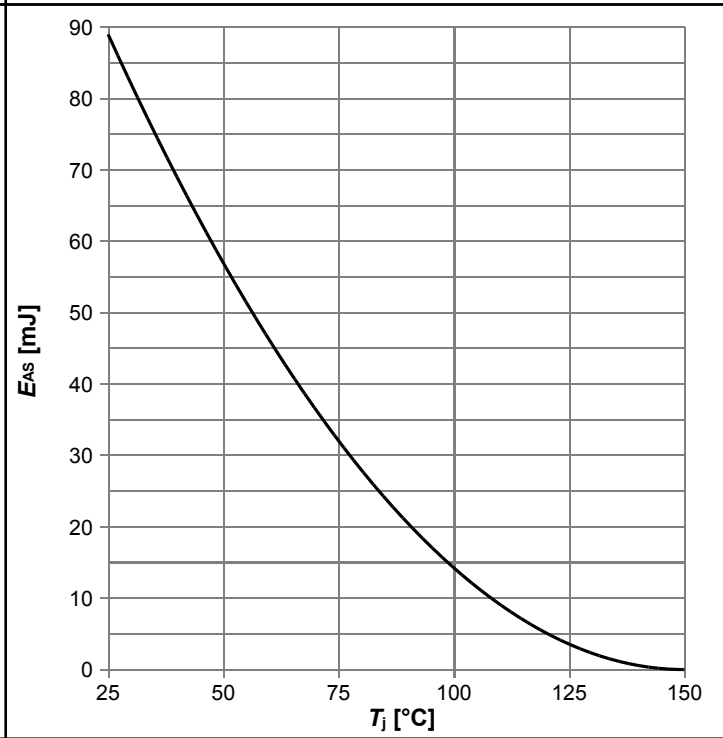
$V_{GS}=f(Q_{gate}); I_D=8.9A \text{ pulsed}; \text{parameter: } V_{DD}$

Diagram 11: Forward characteristics of reverse diode



$I_F=f(V_{SD}); \text{parameter: } T_j$

Diagram 12: Avalanche energy

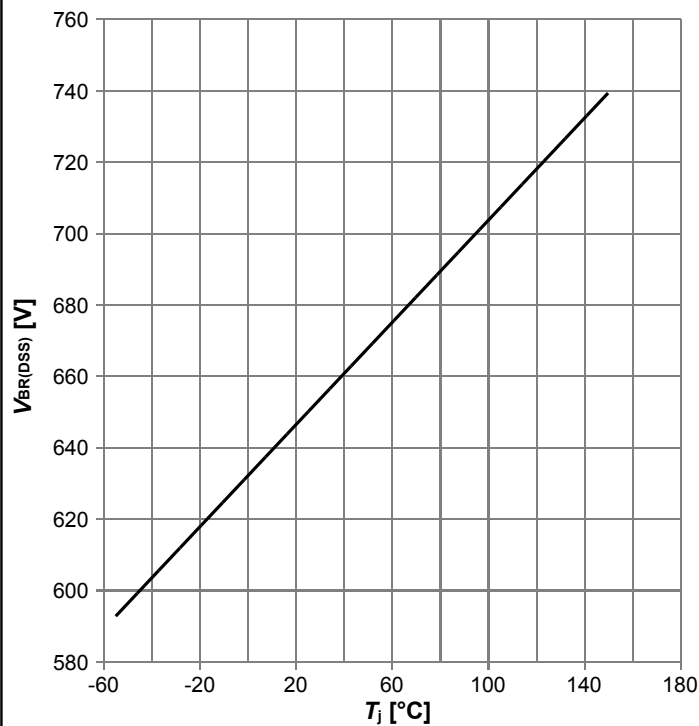


$E_{AS}=f(T_j); I_D=7.1 A; V_{DD}=50 V$



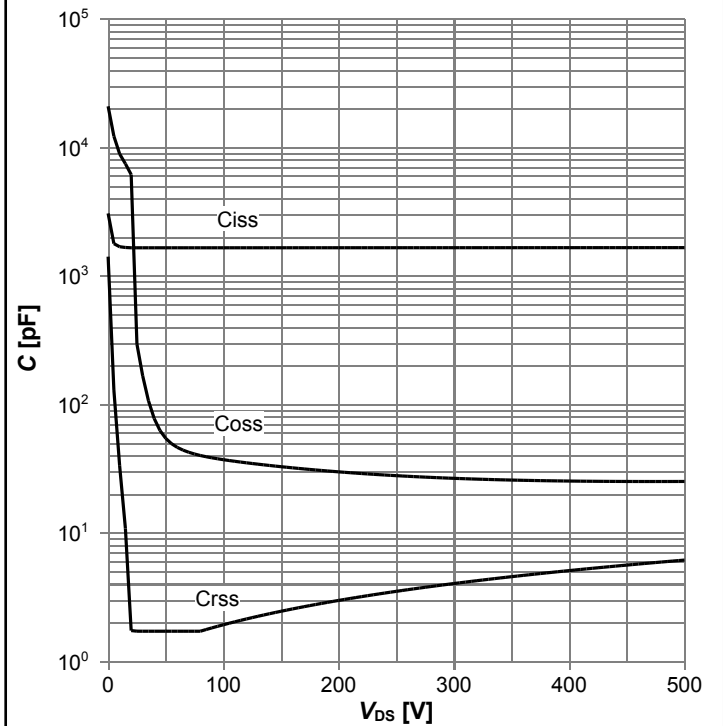
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Diagram 13: Drain-source breakdown voltage



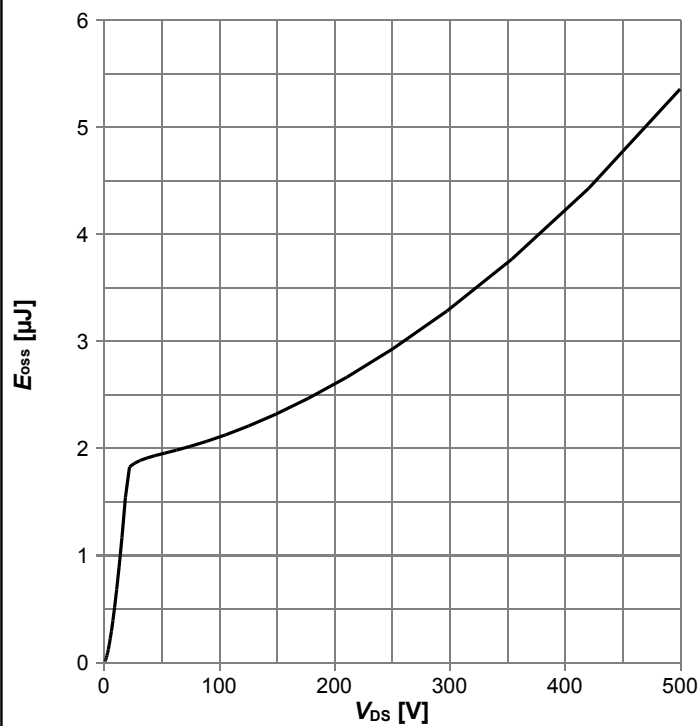
$V_{BR(DSS)}=f(T_j); I_D=1\text{ mA}$

Diagram 14: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0\text{ V}; f=250\text{ kHz}$

Diagram 15: Typ. Coss stored energy



$E_{oss}=f(V_{DS})$

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5 Test Circuits

Table 8 Diode characteristics

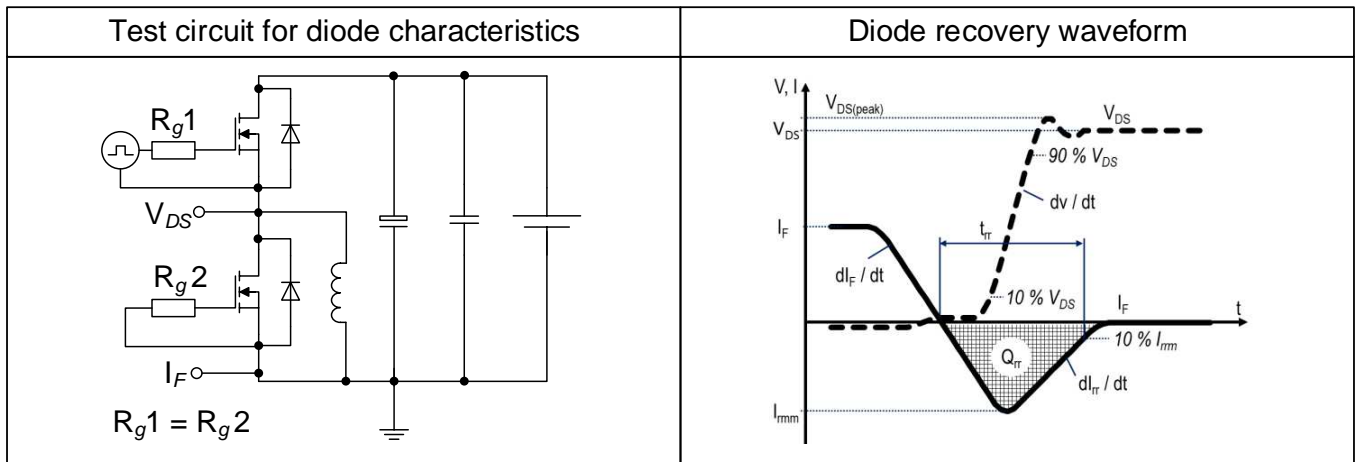


Table 9 Switching times (ss)

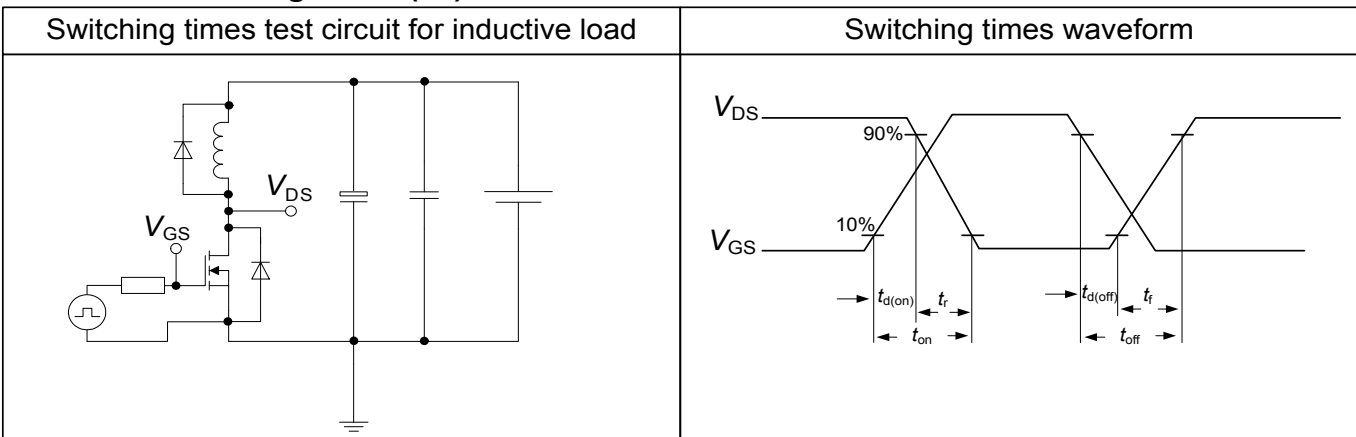
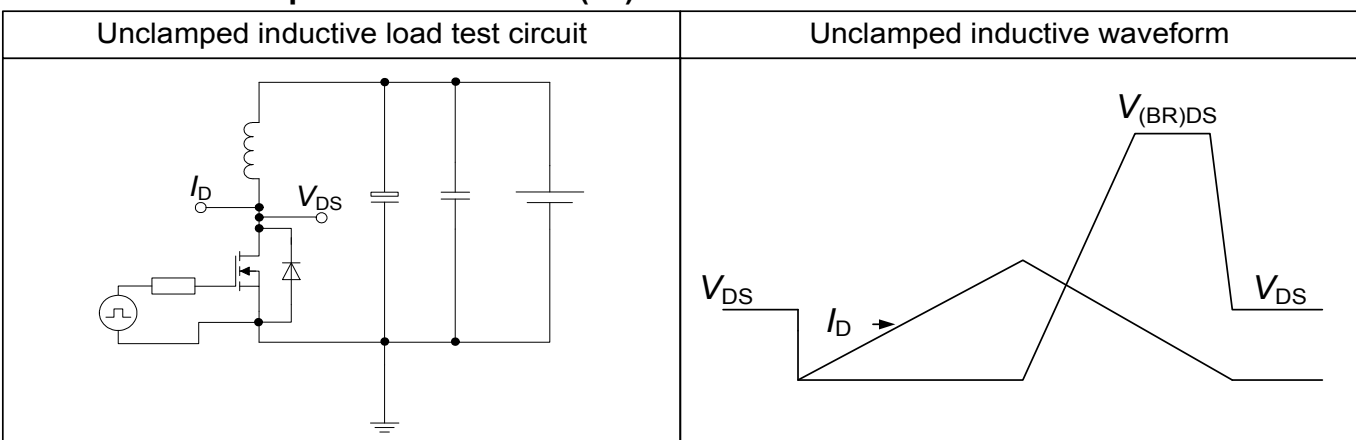


Table 10 Unclamped inductive load (ss)



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6 Package Outlines

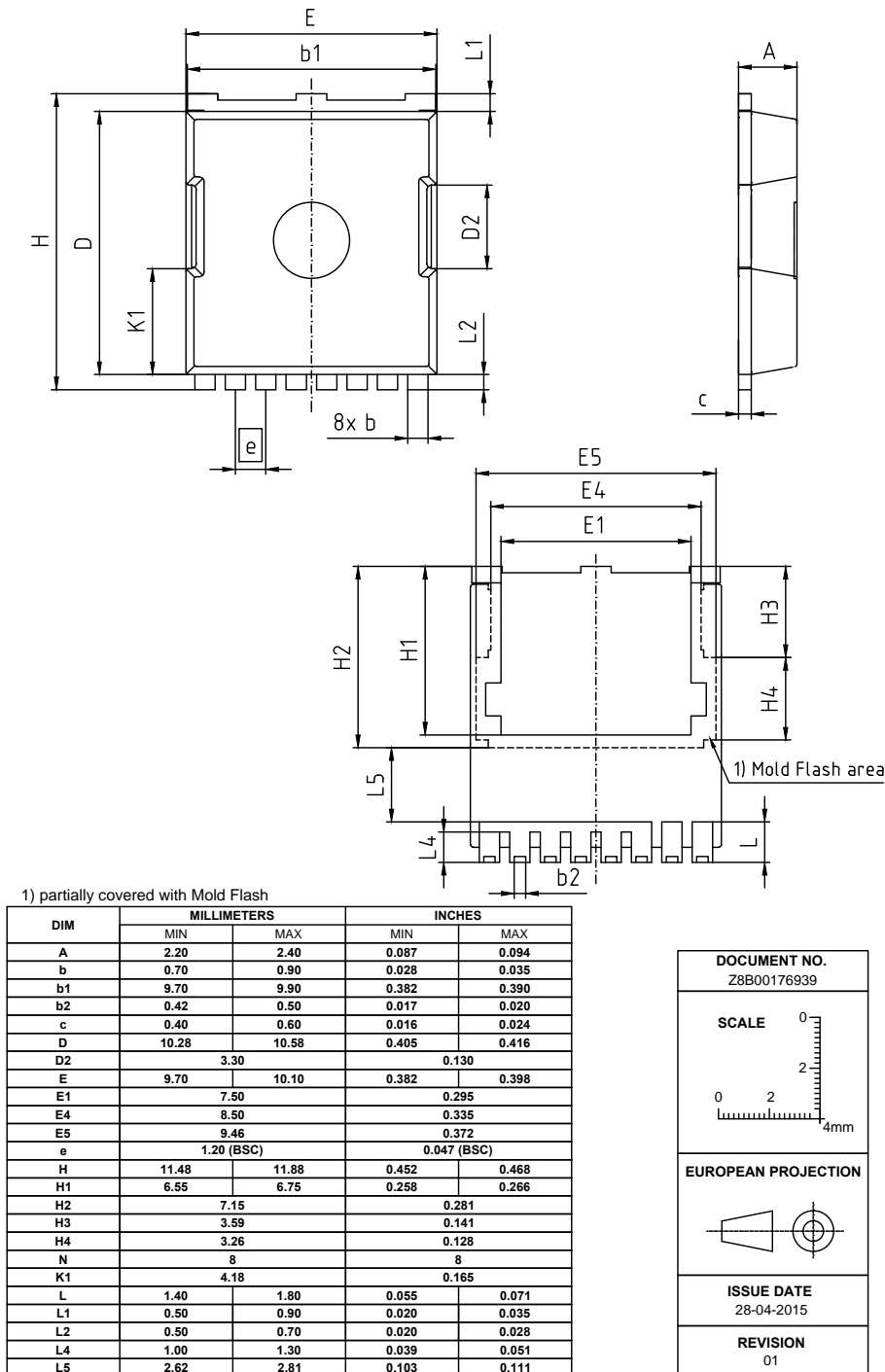


Figure 1 Outline PG-HSOF-8, dimensions in mm/inches



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7 Appendix A

Table 11 Related Links

- IFX CoolMOS™ G7 Webpage: www.infineon.com
- IFX CoolMOS™ G7 application note: www.infineon.com
- IFX CoolMOS™ G7 simulation model: www.infineon.com
- IFX Design tools: www.infineon.com



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Revision History

IPT65R105G7

Revision: 2020-10-28, Rev. 2.3

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2016-03-01	Release of final version
2.1	2016-03-14	Page 1 format update
2.2	2017-03-20	page1 marking changed
2.3	2020-10-28	Content update diagram 2,3,4,7,8 and format update

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