

IRF7105PBF Datasheet



DiGi Electronics Part Number	IRF7105PBF-DG
Manufacturer	Infineon Technologies
Manufacturer Product Number	IRF7105PBF
Description	MOSFET N/P-CH 25V 3.5A/2.3A 8SO
Detailed Description	Mosfet Array 25V 3.5A, 2.3A 2W Surface Mount 8-SO

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Purchase and inquiry

Manufacturer Product Number:

IRF7105PBF

Series:

HEXFET®

Technology:

MOSFET (Metal Oxide)

FET Feature:

-

Current - Continuous Drain (Id) @ 25°C:

3.5A, 2.3A

Vgs(th) (Max) @ Id:

3V @ 250µA

Input Capacitance (Ciss) (Max) @ Vds:

330pF @ 15V

Operating Temperature:

-55°C ~ 150°C (Tj)

Package / Case:

8-SOIC (0.154", 3.90mm Width)

Base Product Number:

IRF71

Manufacturer:

Infineon Technologies

Product Status:

Discontinued at Digi-Key

Configuration:

N and P-Channel

Drain to Source Voltage (Vdss):

25V

Rds On (Max) @ Id, Vgs:

100mOhm @ 1A, 10V

Gate Charge (Qg) (Max) @ Vgs:

27nC @ 10V

Power - Max:

2W

Mounting Type:

Surface Mount

Supplier Device Package:

8-SO

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8541.29.0095

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

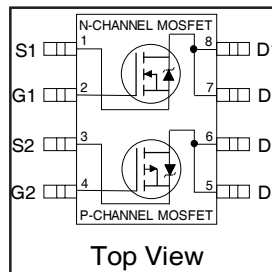
International IOR Rectifier

PD - 95164

IRF7105PbF

HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- Dual N and P Channel Mosfet
- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- Fast Switching
- Lead-Free

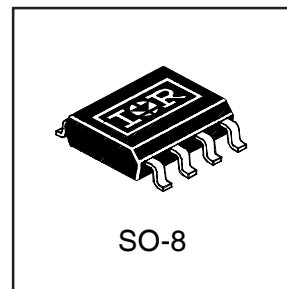


	N-Ch	P-Ch
V_{DSS}	25V	-25V
$R_{DS(on)}$	0.10Ω	0.25Ω
I_D	3.5A	-2.3A

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The SO-8 has been modified through a customized leadframe for enhanced thermal characteristics and multiple-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infra red, or wave soldering techniques. Power dissipation of greater than 0.8W is possible in a typical PCB mount application.



Absolute Maximum Ratings

	Parameter	Max.		Units
		N-Channel	P-Channel	
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	3.5	-2.3	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	2.8	-1.8	
I_{DM}	Pulsed Drain Current ①	14	-10	
$P_D @ T_C = 25^\circ C$	Power Dissipation	2.0		W
	Linear Derating Factor	0.016		W/°C
V_{GS}	Gate-to-Source Voltage	± 20		V
dv/dt	Peak Diode Recovery dv/dt ②	3.0	-3.0	V/nS
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150		°C

Thermal Resistance Ratings

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ④	—	—	62.5	°C/W

IRF7105PbF

International
IR RectifierElectrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Parameter	Description		Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	N-Ch	25	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
		P-Ch	-25	—	—		$V_{GS} = 0V, I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	N-Ch	—	0.030	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
		P-Ch	—	-0.015	—		Reference to $25^\circ\text{C}, I_D = -1\text{mA}$
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	N-Ch	—	0.083	0.10	Ω	$V_{GS} = 10V, I_D = 1.0A$ ③
		N-Ch	—	0.14	0.16		$V_{GS} = 4.5V, I_D = 0.50A$ ③
		P-Ch	—	0.16	0.25		$V_{GS} = -10V, I_D = -1.0A$ ③
		P-Ch	—	0.30	0.40		$V_{GS} = -4.5V, I_D = -0.50A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	N-Ch	1.0	—	3.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
		P-Ch	-1.0	—	-3.0		$V_{DS} = V_{GS}, I_D = -250\mu A$
g_{fs}	Forward Transconductance	N-Ch	—	4.3	—	S	$V_{DS} = 15V, I_D = 3.5A$ ③
		P-Ch	—	3.1	—		$V_{DS} = -15V, I_D = -3.5A$ ③
I_{DSS}	Drain-to-Source Leakage Current	N-Ch	—	—	2.0	μA	$V_{DS} = 20V, V_{GS} = 0V$
		P-Ch	—	—	-2.0		$V_{DS} = -20V, V_{GS} = 0V$
		N-Ch	—	—	25		$V_{DS} = 20V, V_{GS} = 0V, T_J = 55^\circ\text{C}$
		P-Ch	—	—	-25		$V_{DS} = -20V, V_{GS} = 0V, T_J = 55^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	N-P	—	—	± 100	$V_{GS} = \pm 20V$	
Q_g	Total Gate Charge	N-Ch	—	9.4	27	nC	N-Channel $I_D = 2.3A, V_{DS} = 12.5V, V_{GS} = 10V$ ③
P-Ch	—	10	25				
Q_{gs}	Gate-to-Source Charge	N-Ch	—	1.7	—	nC	P-Channel $I_D = -2.3A, V_{DS} = -12.5V, V_{GS} = -10V$
P-Ch	—	1.9	—				
Q_{gd}	Gate-to-Drain ("Miller") Charge	N-Ch	—	3.1	—	nC	P-Channel $I_D = -2.3A, V_{DS} = -12.5V, V_{GS} = -10V$
P-Ch	—	2.8	—				
$t_{d(on)}$	Turn-On Delay Time	N-Ch	—	7.0	20	ns	N-Channel $V_{DD} = 25V, I_D = 1.0A, R_G = 6.0\Omega, R_D = 25\Omega$ ③
P-Ch	—	12	40				
t_r	Rise Time	N-Ch	—	9.0	20	ns	P-Channel $V_{DD} = -25V, I_D = -1.0A, R_G = 6.0\Omega, R_D = 25\Omega$ ③
P-Ch	—	13	40				
$t_{d(off)}$	Turn-Off Delay Time	N-Ch	—	45	90	ns	P-Channel $V_{DD} = -25V, I_D = -1.0A, R_G = 6.0\Omega, R_D = 25\Omega$ ③
P-Ch	—	45	90				
t_f	Fall Time	N-Ch	—	25	50	ns	P-Channel $V_{DD} = -25V, I_D = -1.0A, R_G = 6.0\Omega, R_D = 25\Omega$ ③
P-Ch	—	37	50				
L_D	Internal Drain Inductance	N-P	—	4.0	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	N-P	—	6.0	—		
C_{iss}	Input Capacitance	N-Ch	—	330	—	pF	N-Channel $V_{GS} = 0V, V_{DS} = 15V, f = 1.0\text{MHz}$
		P-Ch	—	290	—		
C_{oss}	Output Capacitance	N-Ch	—	250	—	pF	P-Channel $V_{GS} = 0V, V_{DS} = -15V, f = 1.0\text{MHz}$
		P-Ch	—	210	—		
C_{riss}	Reverse Transfer Capacitance	N-Ch	—	61	—	pF	P-Channel $V_{GS} = 0V, V_{DS} = -15V, f = 1.0\text{MHz}$
P-Ch	—	67	—				

Source-Drain Ratings and Characteristics

Parameter	Description		Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	N-Ch	—	—	2.0	A	
		P-Ch	—	—	-2.0		
I_{SM}	Pulsed Source Current (Body Diode) ①	N-Ch	—	—	14	A	
		P-Ch	—	—	-9.2		
V_{SD}	Diode Forward Voltage	N-Ch	—	—	1.2	V	$T_J = 25^\circ\text{C}, I_S = 1.3A, V_{GS} = 0V$ ③
		P-Ch	—	—	-1.2		$T_J = 25^\circ\text{C}, I_S = -1.3A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	N-Ch	—	36	54	ns	N-Channel $T_J = 25^\circ\text{C}, I_F = 1.3A, di/dt = 100A/\mu s$ ③
		P-Ch	—	69	100		
Q_{rr}	Reverse Recovery Charge	N-Ch	—	41	75	nC	P-Channel $T_J = 25^\circ\text{C}, I_F = -1.3A, di/dt = 100A/\mu s$ ③
		P-Ch	—	90	180		
t_{on}	Forward Turn-On Time	N-P	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② N-Channel $I_{SD} \leq 3.5A, di/dt \leq 90A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$
P-Channel $I_{SD} \leq -2.3A, di/dt \leq 90A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$
- ③ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ④ Surface mounted on FR-4 board, $t \leq 10\text{sec}$.

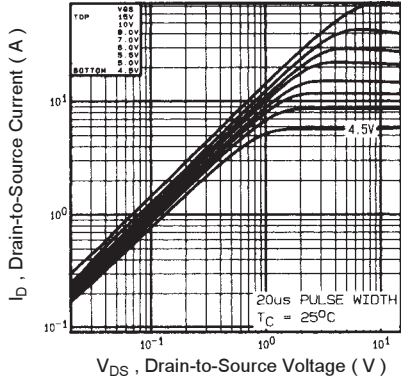


Fig 1. Typical Output Characteristics

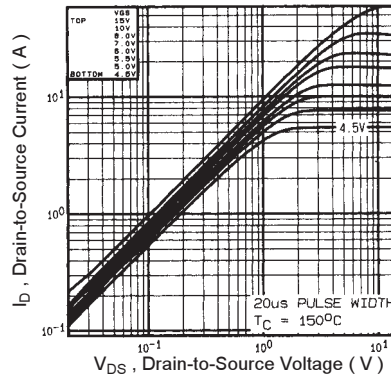


Fig 2. Typical Output Characteristics

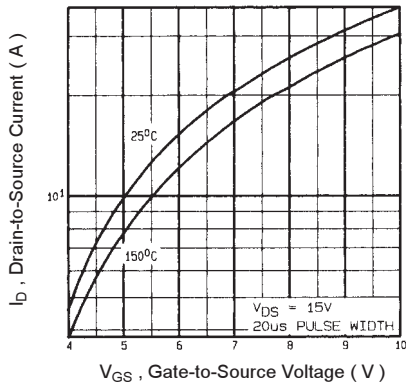


Fig 3. Typical Transfer Characteristics

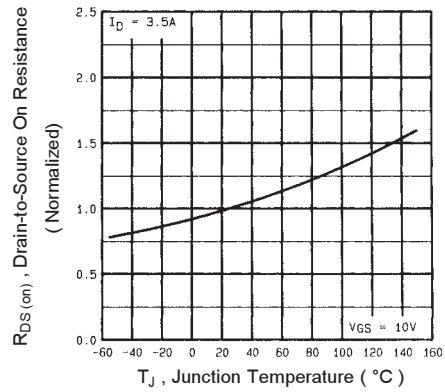


Fig 4. Normalized On-Resistance Vs. Temperature

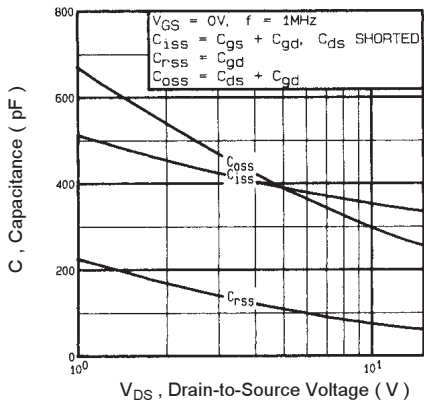


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

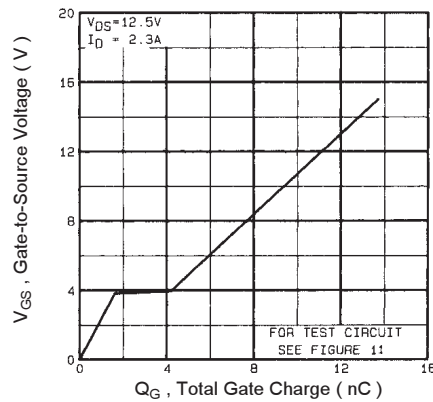


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

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N-Channel

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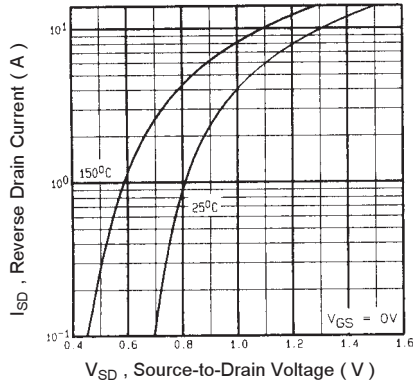


Fig 7. Typical Source-Drain Diode Forward Voltage

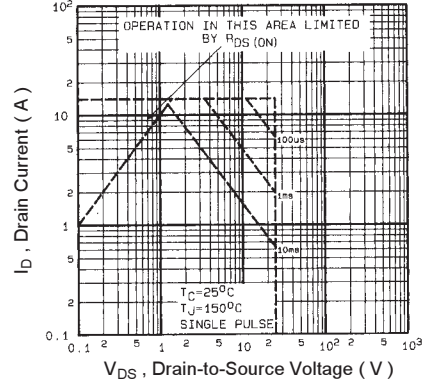


Fig 8. Maximum Safe Operating Area

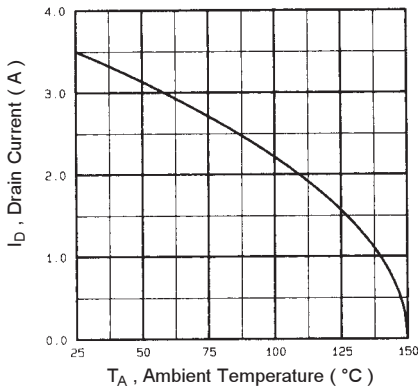


Fig 9. Maximum Drain Current Vs. Ambient Temperature

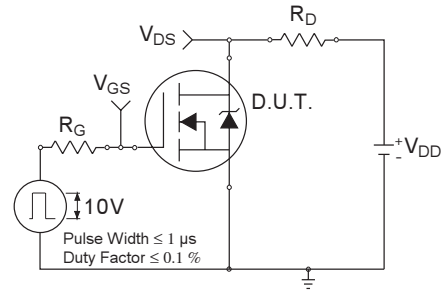


Fig 10a. Switching Time Test Circuit

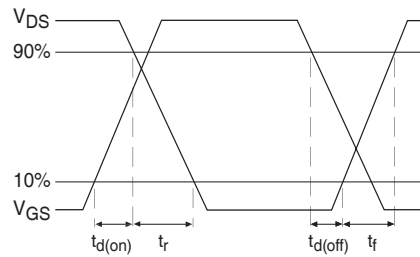


Fig 10b. Switching Time Waveforms

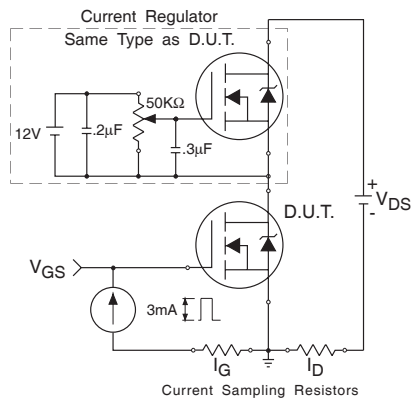


Fig 11a. Gate Charge Test Circuit

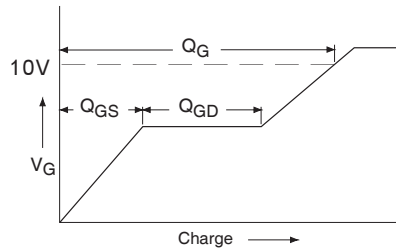


Fig 11b. Basic Gate Charge Waveform

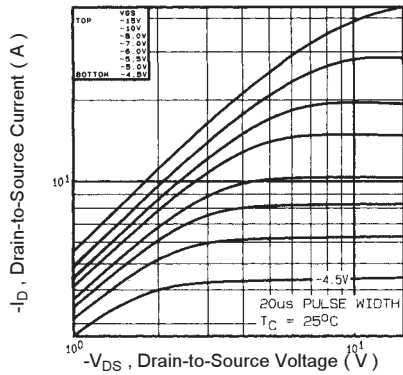


Fig 12. Typical Output Characteristics

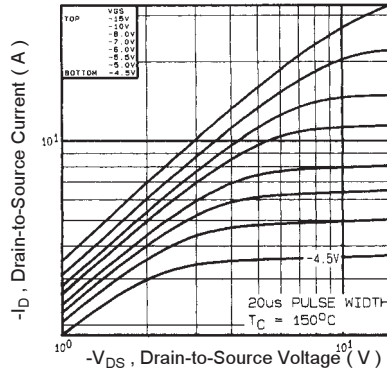


Fig 13. Typical Output Characteristics

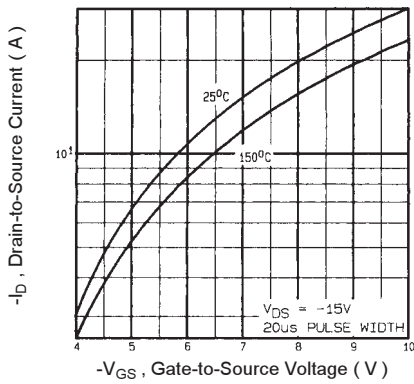


Fig 14. Typical Transfer Characteristics

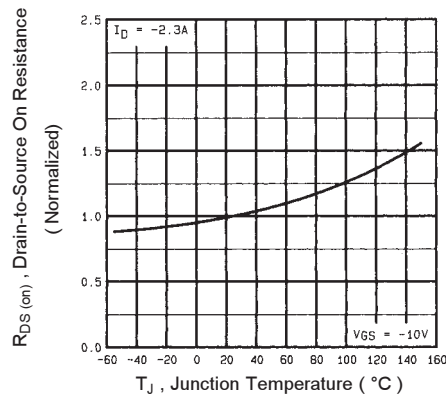


Fig 15. Normalized On-Resistance Vs. Temperature

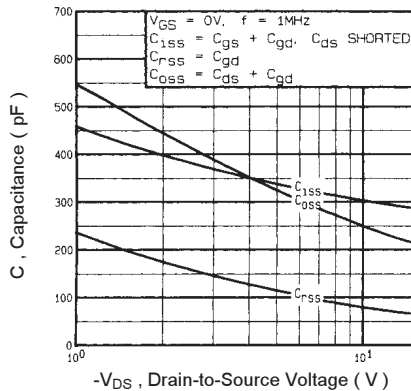


Fig 16. Typical Capacitance Vs. Drain-to-Source Voltage

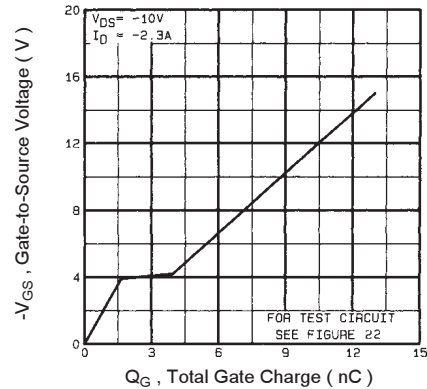


Fig 17. Typical Gate Charge Vs. Gate-to-Source Voltage

IRF7105PbF

P-Channel

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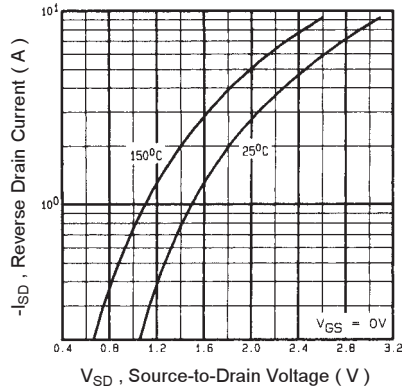


Fig 18. Typical Source-Drain Diode Forward Voltage

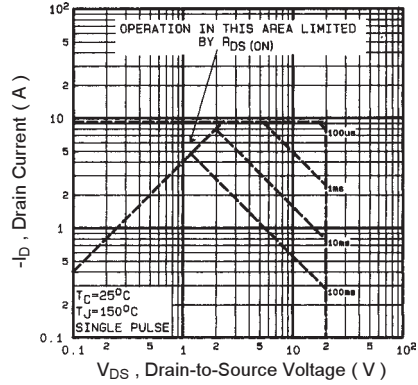


Fig 19. Maximum Safe Operating Area

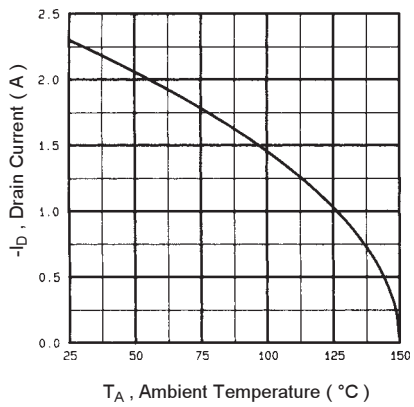


Fig 20. Maximum Drain Current Vs. Ambient Temperature

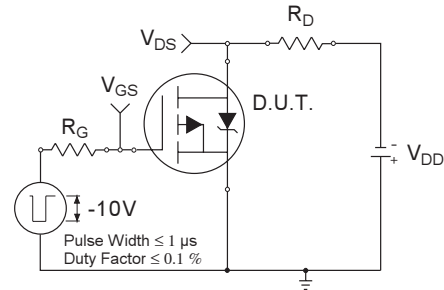


Fig 21a. Switching Time Test Circuit

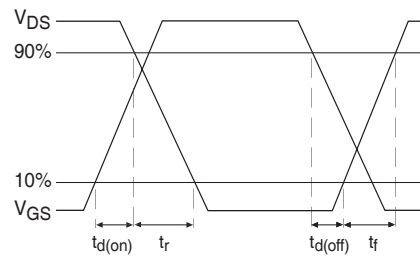


Fig 21b. Switching Time Waveforms

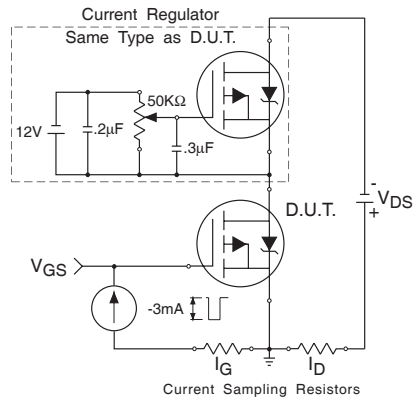


Fig 22a. Gate Charge Test Circuit

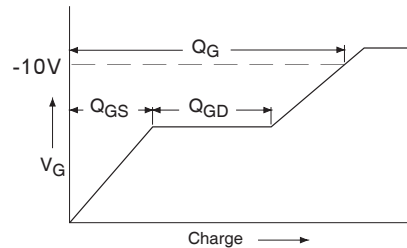


Fig 22b. Basic Gate Charge Waveform

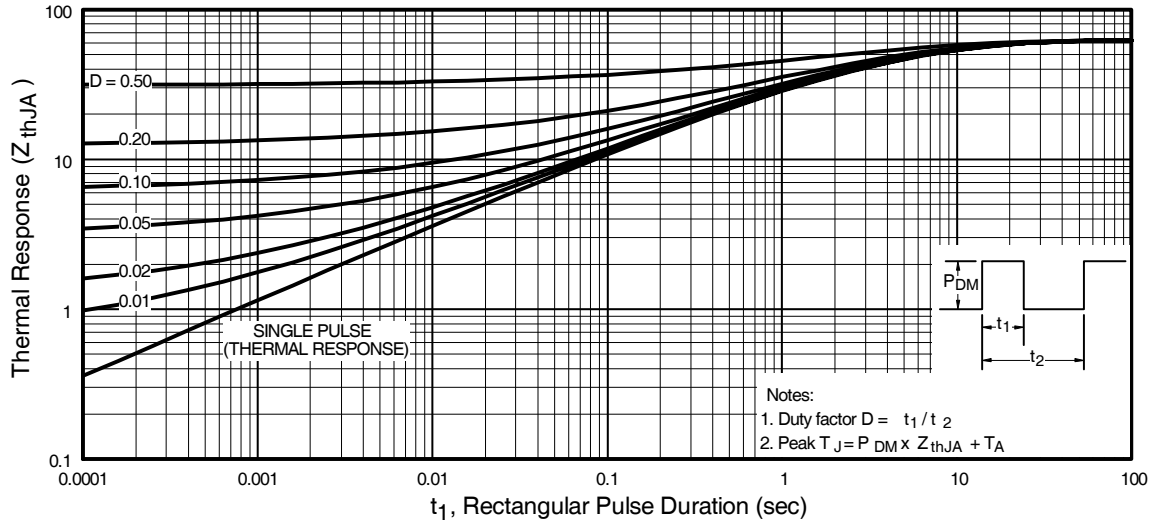
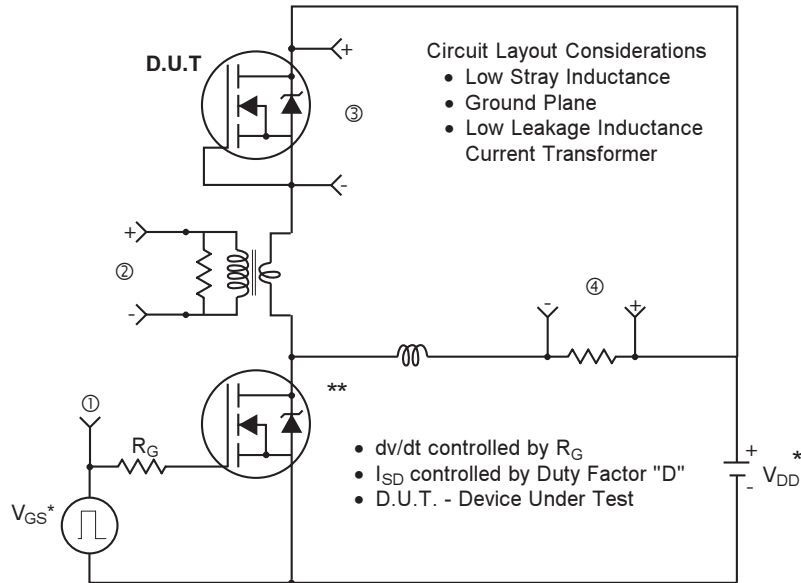


Fig 23. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

IRF7105PbF

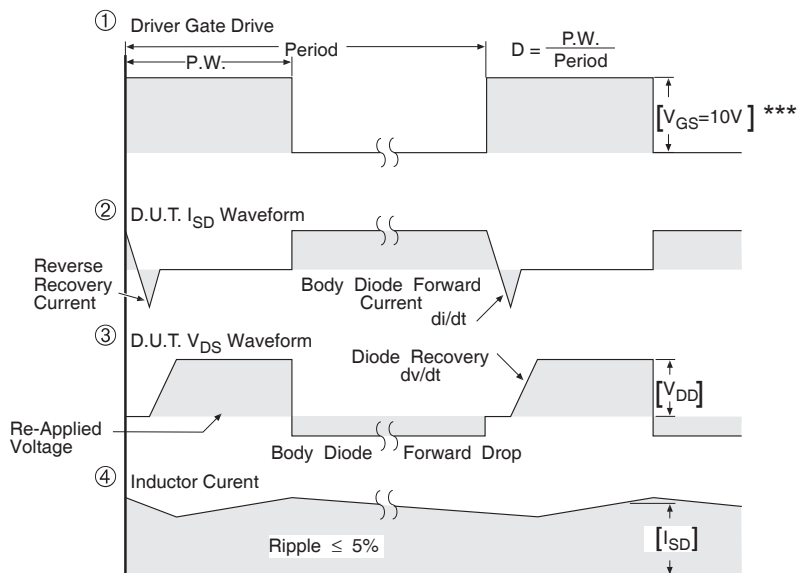
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Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity for P-Channel

** Use P-Channel Driver for P-Channel Measurements

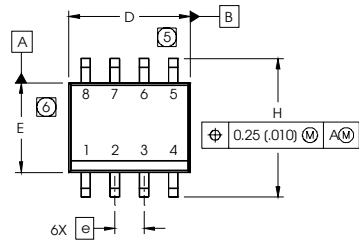


*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

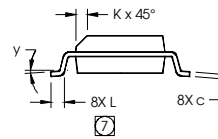
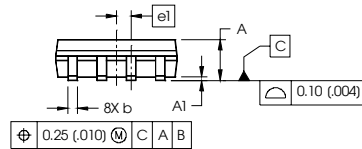
Fig 24. For N and P Channel HEXFETS

SO-8 Package Outline

Dimensions are shown in millimeters (inches)

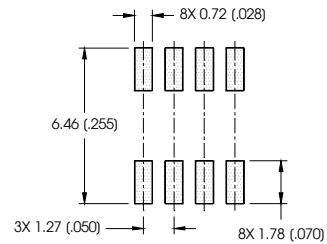


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°



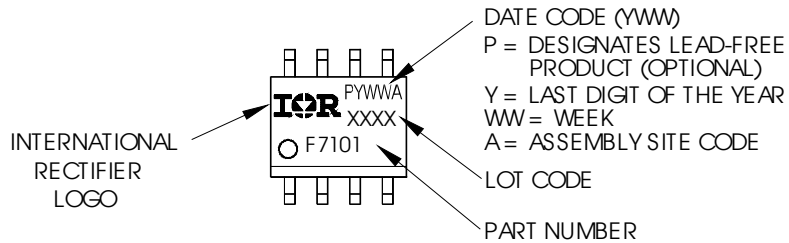
- NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
 2. CONTROLLING DIMENSION: MILLIMETER
 3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
 4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
 5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 (.006).
 6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 (.010).
 7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

FOOTPRINT



SO-8 Part Marking Information (Lead-Free)

EXAMPLE: THIS IS AN IRF7101 (MOSFET)

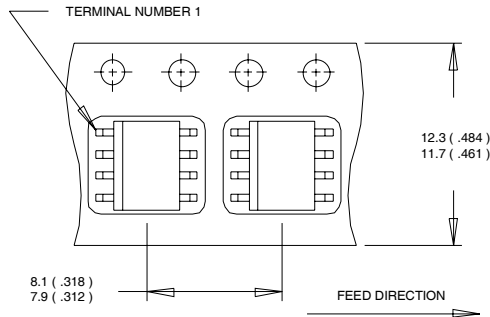


IRF7105PbF



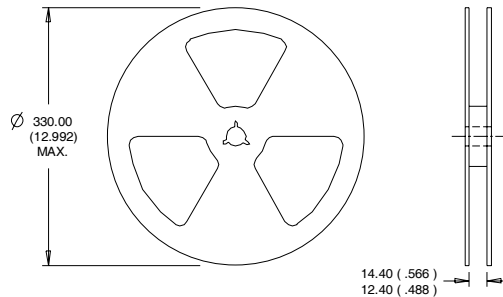
SO-8 Tape and Reel

Dimensions are shown in millimeters (inches)



NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Data and specifications subject to change without notice.
 This product has been designed and qualified for the Consumer market.
 Qualification Standards can be found on IR's Web site.



IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
 TAC Fax: (310) 252-7903

Visit us at www.irf.com for sales contact information.10/04

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The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

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