

IRF7204PBF Datasheet



DiGi Electronics Part Number	IRF7204PBF-DG
Manufacturer	Infineon Technologies
Manufacturer Product Number	IRF7204PBF
Description	MOSFET P-CH 20V 5.3A 8SO
Detailed Description	P-Channel 20 V 5.3A (Ta) 2.5W (Tc) Surface Mount 8-SO

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Purchase and inquiry

Manufacturer Product Number:

IRF7204PBF

Series:

HEXFET®

FET Type:

P-Channel

Drain to Source Voltage (Vdss):

20 V

Drive Voltage (Max Rds On, Min Rds On):

4.5V, 10V

Vgs(th) (Max) @ Id:

2.5V @ 250µA

Vgs (Max):

±12V

FET Feature:

-

Operating Temperature:

-55°C ~ 150°C (Tj)

Supplier Device Package:

8-SO

Manufacturer:

Infineon Technologies

Product Status:

Discontinued at Digi-Key

Technology:

MOSFET (Metal Oxide)

Current - Continuous Drain (Id) @ 25°C:

5.3A (Ta)

Rds On (Max) @ Id, Vgs:

60mOhm @ 5.3A, 10V

Gate Charge (Qg) (Max) @ Vgs:

25 nC @ 10 V

Input Capacitance (Ciss) (Max) @ Vds:

860 pF @ 10 V

Power Dissipation (Max):

2.5W (Tc)

Mounting Type:

Surface Mount

Package / Case:

8-SOIC (0.154", 3.90mm Width)

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8541.29.0095

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

International IOR Rectifier

PD - 95165

IRF7204PbF

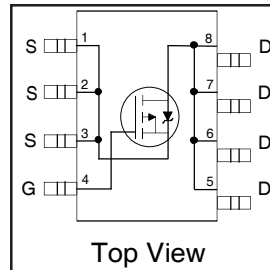
HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- P-Channel MOSFET
- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- Fast Switching
- Lead-Free

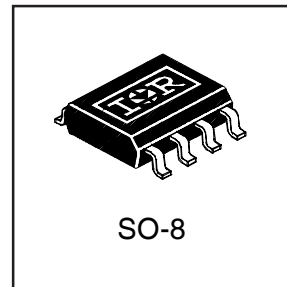
Description

Fourth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The SO-8 has been modified through a customized leadframe for enhanced thermal characteristics and dual-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infra red, or wave soldering techniques. Power dissipation of greater than 0.8W is possible in a typical PCB mount application.



$V_{DSS} = -20V$
$R_{DS(on)} = 0.060\Omega$
$I_D = -5.3A$



Absolute Maximum Ratings

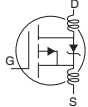
	Parameter	Max.	Units
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	-5.3	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	-4.2	
I_{DM}	Pulsed Drain Current ①	-21	
$P_D @ T_C = 25^\circ C$	Power Dissipation	2.5	W
	Linear Derating Factor	0.020	W/°C
V_{GS}	Gate-to-Source Voltage	± 12	V
dv/dt	Peak Diode Recovery dv/dt ②	-1.7	V/nS
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150	°C

Thermal Resistance Ratings

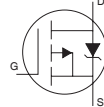
	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ④	—	—	50	°C/W

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International
IR RectifierElectrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-20	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.022	—	V/°C	Reference to 25°C , $I_D = -1\text{mA}$
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	—	—	0.060	Ω	$V_{GS} = -10V, I_D = -5.3A$ ③
		—	—	0.10		$V_{GS} = -4.5V, I_D = -2.0A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	—	-2.5	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
g_{fs}	Forward Transconductance	—	7.9	—	S	$V_{DS} = -15V, I_D = -5.3A$ ③
I_{DSS}	Drain-to-Source Leakage Current	—	—	-25	μA	$V_{DS} = -16V, V_{GS} = 0V$
		—	—	-250		$V_{DS} = -16V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	$V_{GS} = -12V$
	Gate-to-Source Reverse Leakage	—	—	100		$V_{GS} = 12V$
Q_g	Total Gate Charge	—	25	—	nC	$I_D = -5.3A$
Q_{gs}	Gate-to-Source Charge	—	5.0	—		$V_{DS} = -10V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	8.0	—		$V_{GS} = -10V$ ③
$t_{d(on)}$	Turn-On Delay Time	—	14	30	ns	$V_{DD} = -10V$
t_r	Rise Time	—	26	60		$I_D = -1.0A$
$t_{d(off)}$	Turn-Off Delay Time	—	100	150		$R_G = 6.0\Omega$
t_f	Fall Time	—	68	100		$R_D = 10\Omega$ ③
L_D	Internal Drain Inductance	—	2.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	—	4.0	—		
C_{iss}	Input Capacitance	—	860	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	750	—		$V_{DS} = -10V$
C_{rss}	Reverse Transfer Capacitance	—	230	—		$f = 1.0\text{MHz}$

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-2.5	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-15		
V_{SD}	Diode Forward Voltage	—	—	-1.2	V	$T_J = 25^\circ\text{C}, I_S = -1.25A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	85	100	ns	$T_J = 25^\circ\text{C}, I_F = -2.4A$
Q_{rr}	Reverse Recovery Charge	—	77	120	nC	$di/dt = 100A/\mu s$ ③
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② $I_{SD} \leq -5.3A, di/dt \leq 90A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$
- ③ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ④ Surface mounted on FR-4 board, $t \leq 10\text{sec}$.

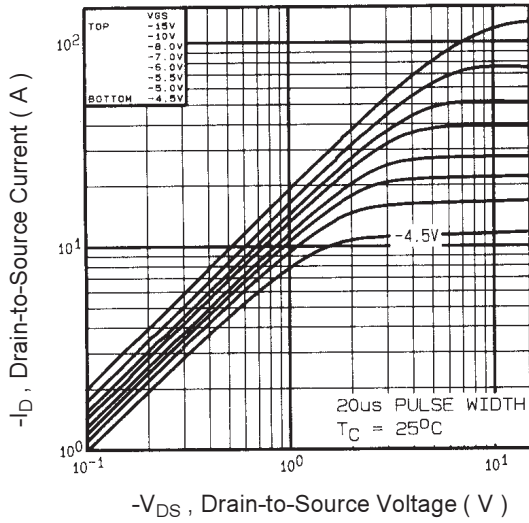


Fig 1. Typical Output Characteristics

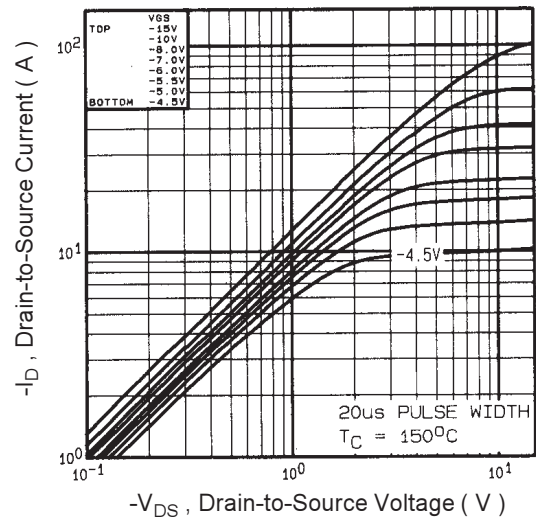


Fig 2. Typical Output Characteristics

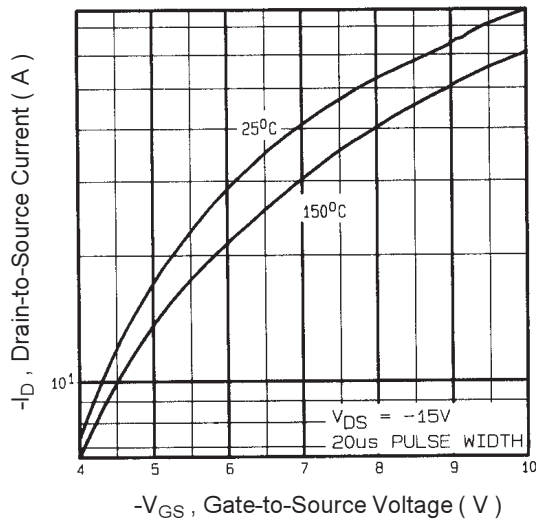


Fig 3. Typical Transfer Characteristics

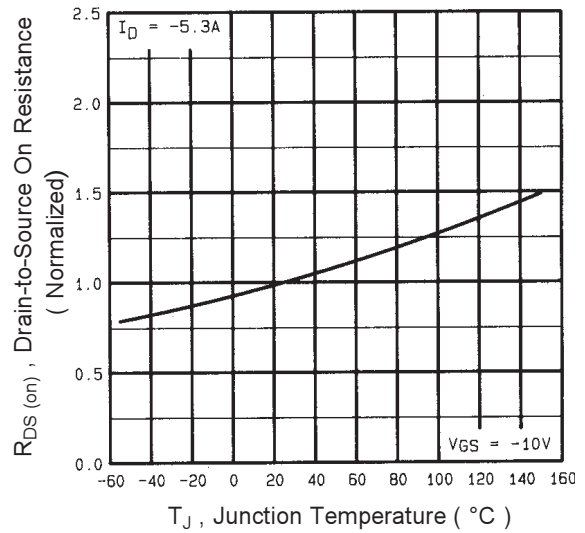


Fig 4. Normalized On-Resistance Vs. Temperature

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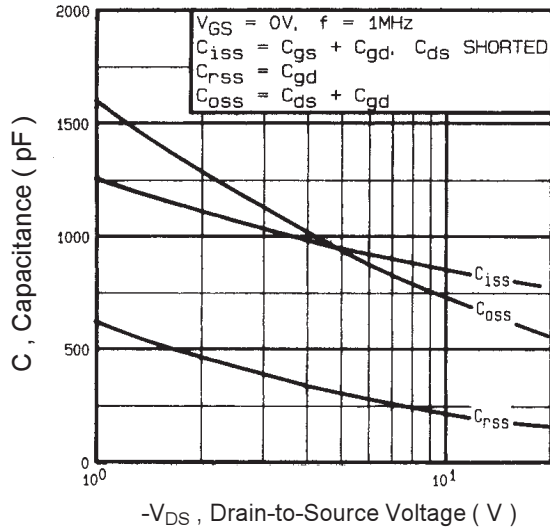


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

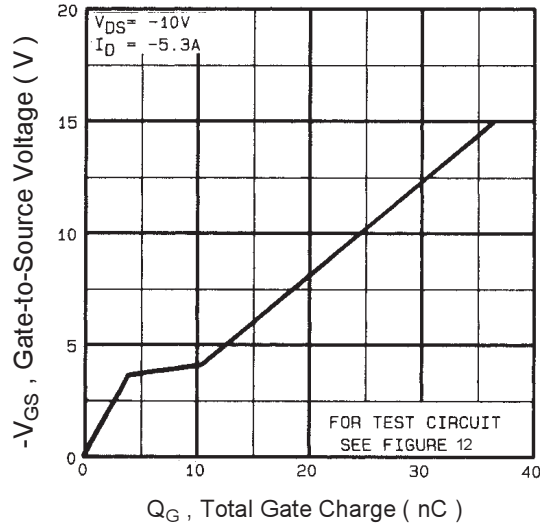


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

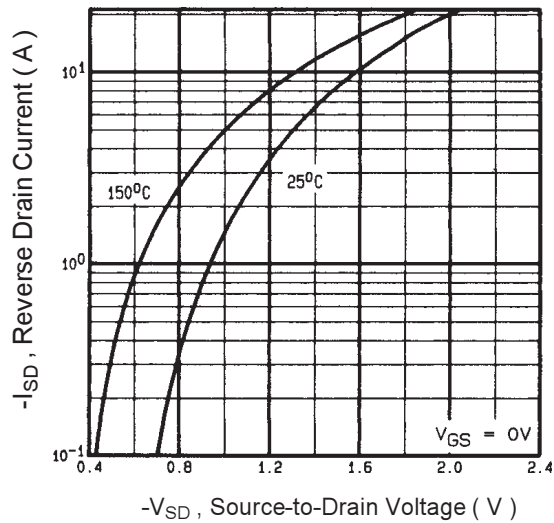


Fig 7. Typical Source-Drain Diode Forward Voltage

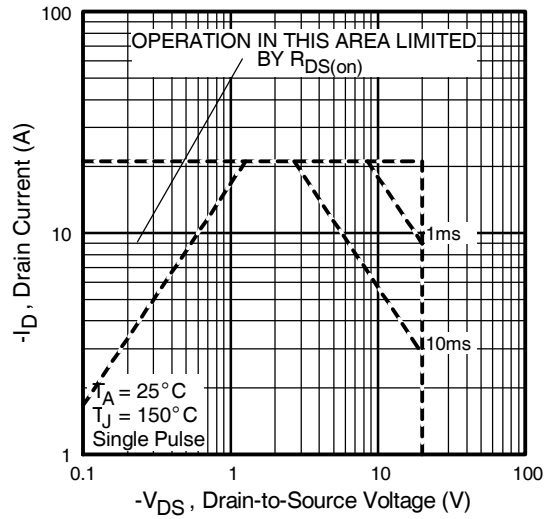


Fig 8. Maximum Safe Operating Area

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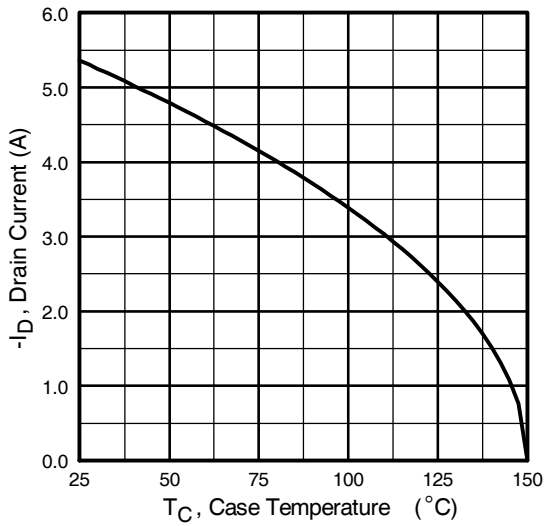


Fig 9. Maximum Drain Current Vs. Ambient Temperature

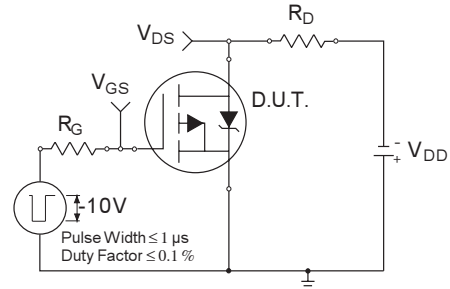


Fig 10a. Switching Time Test Circuit

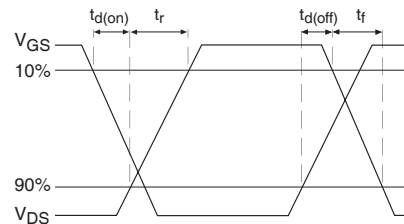


Fig 10b. Switching Time Waveforms

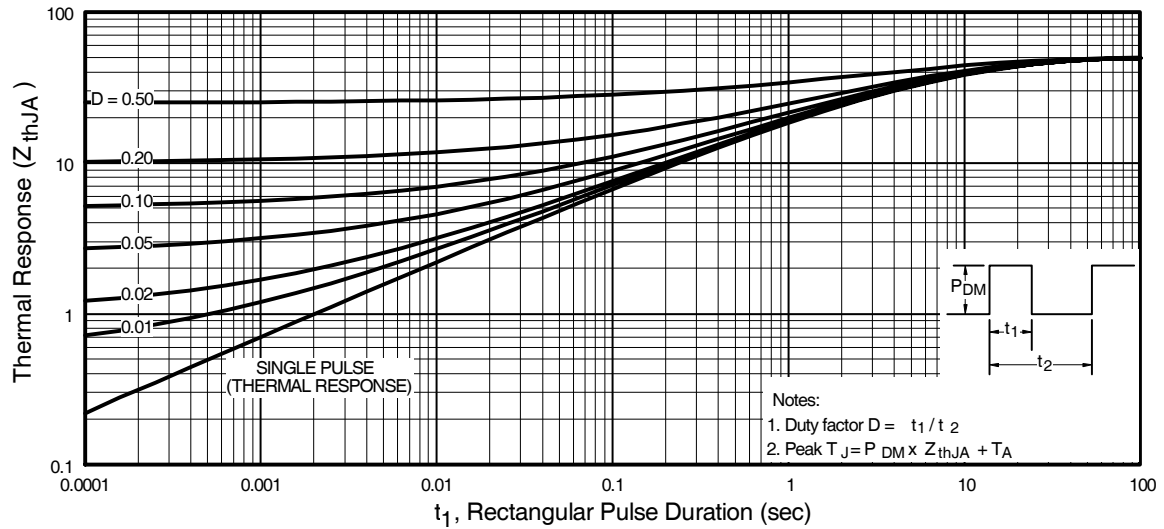


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

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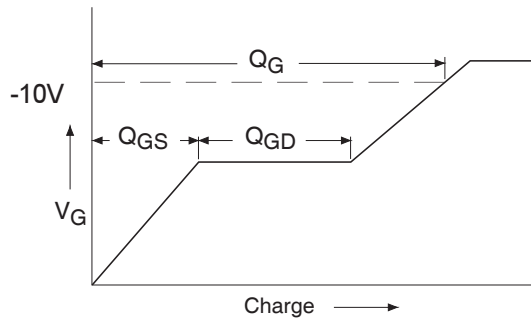


Fig 12a. Basic Gate Charge Waveform

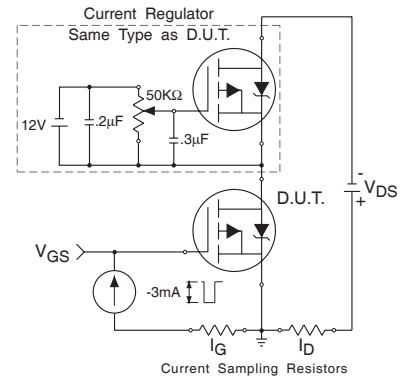
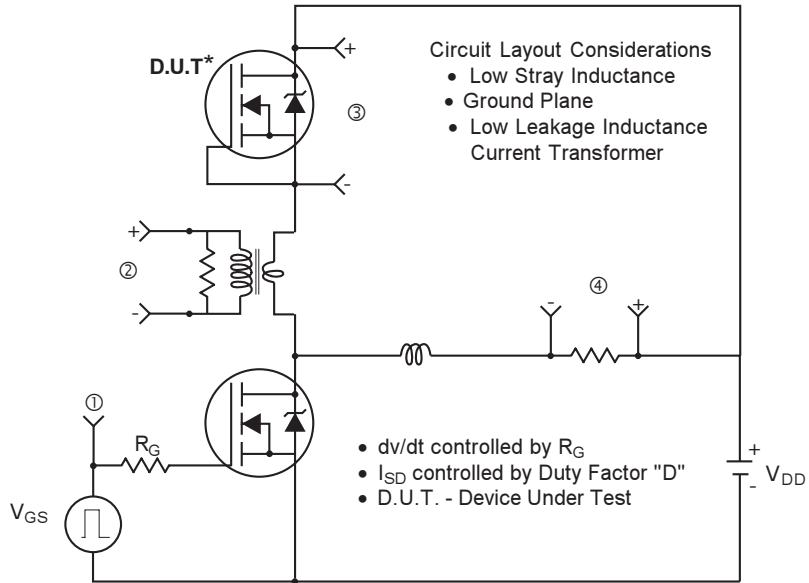
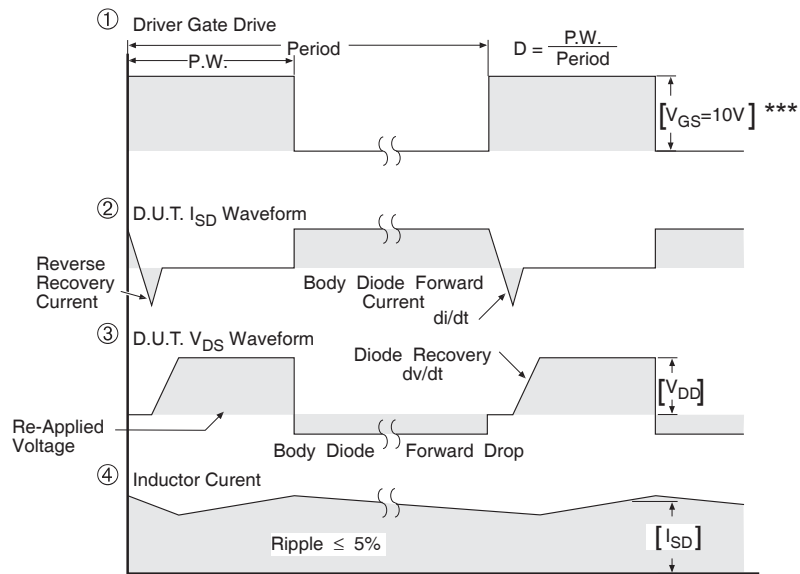


Fig 12b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel



*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

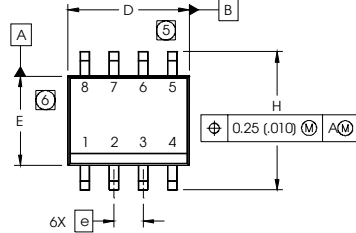
Fig 13. For P-Channel HEXFETS

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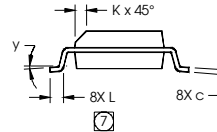
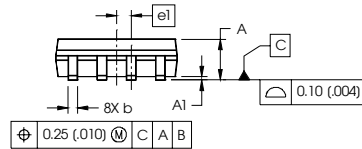


SO-8 Package Outline

Dimensions are shown in millimeters (inches)



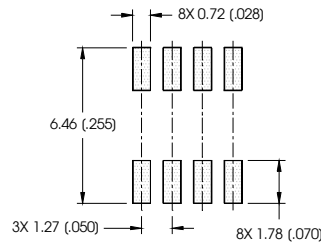
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°



NOTES:

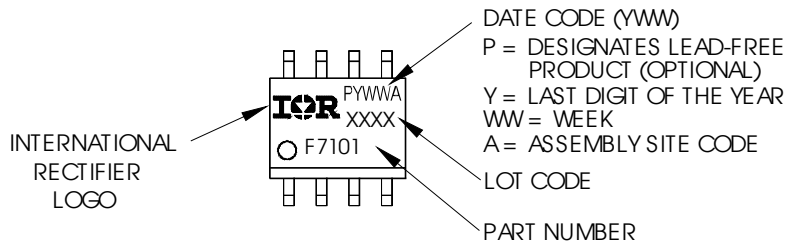
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 (.006).
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 (.010).
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO SUBSTRATE.

FOOTPRINT



SO-8 Part Marking Information (Lead-Free)

EXAMPLE: THIS IS AN IRF7101 (MOSFET)

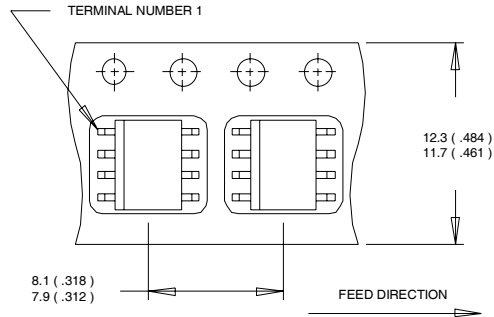




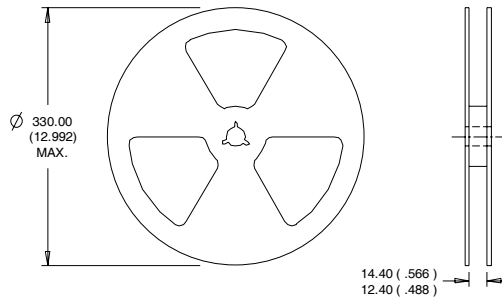
IRF7204PbF

SO-8 Tape and Reel

Dimensions are shown in millimeters (inches)



- NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
 2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Data and specifications subject to change without notice.
 This product has been designed and qualified for the Consumer market.
 Qualifications Standards can be found on IR's Web site.



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