IRF7907PBF Datasheet

DiGi Electronics Part Number	IRF7907PBF-DG
Manufacturer	Infineon Technologies
Manufacturer Product Number	IRF7907PBF
Description	MOSFET 2N-CH 30V 9.1A/11A 8SO
Detailed Description	Mosfet Array 30V 9.1A, 11A 2W Surface Mount 8-SO

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
IRF7907PBF	Infineon Technologies
Series:	Product Status:
HEXFET®	Discontinued at Digi-Key
Technology:	Configuration:
MOSFET (Metal Oxide)	2 N-Channel (Dual)
FET Feature:	Drain to Source Voltage (Vdss):
Logic Level Gate	30V
Current - Continuous Drain (Id) @ 25°C:	Rds On (Max) @ Id, Vgs:
9.1A, 11A	16.4mOhm @ 9.1A, 10V
Vgs(th) (Max) @ Id:	Gate Charge (Qg) (Max) @ Vgs:
2.35V @ 25µA	10nC @ 4.5V
Input Capacitance (Ciss) (Max) @ Vds:	Power - Max:
850pF @ 15V	2W
Operating Temperature:	Mounting Type:
-55°C ~ 150°C (TJ)	Surface Mount
Package / Case:	Supplier Device Package:
8-SOIC (0.154", 3.90mm Width)	8-SO
Base Product Number:	
IRF7907	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8541.29.0095	

International
IOR Rectifier

PD - 97066A

IRF7907PbF

HEXFET® Power MOSFET

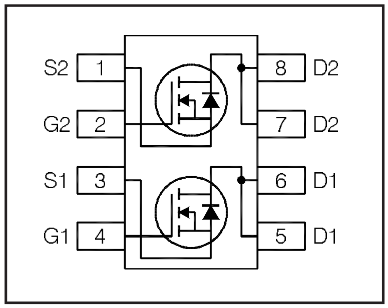
V_{DSS}	$R_{DS(on)}$ max	I_D
30V	Q1 16.4mΩ@V_{GS} = 10V	9.1A
	Q2 11.8mΩ@V_{GS} = 10V	11A

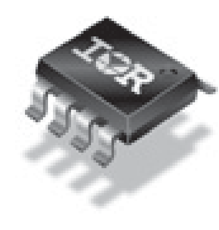
Applications

- Dual SO-8 MOSFET for POL Converters in Notebook Computers, Servers, Graphics Cards, Game Consoles and Set-Top Box

Benefits

- Very Low $R_{DS(on)}$ at 4.5V V_{GS}
- Low Gate Charge
- Fully Characterized Avalanche Voltage and Current
- 20V V_{GS} Max. Gate Rating
- Improved Body Diode Reverse Recovery
- 100% Tested for R_G
- Lead-Free





SO-8

Absolute Maximum Ratings

	Parameter	Q1 Max.	Q2 Max.	Units
V_{DS}	Drain-to-Source Voltage	30		V
V_{GS}	Gate-to-Source Voltage	± 20		
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 10V	9.1	11	A
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ 10V	7.3	8.8	
I_{DM}	Pulsed Drain Current ①	76	85	
P_D @T_A = 25°C	Power Dissipation	2.0	2.0	W
P_D @T_A = 70°C	Power Dissipation	1.3	1.3	
	Linear Derating Factor	0.016	0.016	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150		°C

Thermal Resistance

	Parameter	Q1 Max.	Q2 Max.	Units
$R_{\theta JL}$	Junction-to-Drain Lead ⑤	42	42	°C/W
$R_{\theta JA}$	Junction-to-Ambient ④⑤	62.5	62.5	

IRF7907PbF

International IOR Rectifier

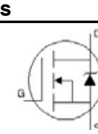
Static @ T_J = 25°C (unless otherwise specified)

	Parameter		Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	Q1&Q2	30	–––	–––	V	V_{GS} = 0V, I_D = 250µA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	Q1	–––	0.024	–––	V/°C	Reference to 25°C, I_D = 1mA
		Q2	–––	0.024	–––		
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	Q1	–––	13.7	16.4		V_{GS} = 10V, I_D = 9.1A ③
			–––	17.1	20.5	mΩ	V_{GS} = 4.5V, I_D = 7.3A ③
		Q2	–––	9.8	11.8		V_{GS} = 10V, I_D = 11A ③
			–––	11.5	13.7		V_{GS} = 4.5V, I_D = 8.8A ③
$V_{GS(th)}$	Gate Threshold Voltage	Q1&Q2	1.35	1.8	2.35	V	Q1: V_{DS} = V_{GS}, I_D = 25µA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	Q1	–––	-4.6	–––	mV/°C	Q2: V_{DS} = V_{GS}, I_D = 50µA
		Q2	–––	-4.9	–––		
I_{DSS}	Drain-to-Source Leakage Current	Q1&Q2	–––	–––	1.0	µA	V_{DS} = 24V, V_{GS} = 0V
		Q1&Q2	–––	–––	150		V_{DS} = 24V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	Q1&Q2	–––	–––	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	Q1&Q2	–––	–––	-100		V_{GS} = -20V
gfs	Forward Transconductance	Q1	19	–––	–––	S	V_{DS} = 15V, I_D = 7.0A
		Q2	24	–––	–––		V_{DS} = 15V, I_D = 8.8A
Q_g	Total Gate Charge	Q1	–––	6.7	10		
		Q2	–––	14	21		
Q_{gs1}	Pre-Vth Gate-to-Source Charge	Q1	–––	1.3	–––		Q1
		Q2	–––	3.0	–––		V_{DS} = 15V
Q_{gs2}	Post-Vth Gate-to-Source Charge	Q1	–––	0.7	–––	nC	V_{GS} = 4.5V, I_D = 7.0A
		Q2	–––	1.3	–––		
Q_{gd}	Gate-to-Drain Charge	Q1	–––	2.5	–––		Q2
		Q2	–––	4.9	–––		V_{DS} = 15V
Q_{godr}	Gate Charge Overdrive	Q1	–––	2.2	–––		V_{GS} = 4.5V, I_D = 8.8A
		Q2	–––	4.8	–––		
Q_{sw}	Switch Charge (Q_{gs2} + Q_{gd})	Q1	–––	3.2	–––		
		Q2	–––	6.2	–––		
Q_{oss}	Output Charge	Q1	–––	4.5	–––	nC	V_{DS} = 16V, V_{GS} = 0V
		Q2	–––	9.0	–––		
R_G	Gate Resistance	Q1	–––	2.6	4.7	Ω	
		Q2	–––	3.0	5.0		
$t_{d(on)}$	Turn-On Delay Time	Q1	–––	6.0	–––		Q1
		Q2	–––	8.0	–––		V_{DD} = 15V, V_{GS} = 4.5V
t_r	Rise Time	Q1	–––	9.3	–––		I_D = 7.0A
		Q2	–––	14	–––	ns	
$t_{d(off)}$	Turn-Off Delay Time	Q1	–––	8.0	–––		Q2
		Q2	–––	13	–––		V_{DD} = 15V, V_{GS} = 4.5V
t_f	Fall Time	Q1	–––	3.4	–––		I_D = 8.8A
		Q2	–––	5.3	–––		Clamped Inductive Load
C_{iss}	Input Capacitance	Q1	–––	850	–––		
		Q2	–––	1790	–––		V_{GS} = 0V
C_{oss}	Output Capacitance	Q1	–––	190	–––	pF	V_{DS} = 15V
		Q2	–––	390	–––		f = 1.0MHz
C_{rss}	Reverse Transfer Capacitance	Q1	–––	88	–––		
		Q2	–––	190	–––		

Avalanche Characteristics

	Parameter	Typ.	Q1 Max.	Q2 Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	–––	10	15	mJ
I_{AR}	Avalanche Current ①	–––	7.0	8.8	A

Diode Characteristics

	Parameter		Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current	Q1	–––	–––	2.8	A	MOSFET symbol
	(Body Diode)	Q2	–––	–––	2.8		showing the 
I_{SM}	Pulsed Source Current	Q1	–––	–––	76	A	integral reverse
	(Body Diode) ①	Q2	–––	–––	85		p-n junction diode.
V_{SD}	Diode Forward Voltage	Q1	–––	–––	1.0	V	T_J = 25°C, I_S = 7.3A, V_{GS} = 0V ③
		Q2	–––	–––	1.0		T_J = 25°C, I_S = 8.8A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	Q1	–––	12	18	ns	Q1 T_J = 25°C, I_F = 7.0A,
		Q2	–––	16	24		V_{DD} = 15V, di/dt = 100A/µs ③
Q_{rr}	Reverse Recovery Charge	Q1	–––	4.1	6.1	nC	Q2 T_J = 25°C, I_F = 8.8A,
		Q2	–––	5.9	8.9		V_{DD} = 15V, di/dt = 100A/µs ③

Typical Characteristics

Q1 - Control FET

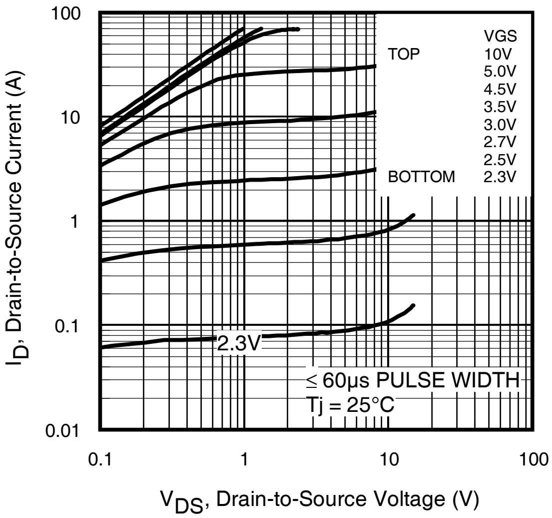


Fig 1. Typical Output Characteristics

Q2 - Synchronous FET

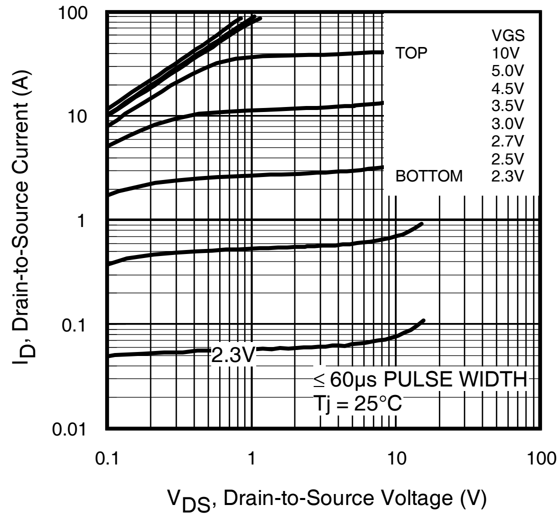


Fig 2. Typical Output Characteristics

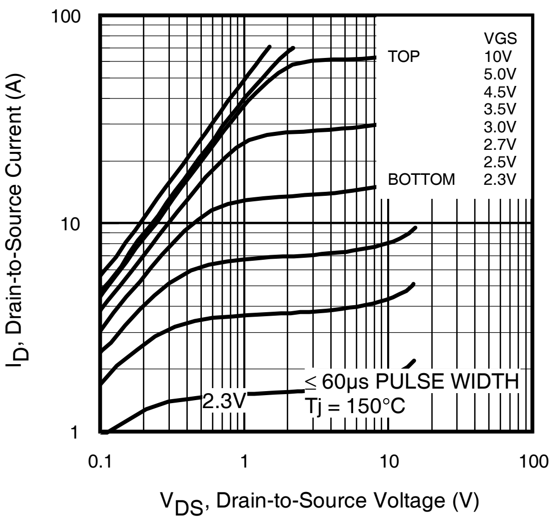


Fig 3. Typical Output Characteristics

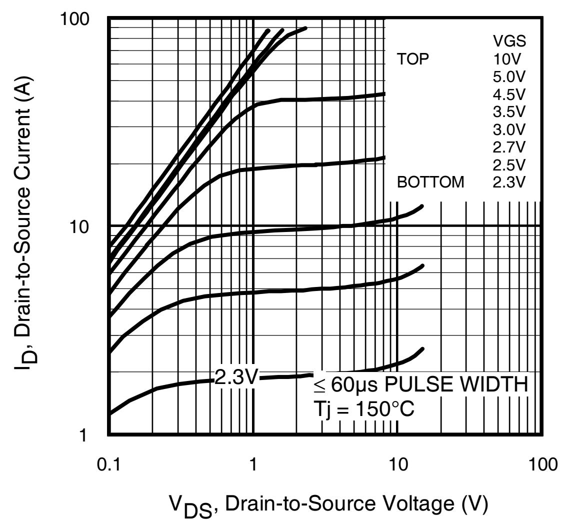


Fig 4. Typical Output Characteristics

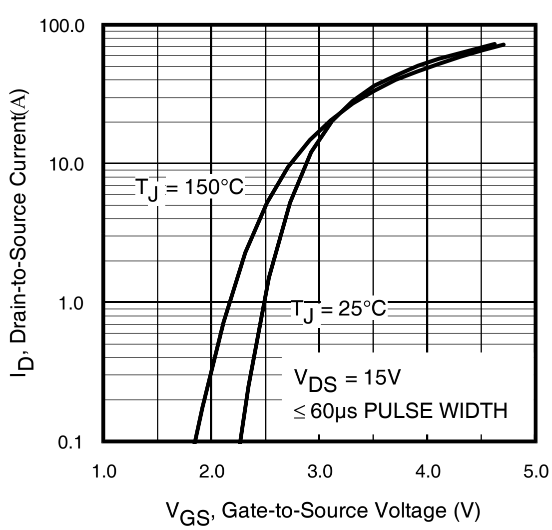


Fig 5. Typical Transfer Characteristics

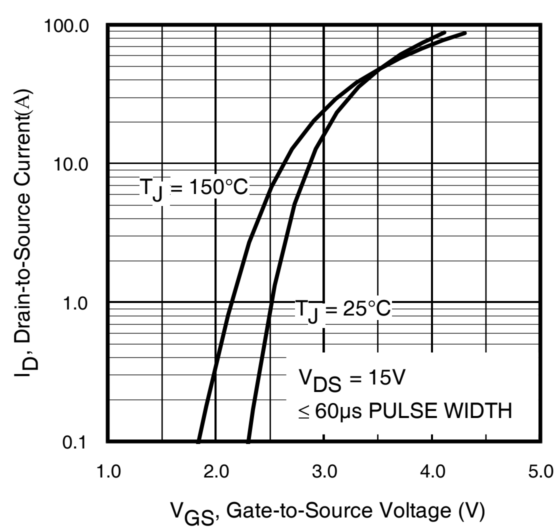


Fig 6. Typical Transfer Characteristics

Typical Characteristics

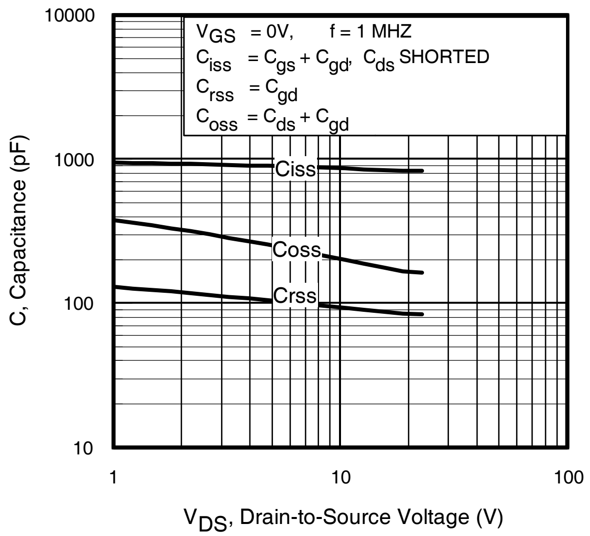


Fig 7. Typical Capacitance vs. Drain-to-Source Voltage

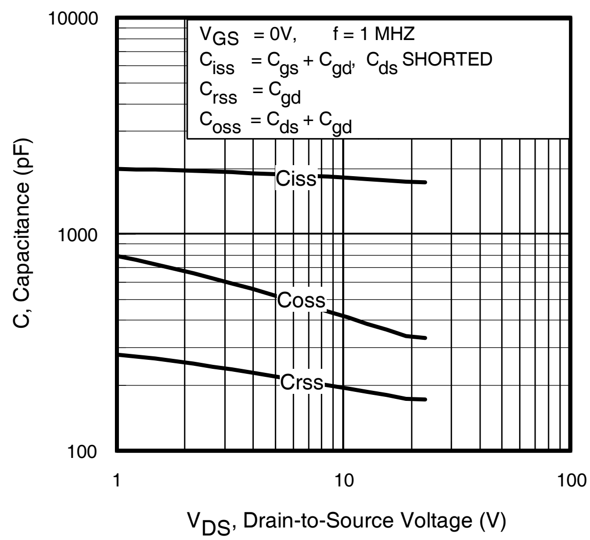


Fig 8. Typical Capacitance vs. Drain-to-Source Voltage

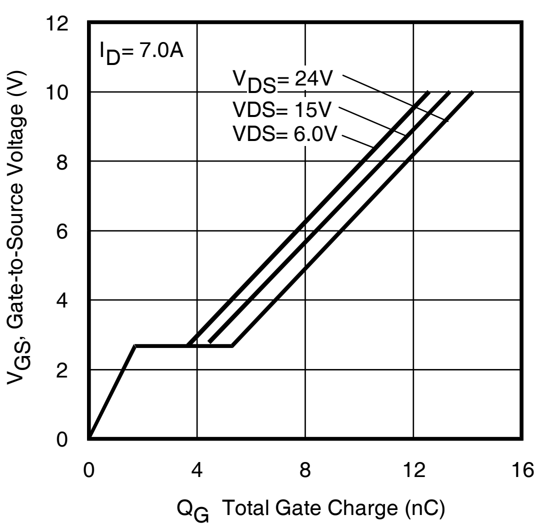


Fig 9. Typical Gate Charge vs. Gate-to-Source Voltage

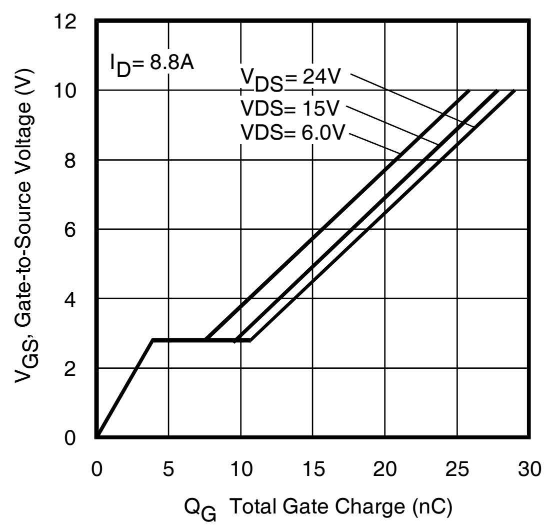


Fig 10. Typical Gate Charge vs. Gate-to-Source Voltage

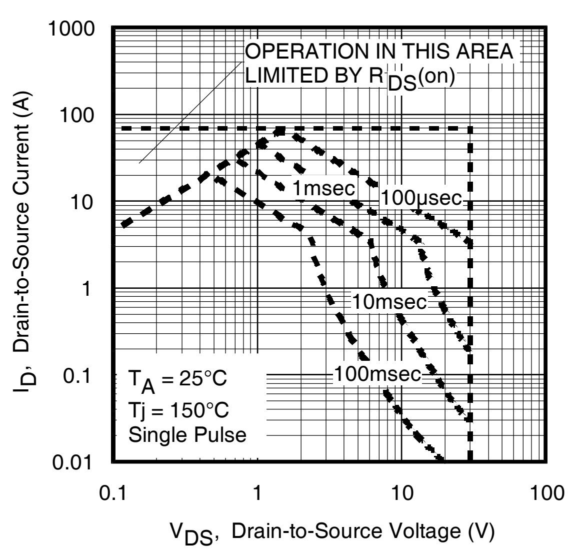


Fig 11. Maximum Safe Operating Area

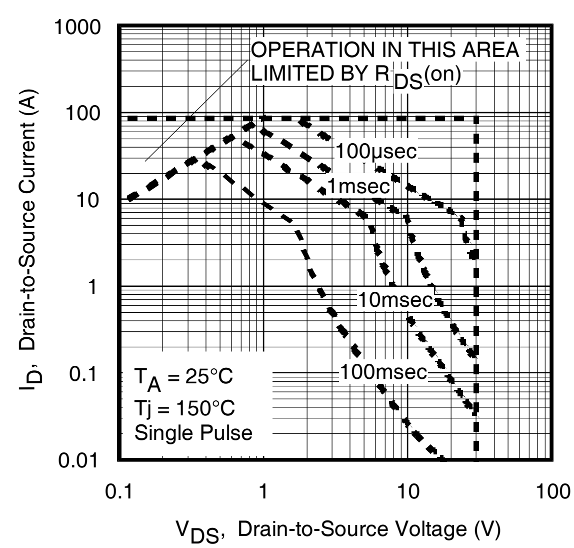


Fig 12. Maximum Safe Operating Area

Typical Characteristics

Q1 - Control FET

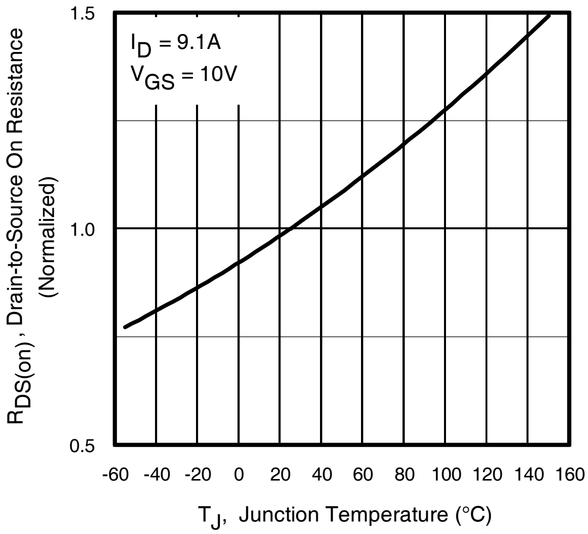


Fig 13. Normalized On-Resistance vs. Temperature

Q2 - Synchronous FET

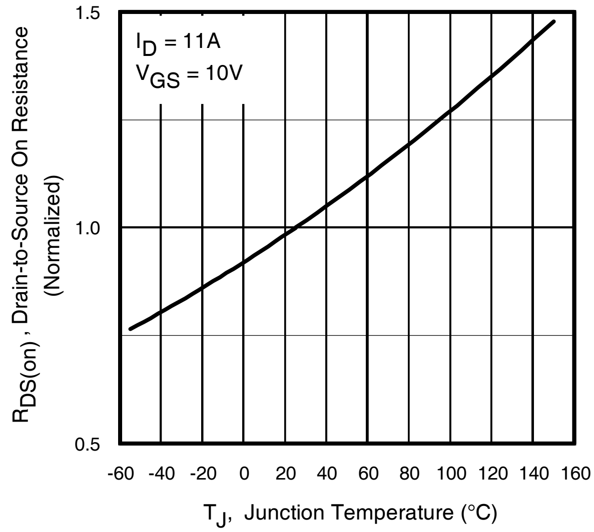


Fig 14. Normalized On-Resistance vs. Temperature

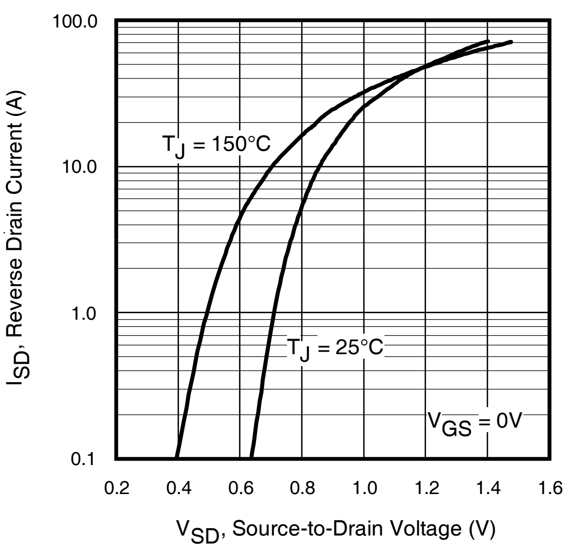


Fig 15. Typical Source-Drain Diode Forward Voltage

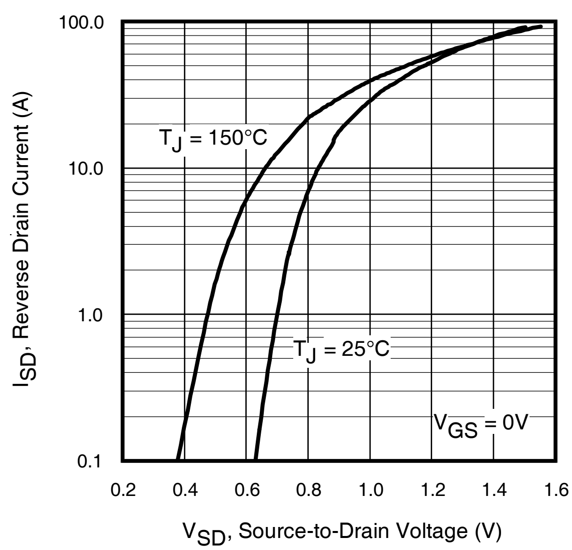


Fig 16. Typical Source-Drain Diode Forward Voltage

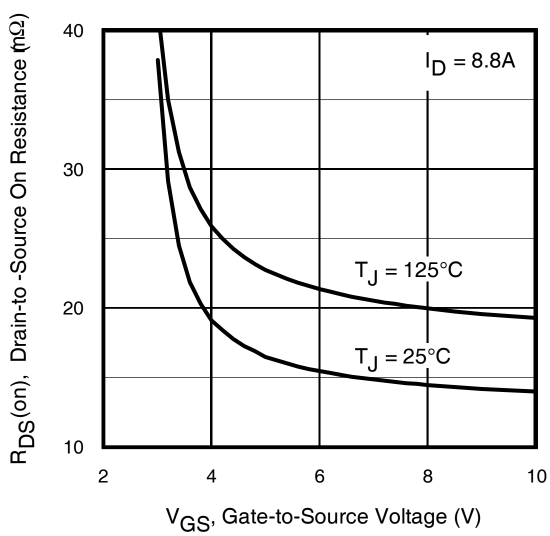


Fig 17. Typical On-Resistance vs.Gate Voltage

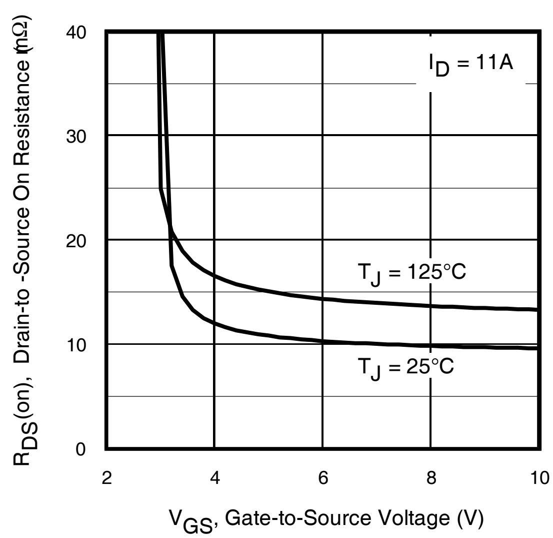


Fig 18. Typical On-Resistance vs.Gate Voltage

Typical Characteristics

Q1 - Control FET

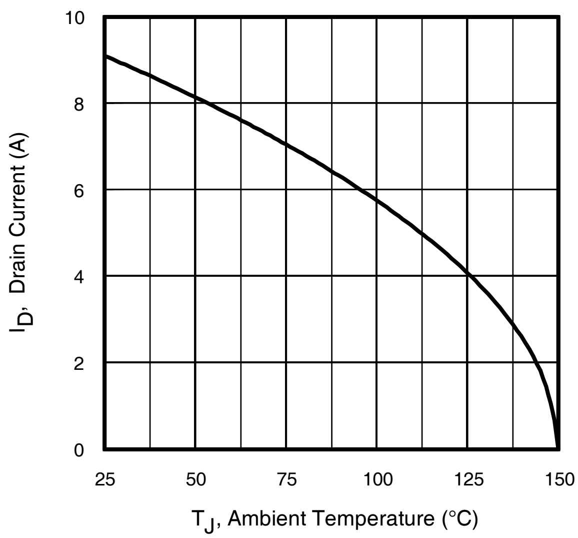


Fig 19. Maximum Drain Current vs. Ambient Temp.

Q2 - Synchronous FET

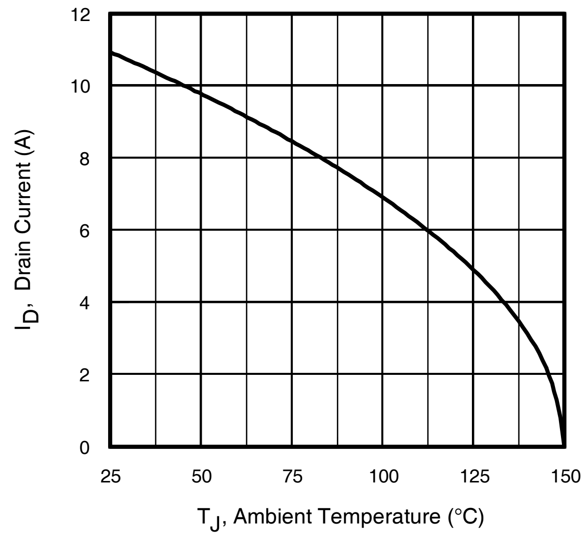


Fig 20. Maximum Drain Current vs. Ambient Temp.

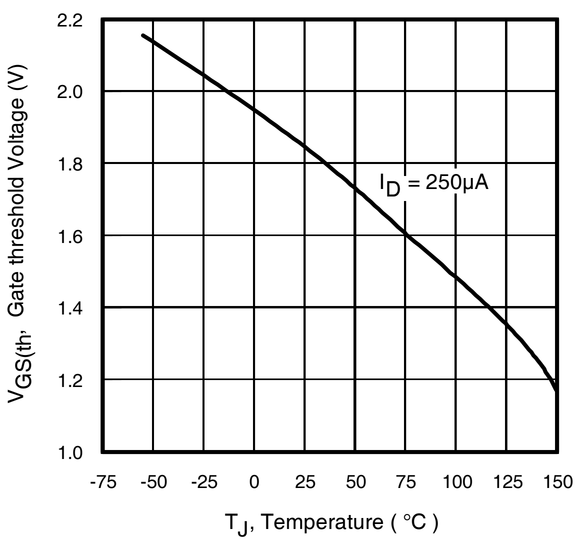


Fig 21. Threshold Voltage vs. Temperature

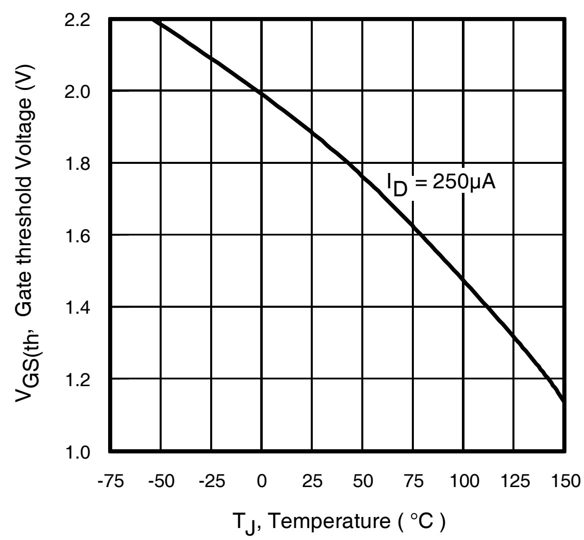


Fig 22. Threshold Voltage vs. Temperature

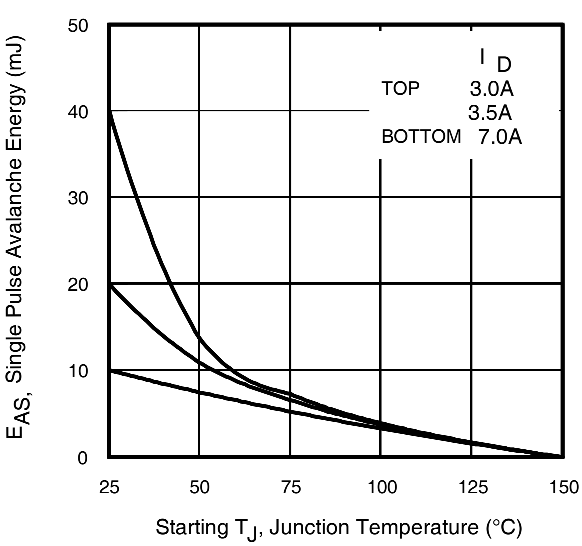


Fig 23. Maximum Avalanche Energy vs. Drain Current

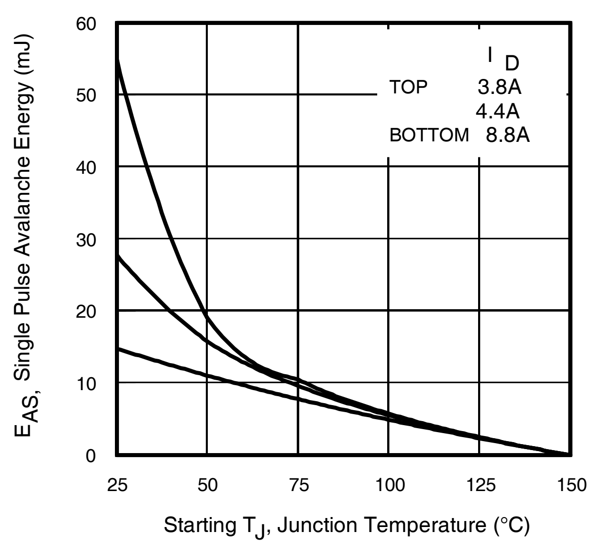


Fig 24. Maximum Avalanche Energy vs. Drain Current

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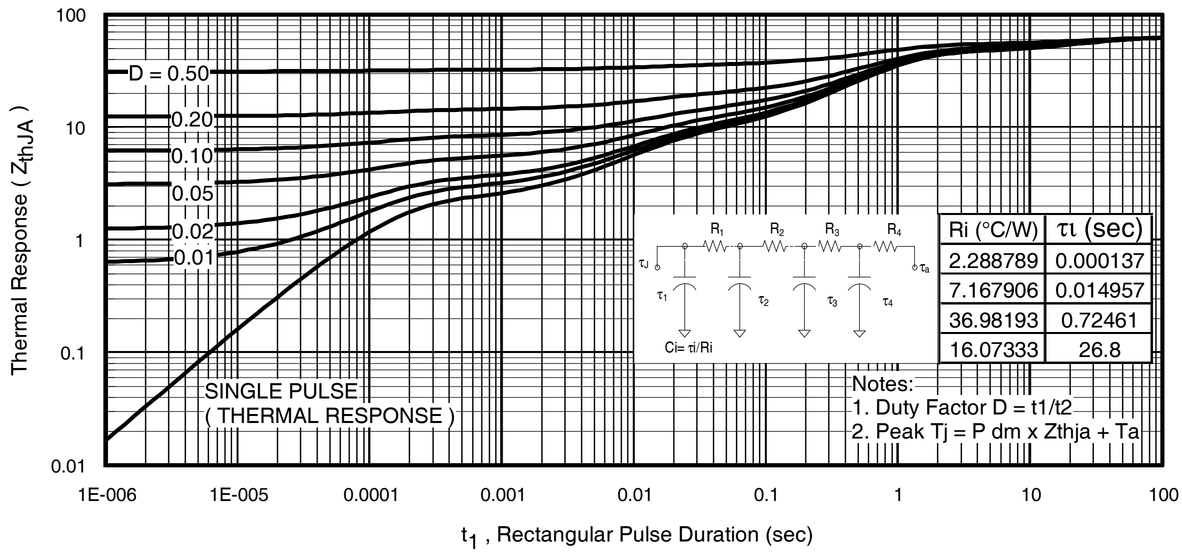


Fig 25. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient (Q1)

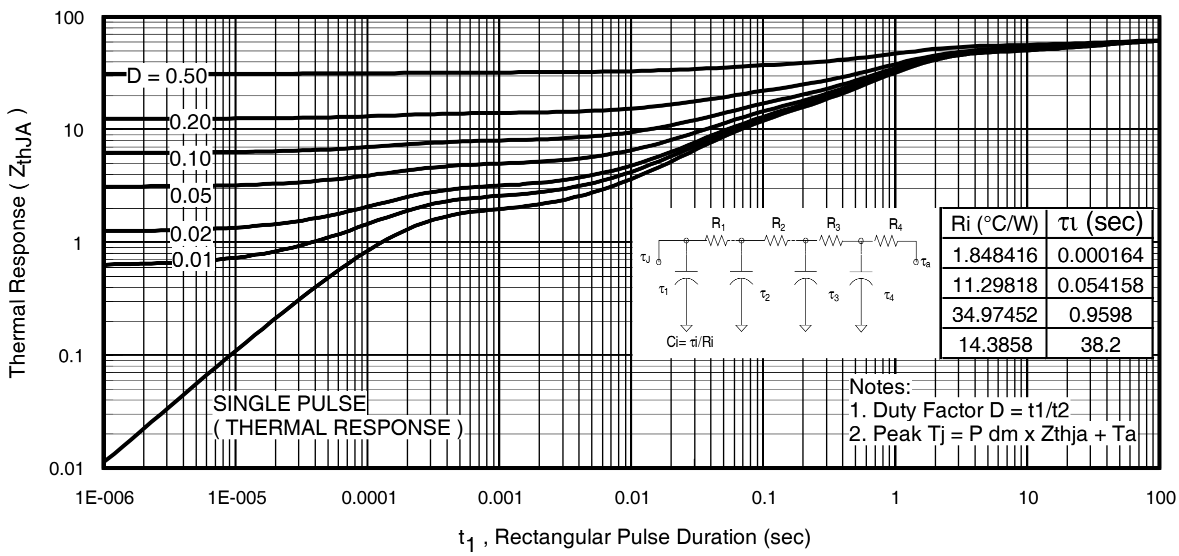


Fig 26. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient (Q2)

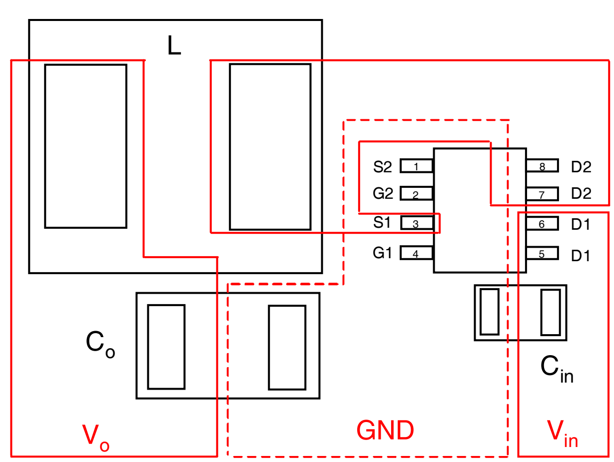


Fig 27. Layout Diagram

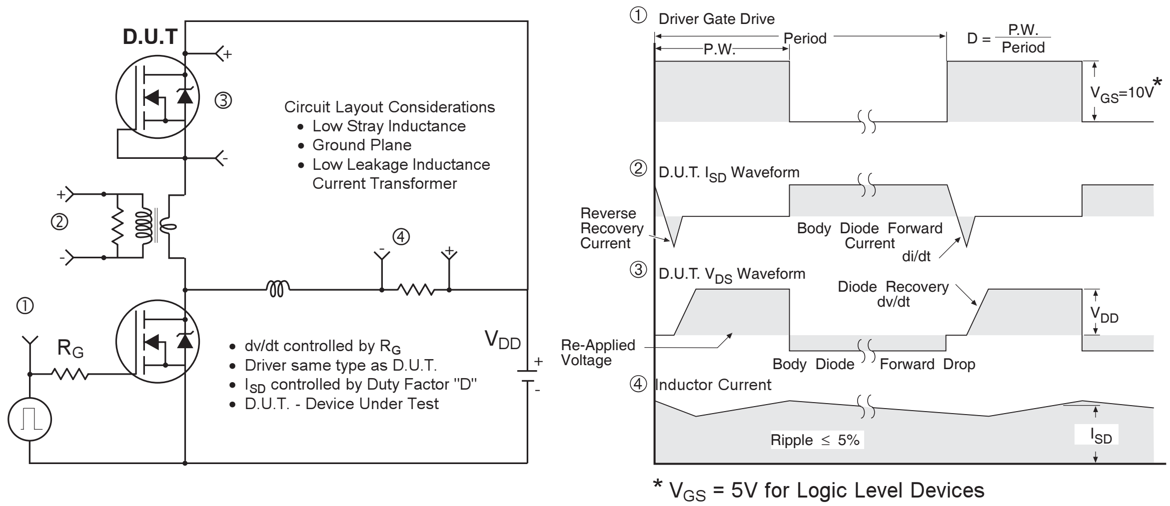


Fig 28. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

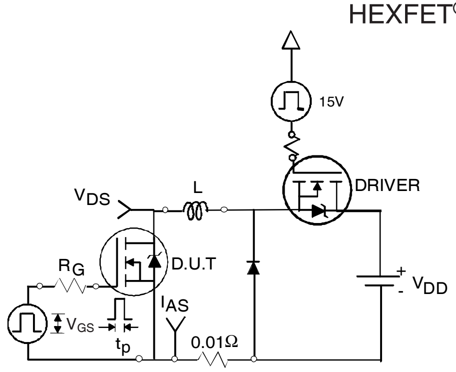


Fig 29a. Unclamped Inductive Test Circuit

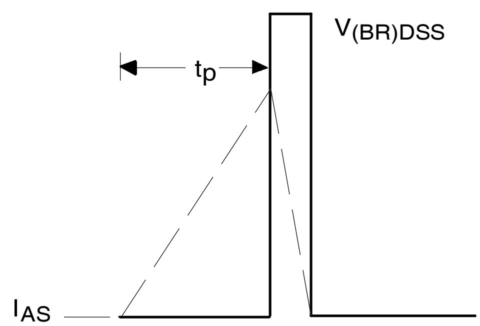


Fig 29b. Unclamped Inductive Waveforms

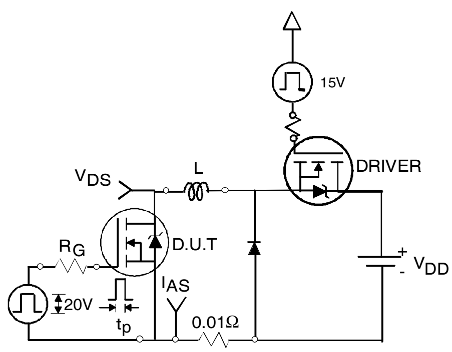


Fig 30a. Switching Time Test Circuit

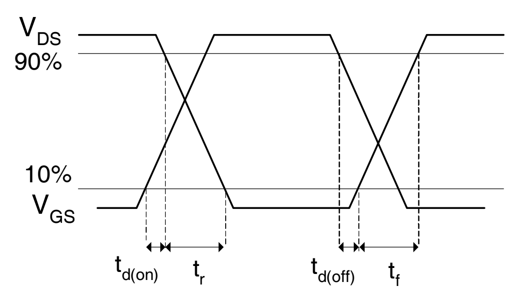


Fig 30b. Switching Time Waveforms

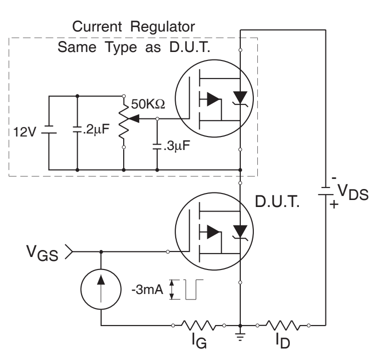


Fig 31a. Gate Charge Test Circuit

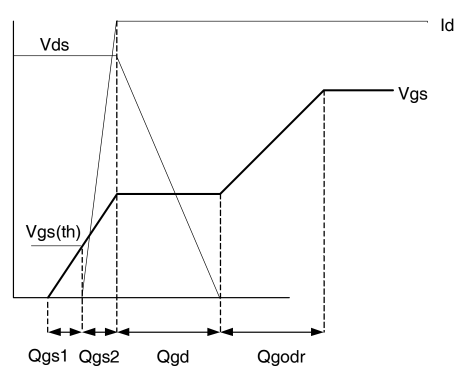
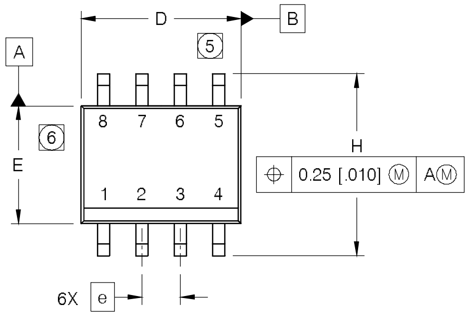


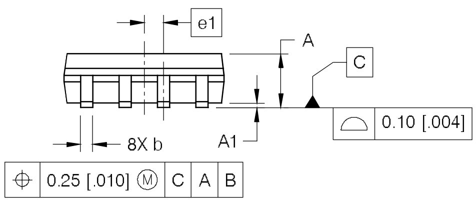
Fig 31b. Gate Charge Waveform

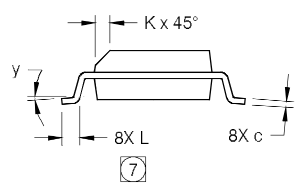
SO-8 Package Outline(Mosfet & Fetky)

Dimensions are shown in milimeters (inches)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°





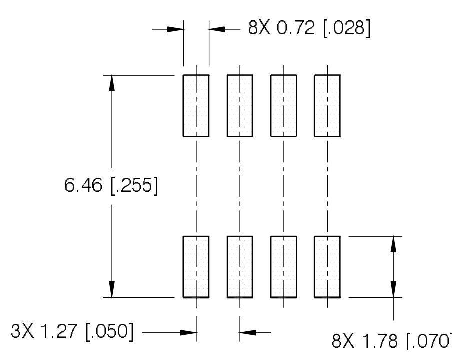
NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].

6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].

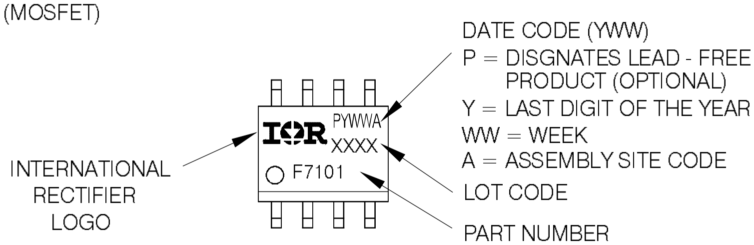
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

FOOTPRINT



SO-8 Part Marking Information

EXAMPLE: THIS IS AN IRF7101 (MOSFET)

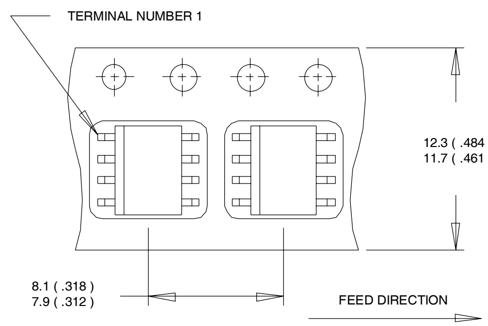


Note: For the most current drawing please refer to IR website at: http://www.irf.com/package/

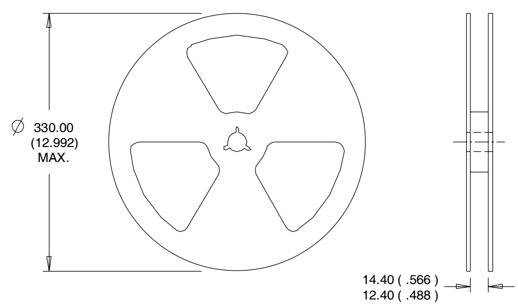
IRF7907PbF

SO-8 Tape and Reel

Dimensions are shown in millimeters (inches)



NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Note: For the most current drawing please refer to IR website at: http://www.irf.com/package/

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting T_J = 25°C, Q1: L = 0.41mH, R_G = 25Ω, I_{AS} = 7.0A;
Q2: L = 0.38mH, R_G = 25Ω, I_{AS} = 8.8A.

③ Pulse width ≤ 400μs; duty cycle ≤ 2%.

④ When mounted on 1 inch square copper board.

⑤ R_θ is measured at T_J approximately 90°C.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information. 07/2008

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