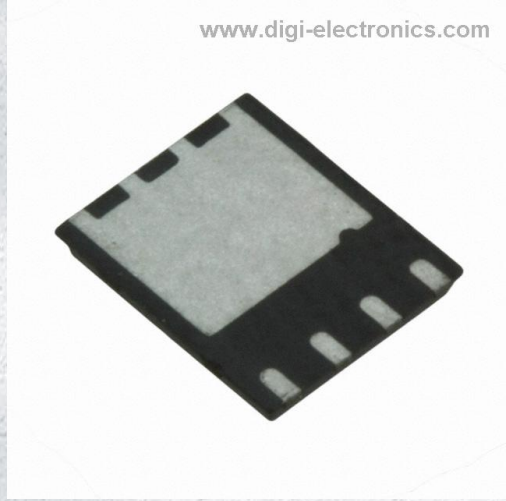
IRFH5004TR2PBF Datasheet



https://www.DiGi-Electronics.com

DiGi Electronics Part Number	IRFH5004TR2PBF-DG
Manufacturer	Infineon Technologies
Manufacturer Product Number	IRFH5004TR2PBF
Description	MOSFET N-CH 40V 28A 8VQFN
Detailed Description	N-Channel 40 V 28A (Ta), 100A (Tc) Surface Mount 8-PQFN (5x6)

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

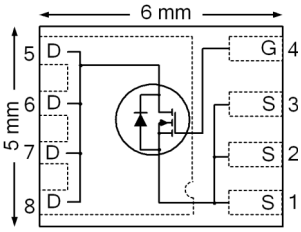
Manufacturer Product Number:	Manufacturer:
IRFH5004TR2PBF	Infineon Technologies
Series:	Product Status:
-	Obsolete
FET Type:	Technology:
N-Channel	MOSFET (Metal Oxide)
Drain to Source Voltage (Vdss):	Current - Continuous Drain (Id) @ 25°C:
40 V	28A (Ta), 100A (Tc)
Rds On (Max) @ Id, Vgs:	Vgs(th) (Max) @ Id:
2.6mOhm @ 50A, 10V	4V @ 150µA
Gate Charge (Qg) (Max) @ Vgs:	Input Capacitance (Ciss) (Max) @ Vds:
110 nC @ 10 V	4490 pF @ 20 V
FET Feature:	Mounting Type:
-	Surface Mount
Supplier Device Package:	Package / Case:
8-PQFN (5x6)	8-PowerVDFN

Environmental & Export classification

Moisture Sensitivity Level (MSL):	REACH Status:
1 (Unlimited)	REACH Unaffected
ECCN:	HTSUS:
EAR99	8541.29.0095

StrongIRFET™ IRFH5004PbF

V_{DSS}	40	V
$R_{DS(on)}$ max	2.6	mΩ
Q_G (typical)	73	nC
R_G (typical)	1.2	Ω
I_D (@T_{mb} = 25°C)	188⑥	A



PQFN 5 x 6 mm

Applications

- Secondary Side Synchronous Rectification
- Inverter for DC Motors
- DC-DC Brick Application
- Boost Converters

Features		Benefits
Low $R_{DS(ON)}$ (≤ 2.6 mΩ)		Lower Conduction Losses
Low Thermal Resistance to PCB (<0.8°C/W)		Enable better Thermal Dissipation
100% Rg Tested		Increased Reliability
Low Profile (≤ 0.9 mm)	results in	Increased Power Density
Industry-Standard Pinout	⇒	Multi-Vendor Compatibility
Compatible with Existing Surface Mount Techniques		Easier Manufacturing
RoHS Compliant, Halogen-Free		Environmentally Friendlier
MSL1, Industrial Qualification		Increased Reliability

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFH5004PbF	PQFN 5 mm x 6 mm	Tape and Reel	4000	IRFH5004TRPbF

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	40	V
V_{GS}	Gate-to-Source Voltage	± 20	
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 10V	28	A
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ 10V	23	
I_D @ T_{mb} = 25°C	Continuous Drain Current, V_{GS} @ 10V	188⑥	
I_D @ T_{mb} = 100°C	Continuous Drain Current, V_{GS} @ 10V	119⑥	
I_{DM}	Pulsed Drain Current①	752	
P_D @T_A = 25°C	Power Dissipation⑤	3.6	W
P_D @T_{mb} = 25°C	Power Dissipation⑤	156	
	Linear Derating Factor⑤	0.029	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Notes ① through ⑦ are on page 9

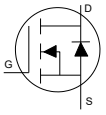
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	40	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.04	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	2.1	2.6	mΩ	V_{GS} = 10V, I_D = 50A ②
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 150µA
$\Delta V_{GS(th)}$	Gate Threshold Voltage Coefficient	—	-5.6	—	mV/°C	
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	µA	V_{DS} = 40V, V_{GS} = 0V
		—	—	250		V_{DS} = 40V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20 V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20 V
gfs	Forward Transconductance	91	—	—	S	V_{DS} = 15 V, I_D = 50A
Q_g	Total Gate Charge	—	73	110	nC	V_{DS} = 20V
Q_{gs1}	Pre-Vth Gate-to-Source Charge	—	15	—		I_D = 50A
Q_{gs2}	Post-Vth Gate-to-Source Charge	—	6.1	—		V_{GS} = 4.5V
Q_{gd}	Gate-to-Drain Charge	—	27	—		See Fig.17 & 18
Q_{godr}	Gate Charge Overdrive	—	25	—		
Q_{sw}	Switch Charge (Q_{gs2} + Q_{gd})	—	33.1	—		
Q_{oss}	Output Charge	—	27	—	nC	V_{DS} = 16V, V_{GS} = 0V
R_G	Gate Resistance	—	1.2	—	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	13	—	ns	V_{DD} = 20V, V_{GS} = 10V
t_r	Rise Time	—	39	—		I_D = 50A
$t_{d(off)}$	Turn-Off Delay Time	—	28	—		R_G = 1.8Ω
t_f	Fall Time	—	16	—		
C_{iss}	Input Capacitance	—	4490	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	970	—		V_{DS} = 20V
C_{rss}	Reverse Transfer Capacitance	—	460	—		f = 1.0MHz

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	340	mJ
I_{AR}	Avalanche Current①		50	A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	156	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)	—	—	752①		
V_{SD}	Diode Forward Voltage	—	—	1.0	V	T_J = 25°C, I_S=50A, V_{GS}=0V ③
t_{rr}	Reverse Recovery Time	—	32	48	ns	T_J = 25°C, I_F = 50A, V_{DD} = 20V
Q_{rr}	Reverse Recovery Charge	—	100	150	nC	di/dt = 300A/µs ③

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$ (Bottom)	Junction-to-Mounting Base	—	0.8	°C/W
$R_{\theta JC}$ (Top)	Junction-to-Case ④	—	15	
$R_{\theta JA}$	Junction-to-Ambient ⑤	—	35	
$R_{\theta JA}$ (<10s)	Junction-to-Ambient ⑤	—	33	

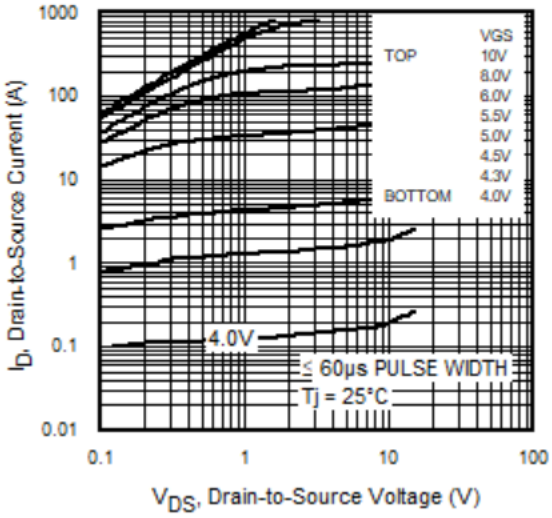


Fig 1. Typical Output Characteristics

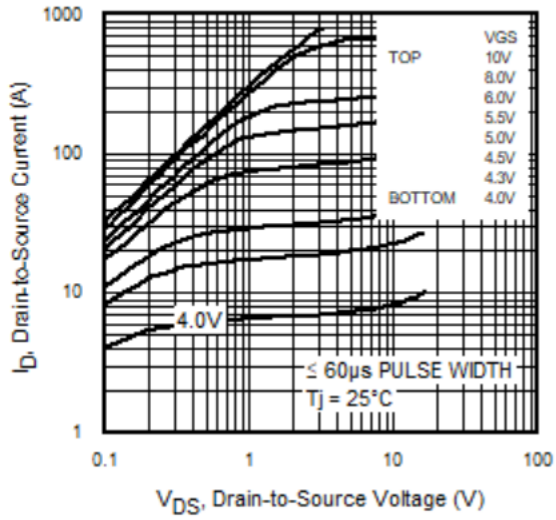


Fig 2. Typical Output Characteristics

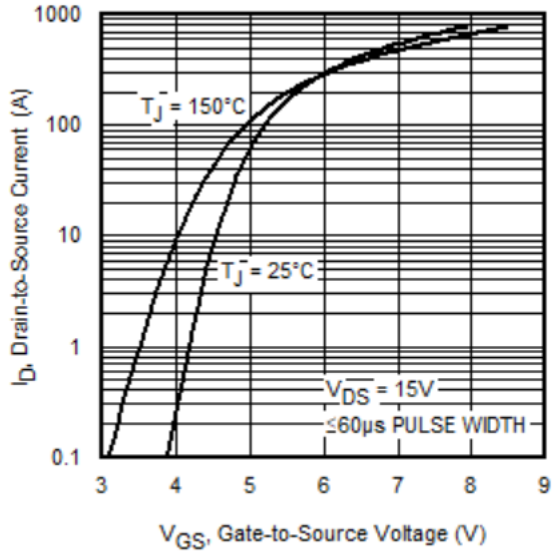


Fig 3. Typical Transfer Characteristics

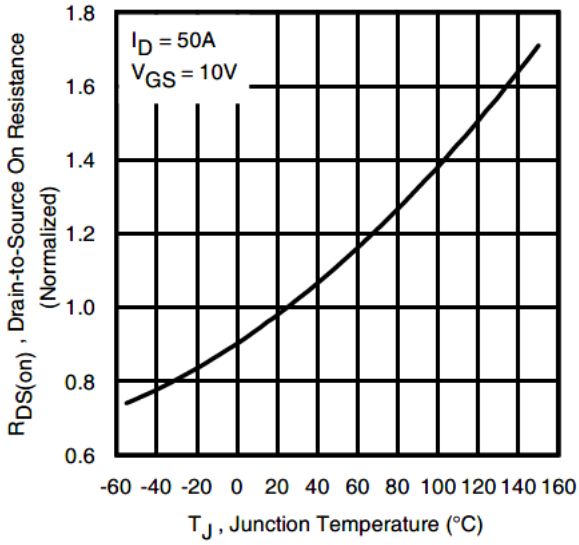


Fig 4. Normalized On-Resistance vs. Temperature

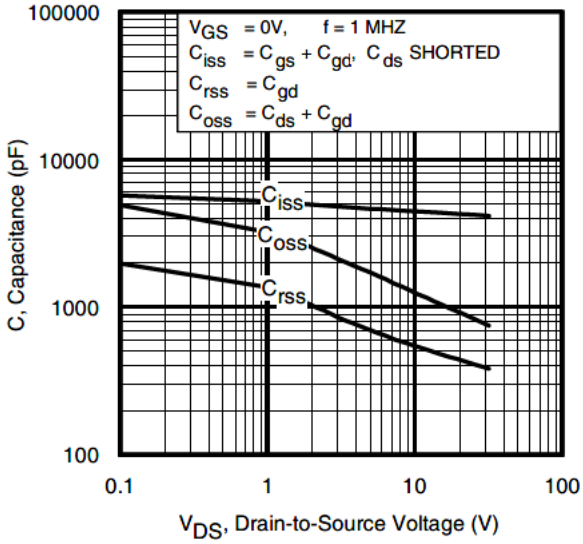


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

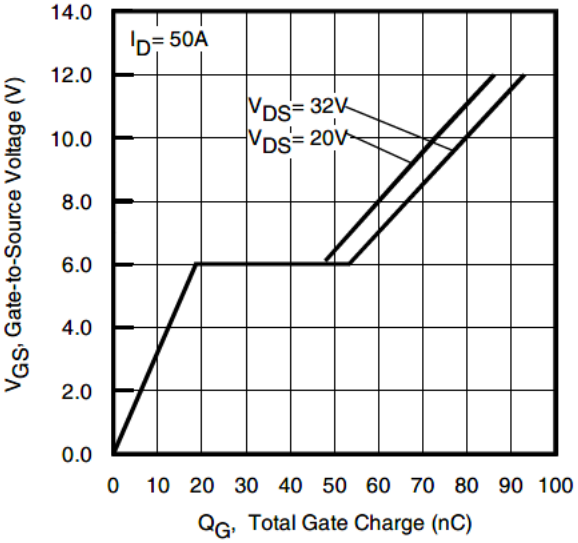


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

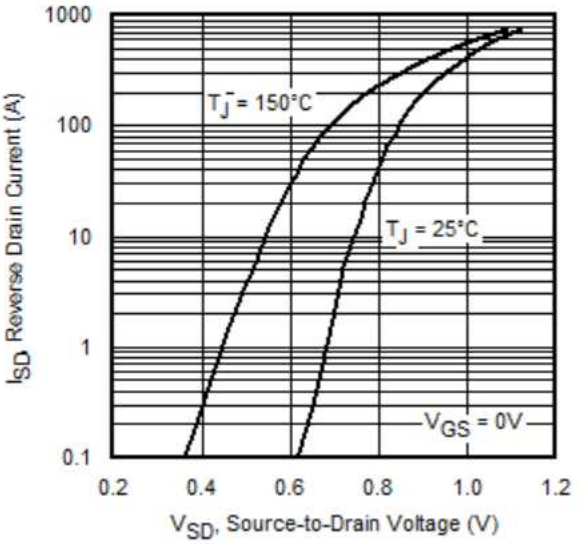


Fig 7. Typical Source-Drain Diode Forward Voltage

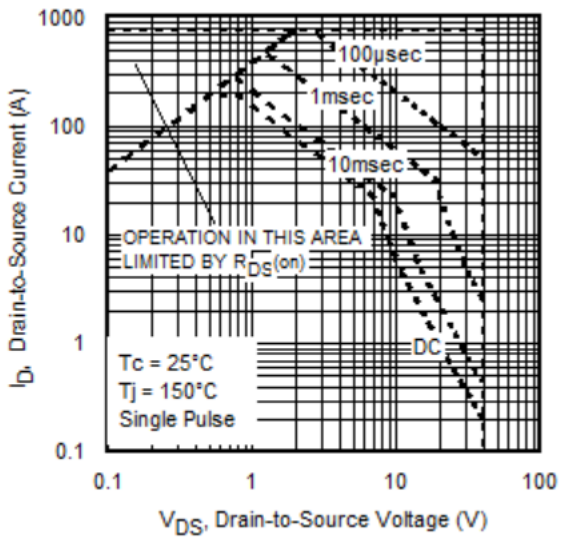


Fig 8. Maximum Safe Operating Area

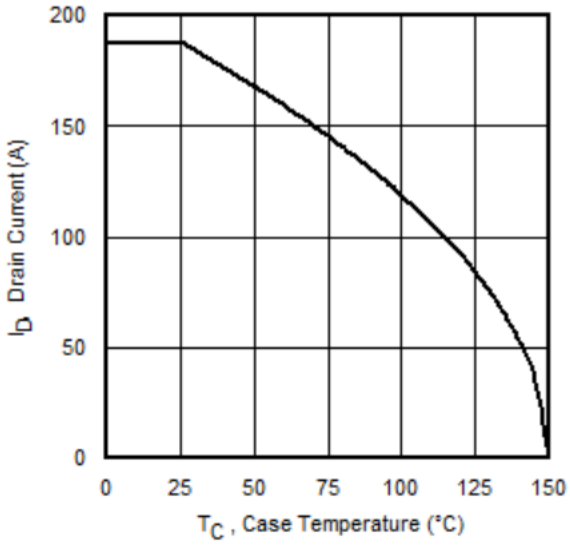


Fig 9. Maximum Drain Current vs. Case Temperature

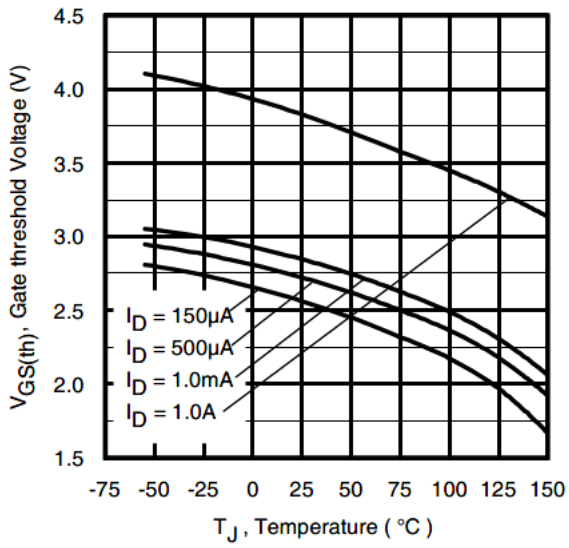


Fig 10. Drain-to-Source Breakdown Voltage

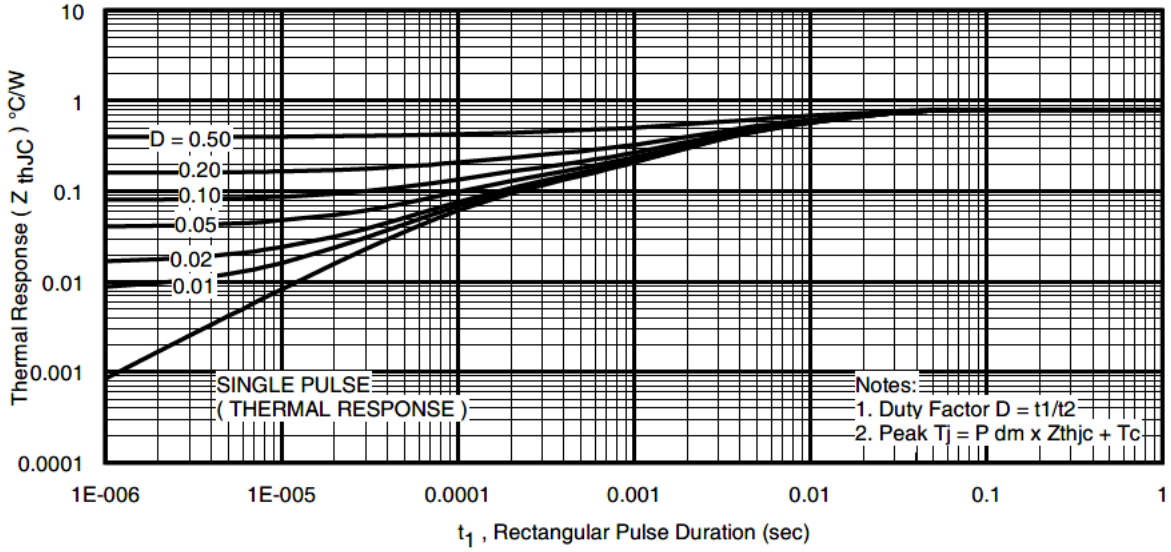


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-

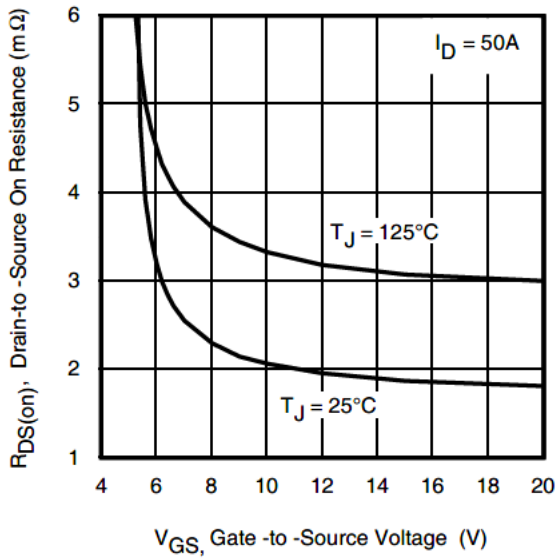


Fig 12. On-Resistance vs. Gate Voltage

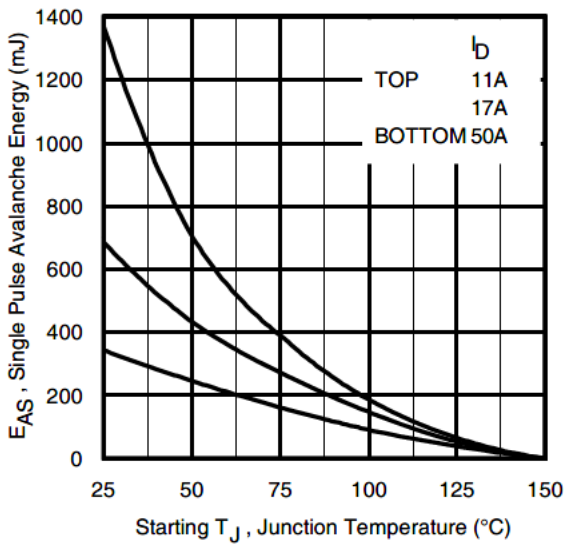


Fig 13. Maximum Avalanche Energy vs. Drain Cur-

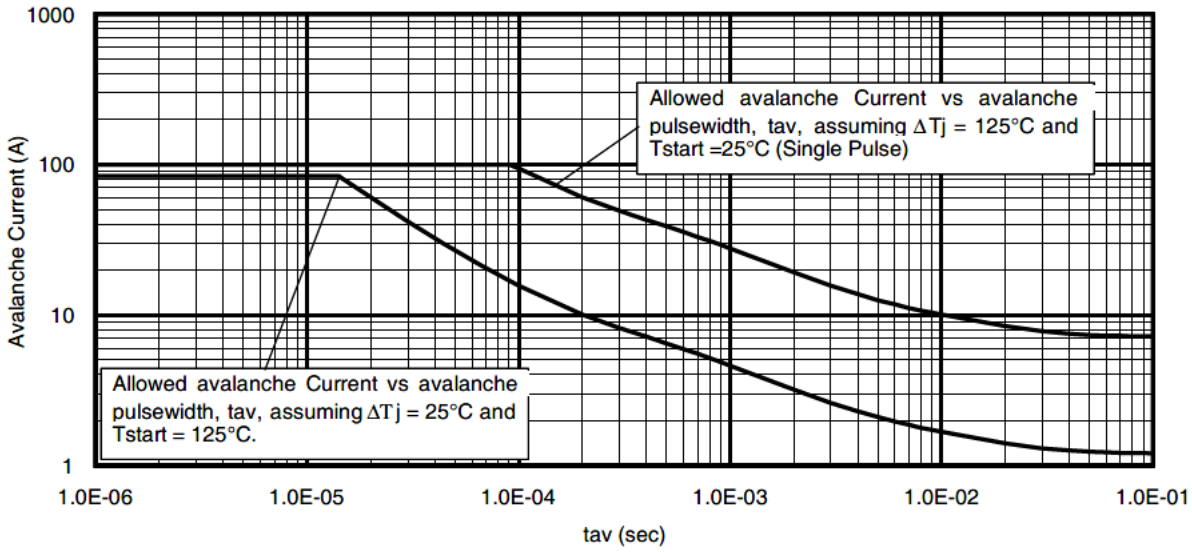


Fig 14. Single Avalanche Event: Pulse Current vs. Pulse Width

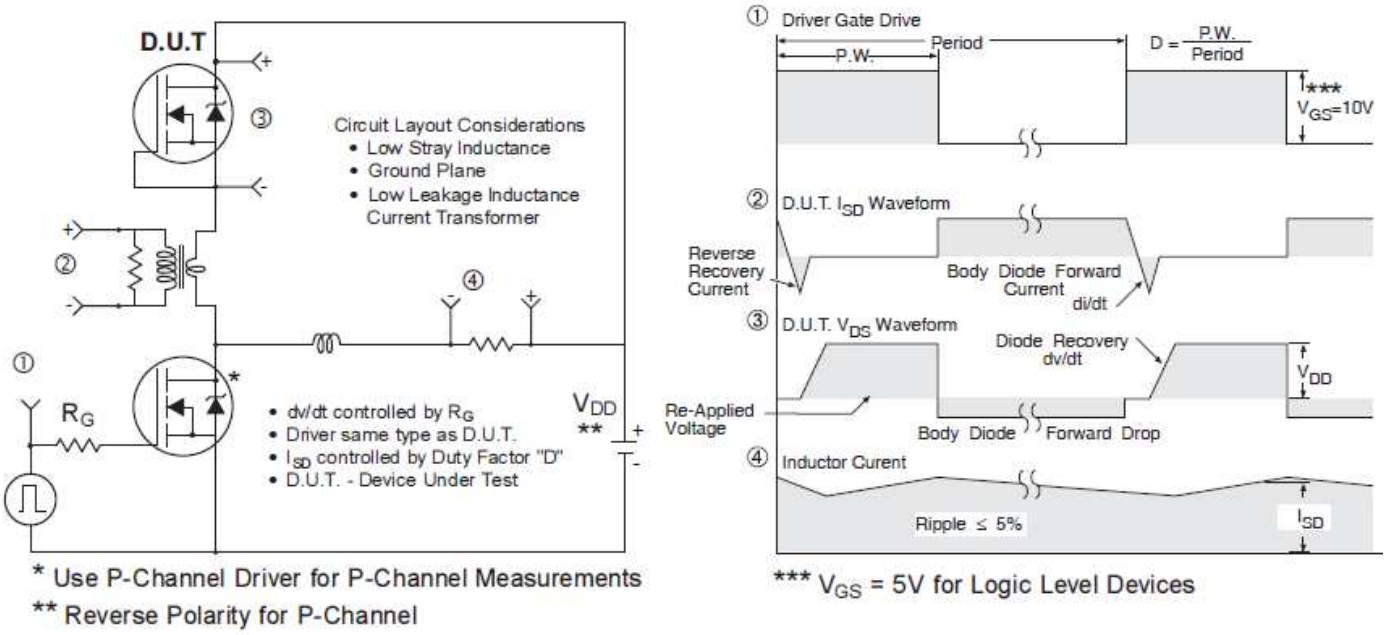


Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

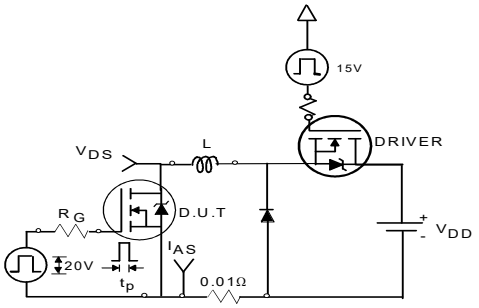


Fig 16a. Unclamped Inductive Test Circuit

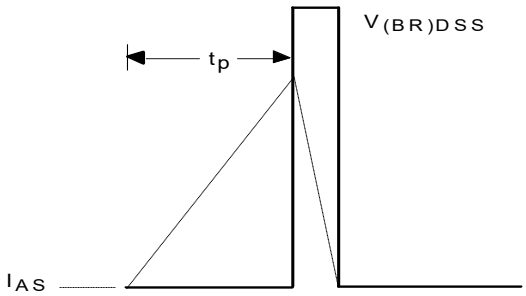


Fig 16b. Unclamped Inductive Waveforms

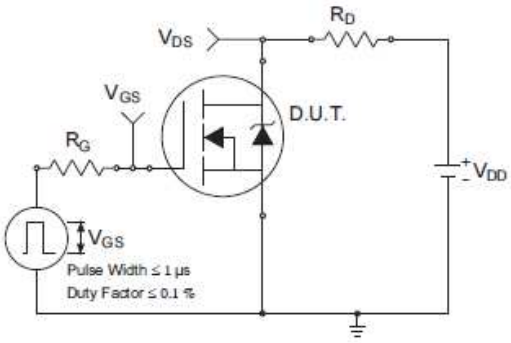


Fig 17a. Switching Time Test Circuit

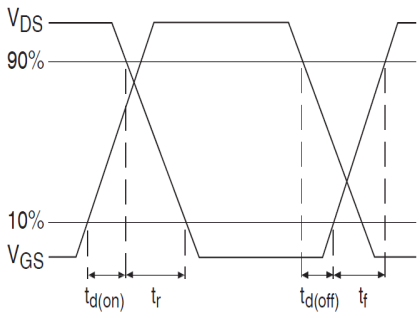


Fig 17b. Switching Time Waveforms

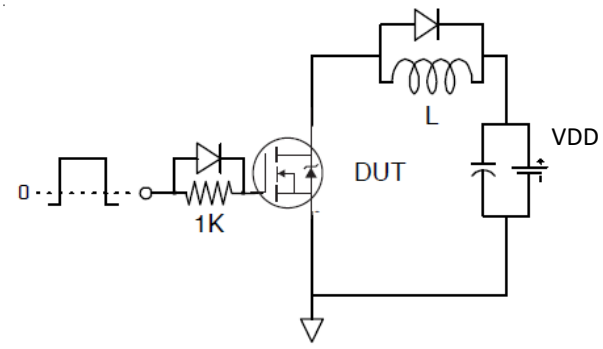


Fig 18. Gate Charge Test Circuit

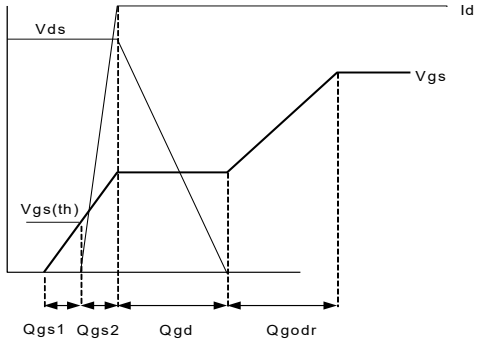
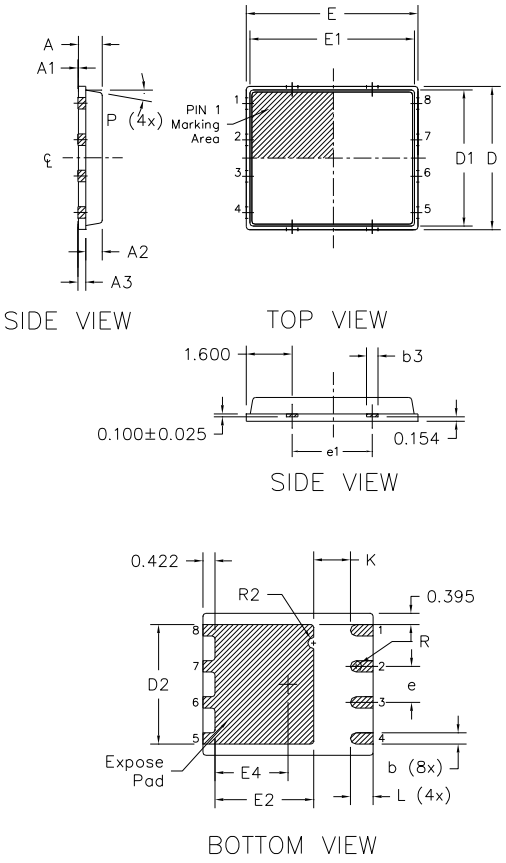


Fig 19. Gate Charge Waveform

PQFN 5x6 Outline "B" Package Details



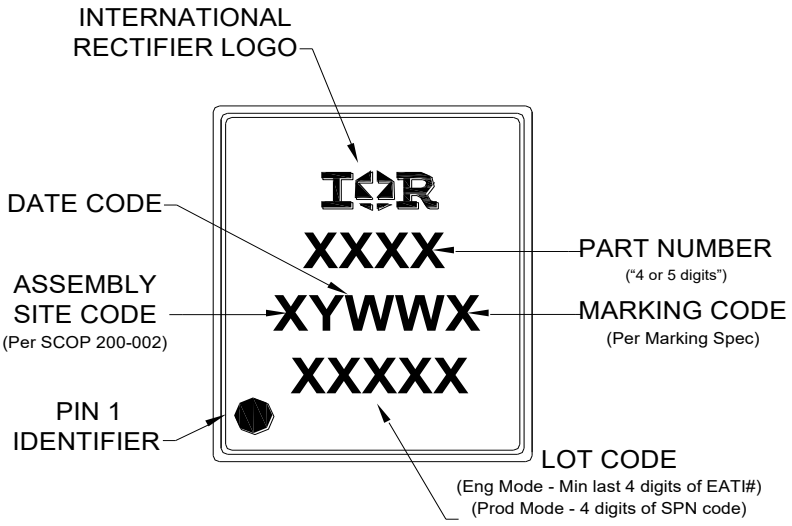
DIM / SYMBOL	MILLIMITERS MIN	MILLIMITERS MAX	INCH MIN	INCH MAX
A	0.800	0.900	0.0315	0.0543
A1	0.000	0.050	0.0000	0.0020
A3	0.200 REF		0.0079 REF	
b	0.350	0.470	0.0138	0.0185
b1	0.025	0.125	0.0010	0.0049
b2	0.210	0.410	0.0083	0.0161
b3	0.150	0.450	0.0059	0.0177
D	5.000 BSC		0.1969 BSC	
D1	4.750 BSC		0.1870 BSC	
D2	4.100	4.300	0.1614	0.1693
E	6.000 BSC		0.2362 BSC	
E1	5.750 BSC		0.2264 BSC	
E2	3.380	3.780	0.1331	0.1488
e	1.270 REF		0.0500 REF	
e1	2.800 REF		0.1102 REF	
K	1.200	1.420	0.0472	0.0559
L	0.710	0.900	0.0280	0.0354
P	0°	12°	0°	12°
R	0.200 REF		0.0079 REF	
R2	0.150	0.200	0.0059	0.0079

Note:

1. Dimensions and toleranceing confirm to ASME Y14.5M–1994
2. Dimension L represents terminal full back from package edge up to 0.1mm is acceptable
3. Coplanarity applies to the expose Heat Slug as well as the terminal
4. Radius on terminal is Optional

For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: http://www.irf.com/technical-info/appnotes/an-1136.pdf
For more information on package inspection techniques, please refer to application note AN-1154: http://www.irf.com/technical-info/appnotes/an-1154.pdf

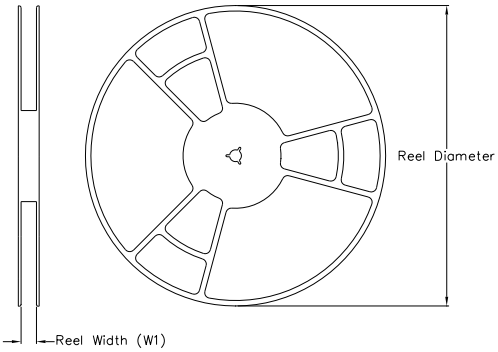
PQFN 5x6 Part Marking



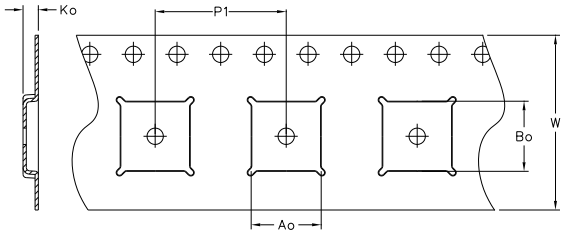
Note: For the most current drawing please refer to IR website at http://www.irf.com/packaging

PQFN 5x6 Tape and Reel

REEL DIMENSIONS

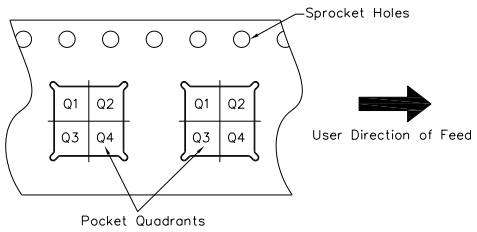


TAPE DIMENSIONS



CODE	DESCRIPTION
Ao	Dimension design to accommodate the component width
Bo	Dimension design to accommodate the component lenght
Ko	Dimension design to accommodate the component thickness
W	Overall width of the carrier tape
P_1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note: All dimension are nominal

Package Type	Reel Diameter (Inch)	QTY	Reel Width W1 (mm)	Ao (mm)	Bo (mm)	Ko (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
5 X 6 PQFN	13	4000	12.4	6.300	5.300	1.20	8.00	12	Q1

Note: For the most current drawing please refer to IR website at http://www.irf.com/packaging

Qualification Information

Qualification Level	Industrial (per JEDEC JESD47F† guidelines)	
Moisture Sensitivity Level	PQFN 5mm x 6mm	MSL1 (per JEDEC J-STD-020D†)
RoHS Compliant	Yes	

† Applicable version of JEDEC standard at the time of product release.

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.
② Starting T_J = 25°C, L = 0.27mH, R_G = 50Ω, I_{AS} = 50A.
③ Pulse width ≤ 400µs; duty cycle ≤ 2%.
④ R_θ is measured at TJ of approximately 90°C.
⑤ When mounted on 1 inch square 2 oz copper pad on 1.5x1.5 in. board of FR-4 material
⑥ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 9. De-rating will be required based on the actual environmental conditions.

Revision History

Date	Rev.	Comments
01/13/2014	2.1	• Updated ordering information to reflect the End-of-Life (EOL) of the mini-reel option (EOL notice #259) • Updated data sheet with the new IR corporate template.
04/28/2015	2.2	• Updated package outline for “option B” and added package outline for “option G” on page 7 • Updated tape and reel on page 8.
5/19/2015	2.3	• Updated package outline for “option G” on page 7 • Updated “IFX logo” on page 1 and page 9
12/08/2020	2.4	• Updated datasheet based on IFX template. • Updated Datasheet based on new current rating and application note :App-AN_1912_PL51_2001_180356

Edition 2016-04-19
Published by
Infineon Technologies AG
81726 Munich, Germany

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Email: erratum@infineon.com

Document reference
ifx1

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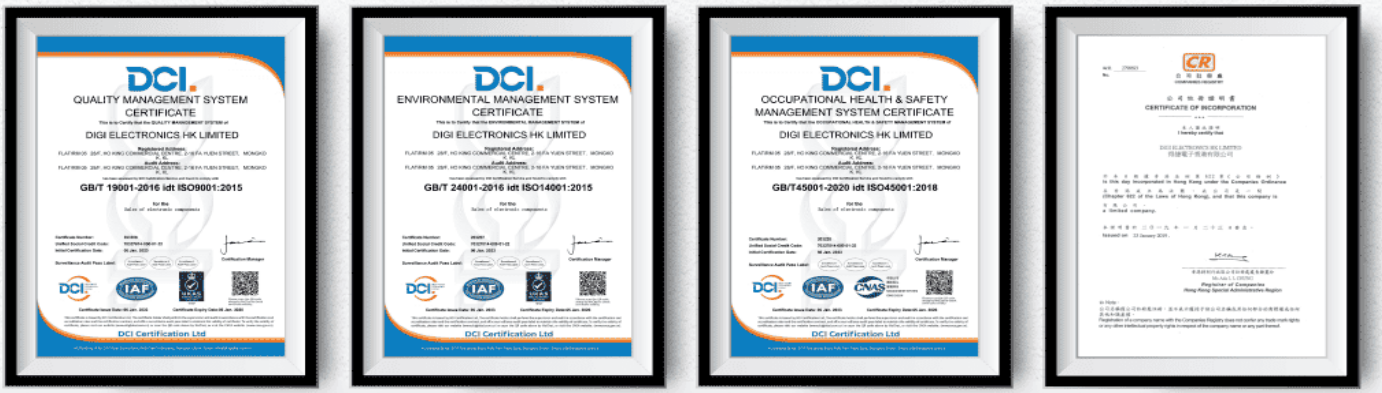

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