IRFH5207TRPBF Datasheet

https://www.DiGi-Electronics.com

DiGi Electronics Part Number	IRFH5207TRPBF-DG
Manufacturer	Infineon Technologies
Manufacturer Product Number	IRFH5207TRPBF
Description	MOSFET N-CH 75V 13A/71A 8PQFN
Detailed Description	N-Channel 75 V 13A (Ta), 71A (Tc) 3.6W (Ta), 105W (Tc) Surface Mount 8-PQFN (5x6)

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
IRFH5207TRPBF	Infineon Technologies
Series:	Product Status:
HEXFET®	Obsolete
FET Type:	Technology:
N-Channel	MOSFET (Metal Oxide)
Drain to Source Voltage (Vdss):	Current - Continuous Drain (Id) @ 25°C:
75 V	13A (Ta), 71A (Tc)
Drive Voltage (Max Rds On, Min Rds On):	Rds On (Max) @ Id, Vgs:
10V	9.6mOhm @ 43A, 10V
Vgs(th) (Max) @ Id:	Gate Charge (Qg) (Max) @ Vgs:
4V @ 100µA	59 nC @ 10 V
Vgs (Max):	Input Capacitance (Ciss) (Max) @ Vds:
±20V	2474 pF @ 25 V
FET Feature:	Power Dissipation (Max):
-	3.6W (Ta), 105W (Tc)
Operating Temperature:	Mounting Type:
-55°C ~ 150°C (TJ)	Surface Mount
Supplier Device Package:	Package / Case:
8-PQFN (5x6)	8-PowerVDFN

Environmental & Export classification

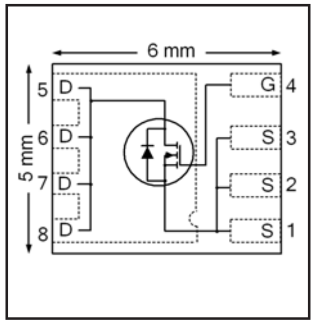
Moisture Sensitivity Level (MSL):	REACH Status:
1 (Unlimited)	REACH Unaffected
ECCN:	HTSUS:
EAR99	8541.29.0095

International
IOR Rectifier

IRFH5207PbF

HEXFET® Power MOSFET

V_{DS}	75	V
$R_{DS(on)}$ max (@V_{GS} = 10V)	9.6	mΩ
Q_g (typical)	40	nC
R_G (typical)	1.7	Ω
I_D (@$T_{c(Bottom)}$ = 25°C)	71	A




PQFN 5X6 mm

Applications

- Secondary Side Synchronous Rectification
- Inverters for DC Motors
- DC-DC Brick Applications
- Boost Converters

Features and Benefits

Features		Benefits
Low RDSon (< 9.6 mΩ)		Lower Conduction Losses
Low Thermal Resistance to PCB (< 1.2°C/W)		Enables better thermal dissipation
100% Rg tested		Increased Reliability
Low Profile (<0.9 mm)	results in	Increased Power Density
Industry-Standard Pinout	⇒	Multi-Vendor Compatibility
Compatible with Existing Surface Mount Techniques		Easier Manufacturing
RoHS Compliant Containing no Lead, no Bromide and no Halogen		Environmentally Friendlier
MSL1, Industrial Qualification		Increased Reliability

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRFH5207TRPbF	PQFN 5mm x 6mm	Tape and Reel	4000	
~~IRFH5207TR2PbF~~	~~PQFN 5mm x 6mm~~	~~Tape and Reel~~	~~400~~	EOL notice # 259

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	75	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 10V	13	A
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ 10V	11	A
I_D @ $T_{C(Bottom)}$ = 25°C	Continuous Drain Current, V_{GS} @ 10V	71	A
I_D @ $T_{C(Bottom)}$ = 100°C	Continuous Drain Current, V_{GS} @ 10V	45	A
I_{DM}	Pulsed Drain Current ①	285	A
P_D @T_A = 25°C	Power Dissipation ⑤	3.6	W
P_D @ $T_{C(Bottom)}$ = 25°C	Power Dissipation ⑤	105	W
	Linear Derating Factor ⑤	0.029	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Notes ① through ⑤ are on page 9

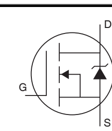
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	75	——	——	V	V_{GS} = 0V, I_D = 250uA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.09	——	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	8.0	9.6	mΩ	V_{GS} = 10V, I_D = 43A ③
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = V_{GS}, I_D = 100μA
$\Delta V_{GS(th)}$	Gate Threshold Voltage Coefficient	——	-8.9	——	mV/°C	
I_{DSS}	Drain-to-Source Leakage Current	——	——	20	μA	V_{DS} = 75V, V_{GS} = 0V
		——	——	250		V_{DS} = 75V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -20V
gfs	Forward Transconductance	51	——	——	S	V_{DS} = 25V, I_D = 43A
Q_g	Total Gate Charge	——	40	60	nC	
Q_{gs1}	Pre-Vth Gate-to-Source Charge	——	6.9	——		V_{DS} = 38V
Q_{gs2}	Post-Vth Gate-to-Source Charge	——	3.8	——		V_{GS} = 10V
Q_{gd}	Gate-to-Drain Charge	——	12	——		I_D = 43A
Q_{godr}	Gate Charge Overdrive	——	17	——		
Q_{sw}	Switch Charge (Q_{gs2} + Q_{gd})	——	15.8	——		
Q_{oss}	Output Charge	——	13	——	nC	V_{DS} = 16V, V_{GS} = 0V
R_G	Gate Resistance	——	1.7	——	Ω	
$t_{d(on)}$	Turn-On Delay Time	——	7.2	——	ns	V_{DD} = 38V, V_{GS} = 10V
t_r	Rise Time	——	12	——		I_D = 43A
$t_{d(off)}$	Turn-Off Delay Time	——	20	——		R_G=1.7Ω
t_f	Fall Time	——	7.1	——		
C_{iss}	Input Capacitance	——	2474	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	313	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	133	——		f = 1.0MHz

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	——	87	mJ
I_{AR}	Avalanche Current ①	——	43	A

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	71	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	285		
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25°C, I_S = 43A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	——	26	39	ns	T_J = 25°C, I_F = 43A, V_{DD} = 38V
Q_{rr}	Reverse Recovery Charge	——	130	195	nC	di/dt = 500A/μs ③
t_{on}	Forward Turn-On Time	Time is dominated by parasitic Inductance				

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$ (Bottom)	Junction-to-Case ④	——	1.2	°C/W
$R_{\theta JC}$ (Top)	Junction-to-Case ④	——	15	
$R_{\theta JA}$	Junction-to-Ambient ⑤	——	35	
$R_{\theta JA}$ (<10s)	Junction-to-Ambient ⑤	——	22	

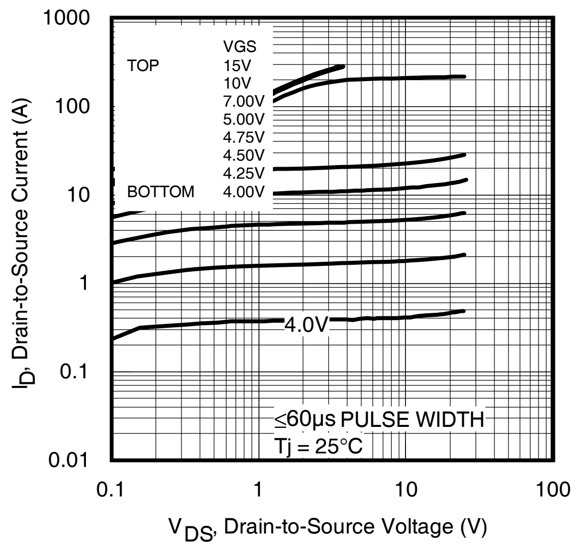


Fig 1. Typical Output Characteristics

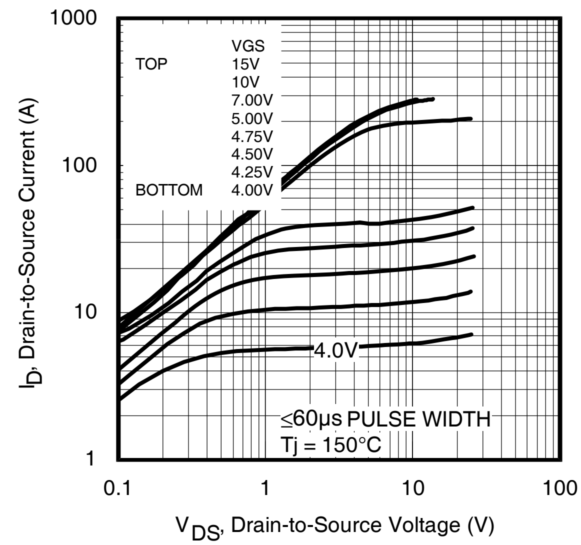


Fig 2. Typical Output Characteristics

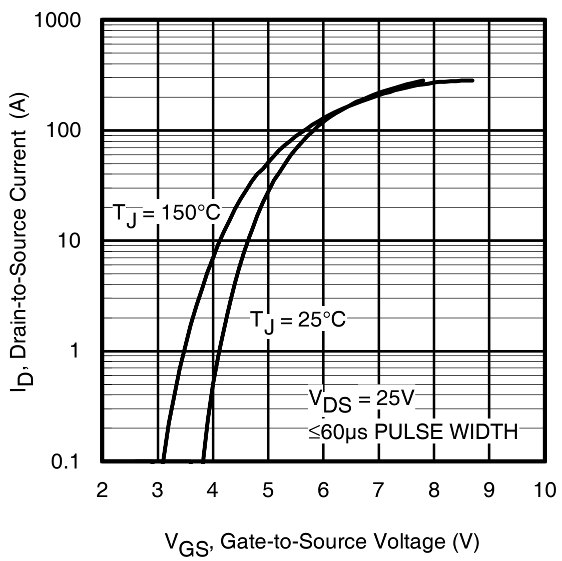


Fig 3. Typical Transfer Characteristics

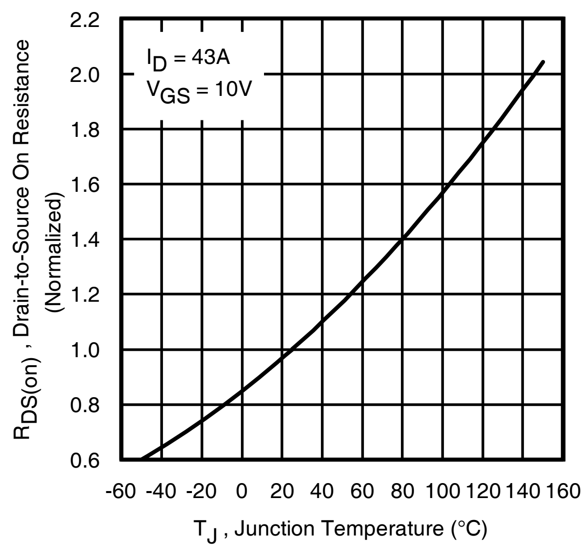


Fig 4. Normalized On-Resistance Vs. Temperature

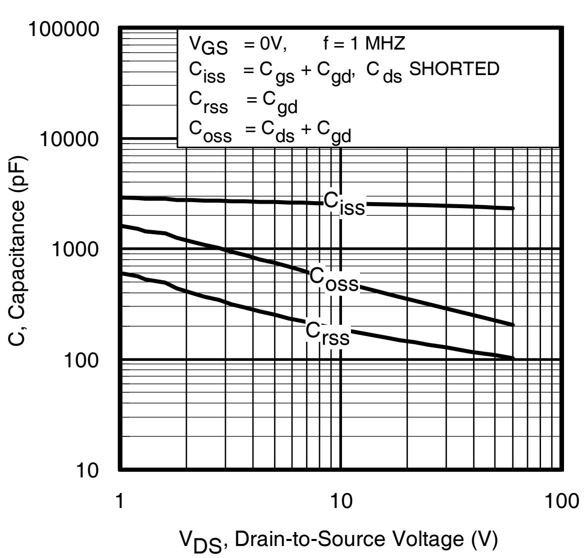


Fig 5. Typical Capacitance Vs.Drain-to-Source Voltage

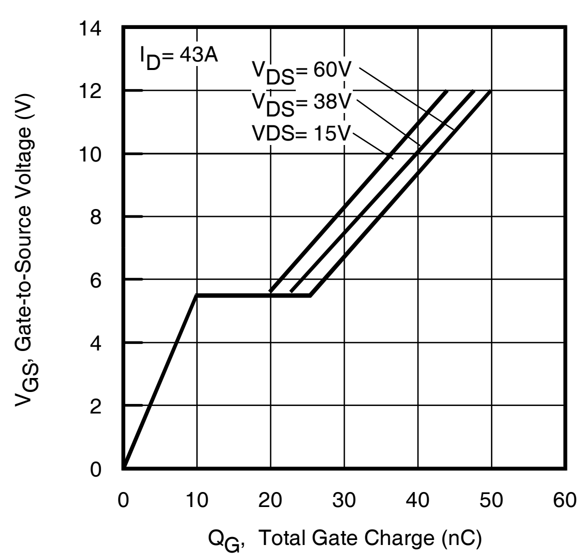


Fig 6. Typical Gate Charge Vs.Gate-to-Source Voltage

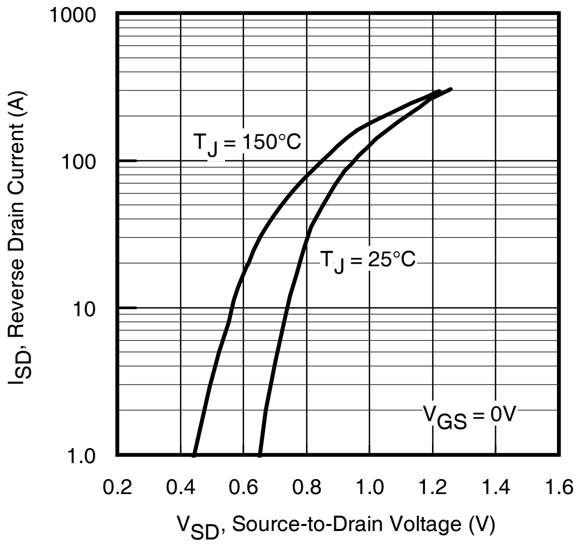


Fig 7. Typical Source-Drain Diode Forward Voltage

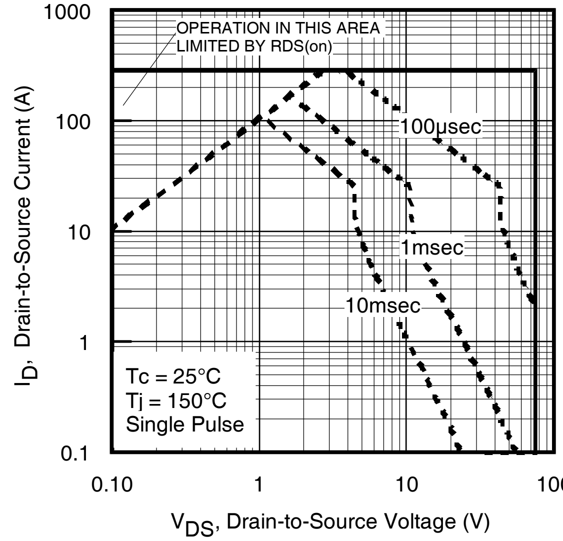


Fig 8. Maximum Safe Operating Area

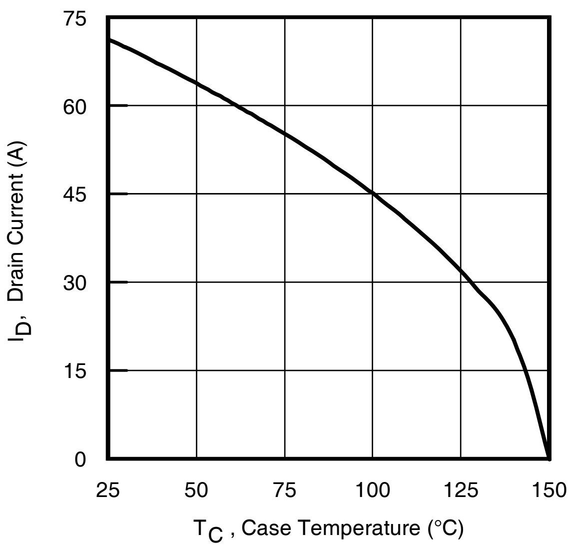


Fig 9. Maximum Drain Current Vs. Case (Bottom) Temperature

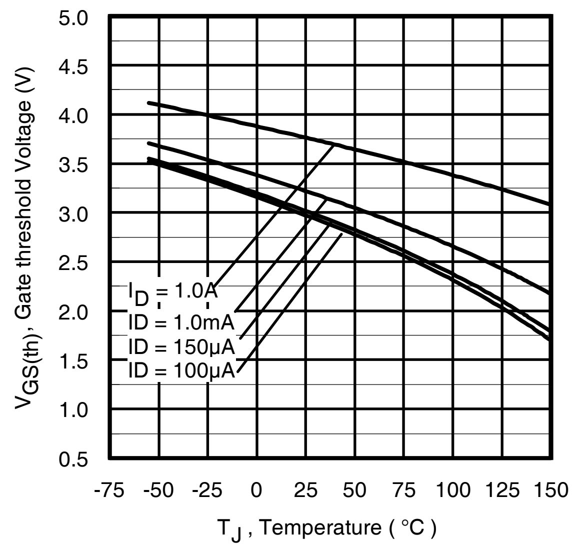


Fig 10. Threshold Voltage Vs. Temperature

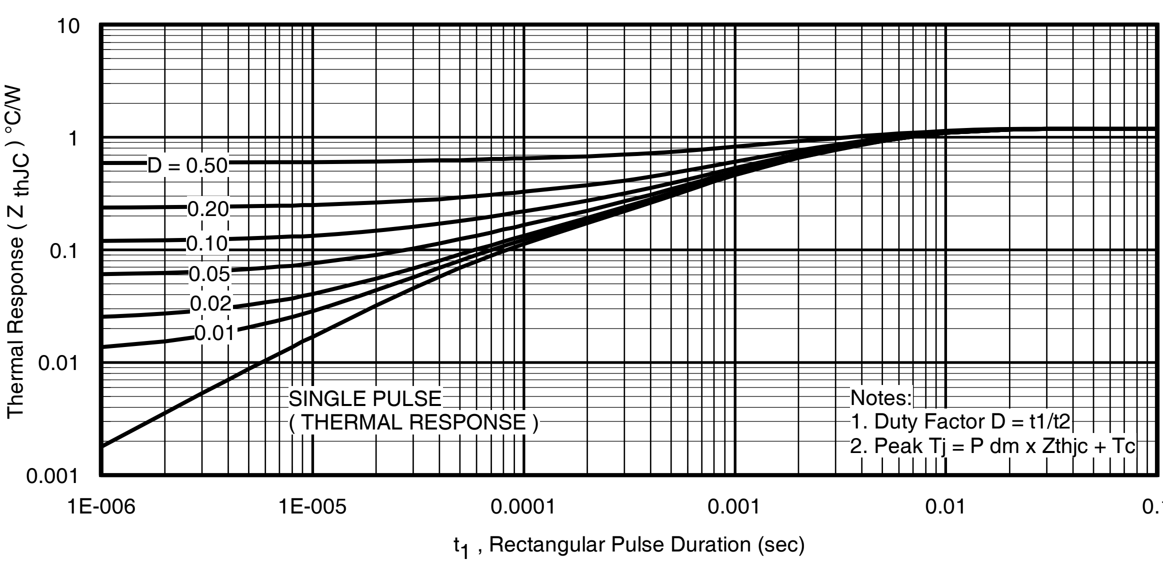


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case (Bottom)

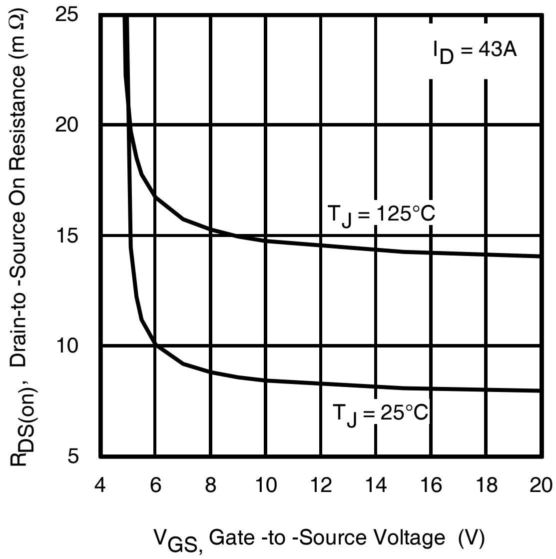


Fig 12. On-Resistance vs. Gate Voltage

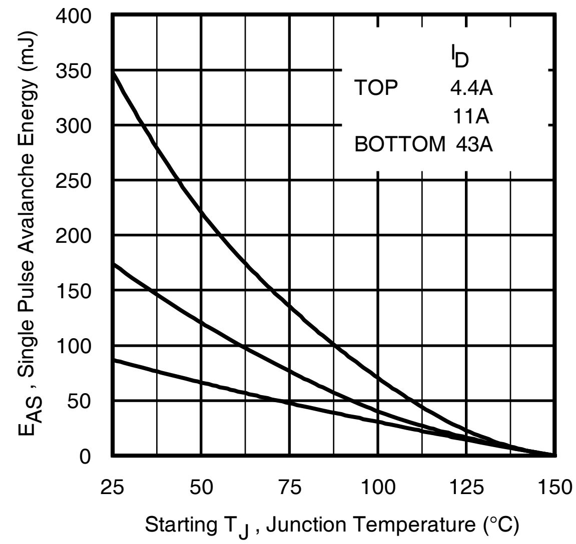


Fig 13. Maximum Avalanche Energy vs. Drain Current

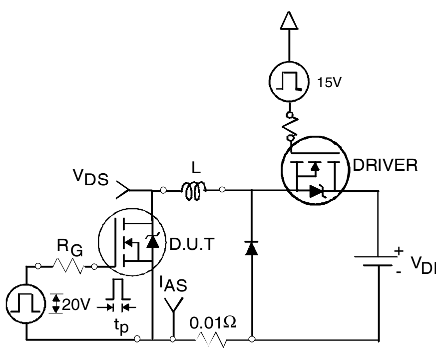


Fig 14a. Unclamped Inductive Test Circuit

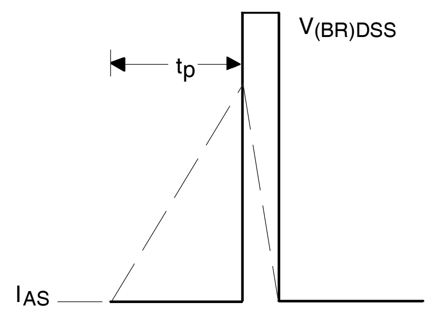


Fig 14b. Unclamped Inductive Waveforms

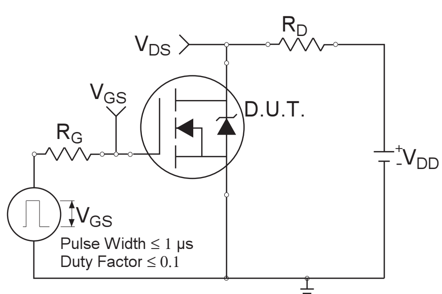


Fig 15a. Switching Time Test Circuit

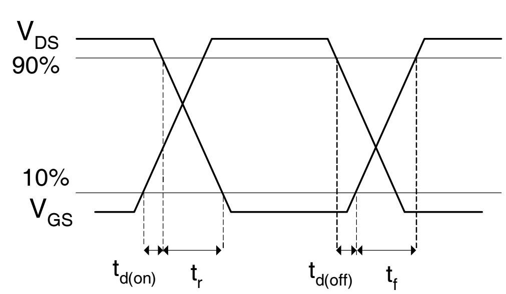


Fig 15b. Switching Time Waveforms

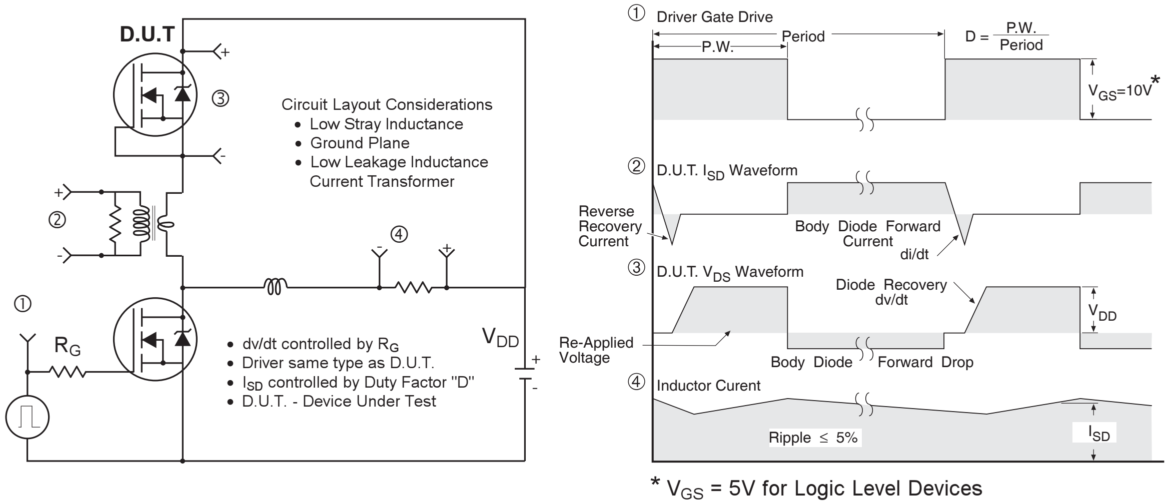


Fig 16. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

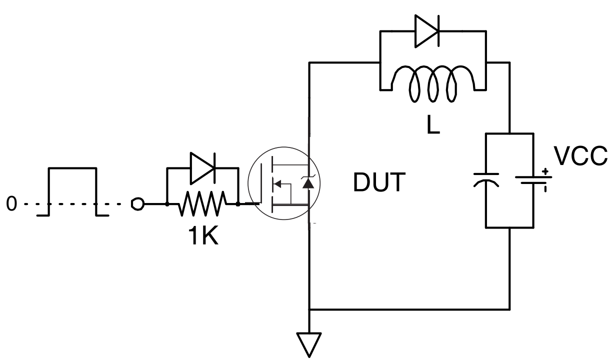


Fig 17. Gate Charge Test Circuit

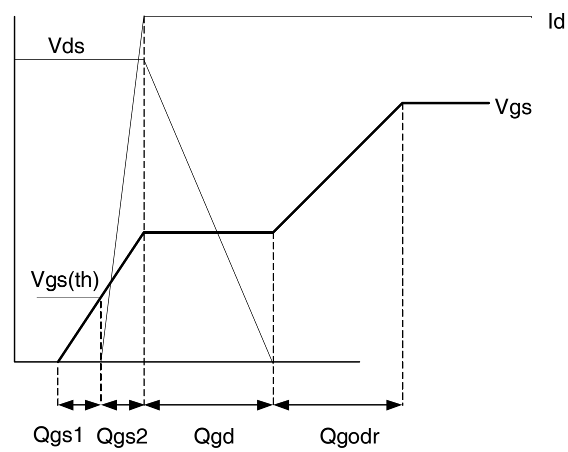
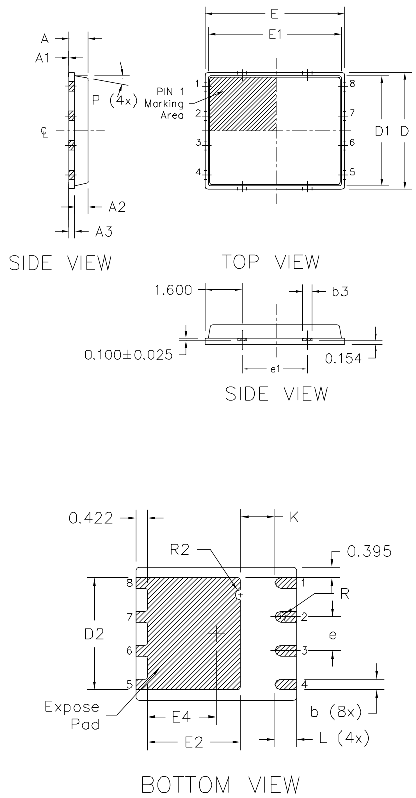


Fig 18. Gate Charge Waveform

PQFN 5x6 Outline "B" Package Details



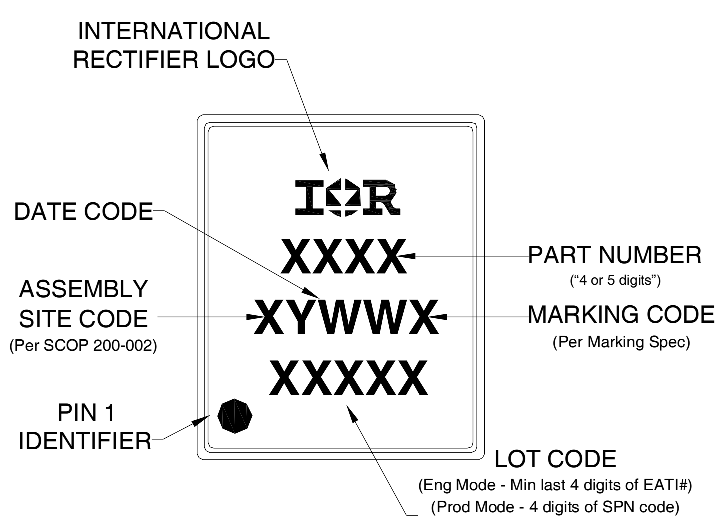
SYMBOL \ DIM	MILLIMITERS		INCH	
	MIN	MAX	MIN	MAX
A	0.800	0.900	0.0315	0.0543
A1	0.000	0.050	0.0000	0.0020
A3	0.200 REF		0.0079 REF	
b	0.350	0.470	0.0138	0.0185
b1	0.025	0.125	0.0010	0.0049
b2	0.210	0.410	0.0083	0.0161
b3	0.150	0.450	0.0059	0.0177
D	5.000 BSC		0.1969 BSC	
D1	4.750 BSC		0.1870 BSC	
D2	4.100	4.300	0.1614	0.1693
E	6.000 BSC		0.2362 BSC	
E1	5.750 BSC		0.2264 BSC	
E2	3.380	3.780	0.1331	0.1488
e	1.270 REF		0.0500 REF	
e1	2.800 REF		0.1102 REF	
K	1.200	1.420	0.0472	0.0559
L	0.710	0.900	0.0280	0.0354
P	0°	12°	0°	12°
R	0.200 REF		0.0079 REF	
R2	0.150	0.200	0.0059	0.0079

Note:

1. Dimensions and toleranceing confirm to ASME Y14.5M−1994
2. Dimension L represents terminal full back from package edge up to 0.1mm is acceptable
3. Coplanarity applies to the expose Heat Slug as well as the terminal
4. Radius on terminal is Optional

For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136:
http://www.irf.com/technical-info/appnotes/an-1136.pdf
For more information on package inspection techniques, please refer to application note AN-1154:
http://www.irf.com/technical-info/appnotes/an-1154.pdf

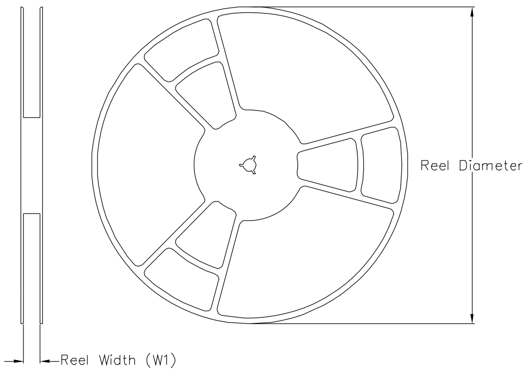
PQFN 5x6 Part Marking



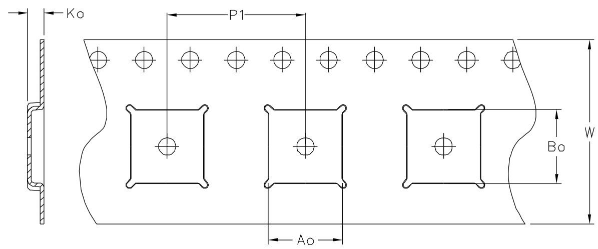
Note: For the most current drawing please refer to IR website at: http://www.irf.com/package/

PQFN 5x6 Tape and Reel

REEL DIMENSIONS

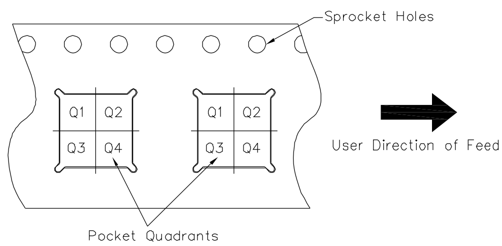


TAPE DIMENSIONS



CODE	DESCRIPTION
Ao	Dimension design to accommodate the component width
Bo	Dimension design to accommodate the component lenght
Ko	Dimension design to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note: All dimension are nominal

Package Type	Reel Diameter (Inch)	QTY	Reel Width W1 (mm)	Ao (mm)	Bo (mm)	Ko (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
5 X 6 PQFN	13	4000	12.4	6.300	5.300	1.20	8.00	12	Q1

Note: For the most current drawing please refer to IR website at: http://www.irf.com/package/

Qualification information†

Qualification level	Industrial†† (per JEDEC JESD47F ††† guidelines)	
Moisture Sensitivity Level	PQFN 5mm x 6mm	MSL1 (per JEDEC J-STD-020D†††)
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/product-info/reliability

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information: http://www.irf.com/whoto-call/salesrep/

††† Applicable version of JEDEC standard at the time of product release.

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.
② Starting T_J = 25°C, L = 0.095mH, R_G = 50Ω, I_{AS} = 43A.
③ Pulse width ≤ 400µs; duty cycle ≤ 2%.
④ $R_θ$ is measured at T_J of approximately 90°C.
⑤ When mounted on 1 inch square 2 oz copper pad on 1.5x1.5 in. board of FR-4 material.

Revision History

Date	Comments
12/16/2013	• Updated ordering information to reflect the End-Of-life (EOL) of the mini-reel option (EOL notice #259) • Updated data sheet with new IR corporate template
3/12/2015	• Updated package outline and tape and reel on pages 7 and 8.

International Rectifier

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DiGi Electronics

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