IRFH7084TRPBF Datasheet

https://www.DiGi-Electronics.com

DiGi Electronics Part Number	IRFH7084TRPBF-DG
Manufacturer	Infineon Technologies
Manufacturer Product Number	IRFH7084TRPBF
Description	MOSFET N-CH 40V 100A 8PQFN
Detailed Description	N-Channel 40 V 100A (Tc) 156W (Tc) Surface Mount 8-PQFN (5x6)

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

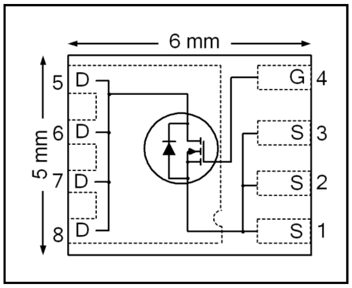
Manufacturer Product Number:	Manufacturer:
IRFH7084TRPBF	Infineon Technologies
Series:	Product Status:
HEXFET®	Active
FET Type:	Technology:
N-Channel	MOSFET (Metal Oxide)
Drain to Source Voltage (Vdss):	Current - Continuous Drain (Id) @ 25°C:
40 V	100A (Tc)
Drive Voltage (Max Rds On, Min Rds On):	Rds On (Max) @ Id, Vgs:
10V	1.25mOhm @ 100A, 10V
Vgs(th) (Max) @ Id:	Gate Charge (Qg) (Max) @ Vgs:
3.9V @ 150µA	190 nC @ 10 V
Vgs (Max):	Input Capacitance (Ciss) (Max) @ Vds:
±20V	6560 pF @ 25 V
FET Feature:	Power Dissipation (Max):
-	156W (Tc)
Operating Temperature:	Mounting Type:
-55°C ~ 150°C (TJ)	Surface Mount
Supplier Device Package:	Package / Case:
8-PQFN (5x6)	8-PowerTDFN
Base Product Number:	
IRFH7084	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8541.29.0095	

Strong*IR*FET™
IRFH7084PbF

Application
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- DC/DC converters
- DC/AC Inverters

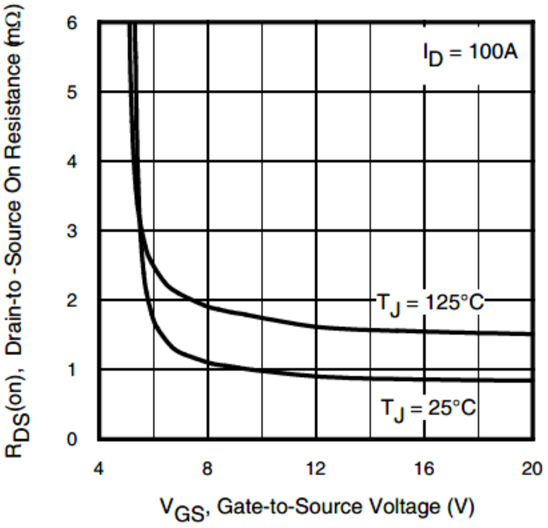


V_{DSS}		40V
$R_{DS(on)}$ typ.		0.95mΩ
max		1.25mΩ
I_D		265A

Benefits
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free, RoHS Compliant


PQFN 5X6 mm

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFH7084PbF	PQFN 5mm x 6mm	Tape and Reel	4000	IRFH7084TRPbF



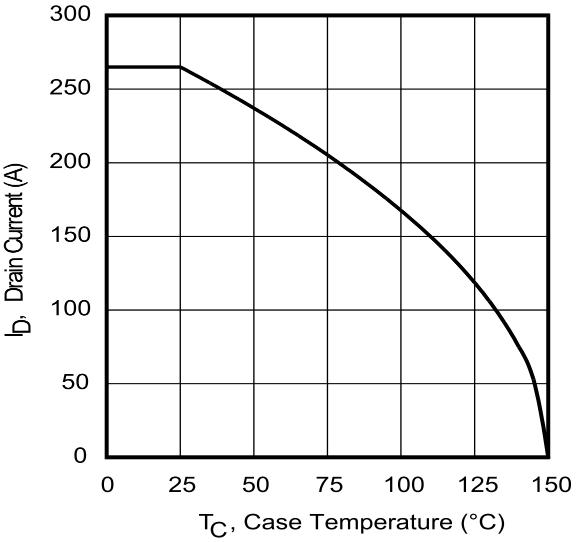


Fig 1. Typical On-Resistance vs. Gate Voltage

Fig 2. Maximum Drain Current vs. Case Temperature

Absolute Maximum Rating

Symbol	Parameter	Max.	Units
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 10V	40	A
I_D @ $T_{C(Bottom)}$ = 25°C	Continuous Drain Current, V_{GS} @ 10V①	265	
I_D @ $T_{C(Bottom)}$ = 100°C	Continuous Drain Current, V_{GS} @ 10V①	170	
I_{DM}	Pulsed Drain Current ②	1060	A
	Linear Derating Factor	1.25	W/°C
P_D @T_C = 25°C	Max Power Dissipation	156	
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Avalanche Characteristics

$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ③	185	mJ
$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ⑨	431	
I_{AR}	Avalanche Current ②	See Fig 14, 15, 23a, 23b	A
E_{AR}	Repetitive Avalanche Energy ②		mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$ (Bottom)	Junction-to-Case ⑧	0.5	0.8	°C/W
$R_{\theta JC}$ (Top)	Junction-to-Case ⑧	——	21	
$R_{\theta JA}$	Junction-to-Ambient ⑩	——	35	
$R_{\theta JA}$ (<10s)	Junction-to-Ambient	——	20	

Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	——	——	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.034	——	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	0.95	1.25	mΩ	V_{GS} = 10V, I_D = 100A
$V_{GS(th)}$	Gate Threshold Voltage	2.2	——	3.9	V	V_{DS} = V_{GS}, I_D = 150μA
I_{DSS}	Drain-to-Source Leakage Current	——	——	1.0	μA	V_{DS} =40 V, V_{GS} = 0V
		——	——	150		V_{DS} =40V,V_{GS} = 0V,T_J =125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -20V
R_G	Gate Resistance	——	1.4	——	Ω	

Notes:

① Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature at 25°C. For higher case temperature please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

② Repetitive rating; pulse width limited by max. junction temperature.

③ Limited by T_{Jmax}, starting T_J = 25°C, L = 0.037mH, R_G = 50Ω, I_{AS} = 100A, V_{GS} =10V.

④ $I_{SD} \leq$ 100A, di/dt $\leq$ 994A/μs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 150°C.

⑤ Pulse width $\leq$ 400μs; duty cycle $\leq$ 2%.

⑥ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑦ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑧ R_θ is measured at T_J approximately 90°C.

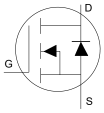
⑨ Limited by T_{Jmax}, starting T_J = 25°C, L = 1mH, R_G = 50Ω, I_{AS} = 29A, V_{GS} =10V.

⑩ When mounted on 1 inch square PCB (FR-4). Please refer to AN-994 for more details: http://www.infineon.com/technical-info/appnotes/an-994.pdf

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	120	——	——	S	V_{DS} = 10V, I_D =100A
Q_g	Total Gate Charge	——	127	190	nC	I_D = 100A
Q_{gs}	Gate-to-Source Charge	——	35	——		V_{DS} = 20V
Q_{gd}	Gate-to-Drain Charge	——	41	——		V_{GS} = 10V
Q_{sync}	Total Gate Charge Sync. (Qg– Qgd)	——	195	——		
$t_{d(on)}$	Turn-On Delay Time	——	16	——	ns	V_{DD} = 20V
t_r	Rise Time	——	31	——		I_D = 30A
$t_{d(off)}$	Turn-Off Delay Time	——	64	——		R_G= 2.7Ω
t_f	Fall Time	——	34	——		V_{GS} = 10V⑤
C_{iss}	Input Capacitance	——	6560	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	940	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	650	——		*ƒ* = 1.0MHz, See Fig.5
$C_{oss\ eff.(ER)}$	Effective Output Capacitance (Energy Related)	——	1120	——		V_{GS} = 0V, VDS = 0V to 32V⑦ See Fig.11
$C_{oss\ eff.(TR)}$	Output Capacitance (Time Related)	——	1300	——		V_{GS} = 0V, VDS = 0V to 32V⑥

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	120	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ②	——	——	1060		
V_{SD}	Diode Forward Voltage⑤	——	——	1.3	V	T_J = 25°C,I_S = 100A,V_{GS} = 0V
dv/dt	Peak Diode Recovery dv/dt ④	——	4.5	——	V/ns	T_J = 150°C,I_S =100A,V_{DS} = 40V
t_{rr}	Reverse Recovery Time	——	36	——	ns	T_J = 25°C V_{DD} = 34V
		——	37	——		T_J = 125°C I_F = 100A,
Q_{rr}	Reverse Recovery Charge	——	38	——	nC	T_J = 25°C di/dt = 100A/μs ⑤
		——	40	——		T_J = 125°C
I_{RRM}	Reverse Recovery Current	——	1.7	——	A	T_J = 25°C

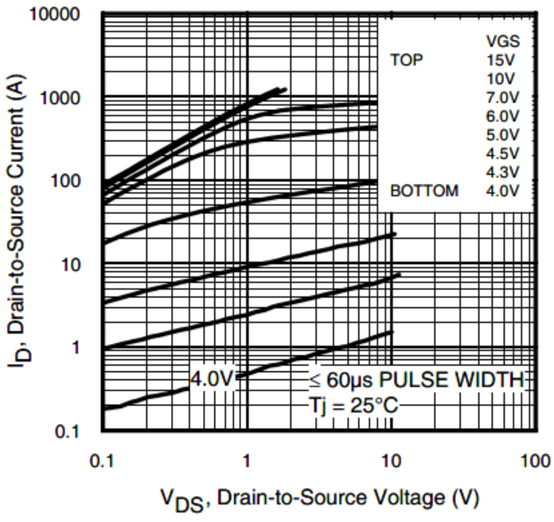


Fig 3. Typical Output Characteristics

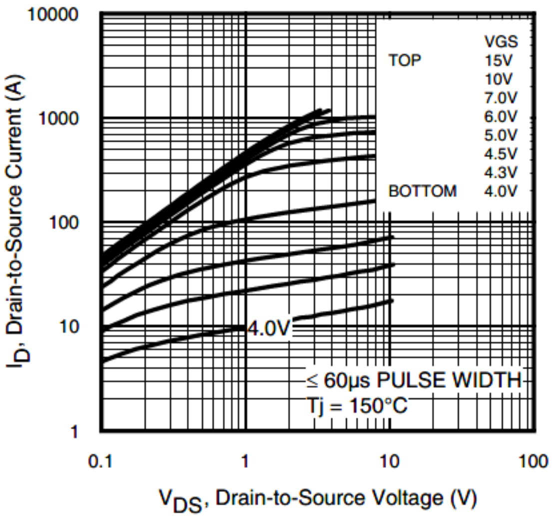
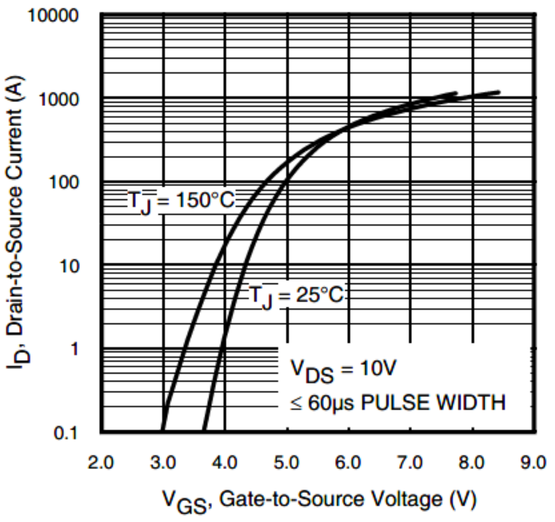


Fig 4. Typical Output Characteristics



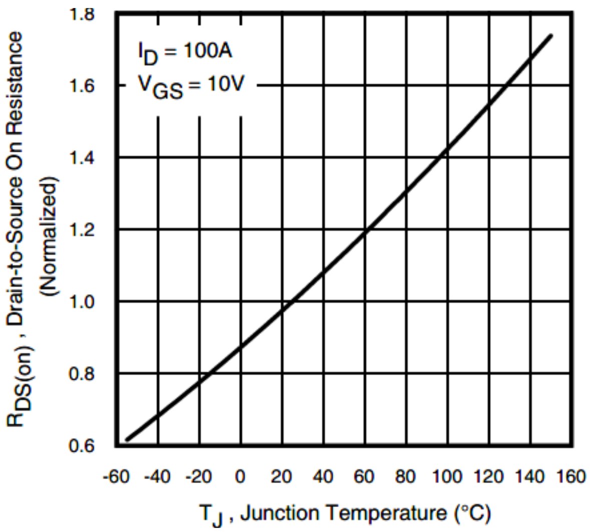
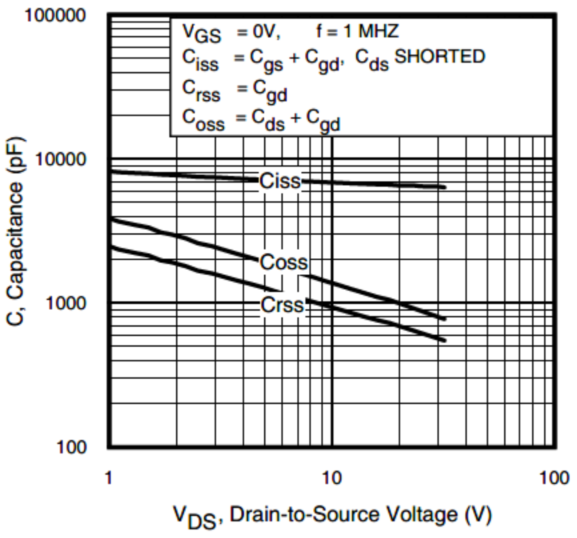


Fig 5. Typical Transfer Characteristics

Fig 6. Normalized On-Resistance vs. Temperature



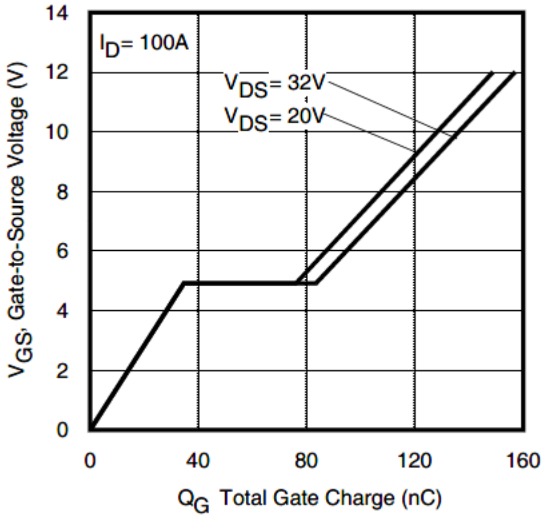


Fig 7. Typical Capacitance vs. Drain-to-Source Voltage

Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage

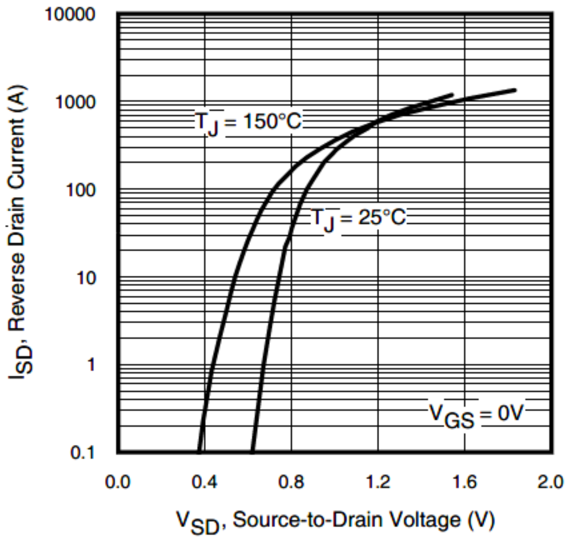


Fig 9. Typical Source-Drain Diode Forward Voltage

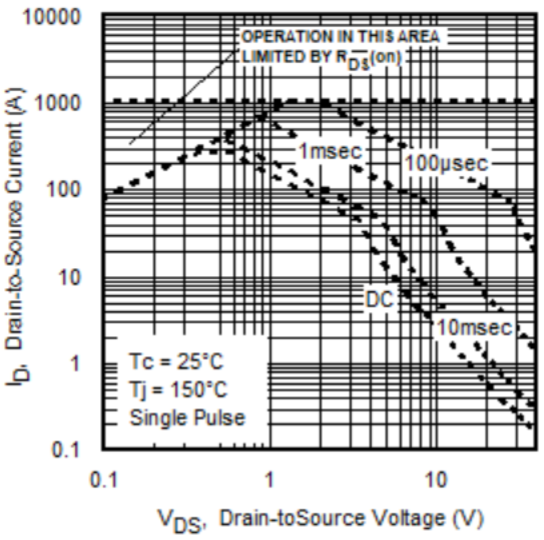


Fig 10. Maximum Safe Operating Area

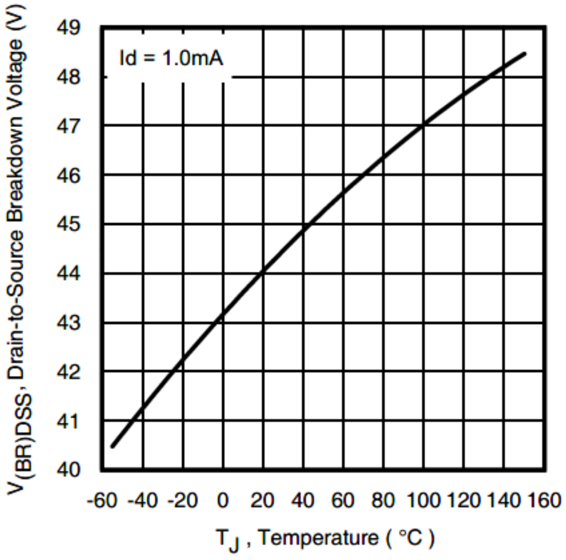


Fig 11. Drain-to–Source Breakdown Voltage

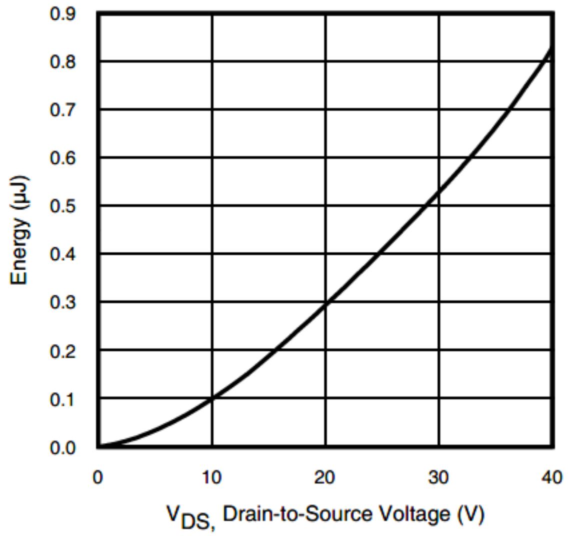


Fig 12. Typical C_{oss} Stored Energy

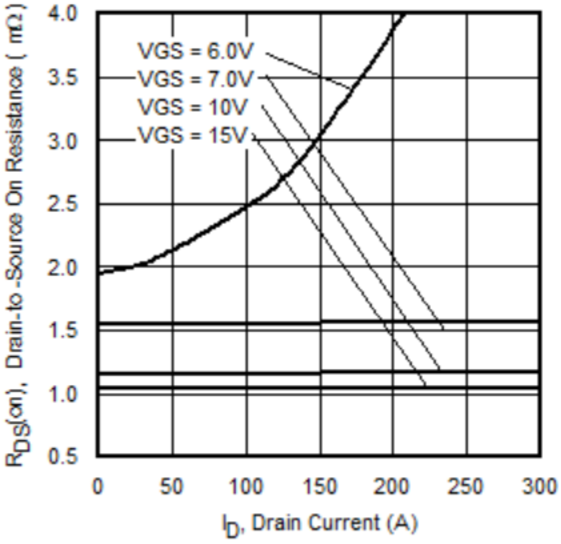


Fig 13. Typical On-Resistance vs. Drain Current

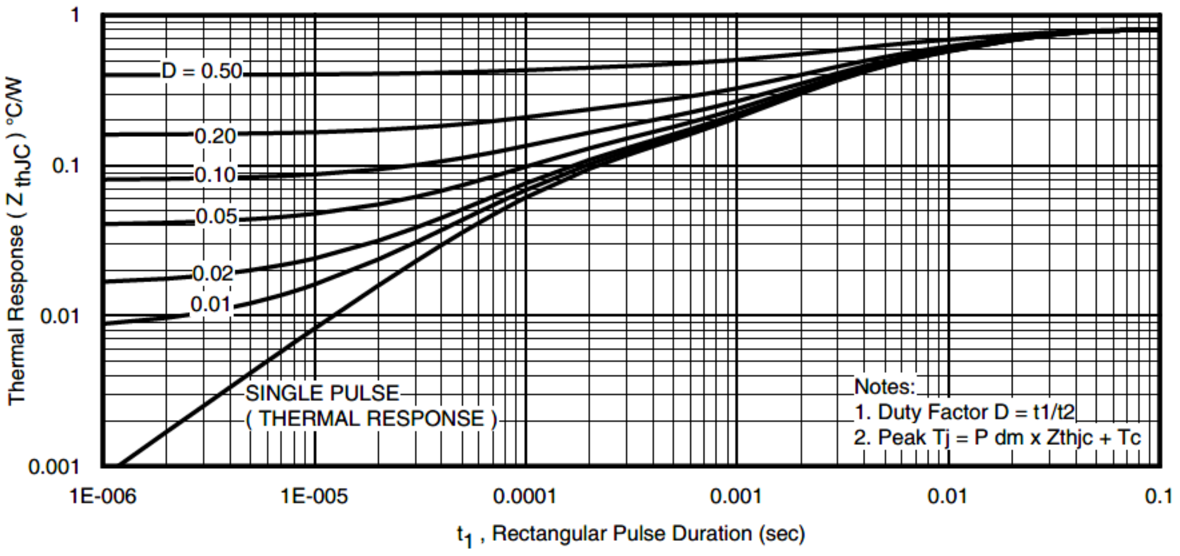


Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case

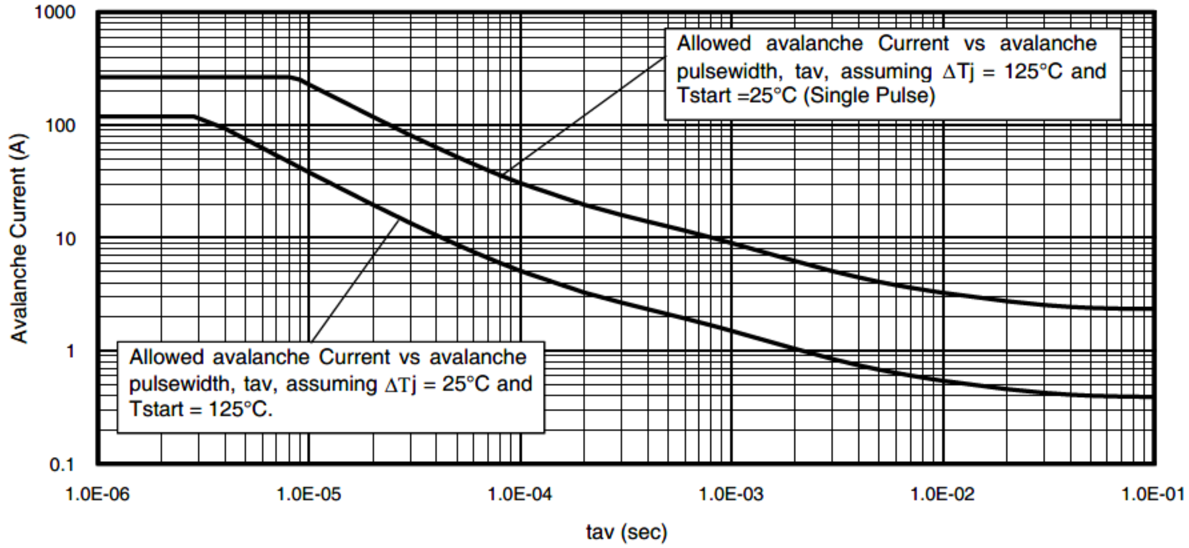


Fig 15. Typical Avalanche Current vs. Pulse width

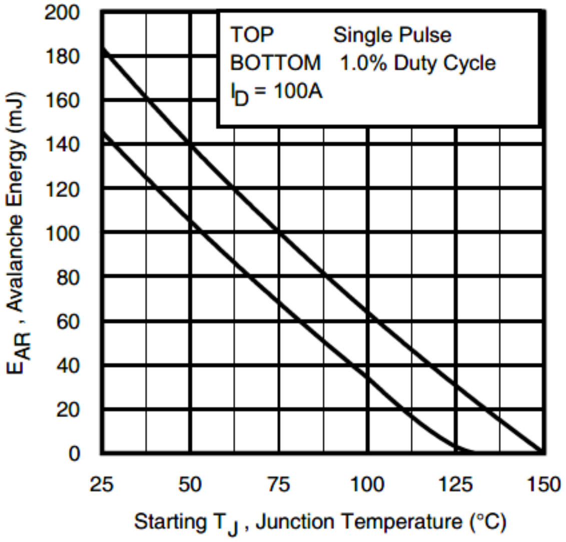


Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.infineon.com)

1.Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long asT_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 22a, 22b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).

t_{av} = Average time in avalanche.
D = Duty cycle in avalanche = tav ·f
$Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)
$PD\ (ave) = 1/2\ (\ 1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$
$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$
$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$

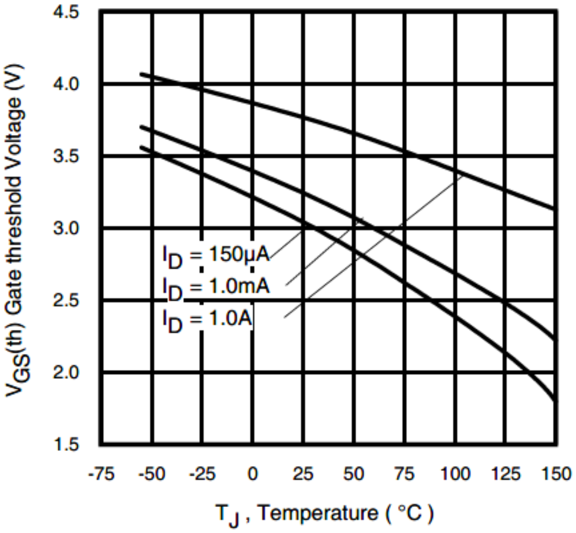


Fig 17. Threshold Voltage vs. Temperature

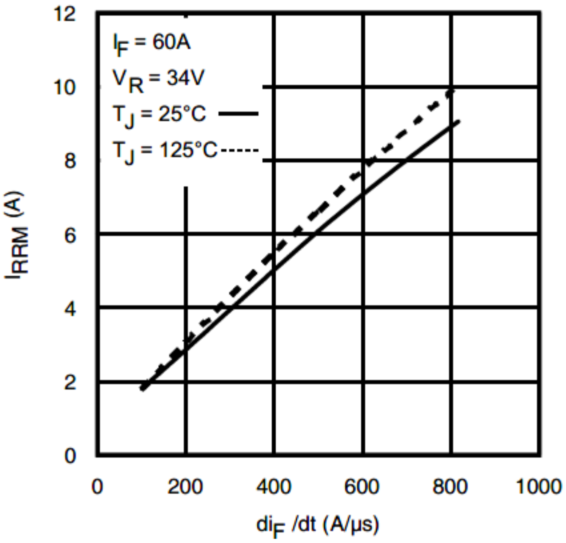


Fig 18. Typical Recovery Current vs. dif/dt

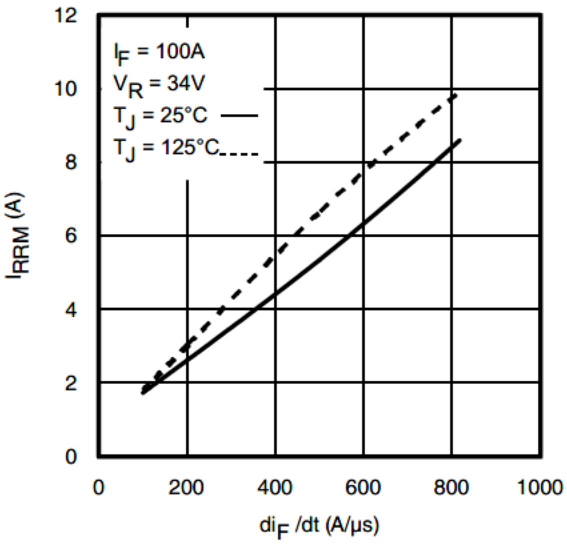


Fig 19. Typical Recovery Current vs. dif/dt

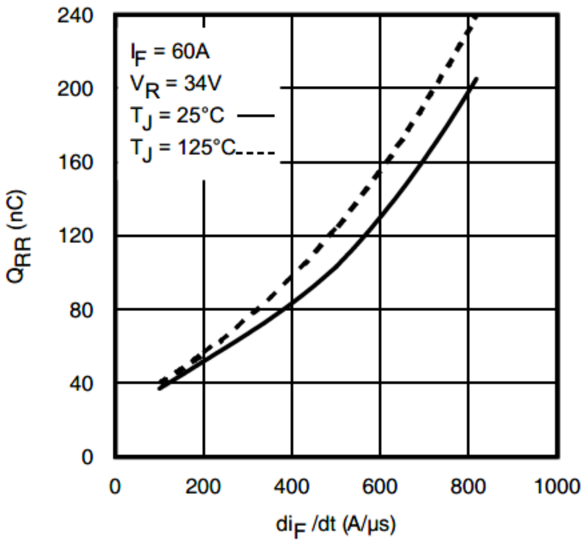


Fig 20. Typical Stored Charge vs. dif/dt

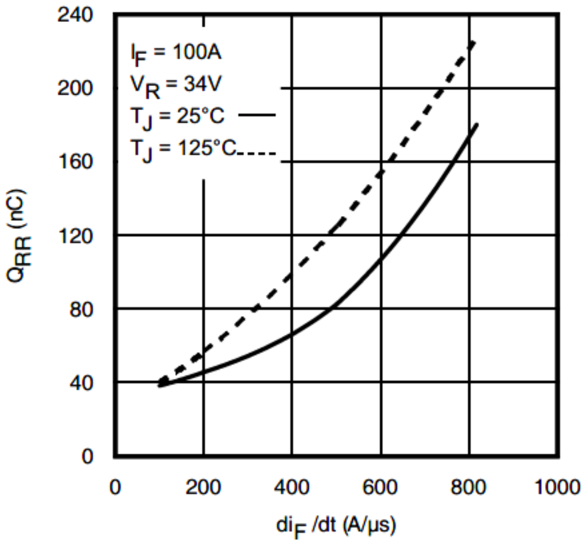
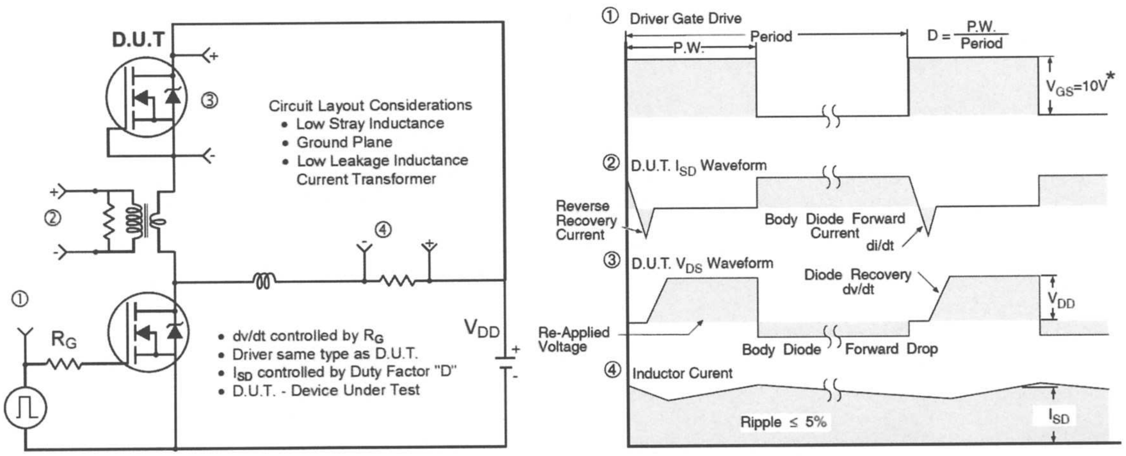


Fig 21. Typical Stored Charge vs. dif/dt



* V_{GS} = 5V for Logic Level Devices

Fig 22. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

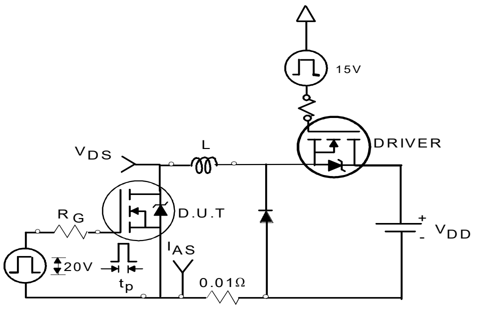


Fig 23a. Unclamped Inductive Test Circuit

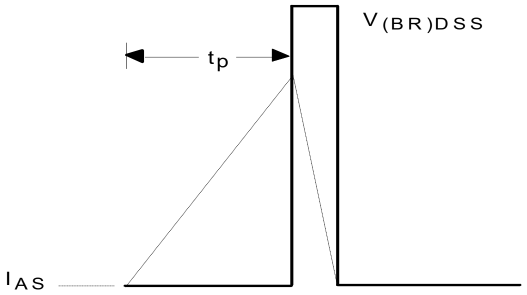


Fig 23b. Unclamped Inductive Waveforms

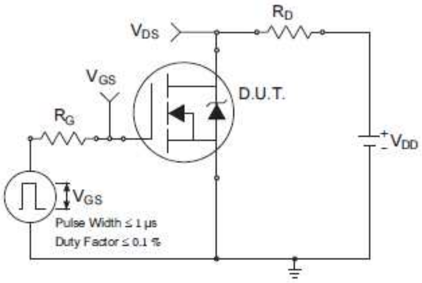


Fig 24a. Switching Time Test Circuit

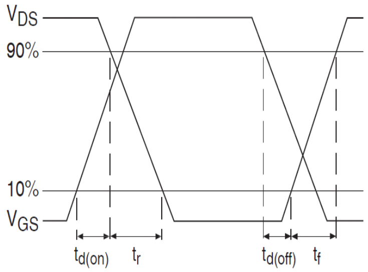


Fig 24b. Switching Time Waveforms

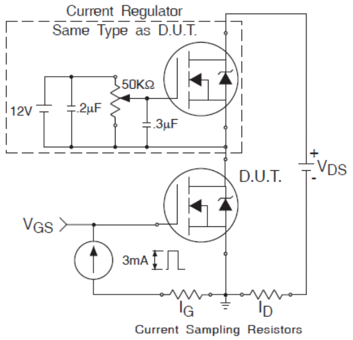


Fig 25a. Gate Charge Test Circuit

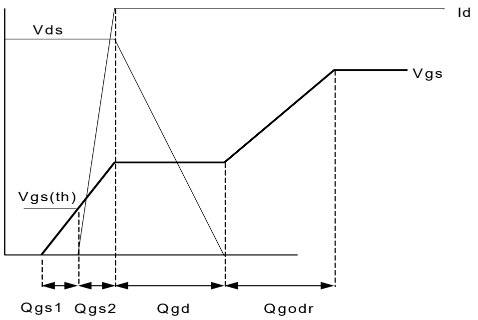
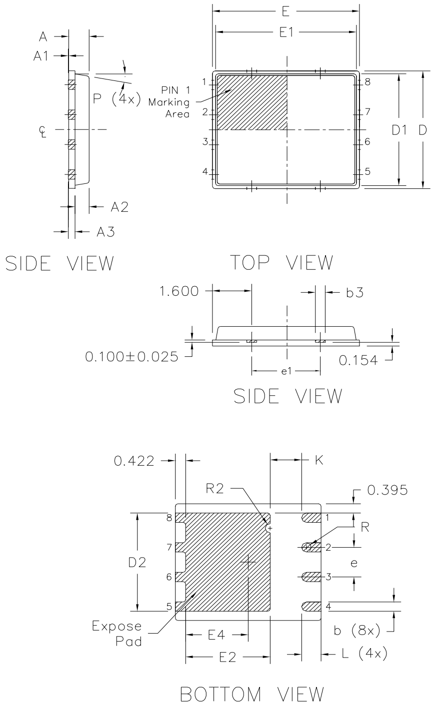


Fig 25b. Gate Charge Waveform

PQFN 5x6 Outline "B" Package Details

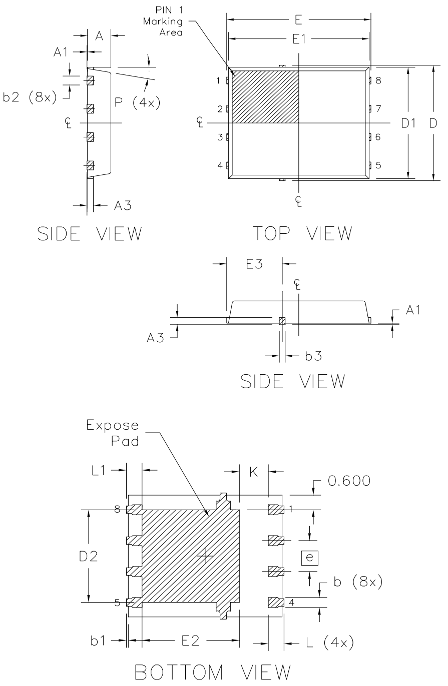


DIM / SYMBOL	MILLIMITERS MIN	MILLIMITERS MAX	INCH MIN	INCH MAX
A	0.800	0.900	0.0315	0.0543
A1	0.000	0.050	0.0000	0.0020
A3	0.200 REF		0.0079 REF	
b	0.350	0.470	0.0138	0.0185
b1	0.025	0.125	0.0010	0.0049
b2	0.210	0.410	0.0083	0.0161
b3	0.150	0.450	0.0059	0.0177
D	5.000 BSC		0.1969 BSC	
D1	4.750 BSC		0.1870 BSC	
D2	4.100	4.300	0.1614	0.1693
E	6.000 BSC		0.2362 BSC	
E1	5.750 BSC		0.2264 BSC	
E2	3.380	3.780	0.1331	0.1488
e	1.270 REF		0.0500 REF	
e1	2.800 REF		0.1102 REF	
K	1.200	1.420	0.0472	0.0559
L	0.710	0.900	0.0280	0.0354
P	0°	12°	0°	12°
R	0.200 REF		0.0079 REF	
R2	0.150	0.200	0.0059	0.0079

Note:

1. Dimensions and toleranceing confirm to ASME Y14.5M−1994
2. Dimension L represents terminal full back from package edge up to 0.1mm is acceptable
3. Coplanarity applies to the expose Heat Slug as well as the terminal
4. Radius on terminal is Optional

PQFN 5x6 Outline "G" Package Details



DIM / SYMBOL	MILLIMETERS MIN.	MILLIMETERS MAX.	INCH MIN.	INCH MAX.
A	0.950	1.050	0.0374	0.0413
A1	0.000	0.050	0.0000	0.0020
A3	0.254 REF		0.0100 REF	
b	0.310	0.510	0.0122	0.0201
b1	0.025	0.125	0.0010	0.0049
b2	0.210	0.410	0.0083	0.0161
b3	0.180	0.450	0.0071	0.0177
D	5.150 BSC		0.2028 BSC	
D1	5.000 BSC		0.1969 BSC	
D2	3.700	3.900	0.1457	0.1535
E	6.150 BSC		0.2421 BSC	
E1	6.000 BSC		0.2362 BSC	
E2	3.560	3.760	0.1402	0.1488
E3	2.270	2.470	0.0894	0.0972
e	1.27 REF		0.050 REF	
K	0.830	1.400	0.0327	0.0551
L	0.510	0.710	0.0201	0.0280
L1	0.510	0.710	0.0201	0.0280
P	10 deg	12 deg	0 deg	12 deg

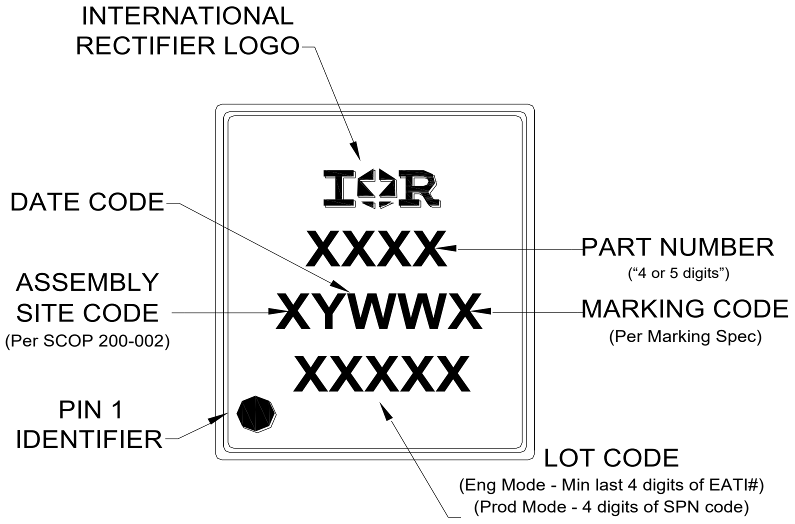
Note:

1. Dimensions and toleranceing confirm to ASME Y14.5M−1994
2. Dimension L represents terminal full back from package edge up to 0.1mm is acceptable
3. Coplanarity applies to the expose Heat Slug as well as the terminal
4. Radius on terminal is Optional

For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: http://www.infineon.com/technical-info/appnotes/an-1136.pdf
For more information on package inspection techniques, please refer to application note AN-1154: http://www.infineon.com/technical-info/appnotes/an-1154.pdf

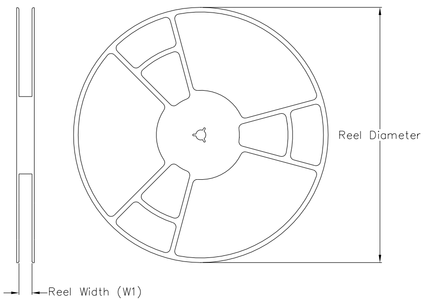
Note: For the most current drawing please refer to IR website at http://www.infineon.com/package/

PQFN 5x6 Part Marking

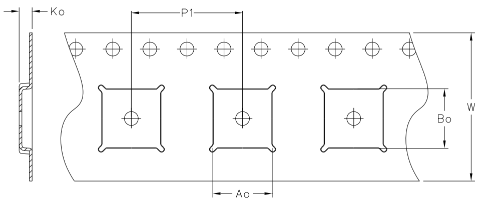


PQFN 5x6 Tape and Reel

REEL DIMENSIONS

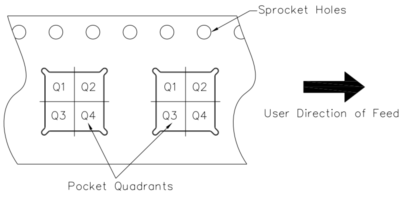


TAPE DIMENSIONS



CODE	DESCRIPTION
Ao	Dimension design to accommodate the component width
Bo	Dimension design to accommodate the component lenght
Ko	Dimension design to accommodate the component thickness
W	Overall width of the carrier tape
P_1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note: All dimension are nominal

Package Type	Reel Diameter (Inch)	QTY	Reel Width W1 (mm)	Ao (mm)	Bo (mm)	Ko (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
5 X 6 PQFN	13	4000	12.4	6.300	5.300	1.20	8.00	12	Q1

Note: For the most current drawing please refer to IR website at http://www.infineon.com/package/

Qualification information†

Qualification level	Industrial†† (per JEDEC JESD47F †† guidelines)	
Moisture Sensitivity Level	PQFN 5mmx 6mm	MSL1 (per JEDEC J-STD-020D††)
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: http://www.infineon.com/product-info/reliability/

†† Applicable version of JEDEC standard at the time of product release.

Revision History

Date	Rev.	Comments
10/16/2014	2.1	• Add Pd at tc=25C on Absolute Max Rating table on page 2
03/05/2015	2.2	• Updated $E_{AS\ (L=1mH)}$ = 431mJ on page 2 • Updated note 8 "Limited by T_{Jmax}, starting T_J = 25°C, L = 1mH, R_G = 50Ω, I_{AS} = 29A, V_{GS} =10V" on page 2
03/19/2015	2.3	• Updated package outline on page 9.
01/24/2017	2.4	• Changed datasheet with Infineon logo - all pages • Added package outline for "option G" on page 9. • Added disclaimer on last page
4/14/2020	2.5	• Updated datasheet based on IFX template. • Updated Datasheet based on new current rating and application note :App-AN_1912_PL51_2001_180356

We Listen to Your Comments
Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:
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Published by
Infineon Technologies AG
81726 München, Germany

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