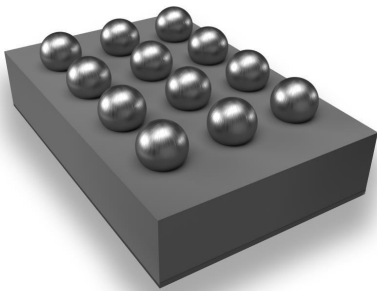


# KTS1663EUW-TR Datasheet

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DiGi Electronics Part Number	KTS1663EUW-TR-DG
Manufacturer	<a href="#">Kinetic Technologies</a>
Manufacturer Product Number	KTS1663EUW-TR
Description	40V ADJUSTABLE OVER-VOLTAGE PROT
Detailed Description	Power Switch/Driver 1:1 N-Channel 4.5A 12-WLCSP (1.28x1.94)



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## Purchase and inquiry

Manufacturer Product Number:

KTS1663EUW-TR

Series:

-

Switch Type:

USB Switch

Ratio - Input:Output:

1:1

Output Type:

N-Channel

Voltage - Load:

2.5V ~ 40V

Current - Output (Max):

4.5A

Input Type:

Non-Inverting

Fault Protection:

Over Temperature, Over Voltage, Short Circuit, UVLO

Mounting Type:

Surface Mount

Package / Case:

12-WFBGA, WLCSP

Manufacturer:

Kinetic Technologies

Product Status:

Active

Number of Outputs:

1

Output Configuration:

High Side

Interface:

On/Off

Voltage - Supply (Vcc/Vdd):

Not Required

Rds On (Typ):

26mOhm

Features:

Power Good, Slew Rate Controlled, Status Flag

Operating Temperature:

-40°C ~ 85°C

Supplier Device Package:

12-WLCSP (1.28x1.94)



## Adjustable Overvoltage Protection Switch

### Features

- Wide Input voltage range: 2.5V to 40V
- Up to 4.5A current capability
- Integrated 26m $\Omega$  (typ) N-Channel MOSFET
- Fast OVP turn-off response time: 100ns
- Selectable trip-point options
  - ▶ Fixed 5.95V
  - ▶ Fixed 10.2V
  - ▶ Fixed 13.5V
  - ▶ Adj. 4V to 28V
- Auto-enabled switch with 18ms debounce time
- Under voltage (UVLO), Short-circuit and thermal shutdown protection
- Open-drain power good output
- VDET output to indicate the presence of VBUS
- ESD Protection
  - ▶ Human Body Model:  $\pm 2.0\text{kV}$
- Pb-free WLCSP-12 package
- -40°C to +85°C Temperature Range

### Applications

- Smartphones
- Mobile Internet Devices
- Tablet Computers
- Peripherals

### Brief Description

The KTS1663 overvoltage protection device features an ultra-low 26m $\Omega$  (typical) on-resistance high current integrated MOSFET which actively protects low-voltage systems from voltage supply faults up to +40V.

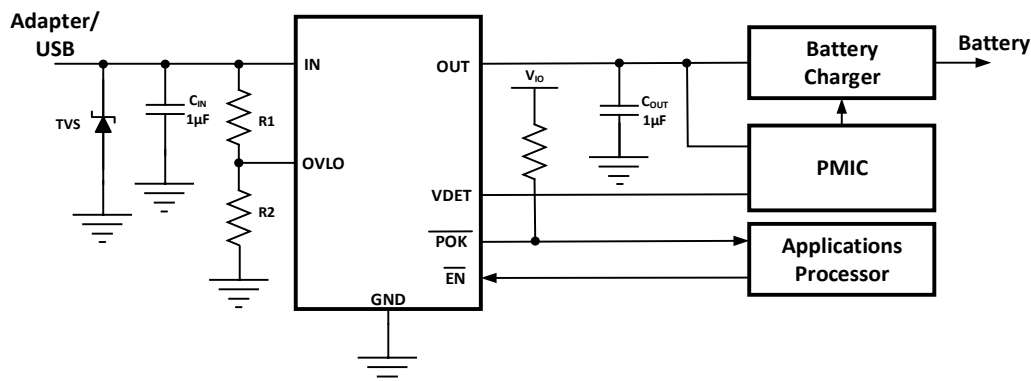
An input voltage exceeding the overvoltage threshold will cause the internal MOSFET to turn off, preventing excessive voltage from damaging downstream devices.

The KTS1663 offers three different fixed OVP options, plus a fully adjustable option. When the OVLO input is connected to GND, the KTS1663 automatically chooses the internal fixed OVLO threshold, preset to 5.95V (typical). Allowing OVLO to float, gives a preset of 10.2V (typical) and connecting a resistor to GND between 30k $\Omega$  and 80k $\Omega$  gives a preset of 13.5V (typical) The overvoltage protection threshold can also be fully adjusted with an optional external resistor divider to a voltage between 4V and 28V.

The KTS1663 features an open-drain output POK indicating a stable supply between the minimum supply voltage and OVLO threshold. In addition, a VDET output is provided to indicate the presence of a voltage at VBUS and is independent of the OVP switch. In case the device temperature exceeds the maximum junction temperature, the device switches off.

The KTS1663 is available in a RoHS and Green compliant 12-Bump 1.28 x 1.94 x 0.62mm WLCSP.

### Typical Application



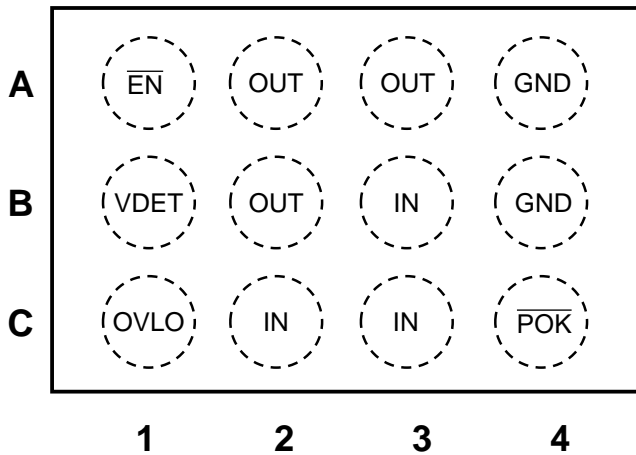


## Pin Descriptions

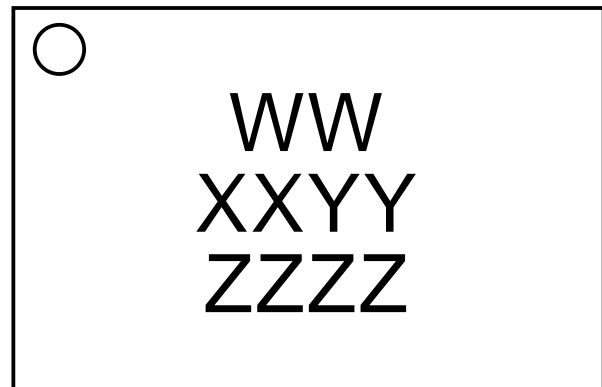
Pin #	Name	Function
A1	$\overline{\text{EN}}$	OUT power path is Enabled when $\overline{\text{EN}}$ is logic Low.
A2, A3, B2	OUT	Power switch output pin
B1	VDET	Output from IN pin, with internal protection clamp. VDET can source 1mA
C4	$\overline{\text{POK}}$	Open-drain power good output. $\overline{\text{POK}}$ is driven low during normal operation and becomes high impedance when an out-of-range condition is detected. Connect a pull-up resistor between the logic pin and the system rail.
A4, B4	GND	Ground. For correct operation, connect all GND pins to GND
C1	OVLO	External OVLO adjustment. See Table 1
B3, C2, C3	IN	Power switch input pin. Bypass IN with 0.1 $\mu$ F capacitor as close as possible to the device.

### WLCSP-12

TOP VIEW



TOP VIEW



12-Bump 1.28mm x 1.94mm x 0.62mm

WLCSP Package

#### Top Mark

WW = Device ID Code,  
 XX = Date Code, YY = Assembly Code,  
 ZZZZ = Serial Number

Table 1. OVP Selection

OVLO Pin	OVP Voltage
GND	5.95V
FLOAT	10.2V
30k $\Omega$ to 80k $\Omega$ to GND	13.5V
Resistive divider from VIN to GND	Adjustable



## Absolute Maximum Ratings<sup>1</sup>

(T<sub>A</sub> = 25°C unless otherwise noted)

Symbol	Description	Value	Units
IN	Input voltage	-0.3 to 42	V
OUT	Output voltage	-0.3 to VIN+0.3	V
OVLO	OVLO Pin	-0.3 to 12	V
P <sub>OK</sub> , V <sub>DET</sub> , $\overline{\text{EN}}$	P <sub>OK</sub> , $\overline{\text{EN}}$ , V <sub>DET</sub> Pins	-0.3 to 7	V
IN, OUT Current	Continuous Current	4.5	A
T <sub>J</sub>	Operating Temperature Range	-40 to 150	°C
T <sub>s</sub>	Storage Temperature Range	-65 to 150	°C
T <sub>LEAD</sub>	Maximum Soldering Temperature (at leads, 10 sec)	260	°C

## Thermal Capabilities

Symbol	Description	Value	Units
$\theta_{JA}$	Thermal Resistance – Junction to Ambient <sup>2</sup>	73	°C/W
P <sub>D</sub>	Maximum Power Dissipation at T <sub>A</sub> ≤ 25°C	1090	mW
$\Delta P_D/\Delta T$	Derating Factor Above T <sub>A</sub> = 25°C	-13.7	mW/°C

## Ordering Information

Part Number	Marking	Operating Temperature	Package
KTS1663EUW-TR	KUXXYYZZZ <sup>3</sup>	-40°C to +85°C	WLCSP-12

## Recommended Operating Range<sup>4</sup>

Description	Value
Input voltage range	2.5V to 40V
Output capacitance range	Up to 100 $\mu$ F

- Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
- Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.
- XX = Date Code, YY = Assembly Code, ZZZZ = Serial Number.
- The device is not guaranteed to function outside of recommended operating condition.

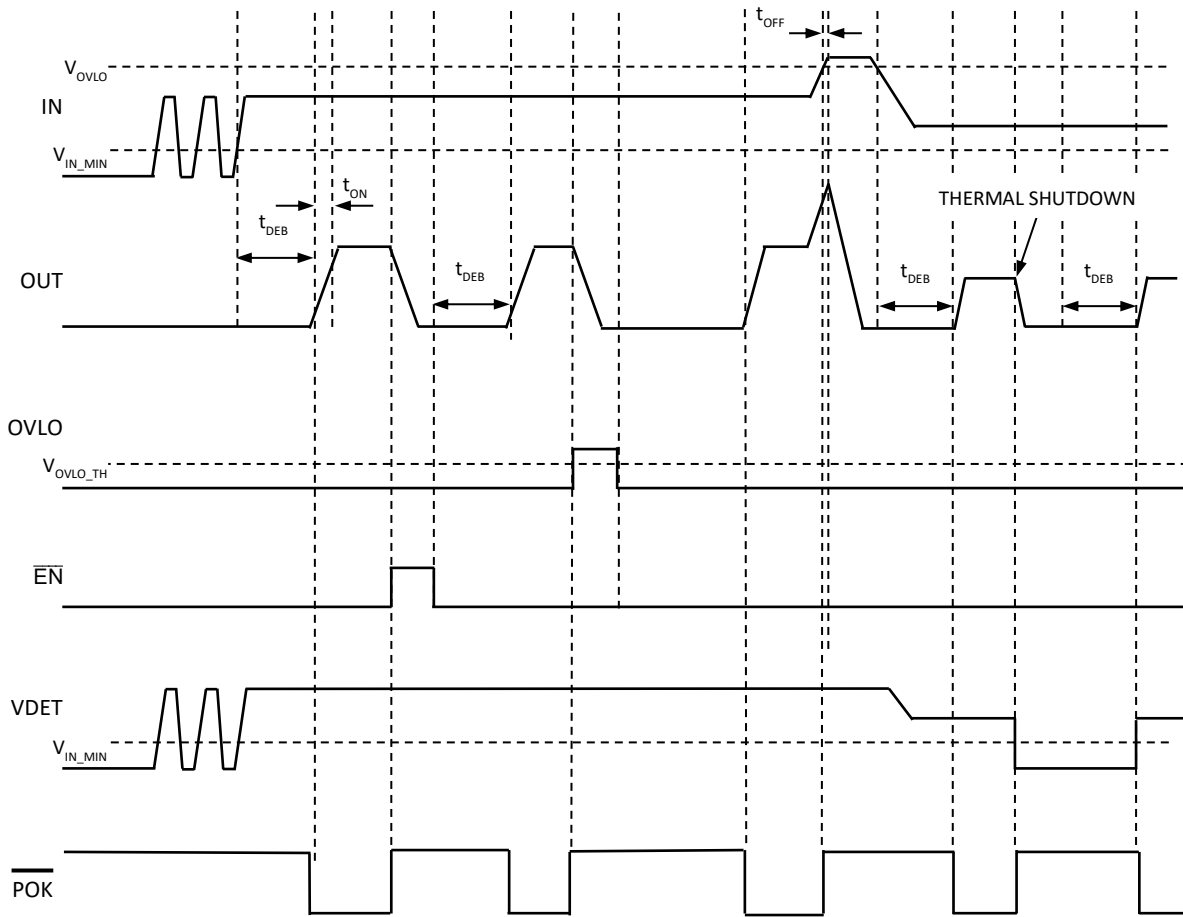


## Electrical Characteristics<sup>5</sup>

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of -40°C to +85°C, while *Typ* values are specified at room temperature (25°C).  $V_{IN} = 5.0V$ ,  $I_{IN} \leq 3A$

Symbol	Description	Conditions	Min	Typ	Max	Units
<b>INPUT Operation</b>						
$V_{IN}$	Input operating range		2.5		40	V
$I_{IN}$	Input supply current	$V_{IN} = 5V$ , $V_{IN} < V_{IN\_OVLO}$ , $\overline{EN} = GND$		85		$\mu A$
$V_{IN\_UVLO}$	Under voltage lockout threshold	$V_{IN}$ rising		2.3		V
$V_{UVLO\_HYST}$	Under voltage lockout hysteresis			0.1		V
<b>OVP</b>						
$V_{IN\_OVLO}$	Internal over voltage trip level 1	$V_{IN}$ rising, $OVLO = GND$		5.95		V
	Internal over voltage trip level 2	$V_{IN}$ rising, $OVLO = FLOAT$		10.2		V
	Internal over voltage trip level 3	$V_{IN}$ rising, $OVLO = 30k\Omega - 80k\Omega$ to GND		13.5		V
$V_{IN\_OVLO\_HYS}$	OVLO Hysteresis	$V_{IN}$ falling		0.10		V
$V_{OVLO\_TH}$	OVLO preset threshold range	$T_A = +25^\circ C$	1.16	1.20	1.24	V
	Adjustable OVLO threshold range		4		28	V
$V_{OVLO\_SEL}$	External OVLO select threshold		0.2		0.3	V
$R_{DS(ON)}$	Switch On-Resistance	$V_{IN} = 5V$ , $I_{IN} = 1.0A$ , $T_A = +25^\circ C$		26		m $\Omega$
$I_{OVLO}$	OVLO input leakage current	$V_{OVLO} = V_{OVLO\_TH}$	-120		120	nA
<b>EN, VDET</b>						
$V_{\overline{EN}\_H}$	$\overline{EN}$ logic high threshold		1.4			V
$V_{\overline{EN}\_L}$	$\overline{EN}$ logic low threshold				0.4	V
$R_{DET}$	VDET Switch On-resistance			25		$\Omega$
$V_{DET\_OUT}$	VDET clamp voltage	$V_{IN} = 20V$ , $V_{\overline{EN}} = 0V$ , $I_{VDET} = 1mA$	4.5	5.0	5.5	V
$V_{DET\_LIM}$	VDET current limit			30		mA
<b>TIMING – Figure 1</b>						
$t_{DEB}$	Debounce time	Time from $2.5V < V_{IN} < V_{IN\_OVLO}$ to $V_{OUT} = 10\%$ of $V_{IN}$		18		ms
$t_{ON}$	Switch turn-on time	$V_{IN} = 5V$ , $R_L = 100\Omega$ , $C_{LOAD} = 100\mu F$ $V_{OUT}$ from 10% $V_{IN}$ to 90% $V_{IN}$		2		ms
$t_{OFF}$	Switch turn-off time	$V_{IN} > V_{IN\_OVLO}$ to $V_{OUT}$ stop rising		100		ns
<b>POK</b>						
$V_{OL}$	POK output voltage low	$V_{IO} = 3.3V$ , $I_{SINK} = 1mA$			0.4	V
$V_{POK\_LEAK}$	POK leakage current	$V_{IO} = 3.3V$ , POK de-asserted	-1		1	$\mu A$
<b>ESD PROTECTION</b>						
$V_{ESD}$	ESD Protection	Human Body Model(HBM) Model = 2		$\pm 2.0$		kV
<b>Thermal Shutdown</b>						
$T_{SHDN}$	Shutdown Temperature			145		$^\circ C$
	Shutdown Temperature Hysteresis			20		$^\circ C$

5. KTS1663 is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.



\* NOTE: WAVEFORMS ARE NOT TO SCALE

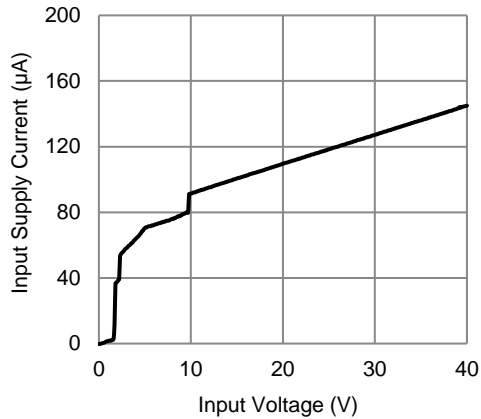
Figure 1. Timing Diagram



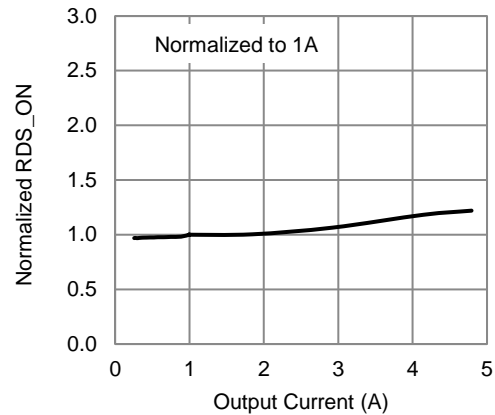
## Typical Characteristics

$V_{IN} = 5V$ ,  $C_{IN} = 0.1\mu F$ ,  $C_{OUT} = 1\mu F$ , OVLO pin = FLOAT,  $\overline{EN} = GND$ , Temp = 25°C unless otherwise specified.

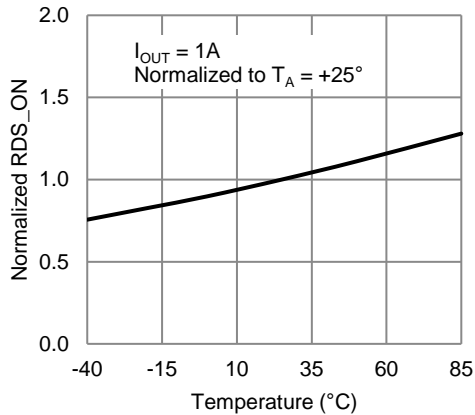
**Input Supply Current vs. Input Voltage**  
(OVLO pin Floating, no load)



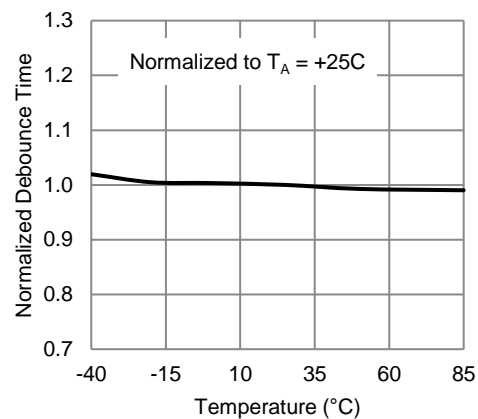
**Normalized RDS\_ON vs. Output Current**



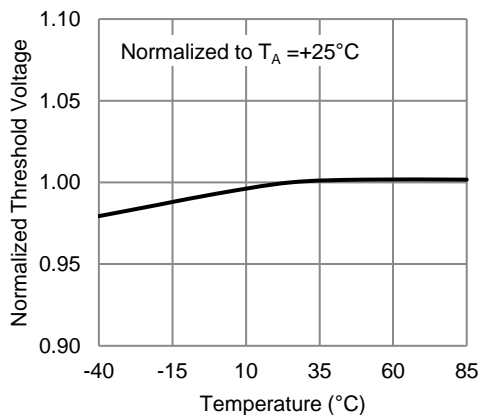
**Normalized RDS\_ON vs. Temperature**



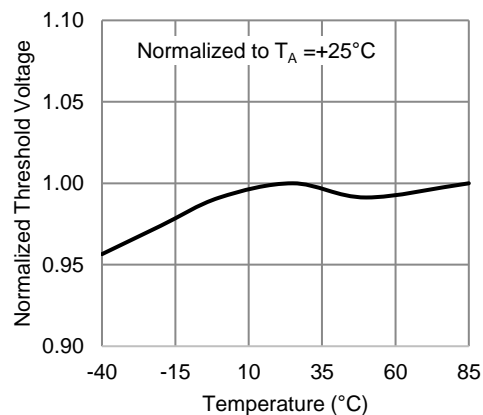
**Normalized Debounce Time vs. Temperature**



**Normalized Fixed OVLO vs. Temperature**  
(OVLO pin GND)



**Normalized Adjustable OVLO vs. Temperature**



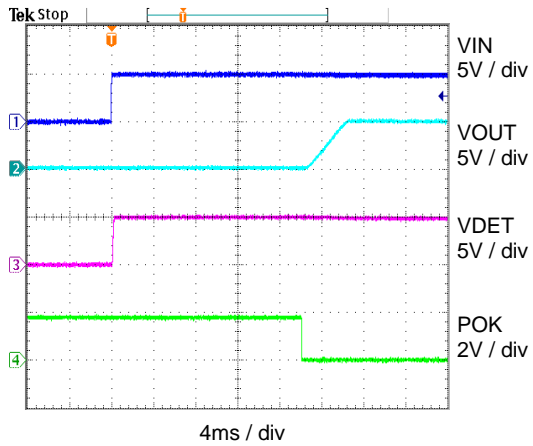




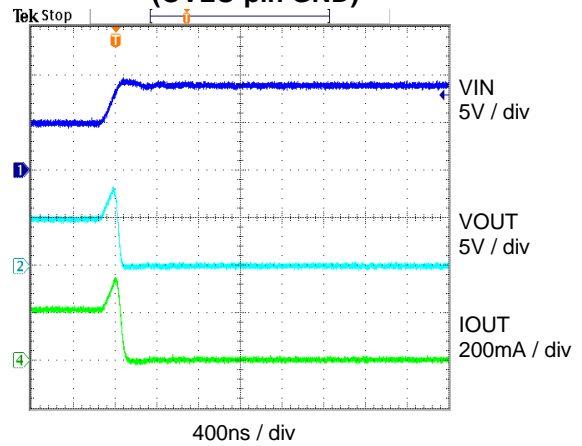
## Typical Characteristics

$V_{IN} = 5V$ ,  $C_{IN} = 0.1\mu F$ ,  $C_{OUT} = 1\mu F$ , OVLO pin = FLOAT,  $\overline{EN} = GND$ , Temp = 25°C unless otherwise specified.

**Power-up ( $C_{OUT} = 1\mu F$ , 100mA load)**

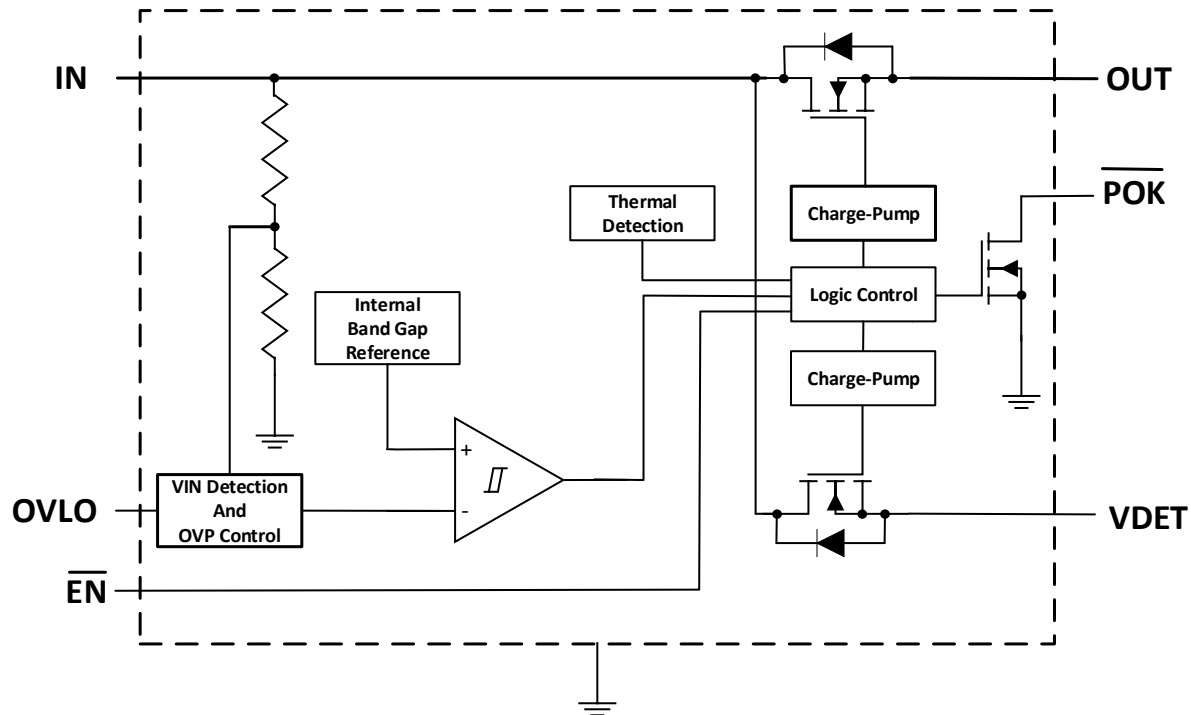


**OVP Transient ( $V_{IN}$  step from 5V to 9V)  
(OVLO pin GND)**





## Functional Block Diagram



## Functional Description

The KTS1663 is inserted between the power supply or charger source and the load to be protected. The KTS1663 consists of a slew-rate controlled, low resistance OVP switch, under-voltage lockout protection (UVLO), overvoltage monitor and protection (OVLO), power OK pin (POK), and a VBUS detect function (VDET).

The KTS1663 overvoltage protection device features a low on-resistance ( $R_{DS(on)}$ ) internal FET and protects low-voltage systems against voltage faults up to +40V. If the input voltage exceeds the overvoltage threshold, the internal FET is turned off to prevent damage to upstream components. The 18ms debounce time (18ms typ.) built into the device prevents false turn on of the internal FET during startup.

In normal operation, the OVP switch acts as a slew-rate controlled load switch, connecting and disconnecting the power supply from IN to OUT. A low resistance N-Channel MOSFET is used to minimize the voltage drop between the voltage source and the load and to reduce power dissipation.

When the voltage at the input exceeds the programmed overvoltage trip point, the device immediately turns off the internal switch disconnecting the load from the abnormal voltage, preventing damage to downstream components.

The power OK flag ( $\overline{POK}$ ) output pin can notify the system of the normal operation by pulling its output low. When an input power overvoltage or over-temperature event occurs, the device releases the internal open-drain and the  $\overline{POK}$  output is set to logic high by the external pull-up resistor in order to notify the system.

The VBUS detection function (VDET pin), provides a “clamped” output voltage whenever a voltage appears on VBUS (IN), and the power switch is enabled, even if the power switch is off due to an overvoltage condition.



In the event that the power dissipation causes the chip temperature to exceed its maximum temperature, the KTS1663 will switch off protecting the device. Once the chip temperature has cooled to below the hysteresis temperature, KTS1663 will re-initiate. Should the over-temperature condition persist, then KTS1663 will continue to thermally cycle on and off, until the input power is removed.

### USB ON-The-Go (OTG) Operation

When used in an OTG application the KTS1663 can provide power from OUT to IN. Initially, the OTG voltage applied at OUT will forward bias the power switch bulk diode and present a voltage drop of approximately 0.7V between OUT and IN. The maximum current in this mode is limited by the thermal performance of the device and at an ambient temperature of 25°C, the maximum current is:

$$I_{MAX} = 1.09W / 0.7V = 1.56A$$

This is purely a transitional condition as once the voltage at IN exceeds the UVLO voltage of 2.3V and the debounce time has elapsed, the main power switch will turn fully ON, significantly reducing the voltage drop from OUT to IN.

N.B. In OTG mode, the OTG voltage will also appear at VDET output.

### UVLO (Under Voltage Lockout)

The device has a built-in under voltage lockout (UVLO) circuit. When  $V_{IN}$  is rising, the output remains disconnected from the input until  $V_{IN}$  voltage is above 2.3V (typical). This circuit has a 100mV hysteresis to provide noise immunity to transient conditions.

### OVLO (Over Voltage Lockout)

The KTS1663 adjustable version has a 1.2V (typ) overvoltage trip threshold on the OVLO pin. With a resistor divider on OVLO pin from IN to GND, the overvoltage protection point of IN can be adjusted between 4V and 28V. For correct operation, OVLO should be > 0.25V within 8ms after power up.

Fixed OVP products are available with an internal resistor divider providing 5.95V(typ), 10.2V (typ), or 13.5V (typ) OVLO threshold trip voltage. To select the internal Fixed OVP, the OVLO pin should be connected to GND (5.95V), allowed to FLOAT (10.2V) or connected to GND via a 30kΩ to 80kΩ resistor (13.5V).

### Internal MOSFET Switch

The KTS1663 incorporates an internal MOSFET with a 26mΩ (typ)  $R_{DS(ON)}$ . The MOSFET gate is driven by an integrated charge pump which generates the necessary voltage above IN.

### $\overline{POK}$ Output

The  $\overline{POK}$  output is an active-low open-drain flag reporting good operation of the device. A pull-up resistor should be connected from the  $\overline{POK}$  pin to the system I/O rail. A fault is flagged when the output is being pulled high in the case of an overvoltage or over-temperature fault occurring.

### Protected Bus Voltage

The KTS1663 passes a protected IN voltage through to VDET. The VDET pin can provide up to 3mA of DC current. VDET contains an internal 5.0V clamp to protect devices connected to VDET, while still allowing the devices to operate from the VDET voltage. The voltage at VDET is not present while the KTS1663 is in thermal shutdown or IN is lower than the input operating range.

### Thermal Protection

The internal FET turns off when the junction temperature exceeds +145°C (typ). The device exits thermal shutdown after the junction temperature cools down by 20°C (typ).



## Application Information

### Input Capacitor

A 0.1 $\mu$ F or larger ceramic capacitor is recommended for CIN. The capacitor should be located close to the device IN pin. Ceramic capacitors are recommended for CIN. Select capacitors with a voltage rating at least 5V higher than the maximum possible voltage during surge. 50V rated capacitors are ideal for most applications.

### Output Capacitor

A small ceramic capacitor of approximately 1 $\mu$ F is recommended at the output. If desired, COUT may be increased to accommodate any load transient condition.

### External OVLO Adjustment

If OVLO is connected to ground, allowed to float or connected to ground via a resistor between the value of 30k $\Omega$  to 80k $\Omega$ , the internal OVLO comparator uses the internally set OVLO value.

The adjustable threshold uses a 1.20V (typical) overvoltage trip threshold on the OVLO pin. With a resistor divider on the OVLO pin from IN to GND, the overvoltage protection point of IN can be adjusted between 4V and 28V. Once the OVLO pin voltage exceeds the OVLO select voltage,  $V_{OVLO\_SELECT}$  (0.25V typical), the comparator reads the OVLO pin voltage (a fraction of IN) set by the external resistor divider (R1, R2).

R1 = 1M $\Omega$  is a good starting value for minimum current consumption. Since  $V_{IN\_OVLO}$ ,  $V_{OVLO\_THRESH}$ , and R1 are known, R2 can be calculated from the following formula:

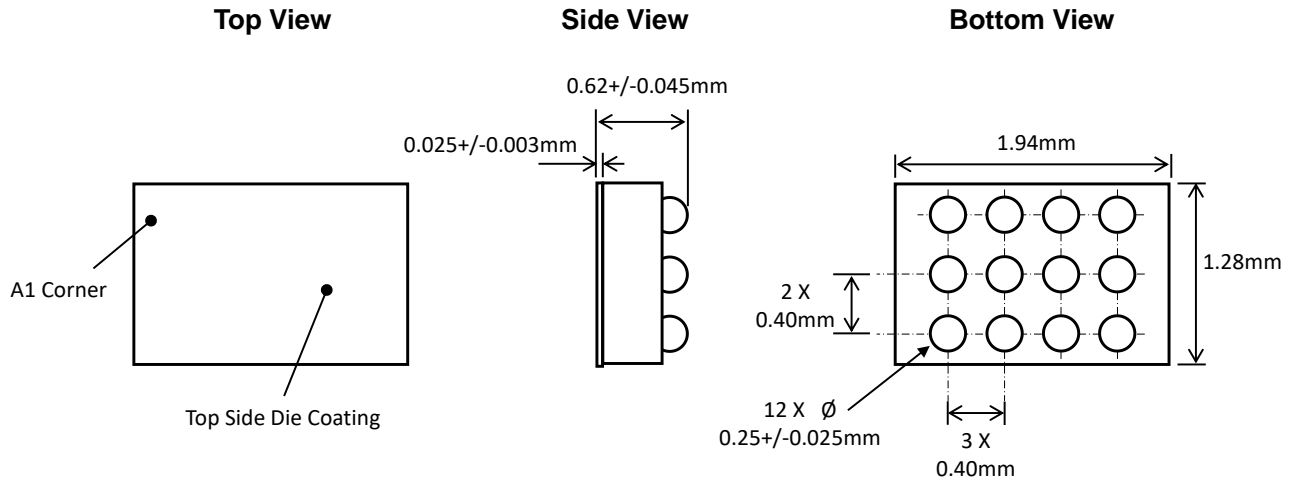
$$V_{IN\_OVLO} = V_{OVLO\_TH} \times (1 + R1/R2) = 1.20V \times (1 + R1/R2)$$

This external resistor-divider is completely independent from the internal resistor-divider.

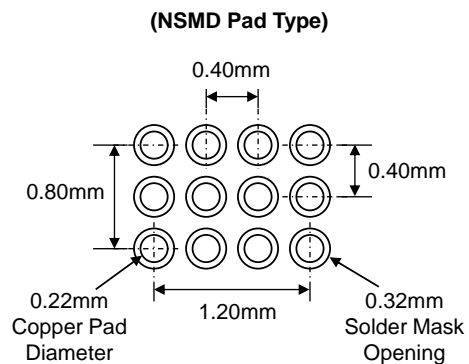


## Packaging Information

### WLCSP34-12, 1.94mm x 1.28mm x 0.62mm Package



### Recommended Footprint



\* Dimensions are in millimeters.

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