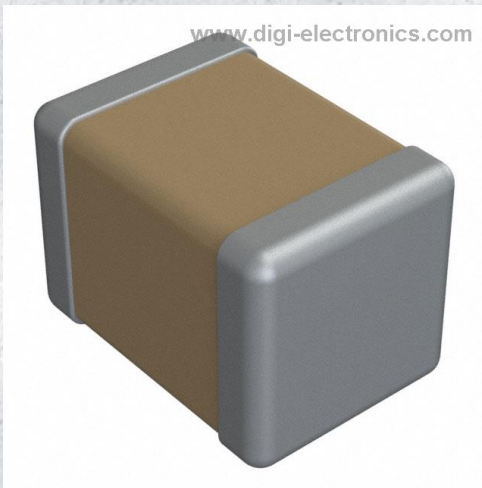


1812J0630120FCT Datasheet



<https://www.DiGi-Electronics.com>

DiGi Electronics Part Number	1812J0630120FCT-DG
Manufacturer	Knowles Syfer
Manufacturer Product Number	1812J0630120FCT
Description	CAP CER 12PF 63V COG/NPO 1812
Detailed Description	12 pF ±1% 63V Ceramic Capacitor COG, NPO (1B) 1812 (4532 Metric)

This model 1812J0630120FCT is available at DiGi Electronics.

DiGi Electronics offers a global database of semiconductor and electronic component datasheets.

We welcome your inquiries regarding pricing, lead time, or other product-related questions.

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DiGi is a global authorized distributor of electronic components.

Purchase and inquiry

Manufacturer Product Number:

1812J0630120FCT

Series:

-

Capacitance:

12 pF

Voltage - Rated:

63V

Operating Temperature:

-55°C ~ 125°C

Ratings:

-

Failure Rate:

-

Package / Case:

1812 (4532 Metric)

Height - Seated (Max):

-

Lead Spacing:

-

Base Product Number:

1812J

Manufacturer:

Knowles Syfer

Product Status:

Active

Tolerance:

±1%

Temperature Coefficient:

COG, NP0 (1B)

Features:

-

Applications:

General Purpose

Mounting Type:

Surface Mount, MLCC

Size / Dimension:

0.177" L x 0.126" W (4.50mm x 3.20mm)

Thickness (Max):

0.098" (2.50mm)

Lead Style:

-

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8532.24.0020

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

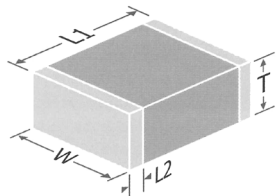


Surface Mount MLC Capacitors



Standard MLCC Ranges

A range of dc rated multi-layer chip capacitors from 0.2pF to 22µF and in case sizes 0402 to 8060 in COG/NPO and X7R dielectrics. Suitable for all general purpose and high reliability applications where package size and reliability are important. All are manufactured using Syfer's unique wet process and can optionally incorporate precious metal electrodes.



Electrical Details		
Capacitance Range		0.2pF to 22µF
Temperature Coefficient of Capacitance (TCC)	COG/NPO	0 ± 30ppm/°C
	X7R	±15% from -55°C to +125°C
Dissipation Factor	COG/NPO	Cr > 50pF ≤ 0.0015 Cr ≤ 50pF = 0.0015(15+Cr+0.7)
	X7R	≤ 0.025
Insulation Resistance (IR)		100GΩ or 1000secs (whichever is the less)
Dielectric Withstand Voltage (DWV)		Voltage applied for 5 ± 1 seconds, 50mA charging current maximum
Ageing Rate	COG/NPO	Zero
	X7R	<2% per time decade

Range Dimensions – Standard MLCC Ranges

Size	Length (L1) mm/inches	Width (W) mm/inches	Max. Thickness (T) mm/inches	Termination Band (L2) mm/inches	
				min	max
0402	1.0 ± 0.10	0.50 ± 0.10	0.6	0.10	0.40
	0.04 ± 0.004	0.02 ± 0.004	0.024	0.004	0.016
0603	1.6 ± 0.15	0.8 ± 0.15	0.9	0.20	0.40
	0.063 ± 0.006	0.032 ± 0.006	0.035	0.008	0.016
0805	2.0 ± 0.2	1.25 ± 0.2	1.3	0.25	0.75
	0.079 ± 0.008	0.049 ± 0.008	0.051	0.010	0.03
1206	3.2 ± 0.2	1.6 ± 0.2	1.7	0.25	0.75
	0.126 ± 0.008	0.063 ± 0.008	0.068	0.01	0.03
1210	3.2 ± 0.2	2.5 ± 0.2	2.0	0.25	0.75
	0.126 ± 0.008	0.098 ± 0.008	0.08	0.01	0.03
1808	4.5 ± 0.35	2.0 ± 0.3	2.0	0.25	1.0
	0.180 ± 0.014	0.08 ± 0.012	0.08	0.01	0.04
1812	4.5 ± 0.30	3.2 ± 0.2	3.2	0.25	1.14
	0.180 ± 0.012	0.126 ± 0.008	0.126	0.01	0.045
1825	4.5 ± 0.30	6.40 ± 0.4	4.0	0.25	1.0
	0.180 ± 0.012	0.252 ± 0.016	0.158	0.01	0.04
2220	5.7 ± 0.40	5.0 ± 0.4	4.0	0.25	1.0
	0.225 ± 0.016	0.197 ± 0.016	0.158	0.01	0.04
2225	5.7 ± 0.4	6.3 ± 0.4	4.0	0.25	1.14
	0.225 ± 0.016	0.25 ± 0.016	0.158	0.01	0.045
3640	9.2 ± 0.5	10.16 ± 0.5	4.0	0.5	1.5
	0.36 ± 0.02	0.4 ± 0.02	0.158	0.02	0.06
5550	14.0 ± 0.711	12.7 ± 0.635	4.0	0.5	1.5
	0.55 ± 0.028	0.5 ± 0.025	0.158	0.02	0.06
8060	20.3 ± 0.5	15.24 ± 0.5	4.0	0.5	1.5
	0.8 ± 0.02	0.6 ± 0.02	0.158	0.02	0.06

Custom chip sizes not included in the table, but larger than 2225, can be considered with minimum tooling charges. Please refer specific requests direct to the sales office. Max thickness relates to standard components and actual thickness may be considerably less. Thicker parts, or components with reduced maximum thickness, can be considered by request - please refer requests to the sales office.

Ordering Information – Standard MLCC Range

1210	Y	100	0103	J	X	T	□□□
Chip Size	Termination	Voltage d.c. (marking code)	Capacitance in Pico farads (pF)	Capacitance Tolerance	Dielectric Codes	Packaging	Suffix Code
0402	Y = FlexiCap™ termination base with nickel barrier (100% matte tin plating). RoHS compliant.	010 = 10V	<1.0pF	H: ± 0.05pF	C = COG/NPO (1B) X = X7R (2R1) P = X5R	T = 178mm (7") reel	Used for specific customer requirements
0603		016 = 16V	Insert a P for the decimal point as the first character.	(only available for values <4.7pF)		R = 330mm (13") reel	
0805	H = FlexiCap™ termination base with nickel barrier (tin/lead plating with min. 10% lead). Not RoHS compliant.	025 = 25V	e.g., P300 = 0.3pF	<10pF	B: ± 0.10pF C: ± 0.25pF D: ± 0.5pF F: ± 1.0pF	B = Bulk pack - tubs or trays	
1206		050 = 50V	Values in 0.1pF steps				
1210	F = Silver Palladium. RoHS compliant	063 = 63V	≥1.0pF & <10pF		G: ± 2% J: ± 5% K: ± 10% M: ± 20%		
1808		100 = 100V	Insert a P for the decimal point as the second character.				
1812	J = Silver base with nickel barrier (100% matte tin plating). RoHS compliant	200 = 200V	e.g., 8P20 = 8.2pF	≥10pF			
1825		250 = 250V	Values are E24 series				
2220	A = Silver base with nickel barrier (tin/lead plating with min. 10% lead). Not RoHS compliant	500 = 500V		First digit is 0.			
2225		630 = 630V	≥10pF	Second and third digits are significant figures of capacitance code.			
3640	6 = Nickel Barrier, Sn/Pb Plated Solder (5-20% Lead, non RoHS)	1K0 = 1kV	First digit is 0.	The fourth digit is the number of zeros following.			
5550		1K2 = 1.2kV		e.g., 0101 = 100 pF			
8060	7 = FlexiCap™ Polymer termination, Nickel barrier, Sn/Pb Plated Solder (5-20% Lead, non RoHS)	1K5 = 1.5kV	Values are E12 series				
		2K0 = 2kV					

Minimum/Maximum Capacitance Values

Note: Knowles Precision Devices operate a continuous improvement process with ranges being expanded and updated regularly. The latest range may differ. Please contact the local sales office or refer to the KPD website – www.knowlescapacitors.com

These values are guidelines only. Please contact your local sales office to discuss your specific requirements.

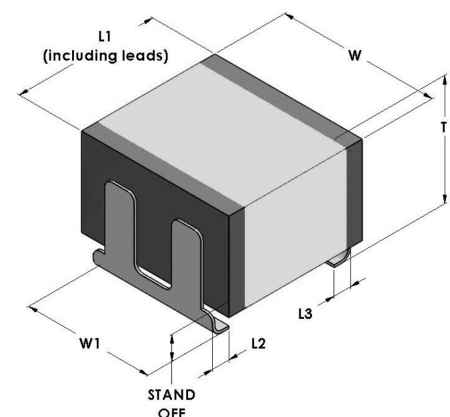
Chip Size	0402	0603	0805	1206	1210	1808	1812	1825	2211	2215	2220*	2225*	3640	5550	8060
Min. value	0.2pF	0.5pF	1.0pF	1.0pF	3.9pF	4.7pF	5.6pF	10pF	100pF	150pF	10pF	10pF	10pF	27pF	47pF
16V	-	100nF	330nF	1.0μF	1.5μF	1.5μF	3.3μF	4.7μF	-	-	5.6μF	6.8μF	-	-	-
25V	10nF	100nF	220nF	820nF	1.2μF	1.2μF	2.2μF	3.9μF			4.7μF	5.6μF	-	-	-
50V	5.6nF	100nF	220nF	470nF	1.0μF	680nF	2.2μF	2.2μF	-	-	3.3μF	3.3μF	10μF	15μF	22μF
63V	5.6nF	100nF	220nF	470nF	1.0μF	680nF	2.2μF	2.2μF	-	-	3.3μF	3.3μF	10μF	15μF	22μF
100V	3.3nF	47nF	100nF	330nF	680nF	560nF	1.5μF	1.5μF	-	-	2.2μF	2.7μF	5.6μF	10μF	15μF
200V	1.0nF	15nF	56nF	150nF	330nF	330nF	1.0μF	1.2μF	560nF	820nF	2.2μF	2.2μF	5.6μF	5.6μF	10μF
250V	1.0nF	15nF	56nF	150nF	330nF	270nF	1.0μF	1.2μF	560nF	820nF	2.2μF	2.2μF	5.6μF	5.6μF	10μF
500Vdc	-	4.7nF	22nF	68nF	150nF	150nF	470nF	560nF	330nF	470nF	1.2μF	1.2μF	2.7μF	1.8μF	3.3μF
630Vdc	-	-	10nF	47nF	100nF	100nF	330nF	470nF	220nF	330nF	1.0μF	1.0μF	2.2μF	1.2μF	2.2μF
1000Vdc	-	-	10nF	27nF	47nF	47nF	180nF	180nF	82nF	120nF	470nF	220nF	1.0μF	390nF	1.0μF
1200Vdc	-	-	-	15nF	22nF	22nF	39nF	68nF	56nF	68nF	82nF	100nF	180nF	220nF	470nF
1500Vdc	-	-	-	10nF	18nF	18nF	33nF	68nF	39nF	56nF	82nF	100nF	100nF	150nF	330nF
2000Vdc	-	-	-	3.3nF	5.6nF	8.2nF	18nF	22nF	18nF	22nF	33nF	47nF	56nF	82nF	150nF
2500Vdc	-	-	-	2.7nF	4.7nF	4.7nF	10nF	18nF	10nF	15nF	22nF	33nF	39nF	68nF	100nF
3000Vdc	-	-	-	1.5nF	3.3nF	3.9nF	4.7nF	10nF	5.6nF	10nF	15nF	18nF	33nF	47nF	82nF
4000Vdc	-	-	-	-	-	2.2nF	3.3nF	2.2nF	3.3nF	4.7nF	6.8nF	10nF	10nF	15nF	33nF
5000Vdc	-	-	-	-	-	680pF	1.2nF	1.8nF	1.2nF	2.2nF	4.7nF	4.7nF	6.8nF	10nF	22nF
6000Vdc	-	-	-	-	-	390pF	1.0nF	1.5nF	560pF	820pF	2.2nF	2.7nF	4.7nF	8.2nF	15nF
8000Vdc	-	-	-	-	-	-	-	-	-	-	-	-	1.5nF	4.7nF	6.8nF
10000Vdc	-	-	-	-	-	-	-	-	-	-	-	-	1.0nF	2.2nF	4.7nF
12000Vdc	-	-	-	-	-	-	-	-	-	-	-	-	820pF	1.2nF	2.2nF

*Leaded options are available on all parts in case sizes 2220 and 2225. Please see below for more information.

Leaded Options

Option on case sizes 2220 & 2225 for all ranges.

- Enhanced performance under critical testing conditions such as thermal shock and mechanical vibration
- Capable of 3000 thermal cycles with no degradation of interconnect when mounted to FR4 board
- Suitable for both industrial and automotive markets
- Offers 3kV and 4kV parts to satisfy the demands of 800V battery system DWV testing
- High voltage ratings allow for component de-rating in application



Range Dimensions – Leaded Options

Size	Length (L1) mm/inches	Width (W) mm/inches	Width (W1) mm/inches	Max. Thickness (T) mm/inches	Lead Width (L2 & L3) mm/inches Typical	STAND OFF mm/inches
2220	5.7 ± 0.40 0.225 ± 0.016	5.0 ± 0.4 0.197 ± 0.016			0.7 0.028	1.0 0.039
2225	5.7 ± 0.4 0.225 ± 0.016	6.3 ± 0.4 0.252 ± 0.016	5.10 ± 0.20 0.200 ± 0.008	5.5 0.217	0.7 0.028	1.0 0.039

Soldering Information

Syfer MLCCs are compatible with all recognised soldering/mounting methods for chip capacitors. A detailed application note is available at syfer.com

Reflow Soldering

Syfer recommend reflow soldering as the preferred method for mounting MLCCs. Syfer MLCCs can be reflow soldered using a reflow profile generally defined in IPC/FEDEC J-STD-020. Sn plated termination chip capacitors are compatible with both conventional and lead free soldering with peak temperatures of 260 to 270°C acceptable.

The heating ramp rate should be such that components see a temperature rise of 1.5 to 4°C per second to maintain temperature uniformity through the MLCC.

The time for which the solder is molten should be maintained at a minimum, so as to prevent solder leaching. Extended times above 230°C can cause problems with oxidation of Sn plating. Use of an inert atmosphere can help if this problem is encountered. Palladium/Silver (Pd/Ag) terminations can be particularly susceptible to leaching with free lead, tin rich solders and trials are recommended for this combination.

Cooling to ambient temperature should be allowed to occur naturally, particularly if larger chip sizes are being soldered. Natural cooling allows a gradual relaxation of thermal mismatch stresses in the solder joints. Forced cooling should be avoided as this can induce thermal breakage.

Wave Soldering

Wave soldering is generally acceptable, but the thermal stresses caused by the wave have been shown to lead to potential problems with larger or thicker chips. Particular care should be taken when soldering SM chips larger than size 1210 and with a thickness greater than 1.0mm for this reason.

Maximum permissible wave temperature is 270°C for SM chips.

The total immersion time in solder should be kept to a minimum. It is strongly recommended that Sn/Ni plated terminations are specified for wave soldering applications.

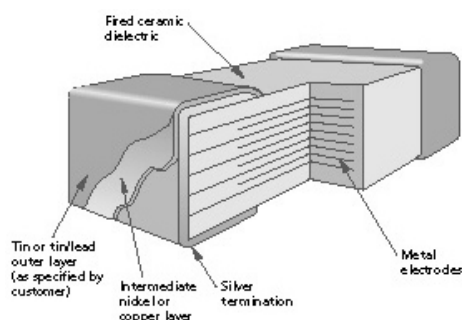
Solder Leaching

Leaching is the term for the dissolution of silver into the solder causing a failure of the termination system which causes increased ESR, $\tan \delta$ and open circuit faults, including ultimately the possibility of the chip becoming detached.

Leaching occurs more readily with higher temperature solders and solders with a high tin content. Pb free solders can be very prone to leaching certain termination systems. To prevent leaching, exercise care when choosing solder allows and minimize both maximum temperature and dwell time with the molten solder.

Plated terminations with nickel or copper anti-leaching barrier layers are available in a range of top coat finishes to prevent leaching occurring. These finishes also include Syfer FlexiCap™ for improved stress resistance post soldering.

Multilayer ceramic chip with nickel or copper barrier termination



Rework of Chip Capacitors

Syfer recommend hot air/gas as the preferred method of applying heat for rework. Apply even heat surrounding the component to minimise internal thermal gradients. Soldering irons or other techniques that apply direct heat to the chip or surrounding area should not be used as these can result in micro cracks being generated.

Minimise the rework heat duration and allow components to cool naturally after soldering.

Use of Silver Loaded Epoxy Adhesives

Chip capacitors can be mounted to circuit boards using silver loaded adhesive provided the termination material of the capacitor is selected to be compatible with the adhesive. This is normally PdAg. Standard tin finishes are often not recommended for use with silver loaded epoxies as there can be electrical and mechanical issues with the joint integrity due to material mismatch.

Handling & Storage

Components should never be handled with fingers; perspiration and skin oils can inhibit solderability and will aggravate cleaning.

Chip capacitors should never be handled with metallic instruments. Metal tweezers should never be used as these can chip the product and leave abraded metal tracks on the product surface. Plastic or plastic coated metal types are readily available and recommended – these should be used with an absolute minimum of applied pressure.

Incorrect storage can lead to problems for the user. Rapid tarnishing of the terminations, with an associated degradation of solderability, will occur if the product comes into contact with industrial gases such as sulphur dioxide and chlorine. Storage in free air, particularly moist or polluted air, can result in termination oxidation.

Packaging should not be opened until the MLCs are required for use. If opened, the pack should be re-sealed as soon as practicable. Alternatively, the contents could be kept in a sealed container with an environmental control agent.

Long term storage conditions, ideally, should be temperature controlled between -5 and +40°C and humidity controlled between 40% and 60% R.H.

Taped product should be stored out of direct sunlight, which might promote deterioration in tape or adhesive performance.

Product, stored under the conditions recommended above, in its "as received" packaging, has a minimum shelf life of 2 years.

SM Pad Design

Syfer conventional 2-terminal chip capacitors can generally be mounted using pad designs in accordance with IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standards, but there are some other factors that have been shown to reduce mechanical stress, such as reducing the pad width to less than the chip width. In addition, the position of the chip on the board should also be considered.

3-terminal components are not specifically covered by IPC-7351, but recommended pad dimensions are included in the Syfer catalogue/website for these components.

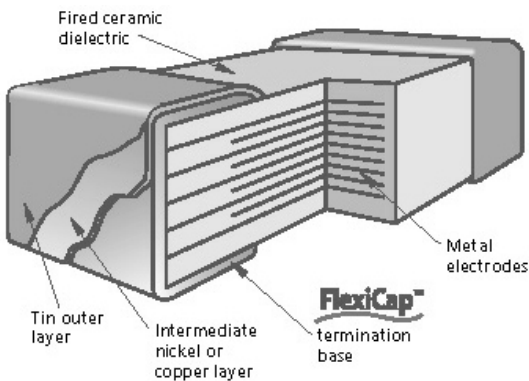
FlexiCap™ Termination

FlexiCap™ has been developed as a result of listening to customer’s experiences of stress damage to MLCCs from many manufacturers, often caused by variations in production processes.

Our answer is a proprietary flexible epoxy polymer termination material that is applied to the device under the usual nickel barrier finish. FlexiCap™ will accommodate a greater degree of board bending than conventional capacitors.

Ranges are available with FlexiCap™ termination material offering increased reliability and superior mechanical performance (board flex and temperature cycling) when compared with standard termination materials. Refer to Syfer application note reference AN0001. FlexiCap™ capacitors enable the board to be bent almost twice as much as before mechanical cracking occurs. Refer to application note AN0002.

FlexiCap™ is also suitable for space applications having passed thermal vacuum outgassing tests. Refer to Syfer application note reference AN0026.



FlexiCap™ MLCC cross section

Syfer has delivered millions of FlexiCap™ components and during that time has collected substantial test and reliability data, working in partnership with customers world wide, to eliminate mechanical cracking.

An additional benefit of FlexiCap™ is that MLCCs can withstand temperature cycling from -55 to 125°C in excess of 1,000 times without cracking.

FlexiCap™ termination has no adverse effect on any electrical parameters, nor affects the operation of the MLCC in any way.

Application Notes

FlexiCap™ may be handled, stored and transported in the same manner as standard terminated capacitors. The requirements for mounting and soldering FlexiCap™ are the same as for standard SMD capacitors.

For customers currently using standard terminated capacitors there should be requirement to change the assembly process when converting to FlexiCap™.

Based upon the board bend tests in accordance with IEC 60384-1 the amount of board bending required to mechanically crack a FlexiCap™ terminated capacitor is significantly increased compared with standard terminated capacitors.

Product: X7R	Typical bend performance under AEC-Q200 test conditions
Standard Termination	2mm to 3mm
FlexiCap™	Typically 8mm to 10mm

REACH (Registration, Evaluation, Authorisation and restriction of Chemicals) Statement

The main purpose of REACH is to improve the protection of human health and the environment from the risks arising from the use of chemicals.

Syfer Technology Ltd maintains both ISO 14001, Environmental Management System and OHSAS 18001 Health & Safety Management System approvals that require and ensure compliance with corresponding legislation such as REACH.

For further information, please contact the sales office at SyferSales@knowles.com

RoHS Compliance

Syfer routinely monitors world wide material restrictions (e.g., EU/China and Korea RoHS mandates) and is actively involved in shaping future legislation.

All standard C0G/NP0, X7R, X5R and High Q Syfer MLCC products are compliant with the EU RoHS directive (see below for special exemptions) and those with plated terminations are suitable for soldering common lead free solder alloys (refer to 'Soldering Information' for more details on soldering limitations). Compliance with EU RoHS directive automatically signifies compliance with some other legislation (e.g., Korea RoHS). Please refer to the Sales Office for details of compliance with other materials legislation.

Breakdown of material content, SGS analysis reports and tin whisker test results are available on request.

Most Syfer MLCC components are available with non-RoHS compliant tin/lead (SnPb) Solderable termination finish for exempt applications and where pure tin is not acceptable. Other tin free termination finishes may also be available – please refer to the Sales Office for further details.

X8R ranges <250Vdc are not RoHS 2011/65/EU compliant.

115Vac 400Hz ranges are not RoHS 2011/65/EU compliant.

Check the website, www.knowlescapacitors.com/syfer for latest RoHS update.

Export Controls and Dual-use Regulations

Certain Syfer catalogue components are defined as 'dual-use' items under international export controls – those that can be used for civil and military purposes which meet certain specified technical standards.

The defining criteria for a dual-use component with respect to Syfer products is one with a voltage rating of >750V and a capacitance value >250nF and a series inductance <10nH.

Components defined as 'dual-use' under the above criteria automatically require a licence for export outside the EU, and may require a licence for export with the EU.

The application for a licence is routine, but customers for these products will be asked to supply further information.

Please refer to the sales office if you require any further information on export restrictions.

Other special components may additionally need to comply with export regulations.

Ageing of Ceramic Capacitors

Capacitor ageing is a term used to describe the negative, logarithmic capacitance change which takes place in ceramic capacitors with time. The crystalline structure for barium titanate based ceramics changes on passing through its Curie temperature (known as the Curie Point) at about 125°C. The domain structure relaxes with time and in doing so, the dielectric constant reduces logarithmically; this is known as the ageing mechanism of the dielectric constant. The more stable dielectrics have the lowest ageing rates.

The ageing process is reversible and repeatable. Whenever the capacitor is heated to a temperature above the Curie Point the ageing process starts again from zero.

The ageing constant, or ageing rate, is defined as the percentage loss of capacitance due to the ageing process of the dielectric which occurs during a decade of time (a tenfold increase in age) and is expressed as percent per logarithmic decade of hours. As the law of decrease of capacitance is logarithmic, this means that for a capacitor with an ageing rate of 1% per decade of time, the capacitance will decrease at a rate of:

- a) 1% between 1 and 10 hours
- b) An additional 1% between the following 10 and 100 hours
- c) An additional 1% between the following 100 and 1000 hours
- d) An additional 1% between the following 1000 and 10000 hours
- e) The ageing rate continues in this manner throughout the capacitor's life.

Typical values of the ageing constant for our MLCCs are

Dielectric Class	Typical Values
Ultra Stable COG/NP0	Negligible capacitance loss through ageing
Stable X7R	<2% per decade of time

Capacitance Measurements

Because of ageing it is necessary to specify an age for reference measurements at which the capacitance shall be within the prescribed tolerance. This is fixed at 1000 hours, since for all practical purposes there is not much further loss of capacitance after this time.

All capacitors shipped are within their specified tolerance at the standard reference age of 1000 hours after having cooled through their Curie temperature.

The ageing curve for any ceramic dielectric is a straight line when plotted on semi-log paper.

Capacitance vs. Time

(Ageing X7R @ 1% per decade)



Tight Tolerance

One of the advantages of Syfer's unique 'wet process' of manufacture is the ability to offer capacitors with exceptionally tight capacitance tolerances.

The accuracy of the printing screens used in the fully automated, computer controlled manufacturing process allows for tolerance as close as ± 1% on COG/NP0 parts greater than or equal to 10pF. For capacitance value less than 4.7pF tolerances can be as tight as ± 0.05pF.

Periodic Tests Conducted and Reliability Data

For standard surface mount capacitors components are randomly selected on a sample basis and the following routine tests conducted:

- Load Test. 1,000 hours @ 125°C (150°C for X8R). Applied voltage depends on components tested
- Humidity Test. 168 hours @ 85°C/85%RH
- Board Deflection (bend test)

Test results are available on request.

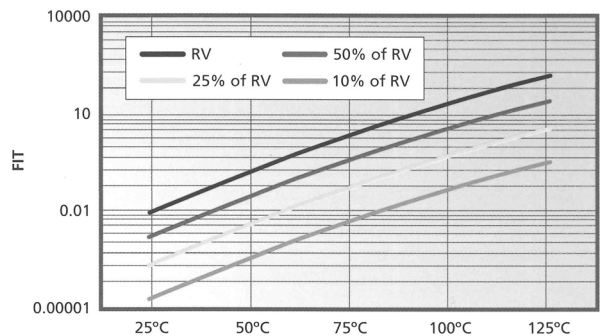
Conversion Factors

From	To	Operation
FITs	MTBF (hours)	$10^9 \div \text{FITs}$
FITs	MTBF (years)	$10^9 \div (\text{FITs} \times 8760)$

FIT = Failures In Time. 1 FIT = 1 failure in 10⁹ hours

MTBF = Mean Time Between Failure

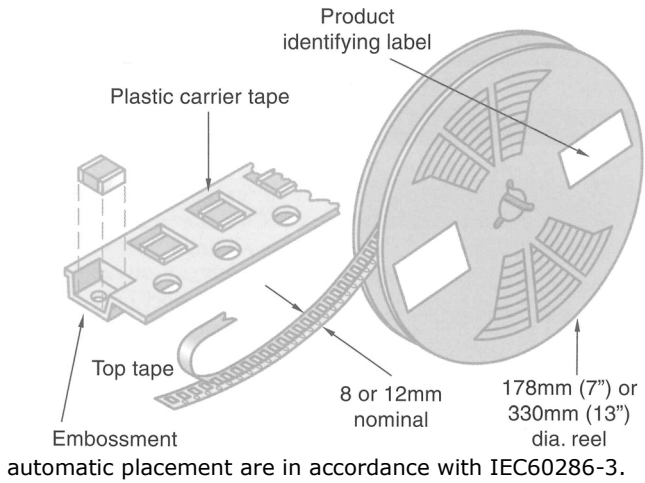
Example of FIT Data Available



- Component type: 0805 (COG/NP0 and X7R)
- Testing Location: Syfer reliability test department
- Results based on: 16,622,000 component test hours

Packaging Information

Tape and reel packing of surface mounting chip capacitors for

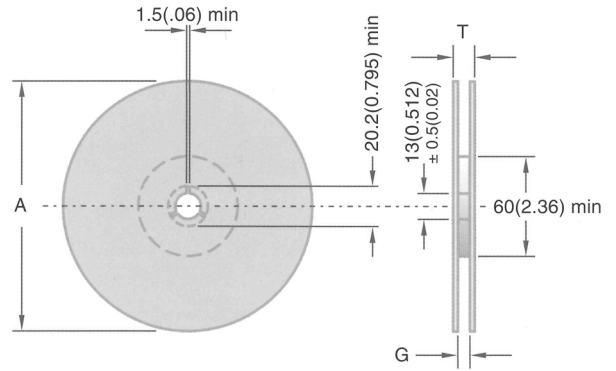


automatic placement are in accordance with IEC60286-3.

Peel Force

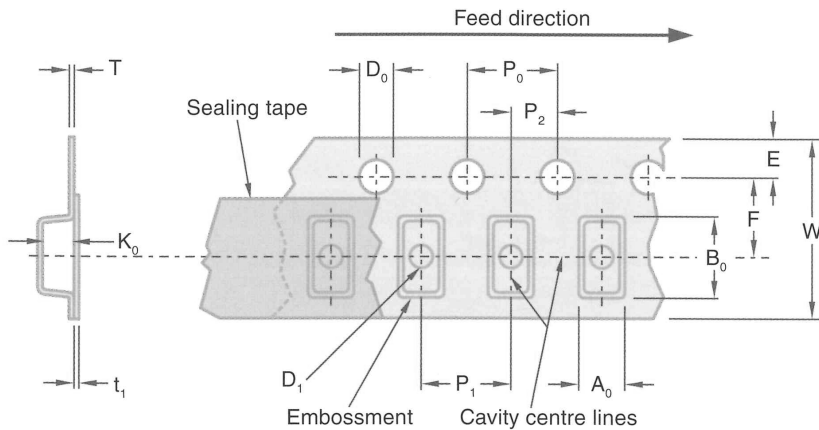
The peel force of the top sealing tape is between 0.2 and 1.0 Newton at 180°. The breaking force of the carrier and sealing tape in the direction of unreeling is greater than 10 Newton.

Reel Dimensions



Symbol	Description	178mm Reel	330mm Reel
A	Reel diameter	178 (7)	330 (13)
G	Reel inside width	8.4 (0.33)	12.4 (0.49)
T	Reel outside width	14.4 (0.56) max	18.4 (0.72) max

Tape Dimensions



		Dimensions mm (inches)	
Symbol	Description	8mm Tape	12mm Tape
A ₀	Width of cavity	Dependent on chip size to minimize rotation	
B ₀	Length of cavity		
K ₀	Depth of cavity		
W	Width of tape	8.0 (0.315)	12.0 (0.472)
F	Distance between drive hole centres and cavity centres	3.5 (0.138)	5.5 (0.213)
E	Distance between drive hole centres and tape edge	1.75 (0.069)	
P ₁	Distance between cavity centres	4.0 (0.156)	8.0 (0.315)
P ₂	Axial distance between drive hole centres and cavity centres	2.0 (0.079)	
P ₀	Axial distance between drive hole centres	4.0 (0.156)	
D ₀	Drive hole diameter	1.5 (0.059)	
D ₁	Diameter of cavity piercing	1.0 (0.039)	1.5 (0.059)
T	Carrier tape thickness	0.3 (0.012) ± 0.1 (0.04)	0.4 (0.016) ± 0.1 (0.04)
t ₁	Top tape thickness	0.1 (0.004) max	

Packing Information

Missing Components

The number of missing components in the tape may not exceed 0.25% of the total quantity with not more than three consecutive components missing. This must be followed by at least six properly placed components

Identification

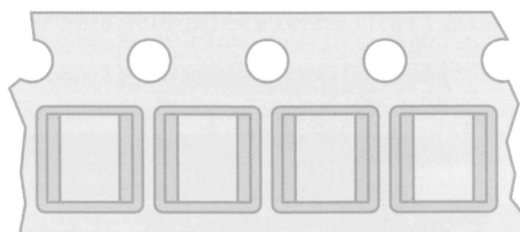
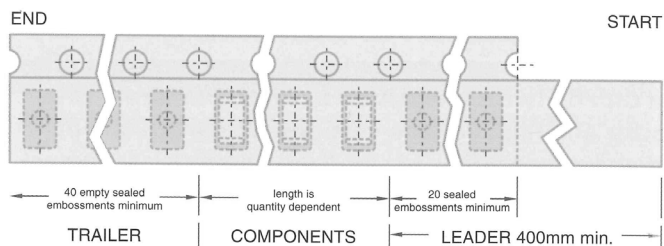
Each reel is labelled with the following information: manufacturer, chip size, capacitance, tolerance, rated voltage, dielectric type, batch number, date code and quantity of components.

Component Orientation

Tape and reeling is in accordance with IEC 60286 part 3, which defines the packaging specifications for leadless components on continuous tapes.

- Notes: 1) IEC60286-3 states A0 < B0
 2) Regarding the orientation of 1825 and 2225 components, the termination bands are right to left, NOT front to back. Please see diagram.

Leader Trailer

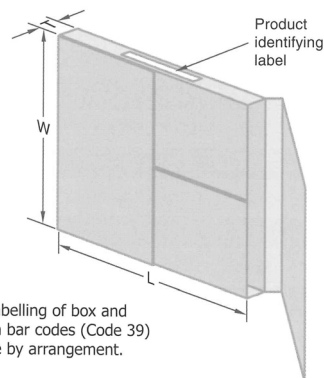


Orientation of 1825 & 2225 components

Outer Packaging

Outer carton dimensions mm (inches) max

Reel Size	No. of Reels	L	W	T
178 (7)	1	185 (7.28)	185 (7.28)	25 (0.98)
178 (7)	4	190 (7.48)	195 (7.76)	75 (2.95)
330 (13)	1	335 (13.19)	335 (13.19)	25 (0.98)



Note: Labelling of box and reel with bar codes (Code 39) available by arrangement.

Reel Quantities

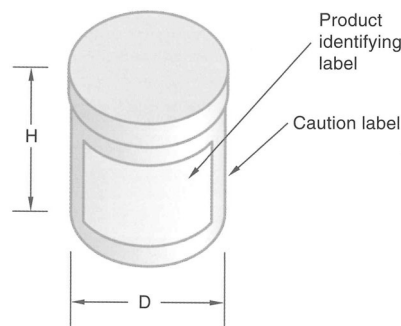
Chip Size	0402	0505	0603	0805	1111	1206	1210	1410	1808	1812	1825	2211	2215	2220	2225
Max. Chip Thickness	0.5mm	1.3mm	0.8mm	1.3mm	2.0mm	1.6mm	2.0mm	2.0mm	2.0mm	2.5mm	2.5mm	2.5mm	2.5mm	2.5mm	2.5mm
	0.02"	0.05"	0.03"	0.05"	0.08"	0.06"	0.08"	0.08"	0.08"	0.1"	0.1"	0.1"	0.1"	0.1"	0.1"
Reel Quantities	178mm (7")	10000	2500	4000	3000	1000	2500	2000	2000	1500	500	500	750	500	500
	330mm (13")	15000	10000	16000	12000	5000	10000	8000	8000	6000	2000	2000	2000	2000	2000

Bulk Packing – Tubs

Chips are supplied in rigid re-sealable plastic tubs together with impact cushioning wadding. Tubs are labelled with the details: chip size, capacitance, tolerance, rated voltage, dielectric type, batch number, date code and quantity of components.

Dimensions mm (inches)

H	60mm (2.36")
D	50mm (1.97")



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