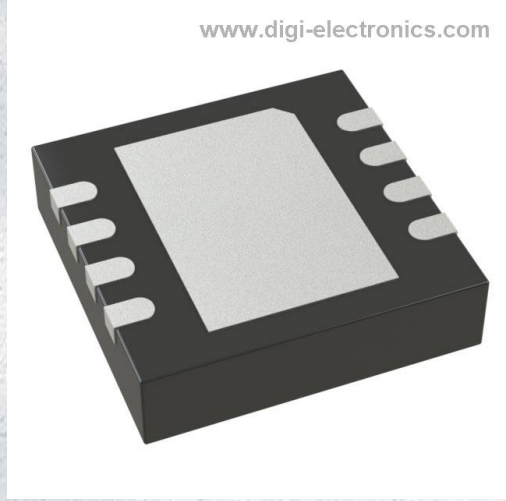
LTC2943IDD-1#TRPBF Datasheet



DiGi Electronics Part Number	LTC2943IDD-1#TRPBF-DG
Manufacturer	Analog Devices Inc.
Manufacturer Product Number	LTC2943IDD-1#TRPBF
Description	IC BATT MONITOR MULTI-CHEM 8DFN
Detailed Description	Battery Battery Monitor IC Multi-Chemistry 8-DFN (3 x3)

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Manufacturer Product Number:	Manufacturer:
LTC2943IDD-1#TRPBF	Analog Devices Inc.
Series:	Product Status:
-	Obsolete
Function:	Battery Chemistry:
Battery Monitor	Multi-Chemistry
Number of Cells:	Fault Protection:
-	Over Current, Over Temperature, Over Voltage
Interface:	Operating Temperature:
I2C	-40°C ~ 85°C (TA)
Mounting Type:	Package / Case:
Surface Mount	8-WFDFN Exposed Pad
Supplier Device Package:	Base Product Number:
8-DFN (3x3)	LTC2943

Environmental & Export classification

Moisture Sensitivity Level (MSL):	ECCN:
1 (Unlimited)	EAR99
HTSUS:	
8542.39.0001	

1A Multicell Battery Gas Gauge with Temperature, Voltage and Current Measurement

FEATURES

- **Measures Accumulated Battery Charge and Discharge**
- **3.6V to 20V Operating Range for Multiple Cells**
- **Integrated 50mΩ High Side Sense Resistor**
- **±1A Current Sense Range**
- **14-Bit ADC Measures Voltage, Current and Temperature**
- **1% Voltage, Current and Charge Accuracy**
- High Side Sense
- General Purpose Measurements for Any Battery Chemistry and Capacity
- I²C/SMBus Interface
- Configurable Alert Output/Charge Complete Input
- Quiescent Current Less Than 120µA
- Small 8-Lead 3mm × 3mm DFN Package

APPLICATIONS

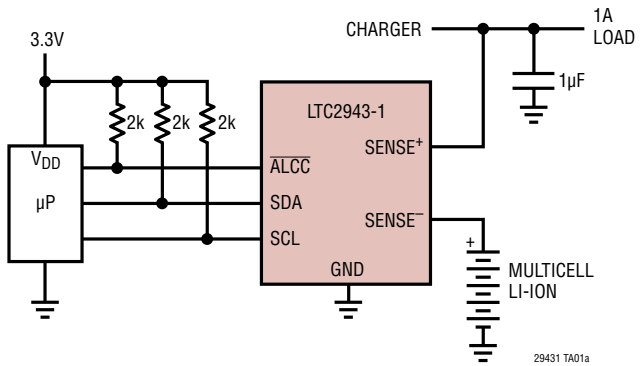
- Power Tools
- Portable Medical Equipment
- Video Cameras

DESCRIPTION

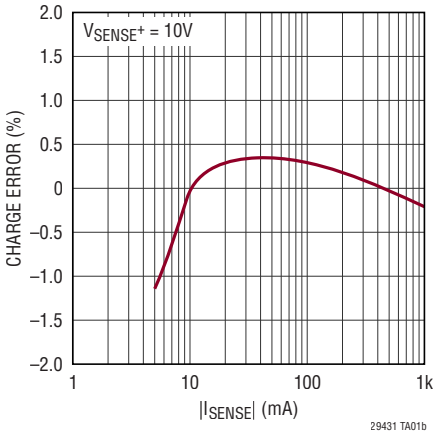
The LTC®2943-1 measures battery charge state, battery voltage, battery current and its own temperature in portable product applications. The wide input voltage range allows use with multicell batteries up to 20V. A precision coulomb counter integrates current through a sense resistor between the battery's positive terminal and the load or charger. Voltage, current and temperature are measured with an internal 14-bit No Latency ΔΣ™ ADC. The measurements are stored in internal registers accessible via the onboard I²C/SMBus Interface.

The LTC2943-1 features programmable high and low thresholds for all four measured quantities. If a programmed threshold is exceeded, the device communicates an alert using either the SMBus alert protocol or by setting a flag in the internal status register.

TYPICAL APPLICATION



Total Charge Error vs Current Sense

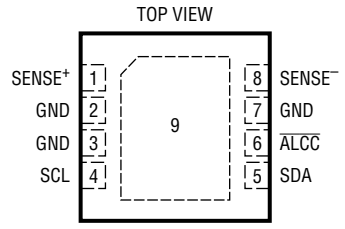


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (SENSE+) ..... –0.3V to 24V
SCL, SDA, $\overline{ALCC}$ Voltage ..... –0.3V to 6V
Sense Current (into SENSE–) .....±2A
Operating Ambient Temperature Range
LTC2943C-1 ..... 0°C to 70°C
LTC2943I-1 .....–40°C to 85°C
Storage Temperature Range .....–65°C to 150°C

PIN CONFIGURATION



DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 150°C, θ_{JA} = 53.4°C/W
EXPOSED PAD (PIN 9) PCB GND CONNECTION OPTIONAL

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2943CDD-1#PBF	LTC2943CDD-1#TRPBF	LGQN	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2943IDD-1#PBF	LTC2943IDD-1#TRPBF	LGQN	8-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Requirements							
V_{SENSE^+}	Supply Voltage			3.6		20	V
I_{SUPPLY}	Supply Current (Note 3)	Battery Gas Gauge On, ADC Sleep Battery Gas Gauge On, ADC On Shutdown	● ● ●		80 650 15	120 750 25	µA µA µA
V_{UVLO}	Undervoltage Lockout Threshold	V_{SENSE^+} Falling	●	3.0	3.3	3.6	V
Coulomb Counter							
I_{SENSE}	Sense Current		●			±1	A
R_{SENSE}	Internal Sense Resistance				50		mΩ
R_{FP}	Pin-to-Pin Resistance from SENSE+ to SENSE–	(Note 8)		50	74	100	mΩ
q_{LSB}	Charge LSB (Note 4)	Prescaler M = 4096(Default)			0.4		mAh
TCE	Total Charge Error (Note 5)	0.2A ≤ $\lvert I_{SENSE^-}\rvert$ ≤ 1A DC 0.2A ≤ $\lvert I_{SENSE^-}\rvert$ ≤ 1A DC, 0°C to 70°C 0.02A ≤ $\lvert I_{SENSE^-}\rvert$ ≤ 1A DC (Note 8)	 ● ●			±1 ±1.5 ±3.5	% % %
V_{OSE}	Effective Differential Offset Current (Note 9)	I_{SENSE} ≥ 10mA, V_{SENSE^+} = 10V	●		100	200	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Voltage Measurement ADC							
	Resolution (No Missing Codes)	(Note 8)	●	14			Bits
$V_{FS(V)}$	Full-Scale Voltage Conversion				23.6		V
ΔV_{LSB}	Quantization Step of 14-Bit Voltage ADC	(Note 6)			1.44		mV
TUE_V	Voltage Total Unadjusted Error		 ●			1 1.3	% %
$Gain_V$	Voltage Gain Accuracy		●			1.3	%
INL_V	Integral Nonlinearity	V_{SENSE^+} > 5V	●		±1	±4	LSB
		3.6V ≤ V_{SENSE^+} ≤ 5V	●			±8	LSB
$T_{CONV(V)}$	Voltage Conversion Time		●			48	ms
Current Measurement ADC							
	Resolution (No Missing Codes)	(Note 8)	●	12			Bits
$V_{FS(I)}$	Full-Scale Current Conversion		●		±1.3		A
V_{SENSE}	Sense Voltage Differential Input Range	$V_{SENSE^+} - V_{SENSE^-}$	●			±1	A
ΔI_{LSB}	Quantization Step of 12-Bit Current ADC	(Note 6)			317.4		µA
$Gain_I$	Current Gain Accuracy	 0°C to 70°C –40°C to 85°C	 ● ●			1 1.3 3	% % %
$V_{OS(I)}$	Offset				±1	±10	LSB
INL_I	Integral Nonlinearity		●		±1	±4	LSB
$T_{CONV(I)}$	Current Conversion Time		●			8	ms
Temperature Measurement ADC							
	Resolution (No Missing Codes)	(Note 8)	●	11			Bits
T_{FS}	Full-Scale Temperature				510		K
ΔT_{LSB}	Quantization Step of 11-Bit Temperature ADC	(Note 6)			0.25		K
TUE_T	Temperature Total Unadjusted Error			±3			K
$T_{CONV(T)}$	Temperature Conversion Time		●			8	ms
Digital Inputs and Digital Outputs							
$V_{ITH(HV)}$	Logic Input Threshold	V_{SENSE^+} ≥ 5V	●	0.8		2.2	V
$V_{ITH(LV)}$		3.6V < V_{SENSE^+} < 5V		0.45		1.8	V
V_{OL}	Low Level Output Voltage, $\overline{ALCC}$, SDA	I = 3mA, V_{SENSE^+} ≥ 5V	●			0.4	V
I_{IN}	Input Leakage, $\overline{ALCC}$, SCL, SDA	V_{IN} = 5V	●			±1	µA
C_{IN}	Input Capacitance, $\overline{ALCC}$, SCL, SDA	(Note 8)	●			10	pF
t_{PCC}	Minimum Charge Complete ($\overline{CC}$) Pulse Width					1	µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I²C Timing Characteristics							
$f_{SCL(MAX)}$	Maximum SCL Clock Frequency		●	400	900		kHz
$t_{BUF(MAX)}$	Bus Free Time Between Stop/Start		●			1.3	µs
$t_{SU(STA(MIN))}$	Minimum Repeated Start Set-Up Time		●			600	ns
$t_{HD(STA(MIN))}$	Minimum Hold Time (Repeated) Start Condition		●			600	ns
$t_{SU(STO(MIN))}$	Minimum Set-Up Time for Stop Condition		●			600	ns
$t_{SU(DAT(MIN))}$	Minimum Data Setup Time Input		●			100	ns
$T_{HD(DAT(MIN))}$	Minimum Data Hold Time Input		●			50	ns
T_{HDDATO}	Data Hold Time Input Output		●	0.3		0.9	µs
T_{OF}	Data Output Fall Time	(Notes 7, 8)	●	20 + 0.1 • C_B		300	ns

Note 1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2. All currents into pins are positive, all voltages are referenced to GND unless otherwise specified.

Note 3. $I_{SUPPLY} = I_{SENSE^+} + I_{SENSE^-}$. In most operating modes, I_{SUPPLY} is flowing in $SENSE^+$ pin. Only during ADC conversions, current is flowing in $SENSE^-$ pin as well. Typically, $I_{SENSE^-} = V_{SENSE^-}/150k$ during ADC voltage conversion and I_{SENSE^-} = 20µA during ADC current conversion.

Note 4. The equivalent charge of an LSB in the accumulated charge register depends on the value of R_{SENSE} and the setting of the internal prescaling factor M:

q_{LSB} = 0.4mAh • (M/4096)

See Choosing Coulomb Counter Prescaler M section for more information. 1mAh = 3.6C (Coulombs)

Note 5. Deviation of q_{LSB} from its nominal value.

Note 6. The quantization step of the 14-bit ADC in voltage mode,12-bit ADC in current mode and 11-bit ADC in temperature mode is not the same as the LSB of the respective combined 16-bit registers. See Voltage, Current and Temperature Registers section for more information.

Note 7. C_B = Capacitance of one bus line in pF (10pF ≤ C_B ≤ 400pF).

Note 8. Guaranteed by design, not subject to test.

Note 9. See Effect of Differential Offset Voltage on Total Charge Error section.

TIMING DIAGRAM

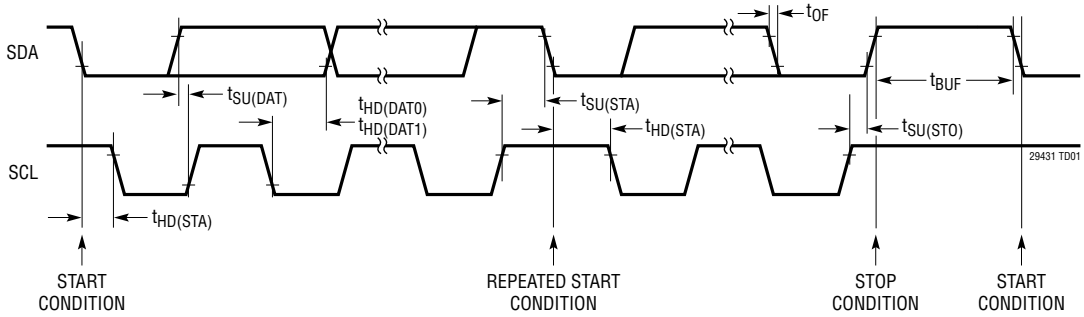
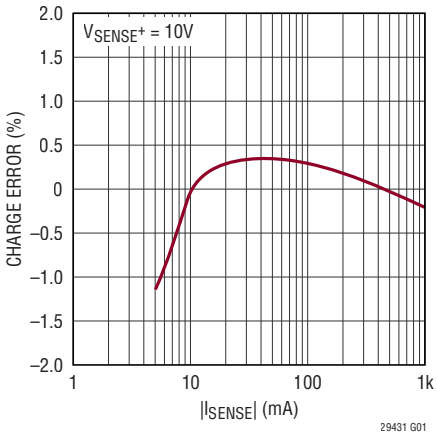


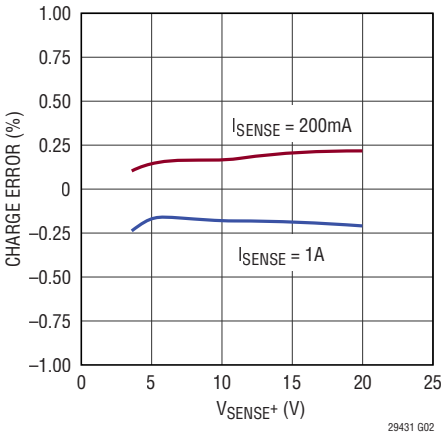
Figure 1. Definition of Timing on I²C Bus

TYPICAL PERFORMANCE CHARACTERISTICS

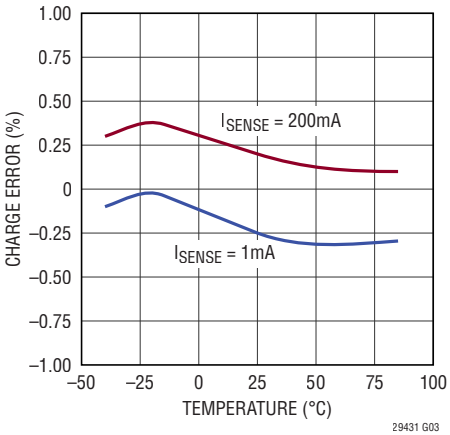
Total Charge Error vs Sense Current



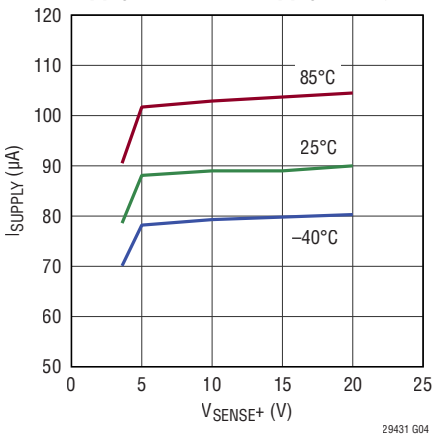
Total Charge Error vs Supply Voltage



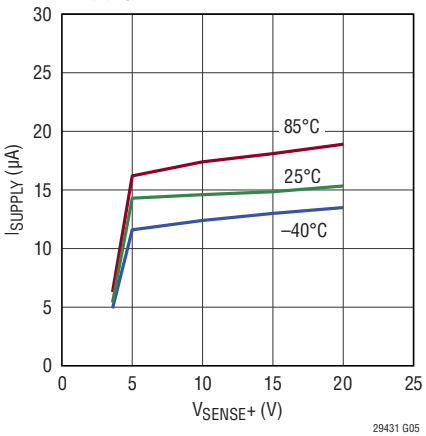
Total Charge Error vs Temperature



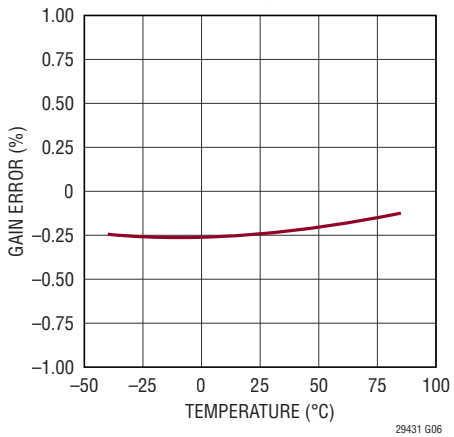
Supply Current vs Supply Voltage



Shutdown Supply Current vs Supply Voltage

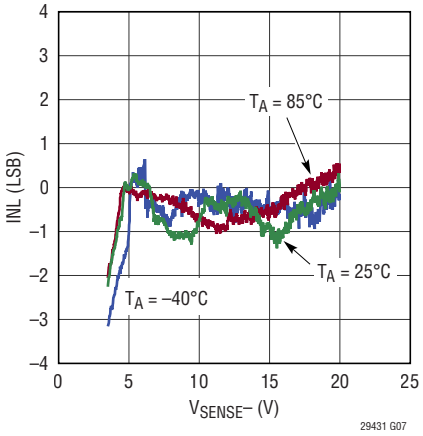


Voltage Measurement ADC Gain Error vs Temperature

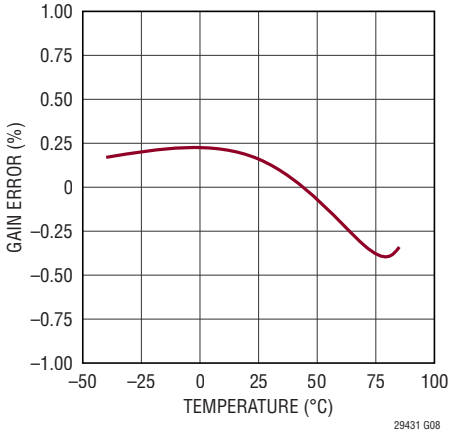


TYPICAL PERFORMANCE CHARACTERISTICS

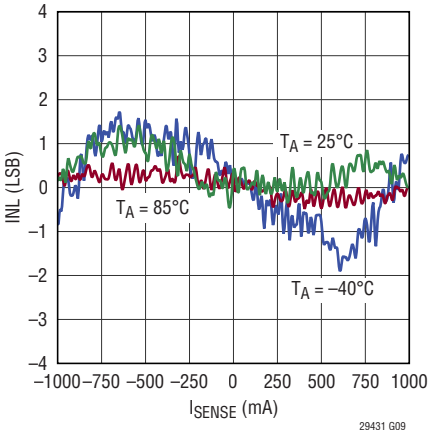
Voltage Measurement ADC Integral Nonlinearity



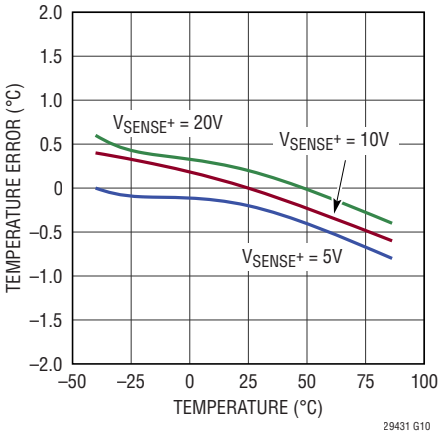
Current Measurement ADC Gain Error vs Temperature



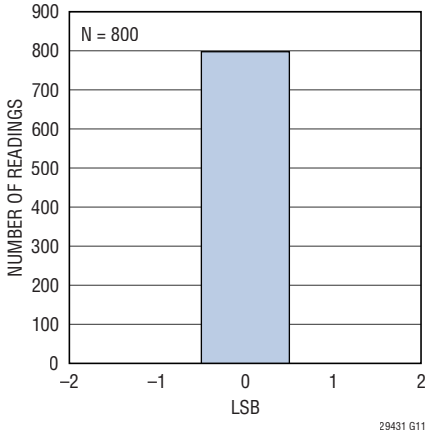
Current Measurement ADC Integral Nonlinearity



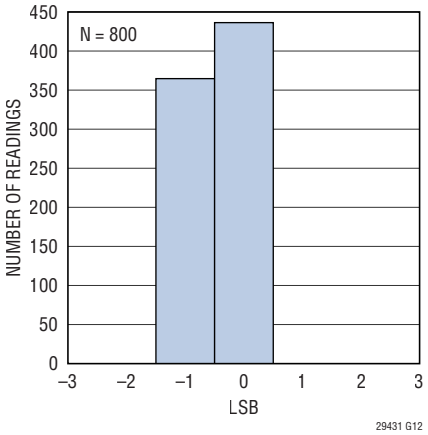
Temperature Error vs Temperature



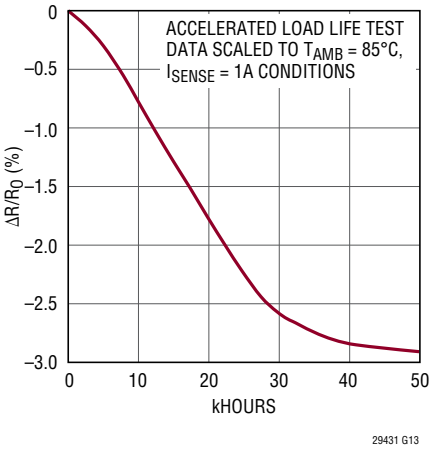
Voltage Measurement Noise



Current Measurement Noise



Sense Resistor Stability



PIN FUNCTIONS

SENSE+ (Pin 1): Positive Current Sense Input and Power Supply. Connect to the load and battery charger output. V_{SENSE^+} operating range is 3.6V to 20V. SENSE+ is also an input to the ADC during current measurement. Bypass to GND with a 1µF capacitor located as close to pin 1 and pin 2 as possible.

GND (Pin 2, Pin 3, Pin 7): Device Ground. Connect directly to the negative battery terminal.

SCL (Pin 4): Serial Bus Clock Input. SCL is internally pulled up with 50µA (Typ) above its logic input high threshold to about 2V (Typ).

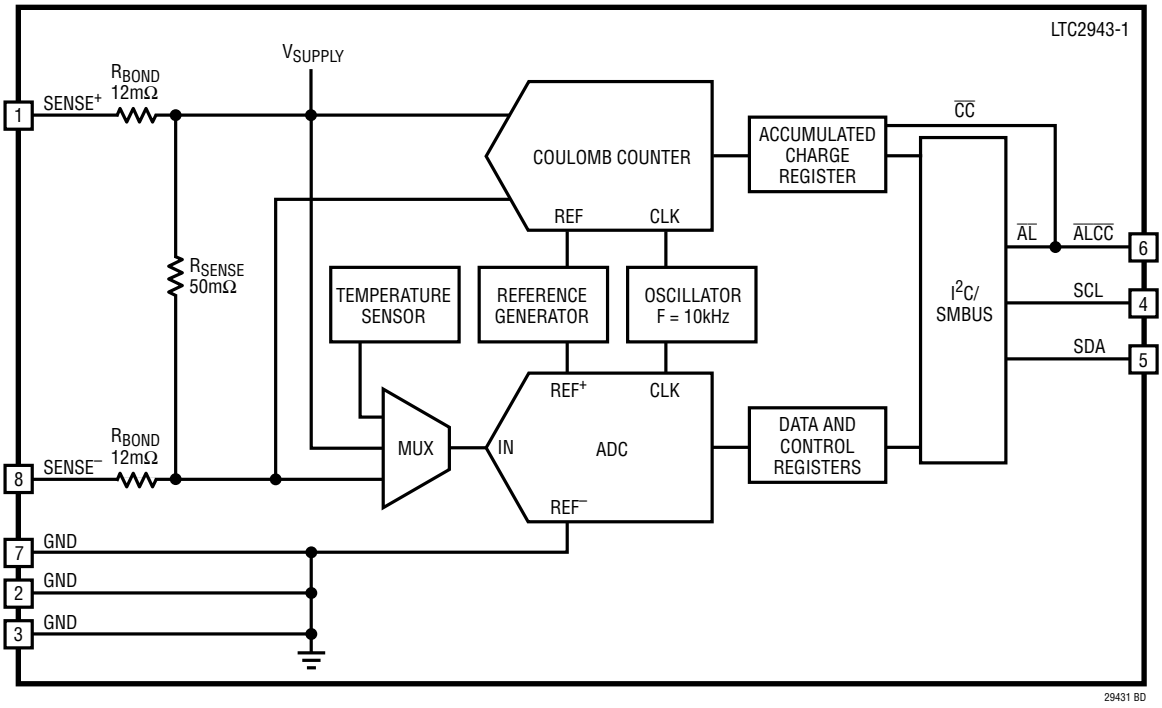
SDA (Pin 5): Serial Bus Data Input and Output. SDA is internally pulled up with 50µA (Typ) above its logic input high threshold to about 2V (Typ).

$\overline{\text{ALCC}}$ (Pin 6): Alert Output or Charge Complete Input. Configured either as an SMBus alert output or charge complete input by control register bits B[2:1]. At power-up, the pin defaults to alert mode conforming to the SMBus alert response protocol. It behaves as an open-drain logic output that pulls to GND when any threshold register value is exceeded. When configured as a charge complete input, connect to the charge complete output from the battery charger circuit. A low level at $\overline{\text{CC}}$ sets the value of the accumulated charge (registers C, D) to FFFFh.

SENSE– (Pin 8): Negative Current Sense Input. Connect SENSE– to the positive battery terminal. Current from/into this pin must not exceed 1A in normal operation. SENSE– is also an input to the ADC during voltage and current measurement.

Exposed Pad (Pin 9): Exposed pad may be left open or connected to device ground (GND).

BLOCK DIAGRAM



OPERATION

Overview

The LTC2943-1 is a battery gas gauge designed for use with multicell batteries with terminal voltages from 3.6V to 20V. It measures battery charge and discharge, battery voltage, current and its own temperature.

A precision analog coulomb counter integrates current through a sense resistor between the battery's positive terminal and the load or charger. Battery voltage, battery current and silicon temperature are measured with an internal ADC.

The integrated, temperature compensated sense resistor offers board space savings and superior change measurement accuracy in applications with currents up to 1A.

Coulomb Counter

Charge is the time integral of current. The LTC2943-1 measures charge by monitoring the voltage developed across an internal sense resistor. The differential voltage is applied to an auto-zeroed differential analog integrator to infer charge.

When the integrator output ramps to REFHI or REFLO levels, switches S1, S2, S3 and S4 toggle to reverse the ramp direction (Figure 2). By observing the condition of the switches and the ramp direction, polarity is determined. This approach also significantly lowers the impact on offset of the analog integrator as described in the Differential Offset Voltage section.

OPERATION

A programmable prescaler effectively increases integration time by a factor M programmable from 1 to 4096. At each underflow or overflow of the prescaler, the accumulated charge register (ACR) value is incremented or decremented one count. The value of accumulated charge is read via the I²C interface.

Voltage, Current and Temperature ADC

The LTC2943-1 includes a 14-bit No Latency ΔΣ analog-to-digital converter, with internal clock and voltage reference circuits.

The ADC can be used to monitor the battery voltage at SENSE⁻ or the battery current flowing through the sense resistor or to convert the output of the on-chip temperature sensor.

Conversion of voltage, current and temperature are triggered by programming the control register via the I²C interface. The LTC2943-1 includes a scan mode where voltage, current and temperature conversion measurements are executed every 10 seconds. At the end of each conversion the corresponding registers are updated and the converter goes to sleep to minimize quiescent current.

The temperature sensor generates a voltage proportional to temperature with a slope of 2mV/K resulting in a voltage of 600mV at 27°C.

Power-Up Sequence

When SENSE⁺ rises above a threshold of approximately 3.3V, the LTC2943-1 generates an internal power-on reset (POR) signal and sets all registers to their default state. In the default state, the coulomb counter is active while the voltage, current and temperature ADC is switched off. The accumulated charge register is set to mid-scale (7FFFh), all low threshold registers are set to 0000h and all high threshold registers are set to FFFFh. The alert mode is enabled and the coulomb counter prescaling factor M is set to 4096.

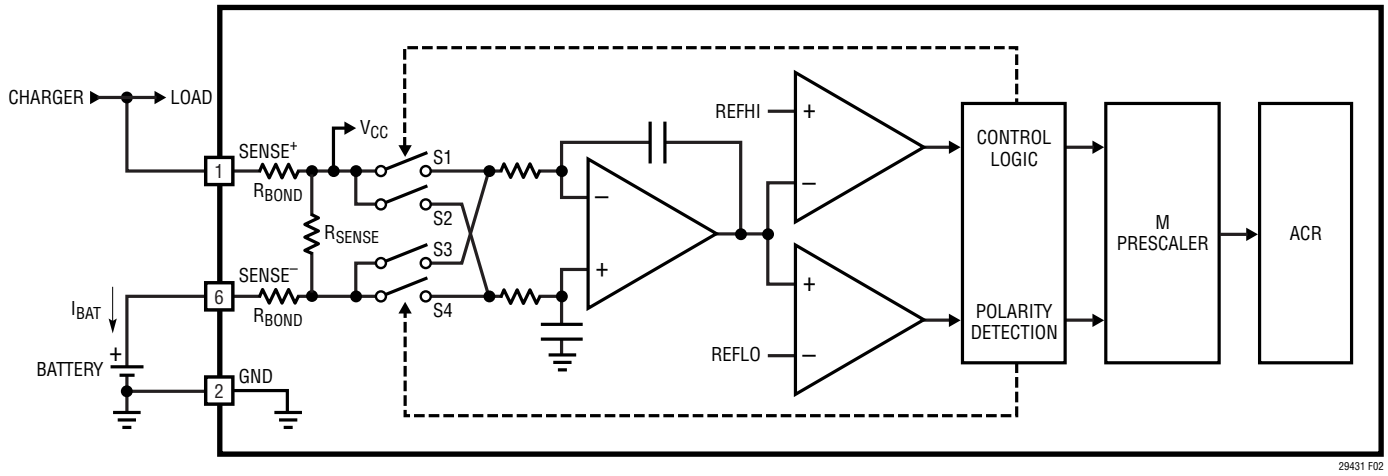


Figure 2. Coulomb Counter Section of the LTC2943-1

APPLICATIONS INFORMATION

Internal Registers

The LTC2943-1 register map is shown in Table 1. The LTC2943-1 integrates current through a sense resistor, measures battery voltage, current and temperature and stores the results in internal 16-bit registers accessible via I^2C. High and low limits can be programmed for each measured quantity. The LTC2943-1 continuously monitors these limits and sets a flag in the status register when a limit is exceeded. If the alert mode is enabled, the $\overline{ALCC}$ pin pulls low.

Table 1. Register Map

ADDRESS	NAME	REGISTER DESCRIPTION	R/W	DEFAULT
00h	A	Status	R	See Table 2
01h	B	Control	R/W	3Ch
02h	C	Accumulated Charge MSB	R/W	7Fh
03h	D	Accumulated Charge LSB	R/W	FFh
04h	E	Charge Threshold High MSB	R/W	FFh
05h	F	Charge Threshold High LSB	R/W	FFh
06h	G	Charge Threshold Low MSB	R/W	00h
07h	H	Charge Threshold Low LSB	R/W	00h
08h	I	Voltage MSB	R	00h
09h	J	Voltage LSB	R	00h
0Ah	K	Voltage Threshold High MSB	R/W	FFh
0Bh	L	Voltage Threshold High LSB	R/W	FFh
0Ch	M	Voltage Threshold Low MSB	R/W	00h
0Dh	N	Voltage Threshold Low LSB	R/W	00h
0Eh	O	Current MSB	R	00h
0Fh	P	Current LSB	R	00h
10h	Q	Current Threshold High MSB	R/W	FFh
11h	R	Current Threshold High LSB	R/W	FFh
12h	S	Current Threshold Low MSB	R/W	00h
13h	T	Current Threshold Low LSB	R/W	00h
14h	U	Temperature MSB	R	00h
15h	V	Temperature LSB	R	00h
16h	W	Temperature Threshold High	R/W	FFh
17h	X	Temperature Threshold Low	R/W	00h

R = Read, W = Write

The status of the charge, voltage, current and temperature alerts is reported in the status register shown in Table 2.

Table 2. Status Register (A)

BIT	NAME	OPERATION	DEFAULT
A[7]	Reserved		
A[6]	Current Alert	Indicates one of the current limits was exceeded	0
A[5]	Accumulated Charge Overflow/ Underflow	Indicates that the value of the ACR hit either top or bottom	0
A[4]	Temperature Alert	Indicates one of the temperature limits was exceeded	0
A[3]	Charge Alert High	Indicates that the ACR value exceeded the charge threshold high limit	0
A[2]	Charge Alert Low	Indicates that the ACR value exceeded the charge threshold low limit	0
A[1]	Voltage Alert	Indicates one of the voltage limits was exceeded	0
A[0]	Undervoltage Lockout Alert	Indicates recovery from undervoltage. If set to 1, a UVLO has occurred and the contents of the registers are uncertain	1

After each voltage, current or temperature conversion, the conversion result is compared to the respective threshold registers. If a value in the threshold registers is exceeded, the corresponding bit A[6], A[4] or A[1] is set.

The accumulated charge register (ACR) is compared to the charge thresholds every time the analog integrator increments or decrements the prescaler. If the ACR value exceeds the threshold register values, the corresponding bit A[3] or A[2] are set. Bit A[5] is set if the accumulated charge registers (ACR) overflows or underflows. At each overflow or underflow, the ACR rolls over and resumes integration.

The undervoltage lockout (UVLO) bit of the status register A[0] is set if, during operation, the voltage on the $SENSE^+$ pin drops below 3.5V without reaching the POR level. The analog parts of the coulomb counter are switched off while

APPLICATIONS INFORMATION

the digital register values are retained. After recovery of the supply voltage the coulomb counter resumes integrating with the stored value in the accumulated charge registers but it has missed any charge flowing while $SENSE^+ < 3.5V$.

All status register bits are cleared after being read by the host, but might be reasserted after the next temperature, voltage or current conversion or charge integration, if the corresponding alert condition is still fulfilled.

Control Register (B)

The operation of the LTC2943-1 is controlled by programming the control register. Table 3 shows the organization of the 8-bit control register B[7:0].

Table 3. Control Register B

BIT	NAME	OPERATION	DEFAULT
B[7:6]	ADC Mode	[11] Automatic Mode: continuously performing voltage, current and temperature conversions [10] Scan Mode: performing voltage, current and temperature conversion every 10s [01] Manual Mode: performing single conversions of voltage, current and temperature then sleep [00] Sleep	[00]
B[5:3]	Prescaler M	Sets coulomb counter prescaling factor M between 1 and 4096. Default is 4096. Maximum value is limited to 4096	[111]

B[5:3]	M
000	1
001	4
010	16
011	64
100	256
101	1024
110	4096
111	4096

BIT	NAME	OPERATION	DEFAULT
B[2:1]	$\overline{ALCC}$ Configure	Configures the $\overline{ALCC}$ pin [10] Alert Mode. Alert functionality enabled. Pin becomes logic output [01] Charge Complete Mode. Pin becomes logic input and accepts charge complete inverted signal (e.g., from a charger) to set accumulated charge register (C,D) to FFFFh [00] $\overline{ALCC}$ pin disabled [11] Not allowed	[10]
B[0]	Shutdown	Shut down analog section to reduce I_{SUPPLY}	[0]

Power Down B[0]

Setting B[0] to 1 shuts down the analog parts of the LTC2943-1, reducing the current consumption to less than 15µA (typical). The circuitry managing I^2C communication remains operating and the values in the registers are retained. Note that any charge flowing while B[0] is 1 is not measured and any charge information below 1LSB of the accumulated charge register is lost.

Alert/Charge Complete Configuration B[2:1]

The $\overline{ALCC}$ pin is a dual function pin configured by the control register. By setting bits B[2:1] to [10] (default), the $\overline{ALCC}$ pin is configured as an alert pin following the SMBus protocol. In this configuration, the $\overline{ALCC}$ is pulled low if one of the four measured quantities (charge, voltage, current, temperature) exceeds its high or low threshold or if the value of the accumulated charge register overflows or underflows. An alert response procedure started by the master resets the alert at the $\overline{ALCC}$ pin. If the configuration of the $\overline{ALCC}$ pin is changed while it is pulled low due to an alert condition, the part will continue to pull $\overline{ALCC}$ low until a successful alert response procedure (ARA) has been issued by the master. For further information see the Alert Response Protocol section.

Setting the control bits B[2:1] to [01] configures the $\overline{ALCC}$ pin as a digital input. In this mode, a low input on the $\overline{ALCC}$ pin indicates to the LTC2943-1 that the battery is full and the accumulated charge register is set to its maximum, value FFFFh.

APPLICATIONS INFORMATION

If neither the alert nor the charge complete functionality is desired, bits B[2:1] should be set to [00]. The $\overline{ALCC}$ pin is then disabled and should be tied to the supply of the I^2C bus with a 10k resistor.

Avoid setting B[2:1] to [11] as it enables the alert and the charge complete modes simultaneously.

Choosing Coulomb Prescaler M B[5:3]

If the battery capacity (Q_{BAT}) is small compared to the maximum current (I_{MAX}) the prescaler value M should be changed from its default value (4096).

In these applications with a small battery but a high maximum current, q_{LSB} can get quite large with respect to the battery capacity. For example, if the battery capacity is 100mAh and the maximum current is 1A, the default value M = 4096 leads to:

$$q_{LSB} = 0.4mAh$$

The battery capacity then corresponds to only 250 q_{LSB} and less than 0.5% of the accumulated charge register is utilized.

To preserve digital resolution in this case, the LTC2943-1 includes a programmable prescaler. Lowering the prescaler factor M reduces q_{LSB} to better match the accumulated charge register to the capacity of the battery. The prescaling factor M can be chosen between 1 and its default value of 4096. The charge LSB then becomes:

$$q_{LSB} = 0.4mAh \bullet \frac{M}{4096}$$

To use as much of the range of the accumulated charge register as possible the prescaler factor M should be chosen for a given battery capacity Q_{BAT} and a sense resistor R_{SENSE} as:

$$M \geq 4096 \bullet \frac{Q_{BAT}}{2^{16} \bullet 0.4mAh}$$

M can be set to 1, 4, 16, ... 4096 by programming B[5:3] of the control register as $M = 2^{2 \bullet (4 \bullet B[5] + 2 \bullet B[4] + B[3])}$. The default value is 4096.

In the above example of a 100mAh battery, the prescaler should be programmed to M = 64. The q_{LSB} is then 6.25µAh and the battery capacity corresponds to 16000 q_{LSB}s.

ADC Mode B[7:6]

The LTC2943-1 features an ADC which measures either voltage on $SENSE^-$ (battery voltage), current through $SENSE^+$ and $SENSE^-$ (battery current) or temperature via an internal temperature sensor. The reference voltage and clock for the ADC are generated internally.

The ADC has four different modes of operation as shown in Table 3. These modes are controlled by bits B[7:6] of the control register. At power-up, bits B[7:6] are set to [00] and the ADC is in sleep mode.

A single conversion of the three measured quantities is initiated by setting the bit B[7:6] to [01]. After three conversions (voltage, current and temperature), the ADC resets B[7:6] to [00] and goes back to sleep.

The LTC2943-1 is set to scan mode by setting B[7:6] to [10]. In scan mode the ADC converts voltage, current, then temperature, then sleeps for approximately 10 seconds. It then reawakens automatically and repeats the three conversions. The chip remains in scan mode until reprogrammed by the host.

Programming B[7:6] to [11] sets the chip into automatic mode where the ADC continuously performs voltage, current and temperature conversions. The chip stays in automatic mode until reprogrammed by the host.

Programming B[7:6] to [00] puts the ADC to sleep. If control bits B[7:6] change within a conversion, the ADC will complete the running cycle of conversions before entering the newly selected mode.

A conversion of voltage requires 33ms (typical), and current and temperature conversions are completed in 4.5ms (typical). At the end of each conversion, the corresponding registers are updated. If the converted quantity exceeds the values programmed in the threshold registers, a flag is set in the status register and the $\overline{ALCC}$ pin is pulled low (if alert mode is enabled).

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Alert Thresholds Registers (E,F,G,H,K,L,M,N,Q,R,S, T,W,X)

For each of the measured quantities (battery charge, voltage, current and temperature) the LTC2943-1 features high and low threshold registers. At power-up, the high thresholds are set to FFFFh while the low thresholds are set to 0000h, with the effect of disabling them. All thresholds can be programmed to a desired value via I^2C. As soon as a measured quantity exceeds the high threshold or falls below the low threshold, the LTC2943-1 sets the corresponding flag in the status register and pulls the $\overline{ALCC}$ pin low if alert mode is enabled via bits B[2:1].

Accumulated Charge Register (C,D)

The coulomb counting circuitry in the LTC2943-1 integrates current through the sense resistor. The result of this charge integration is stored in the 16-bit accumulated charge register (registers C, D). As the LTC2943-1 does not know the actual battery status at power-up, the accumulated charge register (ACR) is set to mid-scale (7FFFh). If the host knows the status of the battery, the accumulated charge (C[7:0] D[7:0]) can be either programmed to the correct value via I^2C or it can be set after charging to FFFFh (full) by pulling the $\overline{ALCC}$ pin low if charge complete mode is enabled via bits B[2:1]. Note that before writing to the accumulated charge registers, the analog section should be temporarily shut down by setting B[0] to 1. In order to avoid a change in the accumulated charge registers between reading MSBs C[7:0] and LSBs D[7:0], it is recommended to read them sequentially as shown in Figure 9.

Voltage Registers (I,J) and Voltage Threshold Registers (K,L,M,N)

The result of the 14-bit ADC conversion of the voltage at $SENSE^-$ is stored in the voltage registers (I, J).

From the result of the 16-bit voltage registers I[7:0]J[7:0] the measured voltage can be calculated as:

$$V_{SENSE^-} = 23.6V \bullet \frac{RESULT_h}{FFFF_h} = 23.6V \bullet \frac{RESULT_{DEC}}{65535}$$

Example 1: a register value I[7:0] = B0h and J[7:0] = 1Ch corresponds to a voltage on $SENSE^-$ of:

$$V_{SENSE^-} = 23.6V \bullet \frac{B01C_h}{FFFF_h} = 23.6V \bullet \frac{45084_{DEC}}{65535} \approx 16.235V$$

Example 2: To set a low level threshold for the battery voltage of 7.2V, register M should be programmed to 4Eh and register N to 1Ah.

Current Registers (O,P) and Current Threshold Registers (Q,R,S,T)

The result of the current conversion is stored in the current registers (O,P).

As the ADC resolution is 12 bits in current mode, the lowest four bits of the combined current registers (O, P) are always zero.

The ADC measures battery current by converting the voltage, V_{SENSE}, across the sense resistor R_{SENSE}. Depending on whether the battery is being charged or discharged, the measured voltage drop on R_{SENSE} is positive or negative. The result is stored in registers O and P in excess –32767 representation. O[7:0] = FFh, P[7:0] = FFh corresponds to the full-scale positive current 1.3A. While O[7:0] = 00h, P[7:0] = 00h corresponds to the full-scale negative current –1.3A. The battery current can be obtained from the two byte register O[7:0]P[7:0] and the value of the chosen sense resistor R_{SENSE}:

$$I_{BAT} = 1.3A \bullet \left(\frac{RESULT_h - 7FFF_h}{7FFF_h} \right) =$$

$$1.3A \bullet \left(\frac{RESULT_{DEC} - 32767}{32767} \right)$$

Positive current is measured when the battery is charging and negative current is measured when the battery is discharging.

APPLICATIONS INFORMATION

Example 1: a register value of O[7:0] = A8h P[7:0] = 40h together with a sense resistor $R_{SENSE} = 50m\Omega$ corresponds to a battery current:

$$I_{BAT} = 1.3A \bullet \left(\frac{A840_h - 7FFF_h}{7FFF_h} \right) =$$

$$1.3A \bullet \left(\frac{43072 - 32767}{32767} \right) \approx 314.5mA$$

The positive current result indicates that the battery is being charged.

The values in the threshold register for the current mode Q,R,S,T are also expressed in excess –32767 representation in the same manner as the current conversion result. The alert after a current measurement is set if the result is higher than the value stored in the high threshold registers Q,R or lower than the value stored in the low value registers S,T.

Example 2: In an application, the user wants to get an alert if the absolute current through the sense resistor, exceeds 1A. This is achieved by setting the upper threshold I_{HIGH} in register [Q,R] to 1A and the lower threshold I_{LOW} in register [S,T] to –1A. The formula for I_{BAT} leads to:

$$I_{HIGH(DEC)} = \left(\frac{1A}{1.3A} \bullet 32767 \right) + 32767 = 57972$$

$$I_{LOW(DEC)} = \left(\frac{-1A}{1.3A} \bullet 32767 \right) + 32767 = 7562$$

Leading the user to set Q[7:0] = E2h, R[7:0] = 74h for the high threshold and S[7:0] = 1Dh and T[7:0] = 8Ah for the low threshold.

Temperature Registers (U,V) and Temperature Threshold Registers (W,X)

As the ADC resolution is 11 bits in temperature mode, the lowest five bits of the combined temperature registers (U, V) are always zero.

The actual temperature can be obtained from the two byte register U[7:0]V[7:0] by:

$$T = 510K \bullet \frac{RESULT_h}{FFFF_h} = 510K \bullet \frac{RESULT_{DEC}}{65535}$$

Example: a register value of U[7:0] = 96h, V[7:0] = 96h corresponds to ~300K or ~27°C

A high temperature limit of 60°C is programmed by setting register W to A7h. Note that the temperature threshold register is a single byte register and only the eight MSBs of the 11 bits temperature result are checked.

Effect of Differential Offset Voltage on Total Charge Error

In battery gas gauges, an important parameter is the differential offset (I_{OS}) of the circuitry monitoring the battery charge. Many coulomb counter devices perform an analog to digital conversion of I_{SENSE} and accumulate the conversion results to infer charge. In such an architecture, the differential offset I_{OS} causes relative charge error of I_{OS}/I_{SENSE}. For small I_{SENSE} values I_{OS} can be the main source of error.

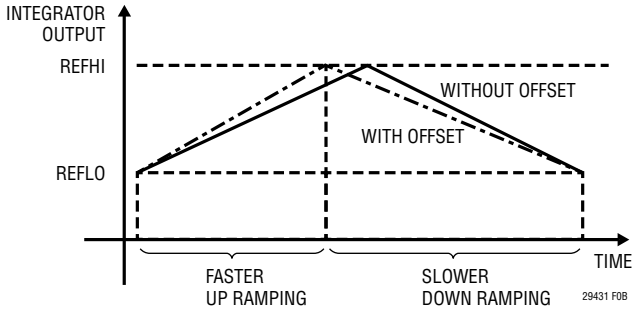
The LTC2943-1 performs the tracking of the charge with an analog integrator. This approach allows to continuously monitor the battery charge and significantly lowers the error due to differential offset. The relative charge error due to offset (CE_{OV}) can be expressed by:

$$CE_{OV} = \left(\frac{I_{OS}}{I_{SENSE}} \right)^2$$

As an example, at a 20mA input signal, a differential voltage offset V_{OS} = 20µV results in a 2% error using digital integration, whereas the error is only 0.04% (a factor of 50 times smaller!) using the analog integration approach of LTC2943-1.

APPLICATIONS INFORMATION

The reduction of the impact of the offset in LTC2943-1 can be explained by its integration scheme depicted in Figure 2. While positive offset accelerates the up ramping of the integrator output from REFLO to REFHI, it slows the down ramping from REFHI to REFLO thus the effect is largely canceled as depicted below.



For input signals with an absolute value smaller than the offset of the internal op amp, the LTC2943-1 stops integrating and does not integrate its own offset.

I²C/SMBus Interface

The LTC2943-1 communicates with a bus master using a 2-wire interface compatible with I²C and SMBus. The 7-bit hard coded I²C address of the LTC2943-1 is 1100100.

The LTC2943-1 is a slave only device. The serial clock line (SCL) is input only while the serial data line (SDA) is bidirectional. The device supports I²C standard and fast mode. For more details refer to the I²C Protocol section.

I²C Protocol

The LTC2943-1 uses an I²C/SMBus-compatible 2-wire interface supporting multiple devices on a single bus. Connected devices can only pull the bus lines low and must never drive the bus high. The bus wires are externally connected to a positive supply voltage via current sources or pull-up resistors. When the bus is idle, all bus lines are high. Data on the I²C bus can be transferred at rates of up to 100kbit/s in standard mode and up to 400kbit/s in fast mode.

Each device on the I²C/SMbus is recognized by a unique address stored in that device and can operate as either a transmitter or receiver, depending on the function of the device. In addition to transmitters and receivers, devices can also be classified as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At the same time any device addressed is considered a slave. The LTC2943-1 always acts as a slave.

Figure 3 shows an overview of the data transmission on the I²C bus.

Start and Stop Conditions

When the bus is idle, both SCL and SDA must be high. A bus master signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high. When the master has finished com-

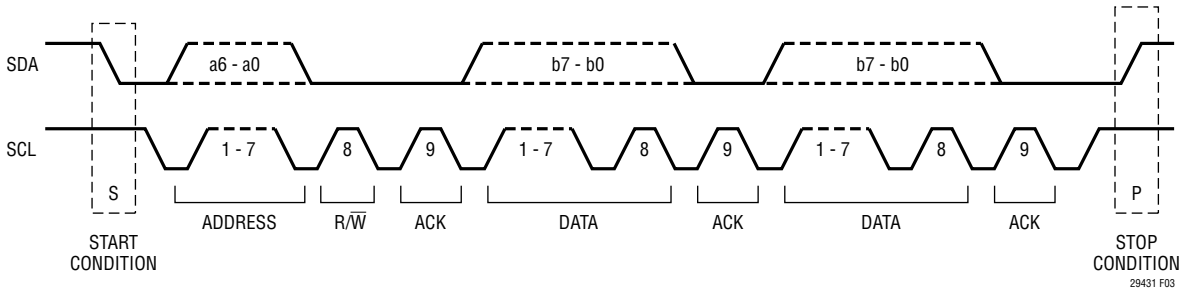


Figure 3. Data Transfer Over I²C or SMBus

APPLICATIONS INFORMATION

municating with the slave, it issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission. When the bus is in use, it stays busy if a repeated START (Sr) is generated instead of a STOP condition. The repeated START (Sr) conditions are functionally identical to the START (S).

Write Protocol

The master begins a write operation with a START condition followed by the seven bit slave address 1100100 and the R/W bit set to zero, as shown in Figure 4. The LTC2943-1 acknowledges this by pulling SDA low and the master sends a command byte which indicates which internal register the master is to write. The LTC2943-1 acknowledges and latches the command byte into its internal register address pointer. The master delivers the data byte, the LTC2943-1 acknowledges once more and latches the data into the desired register. The transmission is ended when the master sends a STOP condition. If the master continues by sending a second data byte instead of a stop, the LTC2943-1 acknowledges again, increments its address pointer and latches the second data byte in the following register, as shown in Figure 5.

S	ADDRESS	$\overline{W}$	A	REGISTER	A	DATA	A	P
	1100100	0	0	01h	0	FCh	0	

29431 F04

FROM MASTER TO SLAVE

FROM SLAVE TO MASTER

A: ACKNOWLEDGE (LOW)
$\overline{A}$: NOT ACKNOWLEDGE (HIGH)
S: START CONDITION
P: STOP CONDITION
R: READ BIT (HIGH)
$\overline{W}$: WRITE BIT (LOW)

Figure 4. Writing FCh to the LTC2943-1 Control Register (B)

S	ADDRESS	$\overline{W}$	A	REGISTER	A	DATA	A	DATA	A	P
	1100100	0	0	02h	0	F0h	0	01h	0	

29431 F05

Figure 5. Writing F001h to the LTC2943-1 Accumulated Charge Register (C, D)

Read Protocol

The master begins a read operation with a START condition followed by the seven bit slave address 1100100 and the R/W bit set to zero, as shown in Figure 6. The LTC2943-1 acknowledges and the master sends a command byte which indicates which internal register the master is to read. The LTC2943-1 acknowledges and then latches the command byte into its internal register address pointer. The master then sends a repeated START condition followed by the same seven bit address with the R/W bit now set to one. The LTC2943-1 acknowledges and sends the contents of the requested register. The transmission is ended when the master sends a STOP condition. If the master acknowledges the transmitted data byte, the LTC2943-1 increments its address pointer and sends the contents of the following register as depicted in Figure 7.

S	ADDRESS	$\overline{W}$	A	REGISTER	A	Sr	ADDRESS	R	A	DATA	$\overline{A}$	P
	1100100	0	0	00h	0		1100100	1	0	01h	1	

29431 F06

Figure 6. Reading the LTC2943-1 Status Register (A)

S	ADDRESS	$\overline{W}$	A	REGISTER	A	Sr	ADDRESS	R	A	DATA	A	DATA	$\overline{A}$	P
	1100100	0	0	08h	0		1100100	1	0	F1h	0	24h	1	

29431 F07

Figure 7. Reading the LTC2943-1 Voltage Register (I, J)

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Alert Response Protocol

In a system where several slaves share a common interrupt line, the master can use the alert response address (ARA) to determine which device initiated the interrupt (Figure 8).

S	ALERT RESPONSE ADDRESS	R	A	DEVICE ADDRESS	$\overline{A}$	P
	0001100	1	0	1100100	1	

29431 F08

Figure 8. LTC2943-1 Serial Bus SDA Alert Response Protocol

S	ADDRESS	$\overline{W}$	A	REGISTER	A	S	ADDRESS	R	A	DATA	A	DATA	$\overline{A}$	P
	1100100	0	0	02h	0		1100100	1	0	80h	0	01h	1	

2943 F09

Figure 9. Reading the LTC2943-1 Accumulated Charge Registers (C, D)

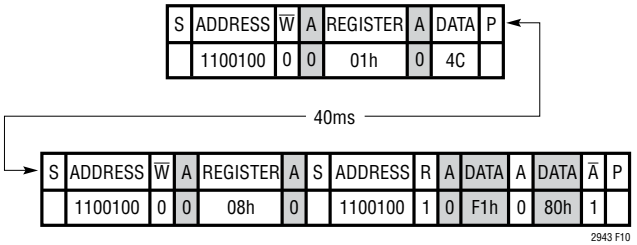


Figure 10. ADC Single Conversion Sequence and Reading of Voltage Registers (I,J)

The master initiates the ARA procedure with a START condition and the special 7-bit ARA bus address (0001100) followed by the read bit (R) = 1. If the LTC2943-1 is asserting the $\overline{ALCC}$ pin in alert mode, it acknowledges and responds by sending its 7-bit bus address (1100100) and a 1. While it is sending its address, it monitors the SDA pin to see if another device is sending an address at the same time using standard I^2C bus arbitration. If the LTC2943-1 is sending a 1 and reads a 0 on the SDA pin on the rising edge of SCL, it assumes another device with a lower address is sending and the LTC2943-1 immediately aborts its transfer and waits for the next ARA cycle to try again. If transfer is successfully completed, the LTC2943-1 will stop pulling down the $\overline{ALCC}$ pin and will not respond to further ARA requests until a new Alert event occurs.

Internal Sense Resistor

The internal sense resistor uses proprietary temperature compensation techniques to reduce the effective temperature coefficient to less than ±50 ppm/K typically. The effective sense resistance as seen by the coulomb counter is factory trimmed to 50mΩ. Both measures, and the lack of thermocouple effects in the sense resistor connections, contribute to the LTC2943-1's superior charge measurement accuracy compared to competing solutions employing a common 1% tolerance, 50ppm/K tempco discrete current sense resistor.

Like all sense resistors, the integrated sense resistor in the LTC2943-1 will exhibit minor long-term resistance shift. The resistance typically drops less than –0.1% per 1000h at 1A current and 85°C ambient temperature; this outperforms most types of discrete sense resistors except those of the *very high* and *ultrahigh* stability variety. See the Typical Performance Characteristics for expected resistor drift performance under worst-case conditions. Drift will be much slower at lower temperatures. Contact LTC applications for more information.

For most coulomb counter applications this aging behavior of the integrated sense resistor is insignificant compared to the change of battery capacity due to battery aging. The LTC2943-1 is factory trimmed to optimum accuracy when new; for applications which require the best possible coulomb count accuracy over the full product lifetime, the coulomb counter gain can be adjusted in software. For instance, if the error contribution of sense resistor drift must be limited to ±1%, coulomb counts may be biased high by 1% (use factor 1.01), and maximum operational temperature and current then must be derated such that sense resistor drift over product lifetime or calibration intervals is less than –2%.

Applications employing the standard external resistor LTC2943 with an external 50mΩ sense resistor may be upgraded to the pin-compatible LTC2943-1 by removing the external sense resistor.

APPLICATIONS INFORMATION

Voltage Drop Between SENSE+ and SENSE–

The LTC2943-1 is trimmed for an effective internal resistance of 50mΩ , but the total pin-to-pin resistance (R_{PP}), consisting of the sense resistor in series with pin and bond wire resistances, is somewhat higher. Assuming a sense resistor temperature coefficient of about 3900ppm/K, the total resistance between SENSE+ and SENSE– at a temperature T is typically:

$$R_{PP}(T) = R_{PP(TNOM)} [1 + 0.0039(T – T_{NOM})]$$

where T_{NOM} = 27°C (or 300K) and $R_{PP}(T_{NOM})$ is from the Electrical Characteristics table. This means that the resistance between SENSE+ and SENSE– may drop by 26% if die temperature changes from 27°C to –40°C or increase by 23% for a 27°C to 85°C die temperature change. Ensure that total voltage drop between SENSE+ and SENSE–, caused by maximum peak current flowing in/out of SENSE–:

$$V_{DROP} = I_{PEAK} • R_{PP}(T_{DIE(MAX)})$$

does not exceed the application's requirements.

Limiting Inrush Current

Inrush currents during events like battery insertion or closure of a mechanical power switch may be substantially higher than peak currents during normal operation. Extremely large inrush currents may require additional circuitry to keep currents through the LTC2943-1 sense resistor below the absolute maximum ratings.

Note that external Schottky clamp diodes between SENSE+ and SENSE– can leak significantly, especially at high temperature, which can cause significant coulomb counter errors. Preferred solutions to limit inrush current include active Hot Swap current limiting or connector designs that include current limiting resistance and staggered pins to ensure a low impedance connection when the connector is fully mated.

Power Dissipation

Power dissipation in the R_{PP} resistance when operated at high currents can increase the die temperature several degrees over ambient. Soldering the exposed pad of the DFN package to a large copper region on the PCB is recommended for applications operating close to the specified maximum current and ambient temperature. Die temperature at a given I_{SENSE} can be estimated by:

$$T_{DIE} = T_{AMB} + 1.22 • \theta_{JA} • R_{PP(MAX)} • I_{SENSE}^2$$

where the factor 1.22 approximates the effect of sense resistor self-heating, $R_{PP(MAX)}$ is the maximum pad-to-pad resistance at nominal temperature (27°C) and θ_{JA} is the thermal resistance from junction to ambient. The θ_{JA} data given for the DFN package is valid for typical PCB layouts; more precise θ_{JA} data for a particular PCB layout may be obtained by measuring the voltage V_{P-P} between SENSE+ and SENSE–, the ambient temperature T_{AMB}, and the die temperature T_{DIE}, and calculating:

$$\theta_{JA} = \frac{T_{DIE} - T_{AMB}}{V_{P-P} • I_{SENSE}}$$

Both T_{AMB} and T_{DIE} temperature may be measured using the internal temperature sensor included in the LTC2943-1. I_{SENSE} should be set to zero to measure T_{AMB}, and high enough during T_{DIE} measurement to achieve a significant temperature increase over T_{AMB}.

PC Board Layout Suggestions

Keep all traces as short as possible to minimize noise and inaccuracy. Use wider traces from the resistor to the battery, load and/or charger (see Figure 11). Put the bypass capacitor close to SENSE+.

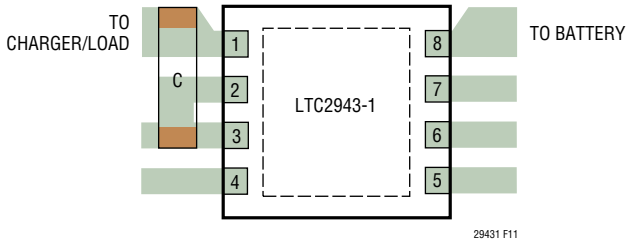
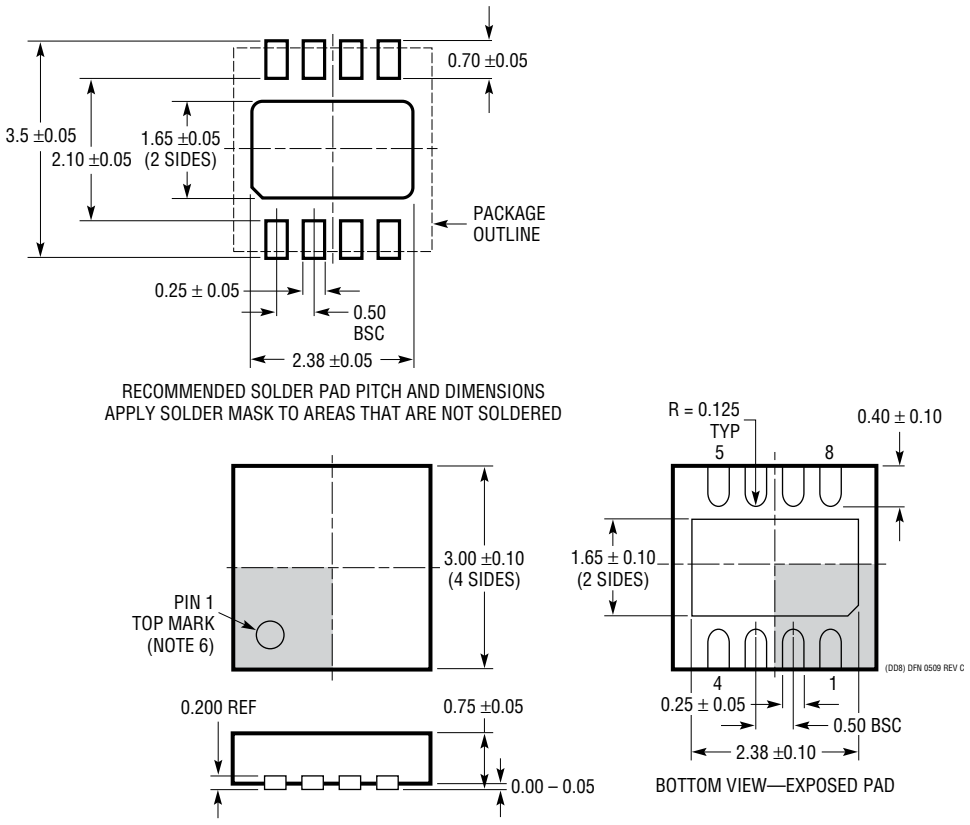


Figure 11. Recommended Layout

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC2943-1#packaging for the most recent package drawings.

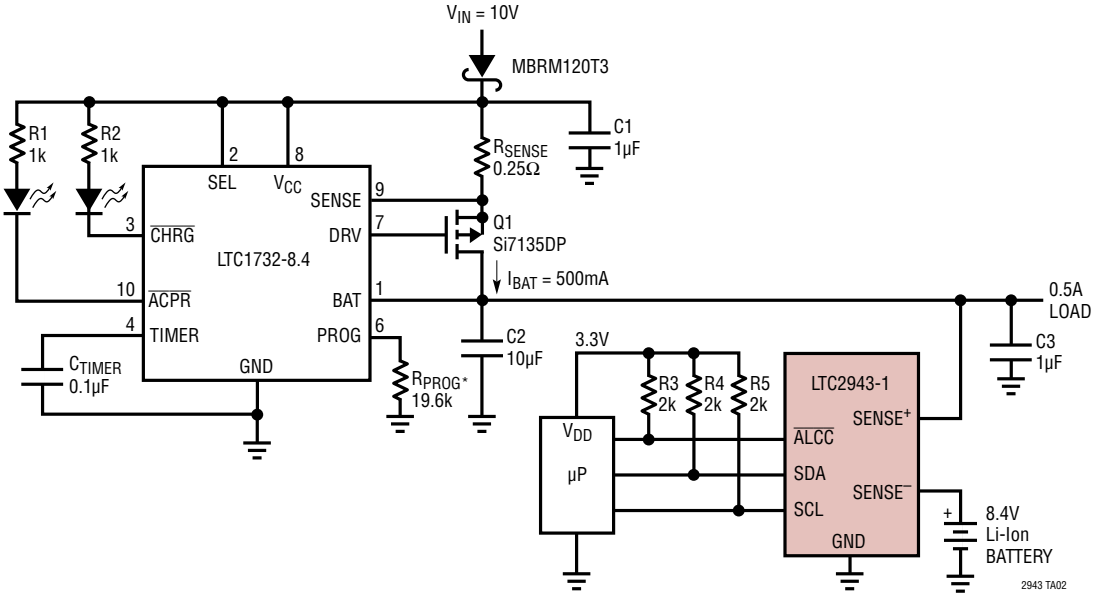
DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698 Rev C)



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

2-Cell 8.4V Linear Charger and Battery Gas Gauge



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Battery Gas Gauges		
LTC2941	Battery Gas Gauge with I²C Interface	2.7V to 5.5V Operation, 6-Lead (2mm × 3mm) DFN Package
LTC2941-1	1A I²C Battery Gas Gauge with Internal Sense Resistor	2.7V to 5.5V Operation, 6-Lead (2mm × 3mm) DFN Package
LTC2942	I²C Battery Gas Gauge with Temperature/Voltage Measurement	2.7V to 5.5V Operation, 14-Bit ΔΣ-ADC, 6-Lead (2mm × 3mm) DFN Package
LTC2942-1	1A I²C Battery Gas Gauge with Internal Sense Resistor and Temperature/Voltage Measurement	2.7V to 5.5V Operation, 14-Bit ΔΣ-ADC, 6-Lead (2mm × 3mm) DFN Package
LTC2943	Battery Gas Gauge with I²C Interface and Voltage, Current and Temperature ADC	3.6V to 20V Operation, 14-Bit ΔΣ-ADC, Pin Compatible with LTC2944, LTC2943-1, or LTC2943, 8-Lead (3mm × 3mm) DFN Package
LTC4150	Coulomb Counter/Battery Gas Gauge	2.7V to 8.5V Operation, 10-Pin MSOP Package
Battery Chargers		
LTC4000	High Voltage High Current Controller for Battery Charging and Power Management	3V to 60V Operation, 28-Lead (4mm × 5mm) QFN or SSOP Packages
LTC4009	High Efficiency, Multi-Chemistry Battery Charger	6V to 28V Operation, 20-Lead (4mm × 4mm) QFN Package
LTC4012	High Efficiency, Multi-Chemistry Battery Charger with PowerPath™ Control	6V to 28V Operation, 20-Lead (4mm × 4mm) QFN Package
LT3652HV	Power Tracking 2A Battery Charger	Input Supply Voltage Regulation Loop for Peak Power Tracking, 5V to 34V Operation, 1MHz, 2A Charge Current, 3mm × 3mm DFN-12 and MSOP-12 Packages
LTC1732	Li-Ion Battery Charger	4.5V to 12V Operation, MSOP-10 Package

OUR CERTIFICATE

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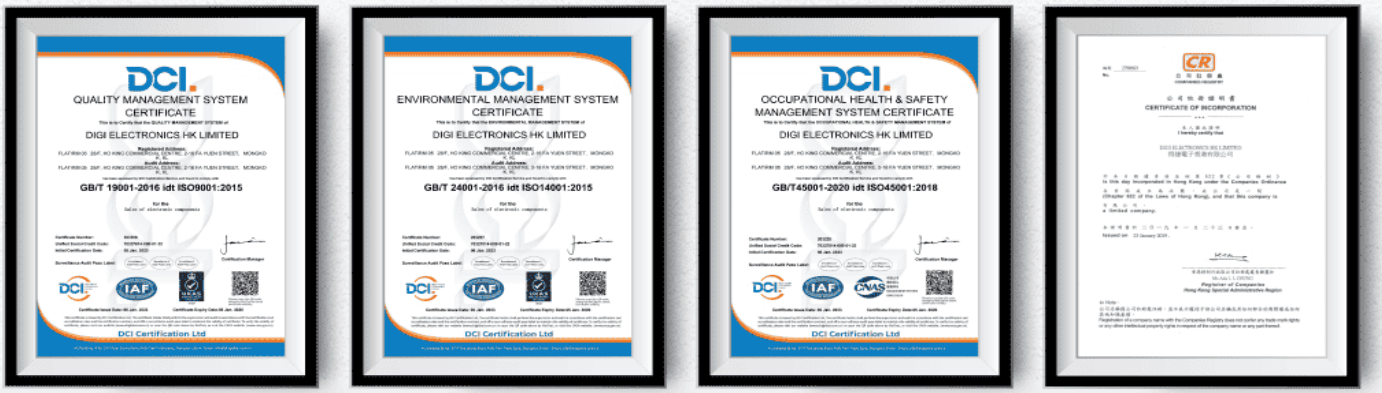

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