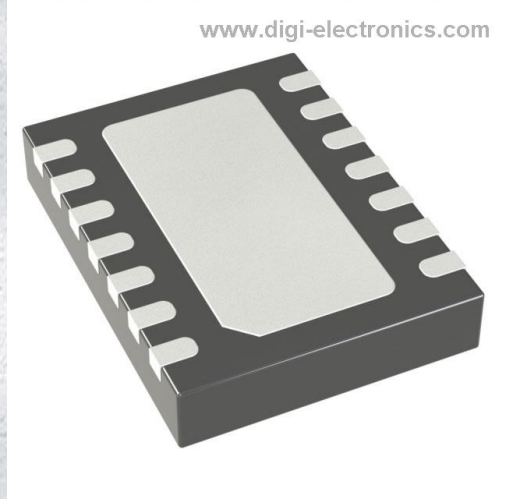
LTC3260IDE#PBF Datasheet



https://www.DiGi-Electronics.com

DiGi Electronics Part Number	LTC3260IDE#PBF-DG
Manufacturer	Analog Devices Inc.
Manufacturer Product Number	LTC3260IDE#PBF
Description	IC REG CHARGE PUMP INV 14DFN
Detailed Description	PMIC - Voltage Regulators - Linear Switching 1 Output Charge Pump 50kHz ~ 500kHz 14-DFN (4x3)

This model LTC3260IDE#PBF is available at DiGi Electronics.

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Manufacturer Product Number:	Manufacturer:
LTC3260IDE#PBF	Analog Devices Inc.
Series:	Product Status:
-	Active
Topology:	Number of Outputs:
Charge Pump	1
Frequency - Switching:	Voltage/Current - Output 1:
50kHz ~ 500kHz	Adj, 100mA
Voltage/Current - Output 2:	Voltage/Current - Output 3:
-	-
w/LED Driver:	w/Supervisor:
No	No
w/Sequencer:	Voltage - Supply:
No	4.5V ~ 32V
Operating Temperature:	Mounting Type:
-40°C ~ 125°C (TJ)	Surface Mount
Package / Case:	Supplier Device Package:
14-WFDFN Exposed Pad	14-DFN (4x3)
Base Product Number:	
LTC3260	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8542.39.0001	

ANALOG DEVICES | ADI Power by Linear™

LTC3260

Low Noise Dual Supply Inverting Charge Pump

FEATURES

- **V_{IN} Range: 4.5V to 32V**
- **Inverting Charge Pump Generates $-V_{IN}$**
- **Charge Pump Output Current Up to 100mA**
- **Low Noise Negative LDO Post Regulator**
- **(I_{LDO}^- = 50mA Max)**
- **Low Noise Independent Positive LDO Regulator**
- **(I_{LDO}^+ = 50mA Max)**
- **100µA Quiescent Current in Burst Mode® Operation with Both LDO Regulators On**
- 50kHz to 500kHz Programmable Oscillator Frequency
- Stable with Ceramic Capacitors
- Short-Circuit/Thermal Protection
- Low Profile 3mm × 4mm 14-Pin DFN and Thermally Enhanced 16-Pin MSOP Packages
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Low Noise Bipolar/Inverting Supplies
- Industrial/Instrumentation Low Noise Bias Generators
- Portable Medical Equipment
- Portable Instruments

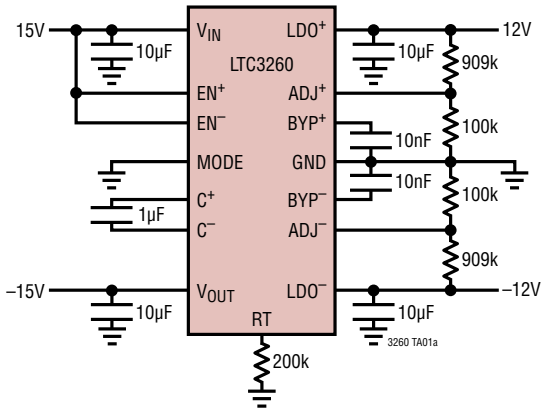
DESCRIPTION

The LTC®3260 is a low noise dual polarity output power supply that includes an inverting charge pump with both positive and negative LDO regulators. The charge pump operates over a wide 4.5V to 32V input range and can deliver up to 100mA of output current. Each LDO regulator can provide up to 50mA of output current. The negative LDO post regulator is powered from the charge pump output. The LDO output voltages can be adjusted using external resistor dividers.

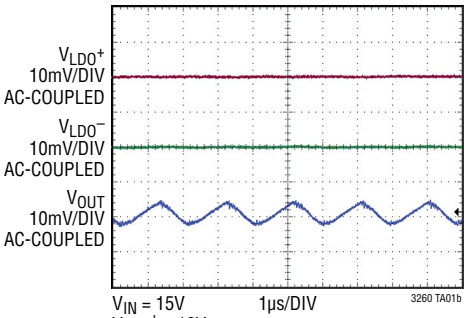
The charge pump employs either low quiescent current Burst Mode operation or low noise constant frequency mode. In Burst Mode operation the charge pump V_{OUT} regulates to $-0.94 \bullet V_{IN}$, and the LTC3260 draws only 100µA of quiescent current with both LDO regulators on. In constant frequency mode the charge pump produces an output equal to $-V_{IN}$ and operates at a fixed 500kHz or to a programmed value between 50kHz to 500kHz using an external resistor. The LTC3260 is available in low profile (0.75mm) 3mm x 4mm 14-pin DFN and thermally enhanced 16-pin MSOP packages.

TYPICAL APPLICATION

±12V Outputs from a Single 15V Input



LDO Rejection of V_{OUT} Ripple

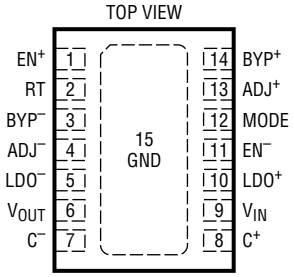


ABSOLUTE MAXIMUM RATINGS (Notes 1, 3)

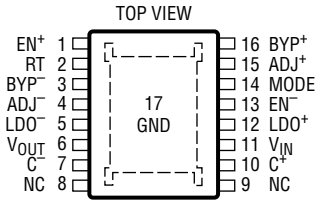
V_{IN}, EN^+, EN^-, MODE.. ..... –0.3V to 36V
LDO^+ ..... –16V to 36V
V_{OUT}, LDO^- ..... –36V to 0.3V
RT, ADJ^+ ..... –0.3V to 6V
BYP^+ ..... –0.3V to 2.5V
ADJ^- ..... –6V to 0.3V
BYP^- ..... –2.5V to 0.3V

V_{OUT}, LDO^+, LDO^- Short-Circuit Duration ..... Indefinite
Operating Junction Temperature Range
(Note 2)..... –55°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
MSE Only..... 300°C

PIN CONFIGURATION



DE PACKAGE
14-LEAD (4mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 15) IS GND, MUST BE SOLDERED TO PCB



MSE PACKAGE
16-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3260EDE#PBF	LTC3260EDE#TRPBF	3260	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3260IDE#PBF	LTC3260IDE#TRPBF	3260	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3260EMSE#PBF	LTC3260EMSE#TRPBF	3260	16-Lead Plastic MSOP	–40°C to 125°C
LTC3260IMSE#PBF	LTC3260IMSE#TRPBF	3260	16-Lead Plastic MSOP	–40°C to 125°C
LTC3260HMSE#PBF	LTC3260HMSE#TRPBF	3260	16-Lead Plastic MSOP	–40°C to 150°C
LTC3260MPMSE#PBF	LTC3260MPMSE#TRPBF	3260	16-Lead Plastic MSOP	–55°C to 150°C
AUTOMOTIVE PRODUCTS**				
LTC3260HMSE#WPBF	LTC3260HMSE#WTRPBF	3260	16-Lead Plastic MSOP	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = EN^+ = EN^- = 12V, MODE = 0V, RT = 200kΩ.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Charge Pump							
V_{IN}	Input Voltage Range		●	4.5		32	V
V_{UVLO}	V_{IN} Undervoltage Lockout Threshold	V_{IN} Rising V_{IN} Falling	● ●	 3.4	3.8 3.6	4	V V
I_{VIN}	V_{IN} Quiescent Current	Shutdown, EN^+ = EN^- = 0V EN^- = 0V, $I_{LDO}{}^+$ = 0mA MODE = V_{IN}, EN^+ = 0V, I_{VOUT} = $I_{LDO}{}^-$ = 0mA MODE = V_{IN}, I_{VOUT} = $I_{LDO}{}^+$ = $I_{LDO}{}^-$ = 0mA MODE = 0V, I_{VOUT} = 0mA			2 30 80 100 3.5	5 50 160 200 5.5	µA µA µA µA mA
V_{RT}	RT Regulation Voltage				1.200		V
V_{OUT}	V_{OUT} Regulation Voltage	MODE = 12V MODE = 0V			–0.94 • V_{IN} $–V_{IN}$		V V
f_{OSC}	Oscillator Frequency	RT = GND		450	500	550	kHz
R_{OUT}	Charge Pump Output Impedance	MODE = 0V, RT = GND			32		Ω
I_{SHORT_CKT}	Max I_{VOUT} Short-Circuit Current	V_{OUT} = GND	●	100	160	250	mA
$V_{MODE(H)}$	MODE Threshold Rising		●		1.1	2.0	V
$V_{MODE(L)}$	MODE Threshold Falling		●	0.4	1.0		V
I_{MODE}	MODE Pin Internal Pull-Down Current	V_{IN} = MODE = 32V			0.7		µA
50mA Positive Regulator							
	LDO^+ Output Voltage Range		●	1.2		32	V
$V_{ADJ}{}^+$	ADJ^+ Reference Voltage		●	1.176	1.200	1.224	V
$I_{ADJ}{}^+$	ADJ+ Input Current	$V_{ADJ}{}^+$ = 1.2V		–50		50	nA
$I_{LDO}{}^+{}_{(SC)}$	LDO^+ Short-Circuit Current		●	50	100		mA
	Line Regulation				0.04		mV/V
	Load Regulation				0.03		mV/mA
$V_{DROPOUT}{}^+$	LDO^+ Dropout Voltage	$I_{LDO}{}^+$ = 50mA			400	800	mV
	Output Voltage Noise	$C_{BYP}{}^+$ = 10nF			100		$µV_{RMS}$
$V_{EN}{}^+{}_{(H)}$	EN^+ Threshold Rising		●		1.1	2.0	V
$V_{EN}{}^+{}_{(L)}$	EN^+ Threshold Falling		●	0.4	1.0		V
$I_{EN}{}^+$	EN^+ Pin Internal Pull-Down Current	V_{IN} = EN^+ = 32V			0.7		µA
50mA Negative Regulator							
	LDO^- Output Voltage Range		●	–32		–1.2	V
$V_{ADJ}{}^-$	ADJ^- Reference Voltage		●	–1.224	–1.200	–1.176	V
$I_{ADJ}{}^-$	ADJ^- Input Current	$V_{ADJ}{}^-$ = –1.2V		–50		50	nA
$I_{LDO}{}^-{}_{(SC)}$	LDO^- Short-Circuit Current		●	50	100		mA
	Line Regulation				0.002		mV/V
	Load Regulation				0.02		mV/mA
$V_{DROPOUT}{}^-$	LDO^- Dropout Voltage	$I_{LDO}{}^-$ = 50mA			200	500	mV
	Output Voltage Noise	$C_{BYP}{}^-$ = 10nF			100		$µV_{RMS}$
$V_{EN(H)}$	EN^- Threshold Rising		●		1.1	2.0	V
$V_{EN(L)}$	EN^- Threshold Falling		●	0.4	1.0		V
$I_{EN}{}^-$	EN^- Pin Internal Pull-Down Current	V_{IN} = EN^- = 32V			1.4		µA

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3260 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3260E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3260I is guaranteed over the –40°C to 125°C operating junction temperature range, the LTC3260H is guaranteed over the –40°C to 150°C operating junction temperature range and the LTC3260MP is tested and guaranteed over the full –55°C to 150°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA}),$$

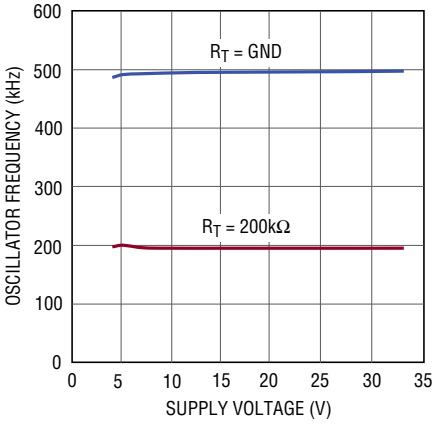
where θ_{JA} = 43°C/W is the package thermal impedance.

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperatures will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

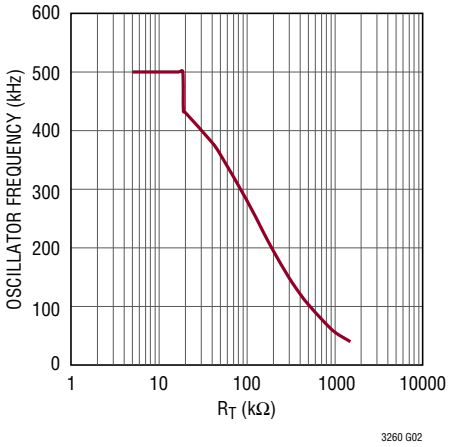
TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C, C_{FLY} = 1µF, C_{IN} = C_{OUT} = C_{LDO}^+ = C_{LDO}^- = 10µF unless otherwise noted)

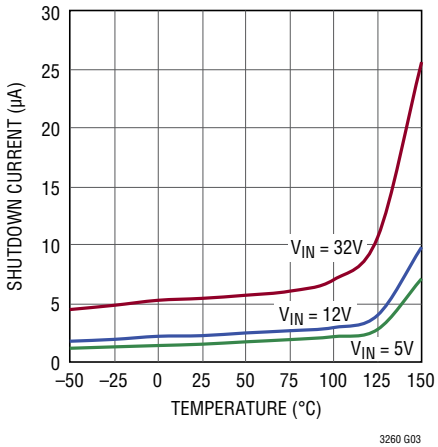
Oscillator Frequency vs Supply Voltage



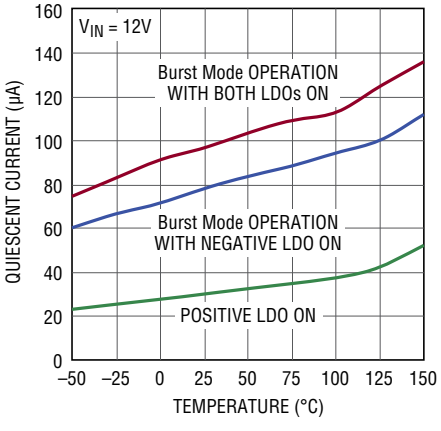
Oscillator Frequency vs R_T



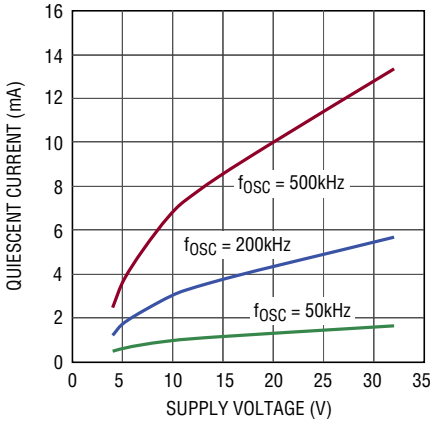
Shutdown Current vs Temperature



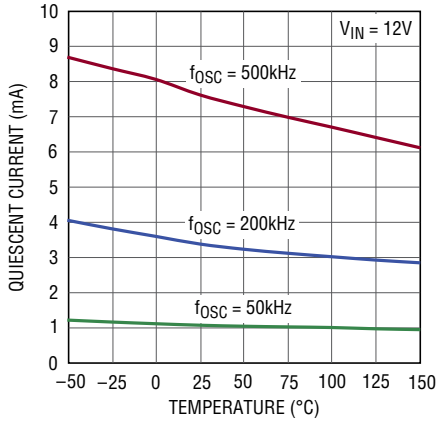
Quiescent Current vs Temperature



Quiescent Current vs Supply Voltage (Constant Frequency Mode)



Quiescent Current vs Temperature (Constant Frequency Mode)

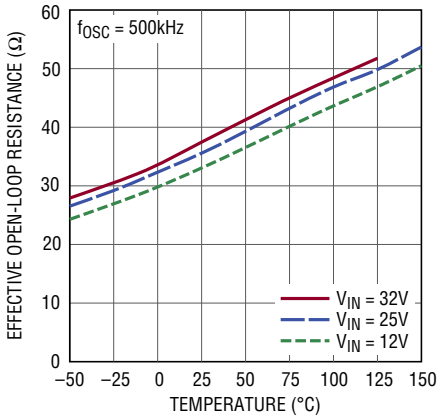


Rev. B

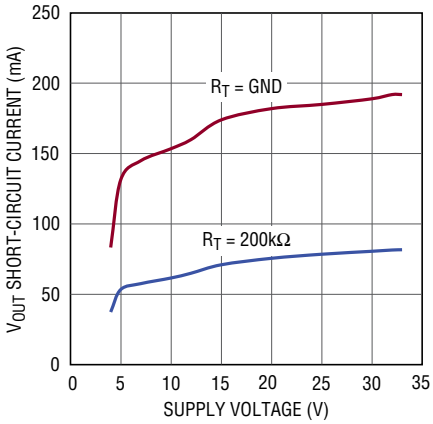
TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C, C_{FLY} = 1µF, C_{IN} = C_{OUT} = C_{LDO^+} = C_{LDO^-} = 10µF unless otherwise noted)

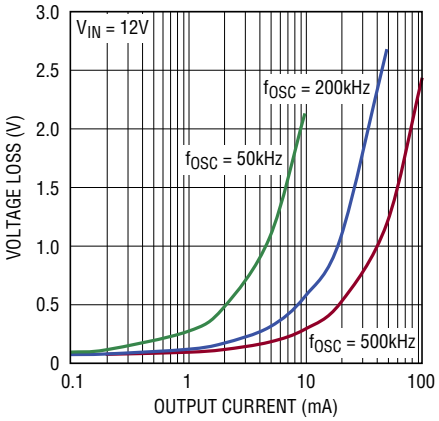
Effective Open-Loop Resistance vs Temperature



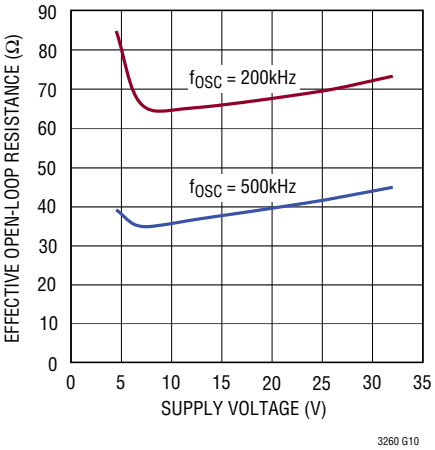
V_{OUT} Short-Circuit Current vs Supply Voltage



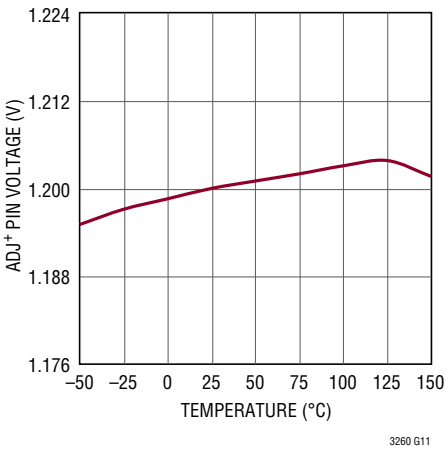
Voltage Loss (V_{IN} – $|V_{OUT}|$) vs Output Current (Constant Frequency Mode)



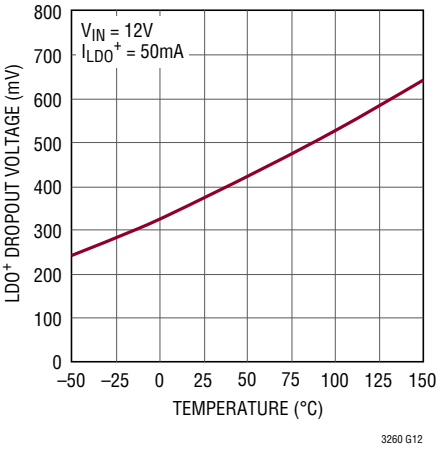
Effective Open-Loop Resistance vs Supply Voltage



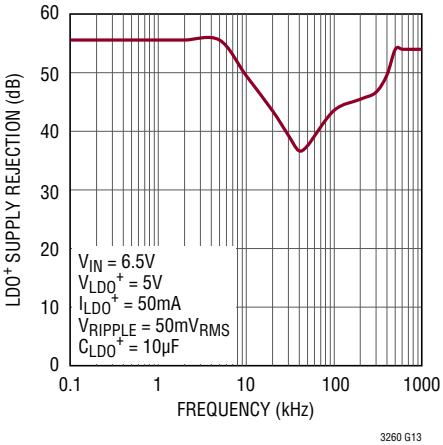
ADJ⁺ Pin Voltage vs Temperature



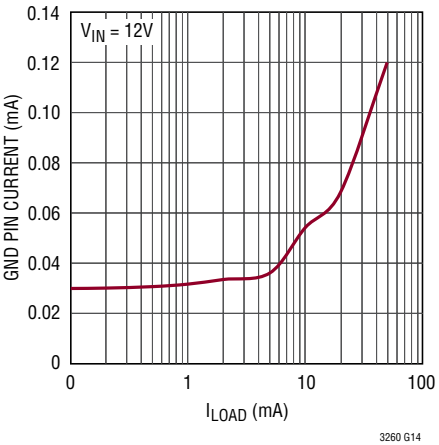
LDO⁺ Dropout Voltage vs Temperature



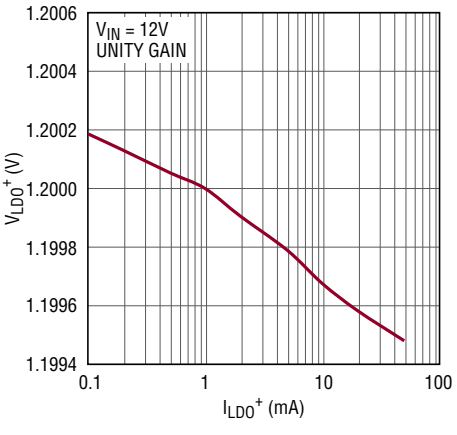
LDO⁺ Supply Rejection



LDO⁺ GND Pin Current vs I_{LOAD}



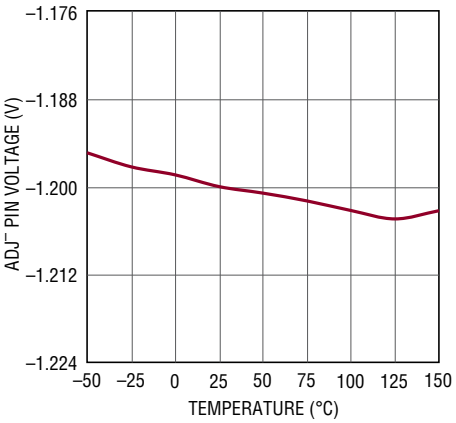
LDO⁺ Load Regulation



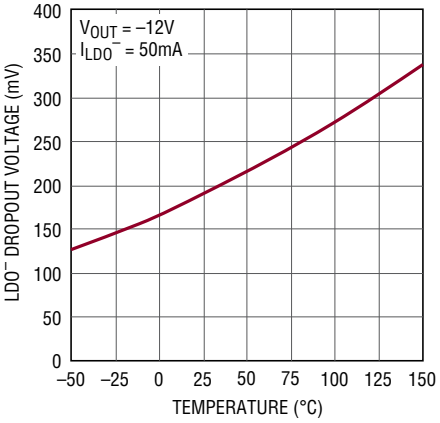
TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C, C_{FLY} = 1µF, C_{IN} = C_{OUT} = C_{LDO^+} = C_{LDO^-} = 10µF unless otherwise noted)

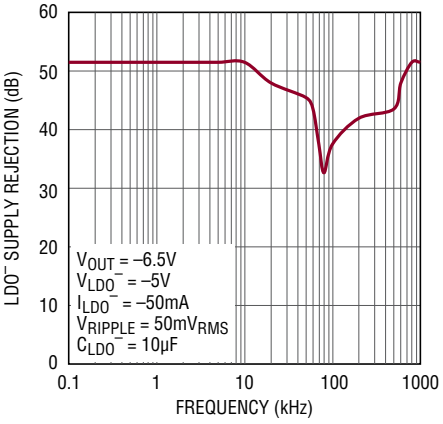
ADJ⁻ Pin Voltage vs Temperature



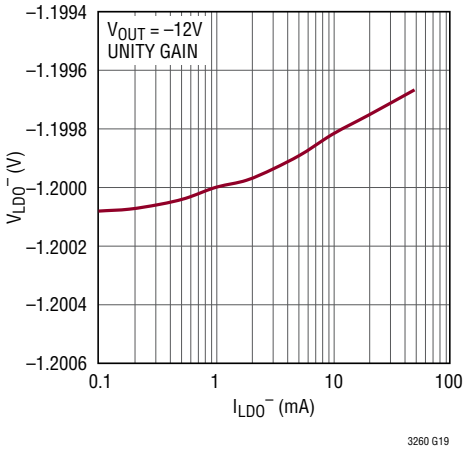
LDO⁻ Dropout Voltage vs Temperature



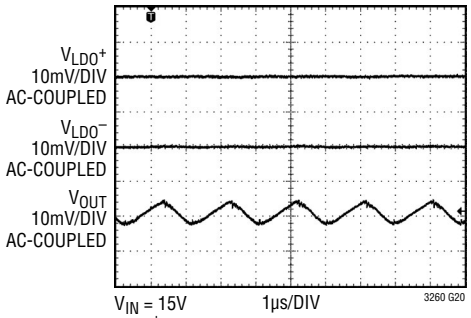
LDO⁻ Power Supply Rejection



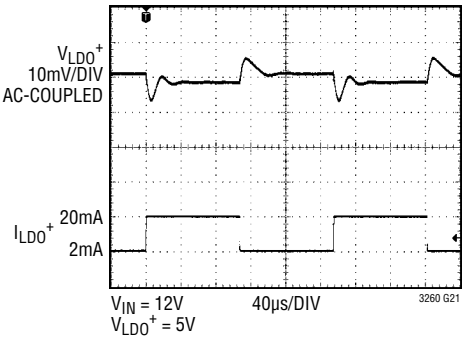
LDO⁻ Load Regulation



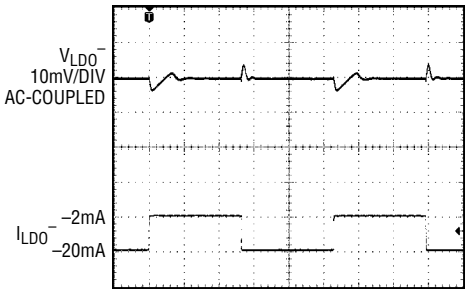
LDO Rejection of V_{OUT} Ripple



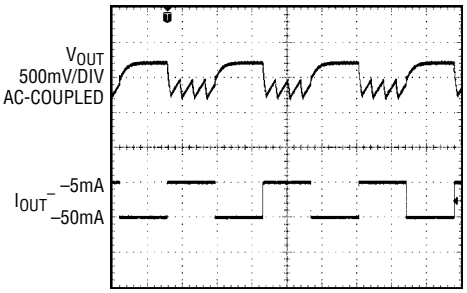
LDO⁺ Load Transient



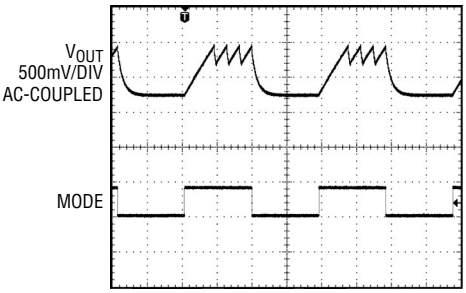
LDO⁻ Load Transient



V_{OUT} Transient (Burst Mode Operation, MODE = H)



V_{OUT} Transient (MODE = Low to High)



PIN FUNCTIONS (DFN/MSOP)

EN^+ (Pin 1/Pin 1): Logic Input. A logic "high" on the EN^+ pin enables the positive low dropout (LDO^+) regulator.

RT (Pin 2/Pin 2): Input Connection for Programming the Switching Frequency. The RT pin servos to a fixed 1.2V when the EN^- pin is driven to a logic "high". A resistor from RT to GND sets the charge pump switching frequency. If the RT pin is tied to GND, the switching frequency defaults to a fixed 500kHz.

BYP^- (Pin 3/Pin 3): LDO^- Reference Bypass Pin. Connect a capacitor from BYP^- to GND to reduce LDO^- output noise. Leave floating if unused.

ADJ^- (Pin 4/Pin 4): Feedback Input for the Negative Low Dropout Regulator. This pin servos to a fixed voltage of –1.2V when the control loop is complete.

LDO^- (Pin 5/Pin 5): Negative Low Dropout (LDO^-) Linear Regulator Output. This pin requires a low ESR (equivalent series resistance) capacitor with at least 2µF capacitance to ground for stability.

V_{OUT} (Pin 6/Pin 6): Charge Pump Output Voltage. In constant frequency mode (MODE = low) this pin is driven to $–V_{IN}$. In Burst Mode operation, (MODE = high) this pin voltage is regulated to $–0.94 • V_{IN}$ using an internal burst comparator with hysteretic control.

C^- (Pin 7/Pin 7): Flying Capacitor Negative Connection.

C^+ (Pin 8/Pin 10): Flying Capacitor Positive Connection.

NC (Pins 8, 9 MSOP Only): No Connect. These pins are not connected to the LTC3260 die. These pins should be left floating, connected to ground or shorted to adjacent pins.

V_{IN} (Pin 9/Pin 11): Input Voltage for Both Charge Pump and Positive Low Dropout (LDO^+) Regulator. V_{IN} should be bypassed with a low impedance ceramic capacitor.

LDO^+ (Pin 10/Pin 12): Positive Low Dropout (LDO^+) Output. This pin requires a low ESR capacitor with at least 2µF capacitance to ground for stability.

EN^- (Pin 11/Pin 13): Logic Input. A logic "high" on the EN^- pin enables the inverting charge pump as well as the negative LDO regulator.

MODE (Pin 12/Pin 14): Logic Input. The MODE pin determines the charge pump operating mode. A logic "high" on the MODE pin forces the charge pump to operate in Burst Mode operation regulating V_{OUT} to approximately $–0.94 • V_{IN}$ with hysteretic control. A logic "low" on the MODE pin forces the charge pump to operate as an open-loop inverter with a constant switching frequency. The switching frequency in both modes is determined by an external resistor from the RT pin to GND. In Burst Mode operation, this represents the frequency of the burst cycles before the part enters the low quiescent current sleep state.

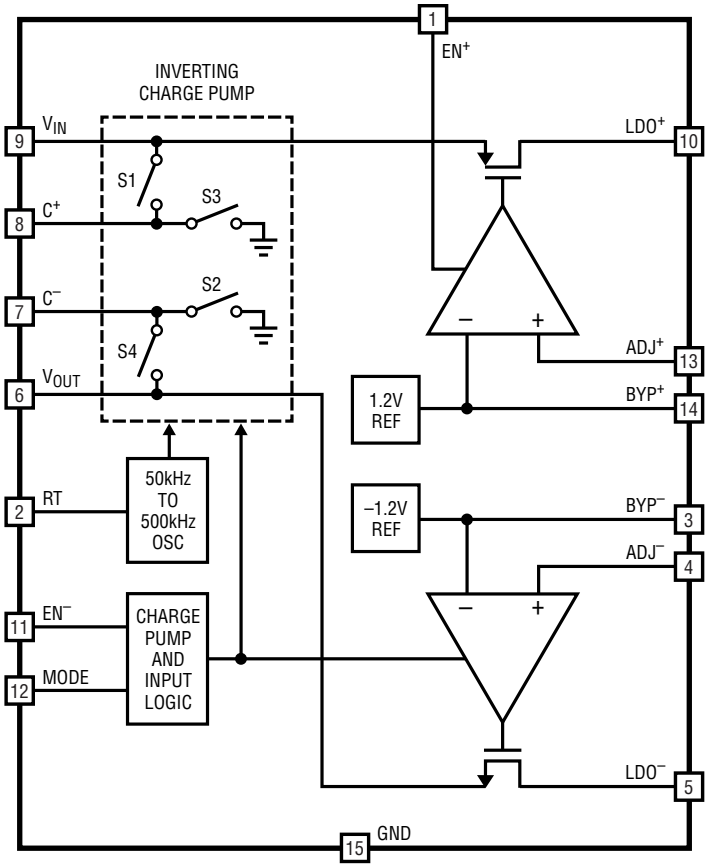
ADJ^+ (Pin 13/Pin 15): Feedback Input for the Positive Low Dropout (LDO^+) Regulator. This pin servos to a fixed voltage of 1.2V when the control loop is complete.

BYP^+ (Pin 14/Pin 16): LDO^+ Reference Bypass Pin. Connect a capacitor from BYP^+ to GND to reduce LDO^+ output noise. Leave floating if unused.

GND (Exposed Pad Pin 15/Exposed Pad Pin 17): Ground. The exposed package pad is ground and must be soldered to the PC board ground plane for proper functionality and for rated thermal performance.

BLOCK DIAGRAM

Note: Pin numbers are as per DFN package. Refer to the Pin Functions section for corresponding MSOP pin numbers.



OPERATION (Refer to the Operation)

The LTC3260 is a high voltage low noise dual output regulator. It includes an inverting charge pump and two LDO regulators to generate bipolar low noise supply rails from a single positive input. It supports a wide input power supply range from 4.5V to 32V.

Shutdown Mode

In shutdown mode, all circuitry except the internal bias is turned off. The LTC3260 is in shutdown when a logic low is applied to both the enable inputs (EN^+ and $EN^–$). The LTC3260 only draws 2µA (typical) from the V_{IN} supply in shutdown.

Charge Pump Constant Frequency Operation

The LTC3260 provides low noise constant frequency operation when a logic low is applied to the MODE pin. The charge pump and oscillator circuit are enabled using the $EN^–$ pin. At the beginning of a clock cycle, switches S1 and S2 are closed. The external flying capacitor across the C^+ and $C^–$ pins is charged to the V_{IN} supply. In the second phase of the clock cycle, switches S1 and S2 are opened, while switches S3 and S4 are closed. In this configuration the C^+ side of the flying capacitor is grounded and charge is delivered through the $C^–$ pin to V_{OUT}. In steady state the V_{OUT} pin regulates at $–V_{IN}$ less any voltage drop due to the load current on V_{OUT} or LDO.

OPERATION (Refer to the Block Diagram)

The charge transfer frequency can be adjusted between 50kHz and 500kHz using an external resistor on the RT pin. At slower frequencies the effective open-loop output resistance (R_{OL}) of the charge pump is larger and it is able to provide smaller average output current. Figure 1 can be used to determine a suitable value of RT to achieve a required oscillator frequency. If the RT pin is grounded, the part operates at a constant frequency of 500kHz.

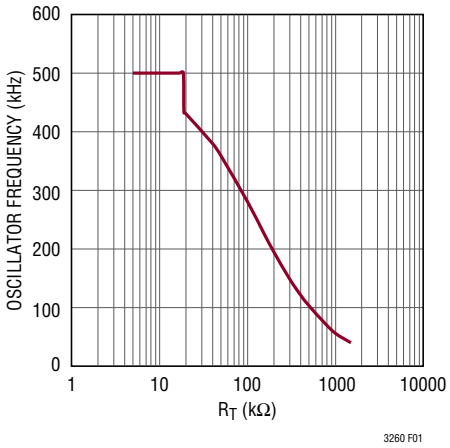


Figure 1. Oscillator Frequency vs R_T

Charge Pump Burst Mode Operation

The LTC3260 provides low power Burst Mode operation when a logic high is applied to the MODE pin. In Burst Mode operation, the charge pump charges the V_{OUT} pin to –0.94 • V_{IN} (typical). The part then shuts down the internal oscillator to reduce switching losses and goes into a low current state. This state is referred to as the sleep state in which the IC consumes only about 100µA with both LDOs enabled. When the output voltage droops enough to overcome the burst comparator hysteresis, the part wakes up and commences charge pump cycles until output voltage exceeds –0.94 • V_{IN} (typical). This mode provides lower operating current at the cost of higher output ripple and is ideal for light load operation.

The frequency of charging cycles is set by the external resistor on the RT pin. The charge pump has a lower R_{OL} at higher frequencies. For Burst Mode operation it is recommended that the RT pin be tied to GND. This minimizes the charge pump R_{OL}, quickly charges the output up to the burst threshold and optimizes the duration of the low current sleep state.

Charge Pump Soft-Start

The LTC3260 has built in soft-start circuitry to prevent excessive current flow during start-up. The soft-start is achieved by internal circuitry that slowly ramps the amount of current available at the output storage capacitor. The soft-start circuitry is reset in the event of a commanded shutdown or thermal shutdown.

Charge Pump Short-Circuit/Thermal Protection

The LTC3260 has built-in short-circuit current limit as well as overtemperature protection. During a short-circuit condition, the part automatically limits its output current to approximately 160mA. If the junction temperature exceeds approximately 175°C the thermal shutdown circuitry disables current delivery to the output. Once the junction temperature drops back to approximately 165°C current delivery to the output is resumed. When thermal protection is active the junction temperature is beyond the specified operating range. Thermal protection is intended for momentary overload conditions outside normal operation. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Positive Low Dropout Linear Regulator (LDO+)

The positive low dropout regulator (LDO+) supports a load of up to 50mA. The LDO+ takes power from the V_{IN} pin and drives the LDO+ output pin to a voltage programmed by the resistor divider connected between the LDO+, ADJ+ and GND pins. For stability, the LDO+ output must be bypassed to ground with a low ESR ceramic capacitor that maintains a capacitance of at least 2µF across operating temperature and voltage.

The LDO+ is enabled or disabled via the EN+ logic input pin. When the LDO+ is enabled, a soft-start circuit ramps its regulation point from zero to the final value over a period of 75µs, reducing the inrush current on V_{IN}.

OPERATION (Refer to the Operation)

Figure 2 shows the LDO+ regulator application circuit. The LDO+ output voltage V_{LDO}^+ can be programmed by choosing suitable values of R1 and R2 such that:

$$V_{LDO}^+ = 1.2V \bullet \left(\frac{R1}{R2} + 1\right)$$

An optional capacitor of 10nF can be connected from the BYP+ pin to ground. This capacitor bypasses the internal 1.2V reference of the LTC3260 and improves the noise performance of the LDO+. If this function is not used the BYP+ pin should be left floating.

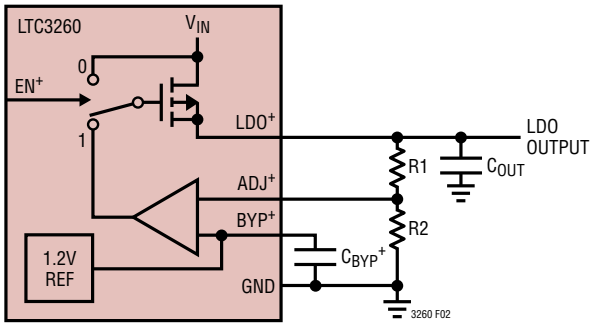


Figure 2. Positive LDO Application Circuit

Negative Low Dropout Linear Regulator (LDO–)

The negative low dropout regulator (LDO–) supports a load of up to 50mA. The LDO– takes power from the V_{OUT} pin (output of the inverting charge pump) and drives the LDO– output pin to a voltage programmed by the resistor divider connected between the LDO–, ADJ– and GND pins. For stability, the LDO– output must be bypassed to ground with a low ESR ceramic capacitor that maintains a capacitance of at least 2µF across operating temperature and voltage.

The LDO– is enabled or disabled via the EN– logic input pin. Initially, when the EN– logic input is low, the charge pump circuitry is disabled and the V_{OUT} pin is at GND. When EN– is switched high, the V_{OUT} pin will be driven negative by the charge pump circuitry. Soft-start circuitry in the charge pump also provides soft-start functionality for the LDO– and prevents excessive inrush currents.

Figure 3 shows the LDO– regulator application circuit. The LDO– output voltage V_{LDO}^- can be programmed by choosing suitable values of R1 and R2 such that:

$$V_{LDO}^- = -1.2V \bullet \left(\frac{R1}{R2} + 1\right)$$

When the inverting charge pump is in Burst Mode operation (MODE = high), the typical hysteresis on the V_{OUT} pin is 2% of V_{IN} voltage. The LDO– voltage should be set high enough above V_{OUT} in order to prevent LDO– from entering dropout during normal operation.

An optional capacitor of 10nF can be connected from the BYP– pin to ground. This capacitor bypasses the internal –1.2V reference of the LTC3260 and improves the noise performance of the LDO–. If this function is not used the BYP– pin should be left floating.

In order to improve transient response, an optional capacitor, C_{ADJ}^-, may be used as shown in Figure 3. A recommended value for C_{ADJ}^- is 10pF. Experimentation with capacitor values between 2pF and 22pF may yield improved transient response.

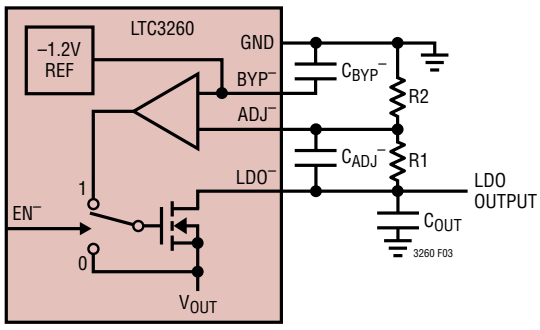


Figure 3. Negative LDO Application Circuit

APPLICATIONS INFORMATION

Effective Open-Loop Output Resistance

The effective open-loop output resistance (R_{OL}) of a charge pump is a very important parameter which determines the strength of the charge pump. The value of this parameter depends on many factors such as the oscillator frequency (f_{OSC}), value of the flying capacitor (C_{FLY}), the nonoverlap time, the internal switch resistances (R_S) and the ESR of the external capacitors.

Typical R_{OL} values as a function of temperature are shown in Figure 4.

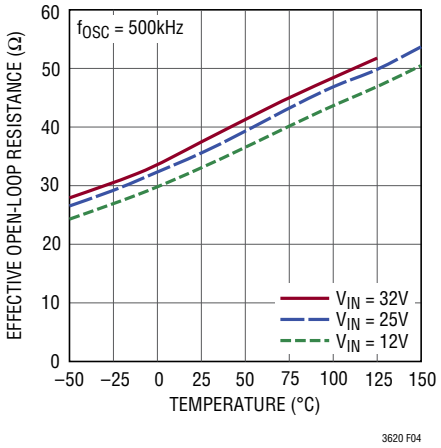


Figure 4. Typical R_{OL} vs Temperature

Input/Output Capacitor Selection

The style and value of capacitors used with the LTC3260 determine several important parameters such as regulator control loop stability, output ripple, charge pump strength and minimum turn-on time. To reduce noise and ripple, it is recommended that low ESR ceramic capacitors be used for the charge pump and LDO outputs. All capacitors should retain at least 2µF of capacitance over operating temperature and bias voltage. Tantalum and aluminum capacitors can be used in parallel with a ceramic capacitor to increase the total capacitance but should not be used alone because of their high ESR. In constant frequency mode, the value of C_{OUT} directly controls the amount of output ripple for a given load current. Increasing the size of C_{OUT} will reduce the output ripple at the expense of higher minimum turn-on time. The peak-to-peak output ripple at the V_{OUT} pin is approximately given by the expression:

$$V_{RIPPLE(P-P)} \approx \frac{I_{OUT}}{C_{OUT}}\left[\frac{1}{f_{OSC}} - t_{ON}\right]$$

where C_{OUT} is the value of the output capacitor, f_{OSC} is the oscillator frequency and t_{ON} is the on-time of the oscillator (1µs typical).

Just as the value of C_{OUT} controls the amount of output ripple, the value of C_{IN} controls the amount of ripple present at the input (V_{IN}) pin. The amount of bypass capacitance required at the input depends on the source impedance driving V_{IN}. For best results it is recommended that V_{IN} be bypassed with at least 2µF of low ESR capacitance. A high ESR capacitor such as tantalum or aluminum will have higher input noise than a low ESR ceramic capacitor. Therefore, a ceramic capacitor is recommended as the main bypass capacitance with a tantalum or aluminum capacitor used in parallel if desired.

Flying Capacitor Selection

The flying capacitor controls the strength of the charge pump. A 1µF or greater ceramic capacitor is suggested for the flying capacitor for applications requiring the full rated output current of the charge pump.

For very light load applications, the flying capacitor may be reduced to save space or cost. For example, a 0.2µF capacitor might be sufficient for load currents up to 20mA. A smaller flying capacitor leads to a larger effective open-loop resistance (R_{OL}) and thus limits the maximum load current that can be delivered by the charge pump.

Ceramic Capacitors

Ceramic capacitors of different materials lose their capacitance with higher temperature and voltage at different rates. For example, a capacitor made of X5R or X7R material will retain most of its capacitance from –40°C to 85°C whereas a Z5U or Y5V style capacitor will lose

APPLICATIONS INFORMATION

considerable capacitance over that range. Z5U and Y5V capacitors may also have a poor voltage coefficient causing them to lose 60% or more of their capacitance when the rated voltage is applied. Therefore when comparing different capacitors, it is often more appropriate to compare the amount of achievable capacitance for a given case size rather than discussing the specified capacitance value. The capacitor manufacture's data sheet should be consulted to ensure the desired capacitance at all temperatures and voltages. Table 1 is a list of ceramic capacitor manufacturers and their websites.

Table 1.

AVX	www.avxcorp.com
Kemet	www.kemet.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com
Vishay	www.vishay.com
TDK	www.component.tdk.com

Layout Considerations

Due to high switching frequency and high transient currents produced by LTC3260, careful board layout is necessary for optimum performance. A true ground plane and short connections to all the external capacitors will improve performance and ensure proper regulation under all conditions. Figure 5 shows an example layout for the LTC3260.

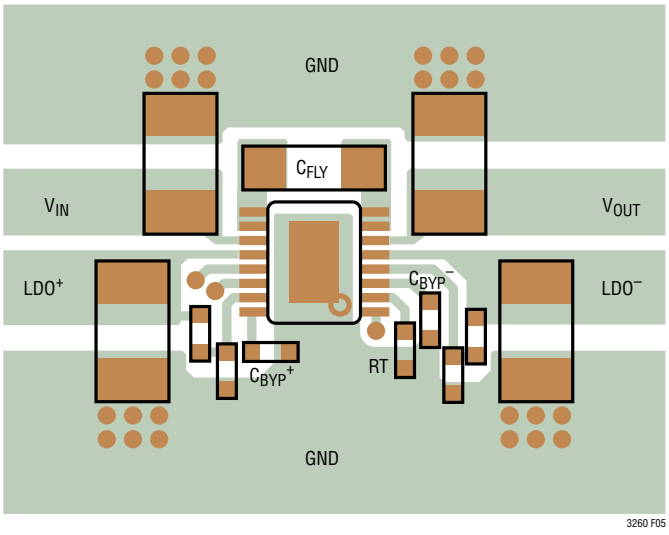


Figure 5. Recommended Layout

The flying capacitor nodes C^+ and C^- switch large currents at a high frequency. These nodes should not be routed close to sensitive pins such as the LDO feedback pins (ADJ^+ and ADJ^-) and internal reference bypass pins (BYP^+ and BYP^-).

Thermal Management

At high input voltages and maximum output current, there can be substantial power dissipation in the LTC3260. If the junction temperature increases above approximately 175°C, the thermal shutdown circuitry will automatically deactivate the output. To reduce the maximum junction temperature, a good thermal connection to the PC board ground plane is recommended. Connecting the exposed pad of the package to a ground plane under the device on two layers of the PC board can reduce the thermal resistance of the package and PC board considerably.

Derating Power at High Temperatures

To prevent an overtemperature condition in high power applications, Figure 6 should be used to determine the maximum combination of ambient temperature and power dissipation.

The power dissipated in the LTC3260 should always fall under the line shown for a given ambient temperature. The power dissipated in the LTC3260 has three components.

Power dissipated in the positive LDO:

$$P_{LDO}^+ = (V_{IN} - V_{LDO}^+) \bullet I_{LDO}^+$$

Power dissipated in the negative LDO:

$$P_{LDO}^- = (|V_{OUT}| - |V_{LDO}^-|) \bullet I_{LDO}^- \text{ and}$$

Power dissipated in the inverting charge pump:

$$P_{CP} = (V_{IN} - |V_{OUT}|) \bullet (I_{OUT} + I_{LDO}^-)$$

where I_{OUT} denotes any additional current that might be pulled directly from the V_{OUT} pin. The LDO^- current is also supplied by the charge pump through V_{OUT} and is therefore included in the charge pump power dissipation.

The total power dissipation of the LTC3260 is given by:

$$P_D = P_{LDO}^+ + P_{LDO}^- + P_{CP}$$

APPLICATIONS INFORMATION

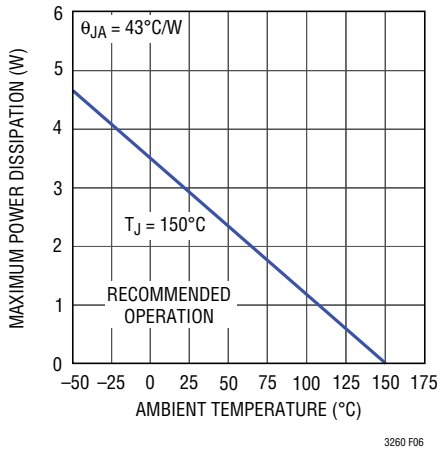


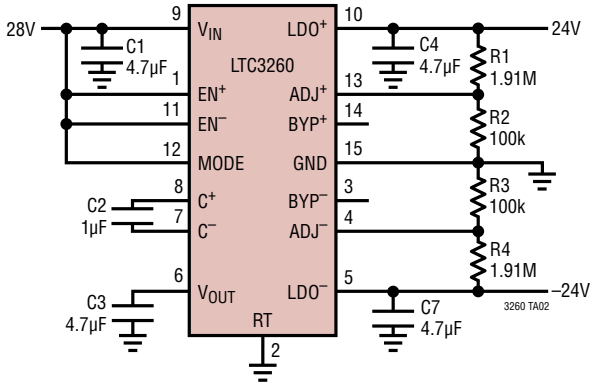
Figure 6. Maximum Power Dissipation vs Ambient Temperature

The derating curve in Figure 6 assumes a maximum thermal resistance, θ_{JA}, of 43°C/W for the package. This can be achieved with a four layer PCB that includes 2oz Cu traces and six vias from the exposed pad of the LTC3260 to the ground plane.

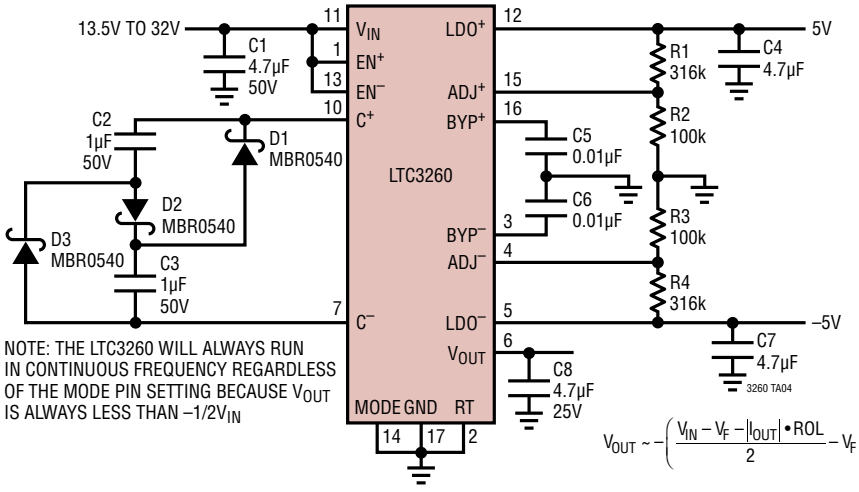
It is recommended that the LTC3260 be operated in the region corresponding to $T_J \leq 150°C$ for continuous operation as shown in Figure 6. Operation beyond 150°C should be avoided as it may degrade part performance and lifetime. At high temperatures, typically around 175°C, the part is placed in thermal shutdown and all outputs are disabled. When the part cools back down to a low enough temperature, typically around 165°C, the outputs are re-enabled and the part resumes normal operation.

TYPICAL APPLICATIONS

Low Power ±24V Power Supply from a Single-Ended 28V Input Supply

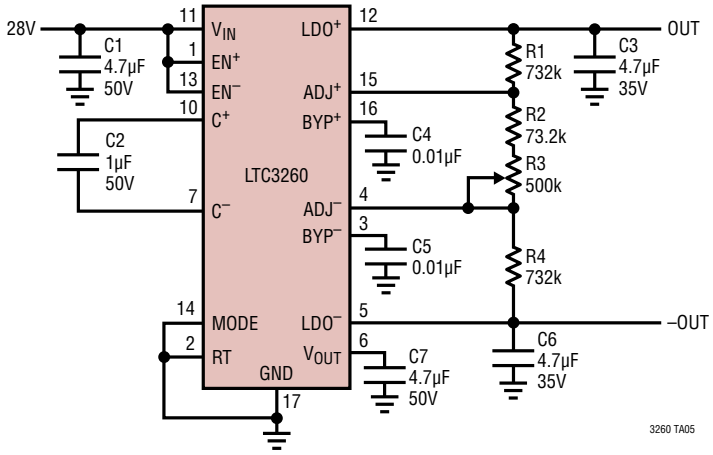


High Voltage Input to Bipolar Output with Highly Efficient Dividing/Inverting Charge Pump



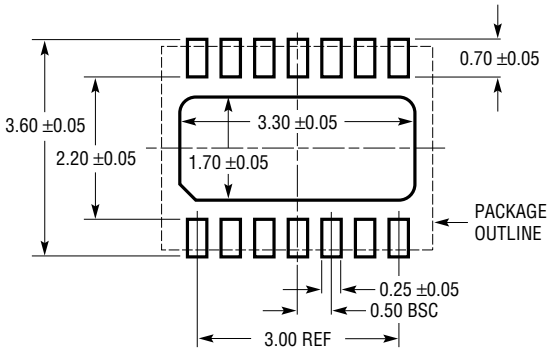
TYPICAL APPLICATIONS

28V Dual Tracking Bipolar Supply with Outputs from ±5V to ±25V

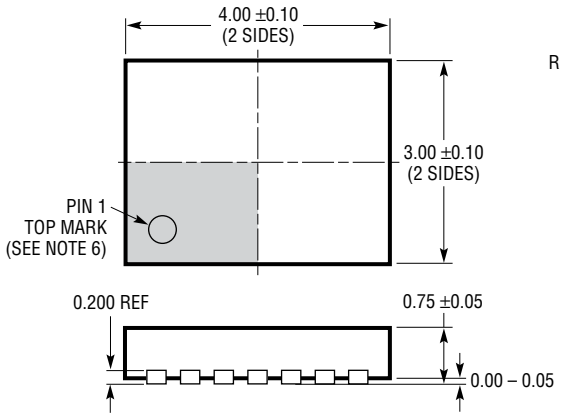


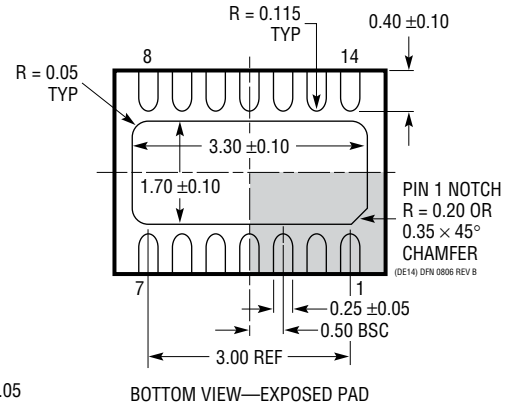
PACKAGE DESCRIPTION

DE Package
14-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1708 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



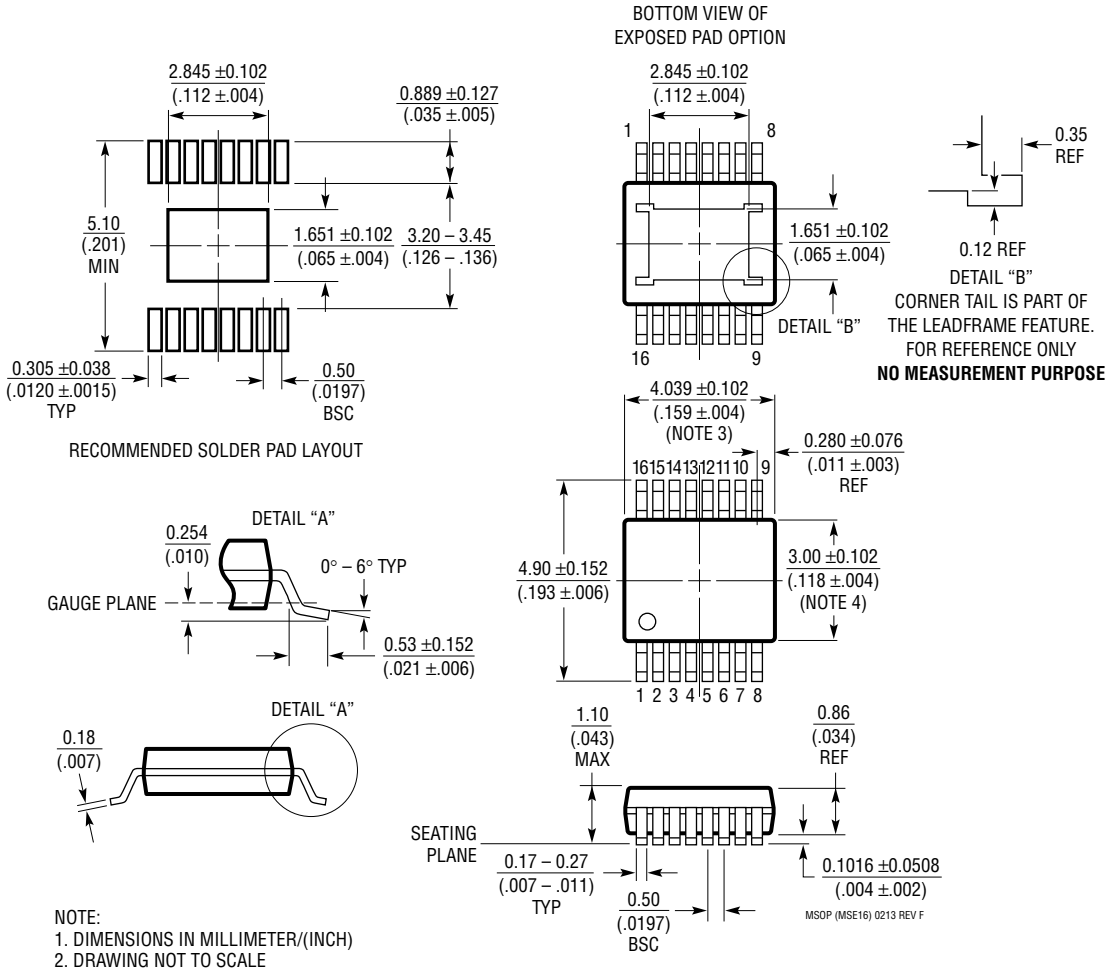


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WGED-3) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev F)



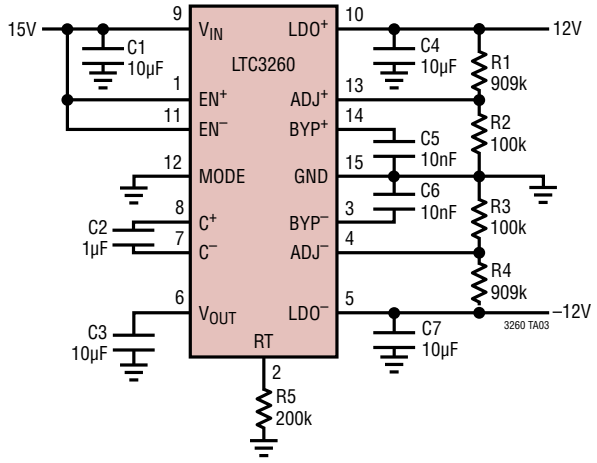
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	09/12	Changed Operating Junction Temperature.	2
		Add H- and MP-grade options.	Throughout
		Add Junction to heading of Electrical Characteristics table.	3
		Add H- and MP-grade into Note 2.	4
		Modified Shutdown Current vs Temperature curve for operation to 150°C.	4
		Modified Quiescent Current vs Temperature curve for operation to 150°C.	4
		Corrected Figure 5 Pinout R_T and C_{BYP}.	12
		Removed Thermal Shutdown curve from Figure 6.	13
		Clarified 150°C Operation in Derating Power section.	12, 13
		Updated Related Parts list.	18
B	11/21	Added AEC-Q100 Qualification in Progress statement.	1
		Added #W models in Ordering Information table.	2

TYPICAL APPLICATION

Low Noise ±12V Power Supply from a Single-Ended 15V Input Supply (Frequency = 200kHz)



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1144	Switched-Capacitor Wide Input Range Voltage Converter with Shutdown	Wide Input Voltage Range: 2V to 18V, I_{SD} < 8µA, SO8 Package
LTC1514/LTC1515	Step-Up/Step-Down Switched-Capacitor DC/DC Converters	V_{IN}: 2V to 10V, V_{OUT}: 3.3V to 5V, I_Q = 60µA, SO8 Package
LT®1611	150mA Output, 1.4MHz Micropower Inverting Switching Regulator	V_{IN}: 0.9V to 10V, V_{OUT} = ±34V, ThinSOT™ Package
LT1614	250mA Output, 600kHz Micropower Inverting Switching Regulator	V_{IN}: 0.9V to 6V, V_{OUT} = ±30V, I_Q = 1mA, MS8, SO8 Packages
LTC1911	250mA, 1.5MHz Inductorless Step-Down DC/DC Converter	V_{IN}: 2.7V to 5.5V, V_{OUT} = 1.5V/1.8V, I_Q = 180µA, MS8 Package
LTC3250/LTC3250-1.2/ LTC3250-1.5	Inductorless Step-Down DC/DC Converters	V_{IN}: 3.1V to 5.5V, V_{OUT} = 1.2V, 1.5V, I_Q = 35µA, ThinSOT Package
LTC3251	500mA Spread Spectrum Inductorless Step-Down DC/DC Converter	V_{IN}: 2.7V to 5.5V, V_{OUT}: 0.9V to 1.6V, 1.2V, 1.5V, I_Q = 9µA, MS10E Package
LTC3252	Dual 250mA, Spread Spectrum Inductorless Step-Down DC/DC Converter	V_{IN}: 2.7V to 5.5V, V_{OUT}: 0.9V to 1.6V, I_Q = 50µA, DFN12 Package
LT1054/LT1054L	Switched-Capacitor Voltage Converters with Regulator	V_{IN}: 3.5V to 15V/7V, I_{OUT} = 100mA/125mA, N8, S08, SO16 Packages
LTC3261	High Voltage, Low Quiescent Current Inverting Charge Pump	V_{IN}: 4.5V to 32V, V_{OUT} = $–V_{IN}$, I_{OUT} = 100mA, MSOP-12 Package

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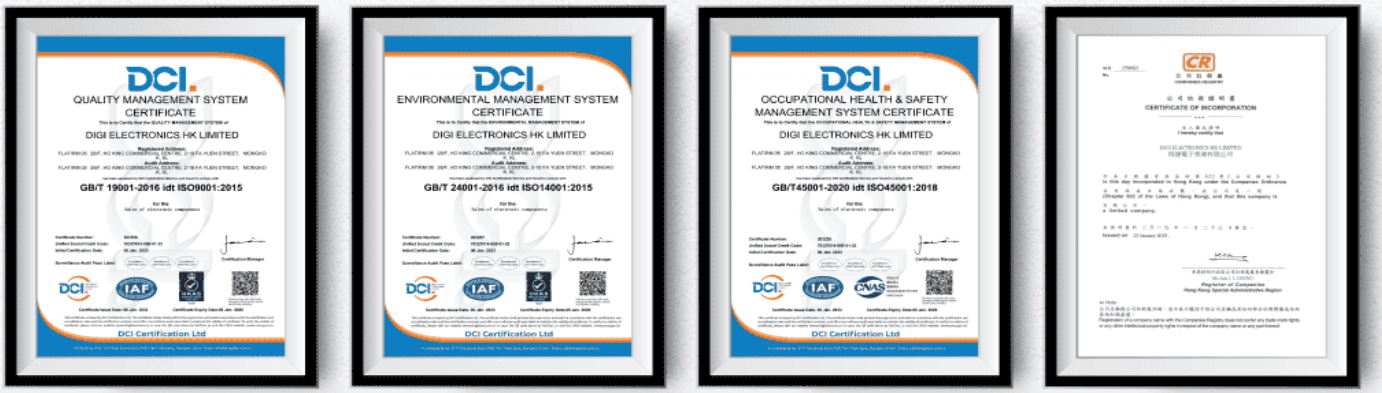

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