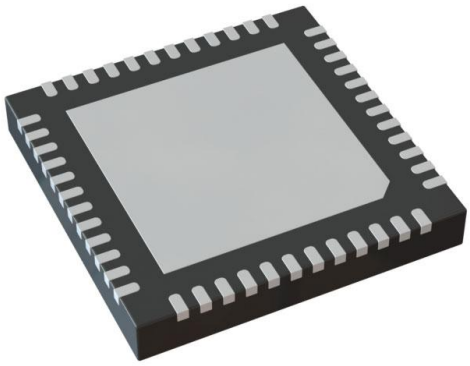
MAX14819ATM+ Datasheet



DiGi Electronics Part Number	MAX14819ATM+-DG
Manufacturer	Analog Devices Inc./Maxim Integrated
Manufacturer Product Number	MAX14819ATM+
Description	IC TRANSCEIVER 48TQFN
Detailed Description	Transceiver IO-Link 48-TQFN (7x7)

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
MAX14819ATM+	Analog Devices Inc./Maxim Integrated
Series:	Product Status:
-	Active
Type:	Protocol:
Transceiver	IO-Link
Number of Drivers/Receivers:	Duplex:
-	-
Data Rate:	Voltage - Supply:
-	9V ~ 36V
Operating Temperature:	Mounting Type:
-40°C ~ 125°C	Surface Mount
Package / Case:	Supplier Device Package:
48-WFQFN Exposed Pad	48-TQFN (7x7)
Base Product Number:	
MAX14819	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8542.39.0001	

EVALUATION KIT AVAILABLE

Click here for production status of specific part numbers.

MAX14819/MAX14819A Dual IO-Link Master Transceiver with Integrated Framers and L+ Supply Controllers

General Description

The MAX14819/MAX14819A low-power, dual-channel, IO-Link® master transceiver with sensor/actuator power-supply controllers is fully compliant with the latest IO-Link and binary input standards and test specifications, IEC 61131-2, IEC 61131-9 SDCI, and IO-Link 1.1.3. This master transceiver also includes two auxiliary digital input (DI_) channels.

The MAX14819/MAX14819A is configurable to operate either with external UARTs or using the integrated framers on the IC.

To ease selection of microcontroller, the master transceiver features frame handlers with UARTs and FIFOs. These are designed to simplify time critical control of all IO-Link M-sequence frame types. The MAX14819/MAX14819A also features autonomous cycle timers, reducing the need for accurate controller timing. Integrated establish-communication sequencers also simplify wake-up management.

The device message response delay on the MAX14819A can be disabled when using the frame handler and the MAX14819A features higher L+ thresholds than the MAX14819. The MAX14819A receivers also feature increased high-frequency signal isolation compared to the MAX14819.

The MAX14819/MAX14819A integrates two low-power sensor supply controllers with advanced current limiting, reverse current-blocking, and reverse polarity protection capability to enable low-power robust solutions.

The MAX14819/MAX14819A is available in a 48-pin (7mm x 7mm) TQFN package and is specified over the extended -40°C to +125°C temperature range.

Applications

- IO-Link Master Systems
- IO-Link Gateways

Benefits and Features

- Low-Power Architecture
  - 1Ω (typ) Driver On-Resistance
  - 1.9mA (typ) Total Supply Current for 2 Channels
  - Current Limiters with 15mV Sense Voltage
- Integrated IO-Link Framer Eliminates Need for External UARTs
  - Integrated Cycle Timer Relieves Microcontroller from Timing-Critical Tasks
- High Configurability and Integration Reduce SKUs
  - Two Auxiliary Type 1/Type 3 Digital Inputs
  - Supports NPN Sensors
  - Dual 24V Sensor Supply Controllers Include:
    - Large Capacitive Load Charge Capability
    - 2A and Higher Load Currents
- Integrated Protection Enables Robust Systems
  - Reverse Polarity Protection on All Interface Pins
  - Overvoltage Tolerance on All Interface Pins
  - C/Q and DI Fully Compliant with IEC 61131-2
  - C/Q Compliant with IO-Link 1.1.3.
  - Reverse Current Blocking on L+ and C/Q
  - 65V Absolute Max Ratings for TVS Flexibility
  - Glitch Filters for Improved Burst Resilience
  - -40°C to +125°C Operating Temperature Range

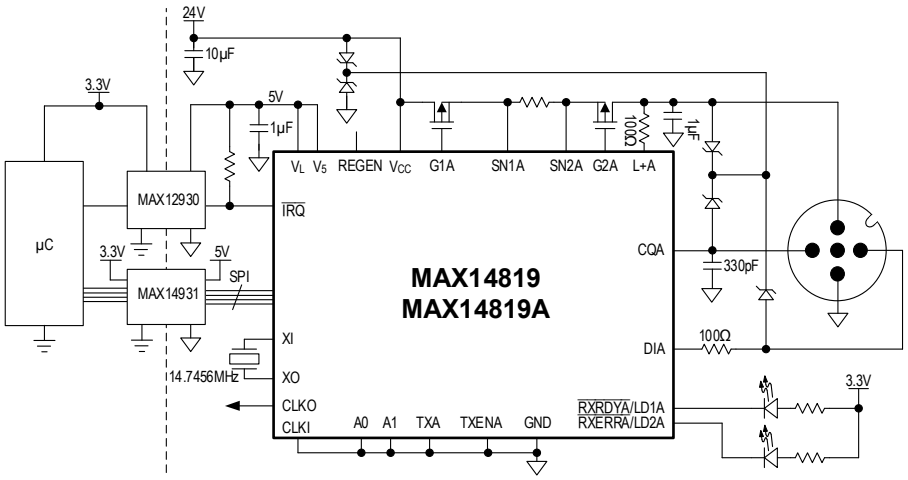
***Ordering Information* appears at end of data sheet.**

IO-Link is a registered trademark of Profibus User Organization (PNO).

19-8744; Rev 3; 3/20

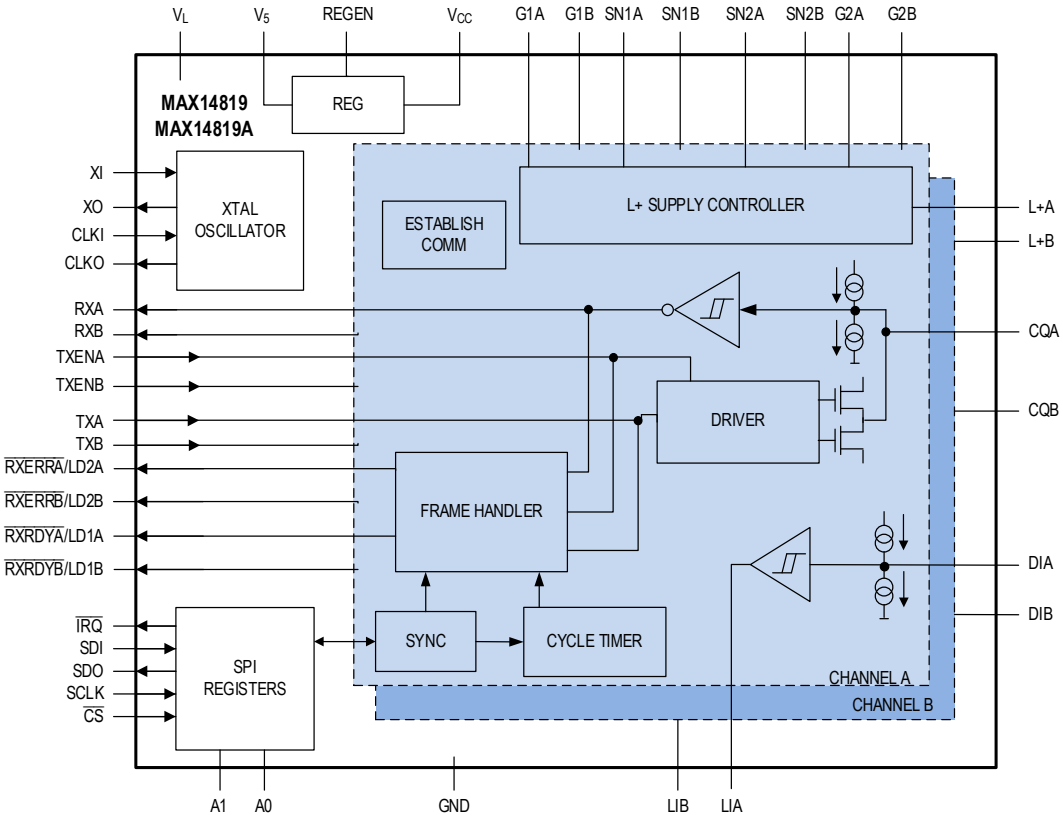
maxim integrated™

Typical Operating Circuit



THE MAX14819/MAX14819A IS A DUAL-CHANNEL MASTER TRANSCEIVER. ONLY ONE CHANNEL IS SHOWN HERE. OPERATED WITH INTERNAL IO-LINK FRAMER.

Functional Diagram



Absolute Maximum Ratings

(All voltages referenced to GND, unless otherwise noted.)

V_{CC} ..... max [(V_{PM} - 70V), ($V_{CQ\_}$ - 70V)] to +65V
V_5, V_L ..... -0.3V to +6V
REGEN ..... -0.3V to the min(V_{CC} + 0.3V or +6V)
CQA, CQB ..... (V_{CC} - 70V) to +65V
DIA, DIB, L+A, L+B ..... (V_{PM} - 70V) to +65V
SN1A, SN1B ..... -0.3V to +65V
SN2A ..... (V_{SN1A} - 0.3V) to (V_{SN1A} + 0.3V)
SN2B ..... (V_{SN1B} - 0.3V) to (V_{SN1B} + 0.3V)
G1A, G2A ..... max (-0.3V, [V_{SN1A} - 14V]) to (V_{SN1A} + 0.3V)
G1B, G2B ..... max (-0.3V, [V_{SN1B} - 14V]) to (V_{SN1B} + 0.3V)
XI, XO ..... -0.3V to (V_5 + 0.3V)
Logic Inputs
  $\overline{CS}$, SDI, SCLK, A_, TXEN_, TX_, CLKI ... -0.3V to (V_L + 0.3V)
Logic Outputs
  SDO, $\overline{IRQ}$, LI_, RX_, $\overline{RXRDY\_}$/LD1_,
  $\overline{RXERR\_}$/LD2_, CLKO ..... -0.3V to (V_L + 0.3V)
Continuous Current Into GND and V_{CC} ..... ±2A
Continuous Current Into CQA and CQB ..... ±1A
Continuous Current Into V_5 ..... ±100mA
Continuous Current Into Any Other Pin ..... ±50mA
Continuous Power Dissipation
  TQFN (derate 40mW/°C above +70°C) 3.2W
Operating Temperature Range ..... -40°C to +125°C
Maximum Junction Temperature ..... Internally Limited
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C

V_{PM} = max (0V, V_{CC}, DIA, DIB, SN1A, SN1B, L+A, L+B)

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 48 TQFN-EP	
Package Code	T4877+4C
Outline Number	**21-0144**
Land Pattern Number	**90-0130**
MULTILAYER BOARD	
Junction to Ambient (θ_{JA})	25°C/W
Junction to Case (θ_{JC})	1°C/W

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

DC Electrical Characteristics

(V_{CC} = 9V to 36V, V_5 = 4.5V to 5.5V, V_L = 1.62V to 5.5V, V_{GND} = 0V, all logic inputs at V_L or GND; T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{CC} = 24V, V_5 = 5V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC} POWER							
V_{CC} Supply Voltage	V_{CC}			9		36	V
V_{CC} Undervoltage-Lockout Threshold	V_{CCUVLO}	V_{CC} rising		7		9	V
V_{CC} Undervoltage-Lockout-Threshold Hysteresis	V_{CCUVLO_HYST}				340		mV
V_{CC} Supply Current	I_{CC}	REGEN = GND, L+EnA = L+EnB = 1, external clock selected, CQ_ in push-pull configuration, CL[1:0] = 00, no load on CQ_	CQ_ outputs low		0.4	0.75	mA
			CQ_ outputs high		0.5	0.85	
V_{CC} Warning Threshold	V_{CC_WRN}			16		18	V
V_{CC} Warning Threshold Hysteresis	V_{CC_WHY}				500		mV
V_5 POWER							
V_5 Supply Voltage	V_5	REGEN = GND		4.5	5	5.5	V
V_5 Supply Current	I_{V5}	REGEN = GND, L+EnA = L+EnB = 1, external clock selected, CQ_ in push-pull configuration, CL[1:0] = 00, no load on CQ_	CQ_ outputs low		1.4	1.9	mA
			CQ outputs high		1.4	1.9	
V_5 LINEAR REGULATOR							
V_5 Output Voltage	V_5	REGEN unconnected, no load on V5, CQ_ disabled, L+EnA = L+EnB = 0		4.75		5.25	V
V_5 Current Limit	I_{CL_V5}	REGEN unconnected, CQ_ disabled, L+EnA = L+EnB = 0		20			mA
V_5 Load Regulation	dV_{V5}	REGEN unconnected, CQ_ disabled, L+EnA = L+EnB = 0, 0mA ≤ I_{LOAD} ≤ 20mA			-0.1		mV/mA
REGEN Pullup Current	I_{REGEN}	V_{REGEN} = 0V		5		30	µA
REGEN Threshold	V_{TH_REGEN}			0.2	1.8	2.6	V

DC Electrical Characteristics (continued)

(V_{CC} = 9V to 36V, V_5 = 4.5V to 5.5V, V_L = 1.62V to 5.5V, V_{GND} = 0V, all logic inputs at V_L or GND; T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{CC} = 24V, V_5 = 5V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_L POWER							
V_L Logic-Level Supply Voltage	V_L			1.62		5.5	V
V_L Undervoltage Threshold	V_{LUVLO}	V_L falling		0.4		1.5	V
V_L Undervoltage Threshold Hysteresis	V_{LUVHYS}				50		mV
V_L Logic-Level Supply Current	I_L	All logic inputs at V_L or GND, all logic outputs unconnected				5	µA
CQ_ DRIVER							
Driver On-Resistance	R_{OH}	High-side enabled, I_{LOAD} = -200mA			1.0	2	Ω
	R_{OL}	Low-side enabled, I_{LOAD} = +200mA			1.0	2.2	Ω
Driver Current Limit	I_{CL}	$V_{CQ\_}$ = (V_{CC} - 3V) or 3V	CL[1:0] = 00	100		150	mA
			CL[1:0] = 01	190		280	mA
			CL[1:0] = 10	280		410	mA
			CL[1:0] = 11	500		650	mA
CQ_, DI_ RECEIVER							
CQ_, DI_ Input Threshold High	V_{TH}	CQ_ driver disabled	IEC3Th_/DiEC3Th = 0	10.5		13.0	V
			IEC3Th_/DiEC3Th = 1	7.5		11.0	V
CQ_, DI_ Input Threshold Low	V_{TL}	CQ_ driver disabled	IEC3Th_/DiEC3Th = 0	8.0		11.5	V
			IEC3Th_ /DiEC3Th = 1	6.0		8.0	V
CQ_, DI_ Input Threshold Hysteresis	V_{HYS}	CQ_ driver disabled	IEC3Th_/DiEC3Th = 0		2		V
			IEC3Th_/DiEC3Th = 1		2		V
CQ_ Current Sink	I_{CQ_SNK}	$V_{CQ\_}$ > 5V, SourceSink_ = 0	2mA pulldown enabled (SinkSel_[1:0] = 10)	2	2.5	2.75	mA
			5mA pulldown enabled (SinkSel_[1:0] = 01)	5	5.8	6.6	mA

DC Electrical Characteristics (continued)

(V_{CC} = 9V to 36V, V_5 = 4.5V to 5.5V, V_L = 1.62V to 5.5V, V_{GND} = 0V, all logic inputs at V_L or GND; T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{CC} = 24V, V_5 = 5V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CQ_ Current Source	I_{CQ_SRC}	(V_{CC} - $V_{CQ\_}$) > 5V, SourceSink_ = 1	2mA pullup enabled (SinkSel_[1:0] = 10)	-2.75	-2.5	-2	mA
			5mA pullup enabled (SinkSel_[1:0] = 01)	-6.6	-5.8	-5	
CQ_ Weak Pulldown Current	I_{CQ_PD}	Driver disabled (DrvDis_ = 1), SourceSink = 0, weak pulldown enabled (SinkSel_[1:0] = 11), $V_{CQ\_}$ > 5V		150		250	µA
CQ_ Weak Pullup Current	I_{CQ_PU}	Driver disabled (DrvDis_ = 1), SourceSink = 1, weak pullup enabled (SinkSel_[1:0] = 11), V_{CC} - $V_{CQ\_}$ > 5V		-250		-150	µA
CQ_ Input Current	I_{CQ}	CQ_ driver enabled (DrvDis = 0), CQ_set to high impedance, pullup and pulldown disabled (SinkSel_[1:0] = 00), receiver enabled, V_{CC} = 24V, -1V < $V_{CQ\_}$ < (V_{CC} + 1V)		-60		+400	µA
CQ_ Input Current, Extended Range	I_{CQ_EXT}	CQ_ driver enabled (DrvDis = 0), CQ_set to high impedance, pullup and pulldown disabled (SinkSel_[1:0] = 00), receiver enabled, V_{CC} = 24V, (V_{CC} - 65V) < $V_{CQ\_}$ < 60V		-200		+500	µA
CQ_ Leakage Current	I_{CQ_LKG}	CQ_ driver disabled (DrvDis = 1), pullup and pulldown disabled (SinkSel_[1:0] = 00), receiver enabled, V_{CC} = 24V, (V_{CC} - 65V) < $V_{CQ\_}$ < 60V		-100		+100	µA
CQ_ Push-Pull High Impedance Current	I_{CQ_HiZ}	CQ_ driver enabled (DrvDis = 0), CQ_in push-pull, pullup and pulldown disabled (SinkSel_[1:0] = 00), receiver enabled, V_{CC} = 24V, 0V < $V_{CQ\_}$ < 24V		-50		+50	µA
DI_ Current Sink	I_{DI_SNK}	$V_{DI\_}$ > 5V, DiCSink = 1		2	2.5	3	mA
DI_ Current Source	I_{DI_SRC}	V_{CC} - $V_{DI\_}$ > 5V, DiCSource = 1		-3	-2.5	-2	mA
DI_ Input Current	I_{DI}	Pullup and pulldown disabled, DI_ receiver enabled, V_{CC} = 24V, -1V < $V_{DI\_}$ < (V_{CC} + 1V)		-5		+50	µA
DI_ Input Current, Extended Range	I_{DI_EXT}	Pullup and pulldown disabled, DI_ receiver enabled, V_{CC} = 24V, (V_{CC} - 65V) < $V_{DI\_}$ < 60V		-100		+100	µA

DC Electrical Characteristics (continued)

(V_{CC} = 9V to 36V, V_5 = 4.5V to 5.5V, V_L = 1.62V to 5.5V, V_{GND} = 0V, all logic inputs at V_L or GND; T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{CC} = 24V, V_5 = 5V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS ($\overline{CS}$, SDI, SCLK, A1, A0, TXENA, TXENB, TXA, TXB, CLKI)						
Logic Input Voltage Low	V_{IL}				0.2 x V_L	V
Logic Input Voltage High	V_{IH}		0.8 x V_L			V
Logic Input Leakage Current	I_{LEAK}	Logic input = GND or V_L	-1		+1	µA
LOGIC OUTPUTS (SDO, $\overline{IRQ}$, LIA, LIB, RXA, RXB, $\overline{RXRDYA}$/LD1A, $\overline{RXERRA}$/LD2A, $\overline{RXRDYB}$/LD1B, $\overline{RXERRB}$/LD2B, CLKO)						
Logic Output Voltage Low	V_{OL}	I_{OUT} = -5mA			0.4	V
Logic Output Voltage High	V_{OH}	RX_, LI_, SDO, and CLKO, I_{OUT} = 5mA	V_L - 0.4			V
Output Leakage Current	I_{OH}	$\overline{RXRDY\_}$/LD1_, $\overline{RXERR\_}$/LD2_, $\overline{IRQ}$, output is high impedance, output is pulled up to 5V	-1		+1	µA
CRYSTAL OSCILLATOR (XI, XO)						
Crystal Oscillator Current Supply	I_{V5_XTAL}	f_{XTAL} = 14.7456MHz, V_5 supply current increase versus external clocking		240		µA
Crystal Equivalent Series Resistance	ESR_{XTAL}	f_{XTAL} = 14.7456MHz (Note 2)			75	Ω
Crystal Shunt Capacitance	C_{OXTAL}	f_{XTAL} = 14.7456MHz (Note 2)			8	pF
Input Capacitance	CIN	XI		10		pF
		XO		10		
INTERNAL OSCILLATOR						
Internal Oscillator Current Consumption	I_{V5_OSC}	(Notes 3, 4)		55		µA
EXTERNAL CLOCK INPUT (CLKI)						
External Clock Frequency	f_{ECLK}			3.686		MHz
External Clock Detection	f_{ECLK_DET}	Minimum CLKI frequency for operation	0.5		2	MHz
CLKI Capacitance	C_{CLKI}			2		pF
L+ SENSOR SUPPLIES WITH CURRENT LIMITING AND REVERSE BLOCKING (L+A, L+B)						
Reverse Current Blocking Threshold	V_{TH_RCB}	V_{RCB} = ($V_{SN1\_}$ -V_{CC})			160	mV
G1_/G2_ Gate-to-Source On-Voltage	V_{G_ON}	$V_{SN1\_}$ > 18V	$V_{SN1\_}$ - 14V		$V_{SN1\_}$ - 11V	V
G2_ Minimum Gate-to-Source Voltage Under Regulation	V_{G2_REG}		$V_{SN1\_}$ - 0.8V			V
G1_ Gate Turn-Off Switch Resistance	R_{G1_OFF}	G1_ pulled to SN1_		50		Ω
G2_ Gate Turn-Off Switch Resistance	R_{G2_OFF}	G2_ pulled to SN2_		50		Ω

DC Electrical Characteristics (continued)

(V_{CC} = 9V to 36V, V_5 = 4.5V to 5.5V, V_L = 1.62V to 5.5V, V_{GND} = 0V, all logic inputs at V_L or GND; T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{CC} = 24V, V_5 = 5V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
L+_ Current-Limit Threshold	V_{CL_T}	$V_{CL\_T} = (V_{SN1\_} - V_{SN2\_})$, L+CL2X_ = 0		12.75	15	18.5	mV
L+_ Double Current-Limit Threshold	V_{CL_2T}	$V_{CL\_2T} = (V_{SN1\_} - V_{SN2\_})$, L+CL2X_ = 1, $V_{CC} = V_{SN1\_}$ = 24V, $V_{L+\_}$ > 18V		25.5	30	36	mV
SN1_ Supply Current	I_{SN1ACT}	V_{L+} > 18V, L+En_ = 1, L+CL2X_ = 1			0.23	0.325	mA
SN2_ Input Current	I_{SN2}	$V_{SN2\_} = V_{SN1\_}$		-10		+10	µA
L+_ Input Current	I_{L+}	$V_{L+\_}$ = 30V				20	µA
L+_ Extended Range Input Current	I_{L+_EXT}	$V_{CC} = V_{SN1\_}$ = 24V, (V_{CC} - 60V) < $V_{L+\_}$ < 60V		-50		+50	µA
L+_ Power Good Threshold	V_{TL+_R}	L+_ rising	MAX14819	16		18	V
			MAX14819A	18		20	
	V_{TL+_F}	L+_ falling	MAX14819	15.5		17.5	V
			MAX14819A	17.5		19.5	
L+_ Power Good Hysteresis	V_{TL+H}				0.4		V
L+_ Dynamic Blanking Threshold	V_{LPDTHR}				8.8		V
THERMAL MANAGEMENT							
Thermal-Warning Threshold	T_{WRN}	Die junction temperature rising, TempW and TempWInt bits are set			+135		°C
Thermal-Warning Threshold Hysteresis	T_{WRN_HYS}	Die junction temperature falling, TempW bit cleared			15		°C
CQ_ Thermal-Shutdown Temperature	T_{SHUT}	Driver temperature rising, temperature at which the driver is turned off. ThShut and ThuShutInt bits are set			+160		°C
Thermal-Shutdown Temperature Hysteresis	T_{SHUT_HYS}	Driver temperature falling. ThShut bit is cleared			15		°C

AC Electrical Characteristics

(V_{CC} = 18V to 30V, V_5 = 4.5V to 5.5V, V_L = 1.62V to 5.5V, V_{GND} = 0V; T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{CC} = 24V, V_5 = 5V, V_L = 3.3, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
CQ_ DRIVER								
Driver Low-to-High Propagation Delay	t_{PDLH}	Push-pull and PNP configuration, Figure 1				0.45	0.90	µs
		NPN configuration, Figure 1 (no capacitive load)				5		
Driver High-to-Low Propagation Delay	t_{PDHL}	Push-pull and NPN configuration, Figure 1				0.43	0.90	µs
		PNP configuration, Figure 1 (no capacitive load)				5		
Driver Skew	t_{SKEW}	$\lvert t_{PDLH} - t_{PDHL} \rvert$, Figure 1					0.2	µs
Driver Rise Time	t_{RISE}	Push-pull and PNP configuration, Figure 1			0.25	0.42	0.75	µs
Driver Fall Time	t_{FALL}	Push-pull and NPN configuration, Figure 1			0.25	0.42	0.75	µs
Driver Enable Time High	t_{ENH}	Push-pull and PNP configuration, Figure 2				0.45	0.9	µs
Driver Enable Time Low	t_{ENL}	Push-pull and NPN configuration, Figure 3				0.26	0.9	µs
Driver Disable Time High	t_{DISH}	Push-pull and PNP configuration, Figure 2				1.9	3	µs
Driver Disable Time Low	t_{DISL}	Push-pull and NPN configuration, Figure 3				1.7	3	µs
CQ_ RECEIVER (Figure 4)								
CQ_ Receiver Low-to-High Propagation Delay	t_{CPRLH}	CQFilterEn_ = 0		MAX14819		0.28	0.5	µs
				MAX14819A		0.53	0.8	
		CQFilterEn_ = 1		MAX14819		1.2	2	
				MAX14819A		1.5	2.3	
CQ_ Receiver High-to-Low Propagation Delay	t_{CPRHL}	CQFilterEn_ = 0		MAX14819		0.25	0.5	µs
				MAX14819A		0.31	0.8	
		CQFilterEn_ = 1		MAX14819		1.2	2	
				MAX14819A		1.3	2.3	
CQ_ Receiver Skew	t_{CRSKEW}	$\lvert t_{CPRLH} - t_{CPRHL} \rvert$ (Note 3)	CQ FilterEn_ = 0	MAX14819			0.1	µs
				MAX14819A			0.4	
			CQ FilterEn_ = 1	MAX14819			0.1	µs
				MAX14819A			0.4	

AC Electrical Characteristics (continued)

(V_{CC} = 18V to 30V, V_5 = 4.5V to 5.5V, V_L = 1.62V to 5.5V, V_{GND} = 0V; T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{CC} = 24V, V_5 = 5V, V_L = 3.3, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DI_ RECEIVER (Figure 4)							
DI_ Receiver Low-to-High Propagation Delay	t_{DPRLH}	DiFilterEn = 0	MAX14819		1.9	3	µs
			MAX14819A		1.3	3	
		DiFilterEn = 1	MAX14819		2.9	4.2	
			MAX14819A		2.3	4.2	
DI_ Receiver High-to-Low Propagation Delay	t_{DPRHL}	DiFilterEn = 0	MAX14819		1.3	3	µs
			MAX14819A		1.0	3	
		DiFilterEn = 1	MAX14819		2.3	4.2	
			MAX14819A		2.0	4.2	
DI_ Receiver Skew	t_{DRSKEW}	$\lvert t_{DPRLH} - t_{DPRHL} \rvert$	DiFilterEn_ = 0		0.5	1	µs
					0.3	1	
			DiFilterEn_ = 1		0.5	1	
					0.3	1	
WAKE-UP PULSE							
Delay Time to Wake-Up Pulse	t_{SU_WU}	(Figure 9)			80		µs
Wake-Up Pulse Duration	t_{WU}	Wake-up (WU) pulse has the opposite polarity of the CQ_ line before the WU pulse was generated		75	80	85	µs
On-Time After Wake-Up	t_{ON_WU}	Driver enabled with original polarity on CQ_ line			2		µs
L+ CURRENT LIMITING							
Reverse Current Blocking Response Time	t_{RCB}	Delay between (V_{RCB} rising > V_{TH_RCB}) and $I_{GATE2\_}$ turned off			10		µs
Reverse Current Blocking Threshold	V_{TH_RCB}	$V_{RCB} = (V_{SN1\_} - V_{CC})$				160	mV
Current-Limit Blanking Time	t_{L+CLBL}	L+BL_[1:0] = 00		5	5.5		ms
		L+BL_[1:0] = 01		15	16.5		
		L+BL_[1:0] = 10		50	55		
		L+BL_[1:0] = 11		150	165		
Current-Limit Retry Delay	t_{L+CLRT}	L+RT_[1:0] = 00, latched off		∞			s
		L+RT_[1:0] = 01			0.5		
		L+RT_[1:0] = 10			4		
		L+RT_[1:0] = 11			10		

AC Electrical Characteristics (continued)

(V_{CC} = 18V to 30V, V_5 = 4.5V to 5.5V, V_L = 1.62V to 5.5V, V_{GND} = 0V; T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{CC} = 24V, V_5 = 5V, V_L = 3.3, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CYCLE TIMER						
Cycle Time	t_{CYCL}	Actual cycle time relative to programmed cycle time, using an external clock or crystal with 100ppm accuracy	0	4	5	%
SPI TIMING ($\overline{CS}$, SCLK, SDI, SDO) (Figure 5)						
Maximum SPI Clock Frequency		1.6V ≤ V_L < 2.5V	15.6			MHz
		V_L ≥ 2.5V	20			
SCLK Clock Period	t_{CH+CL}	1.6V ≤ V_L < 2.5V	64			ns
		V_L ≥ 2.5V	50			
SCLK Pulse-Width High	t_{CH}	1.6V ≤ V_L < 2.5V	32			ns
		V_L ≥ 2.5V	25			
SCLK Pulse-Width Low	t_{CL}	1.6V ≤ V_L < 2.5V	32			ns
		V_L ≥ 2.5V	25			
$\overline{CS}$ Fall to SCLK Rise Time	t_{CSS}	1.6V ≤ V_L < 2.5V	10			ns
		V_L ≥ 2.5V	7			
SDI Hold Time	t_{DH}	1.6V ≤ V_L < 2.5V	0			ns
		V_L ≥ 2.5V	0			
SDI Setup Time	t_{DS}	1.6V ≤ V_L < 2.5V	25			ns
		V_L ≥ 2.5V	23			
SDO Output Data Propagation Delay	t_{DO}	1.6V ≤ V_L < 2.5V			35	ns
		V_L ≥ 2.5V			15	
SDO Rise and Fall Times	t_{FT}	V_L = 1.8V		1.4		ns
		V_L ≥ 2.5V		0.7		
Minimum $\overline{CS}$ Pulse High	t_{CSW}	1.6V ≤ V_L < 2.5V	10			ns
		V_L ≥ 2.5V	10			
$\overline{CS}$ Hold Time	t_{CSH}	1.6V ≤ V_L < 2.5V	32			
		V_L ≥ 2.5V	25			

Note 1: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.
Note 2: Includes stray capacitance or resistance. Required characteristic of the external crystal.
Note 3: Not production tested. Guaranteed by design.
Note 4: V_5 supply current increases when the internal oscillator is selected.

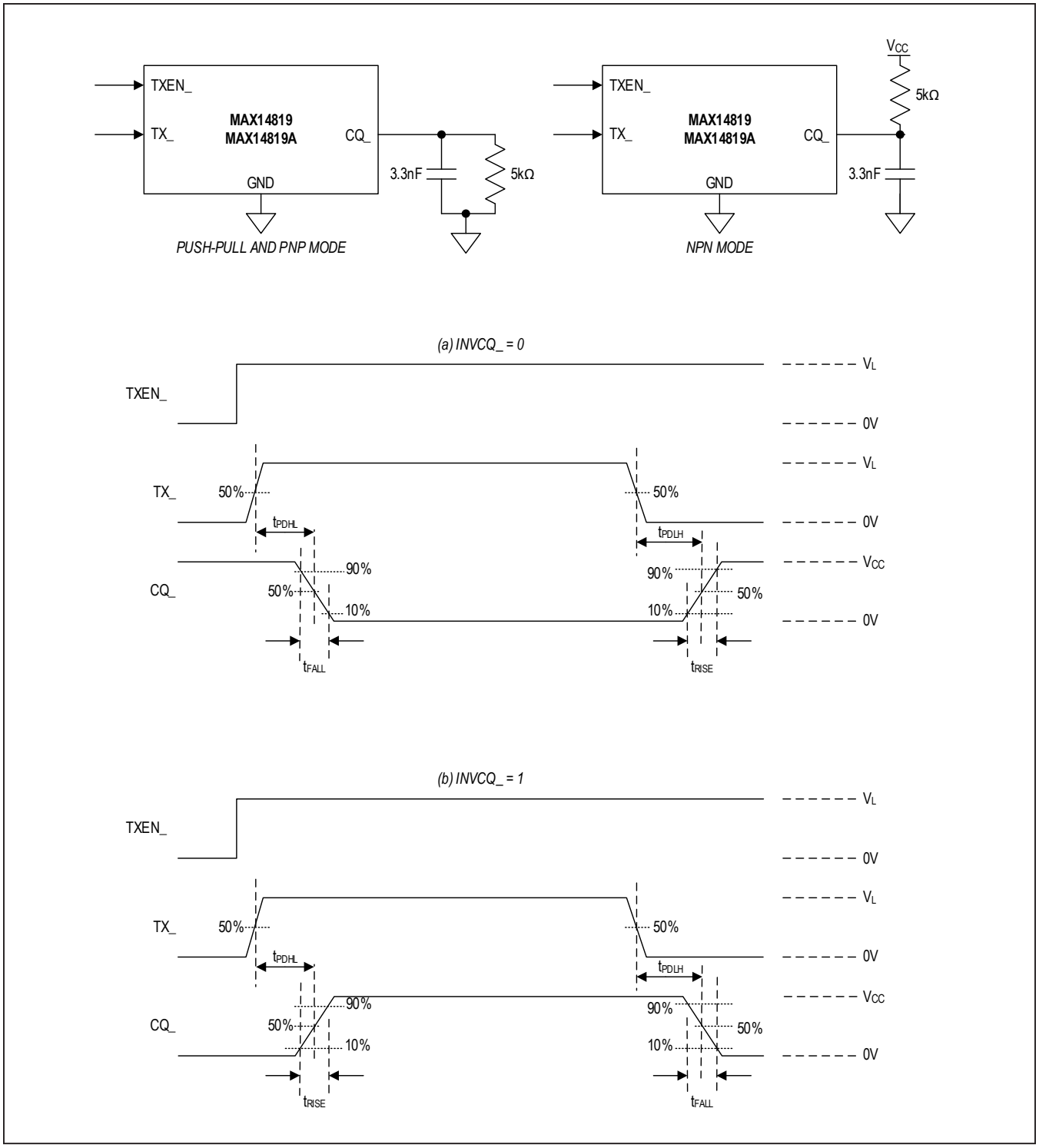


Figure 1. C/Q Driver Propagation Delays and Rise/Fall Times

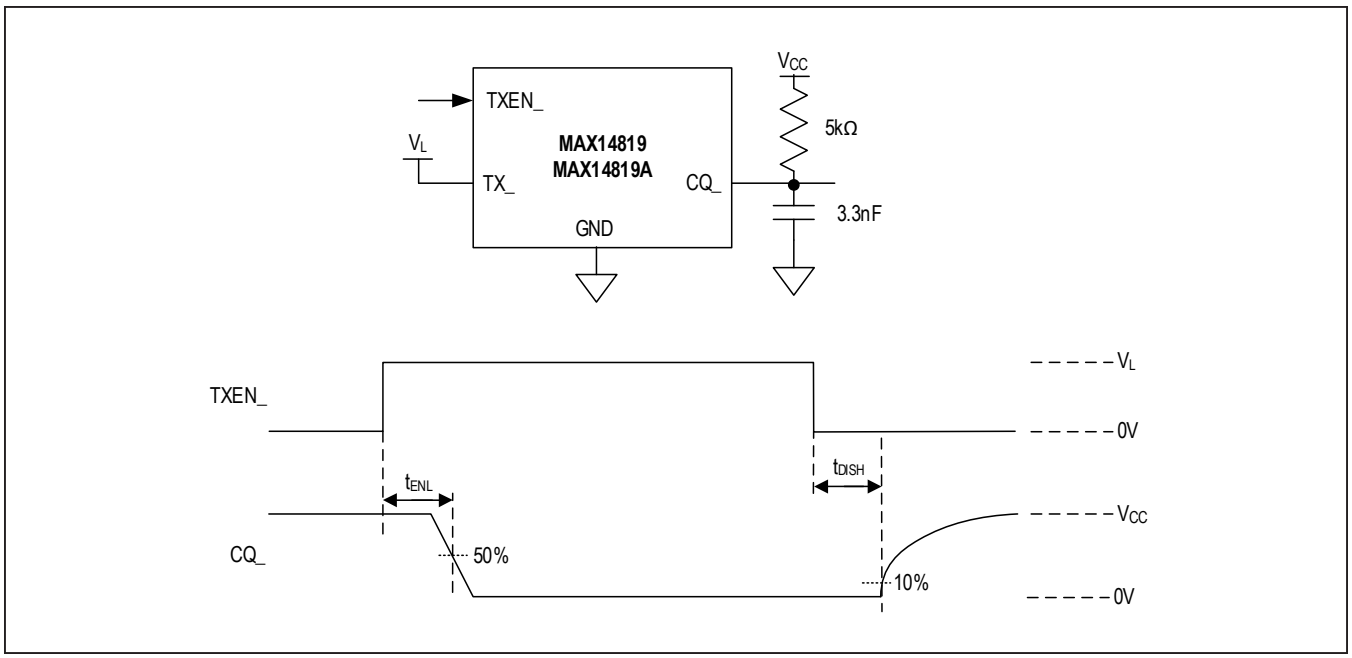


Figure 2. C/Q Driver Enable Low and Disable High Timing with External Pullup Resistor (INVCQ_ = 0)

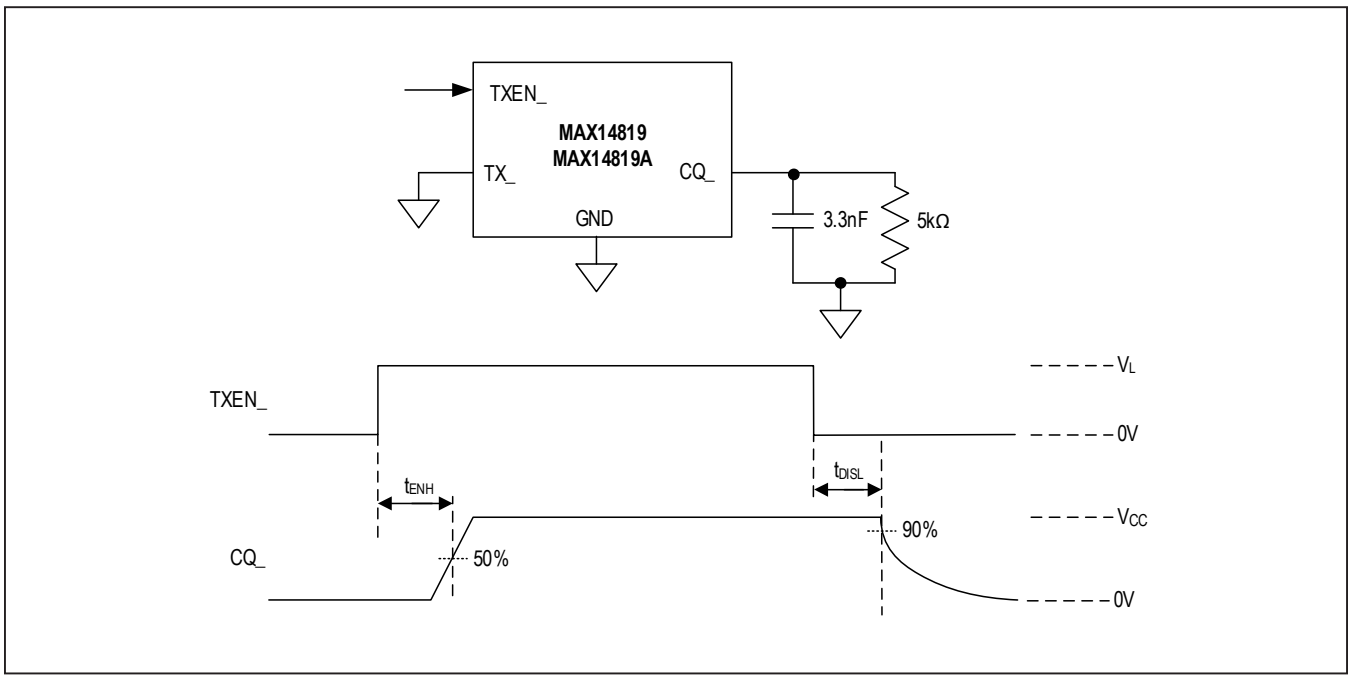


Figure 3. C/Q Driver Enable High and Disable Low Timing (INVCQ_ = 0)

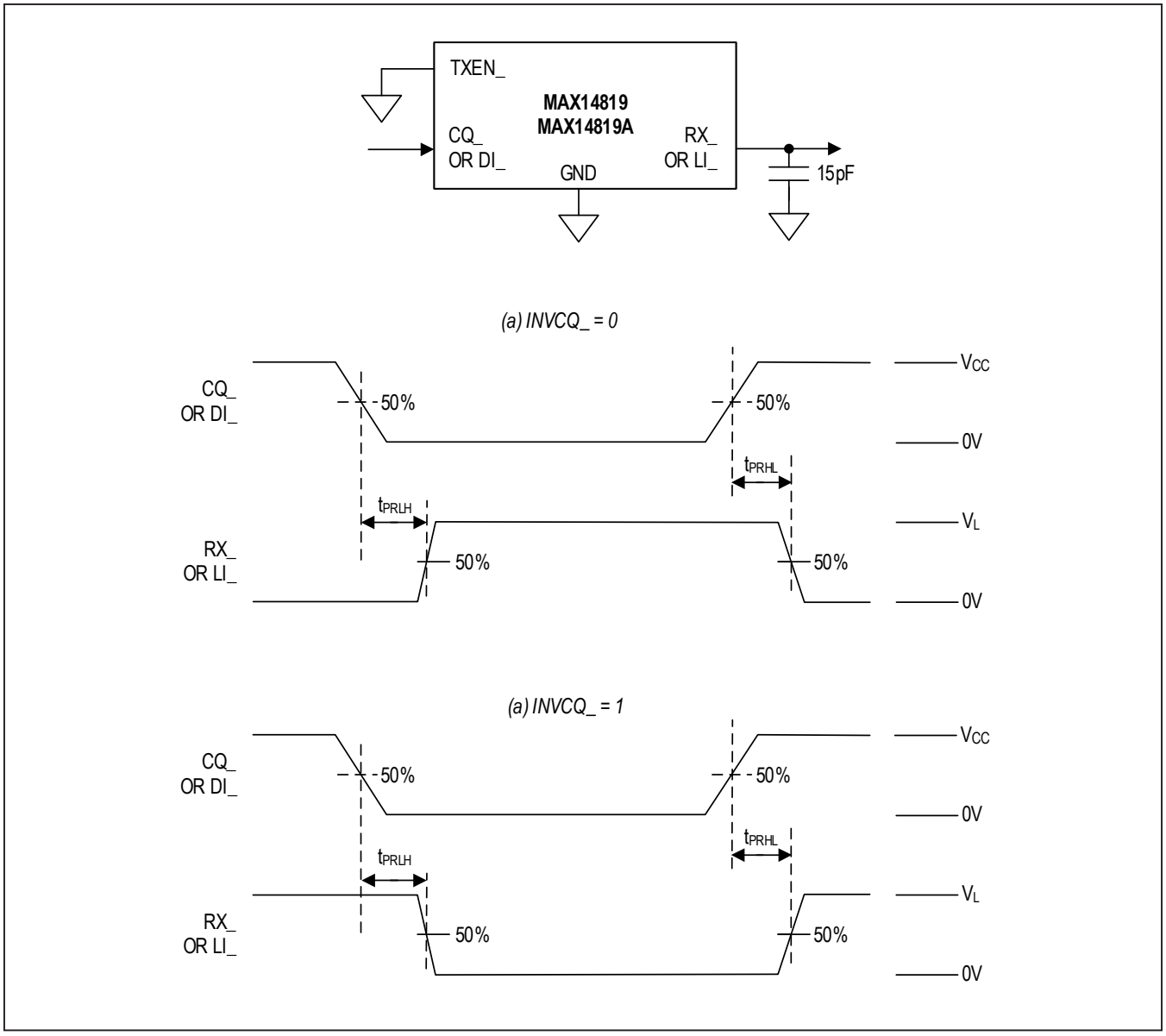


Figure 4. C/Q Receiver Propagation Delays

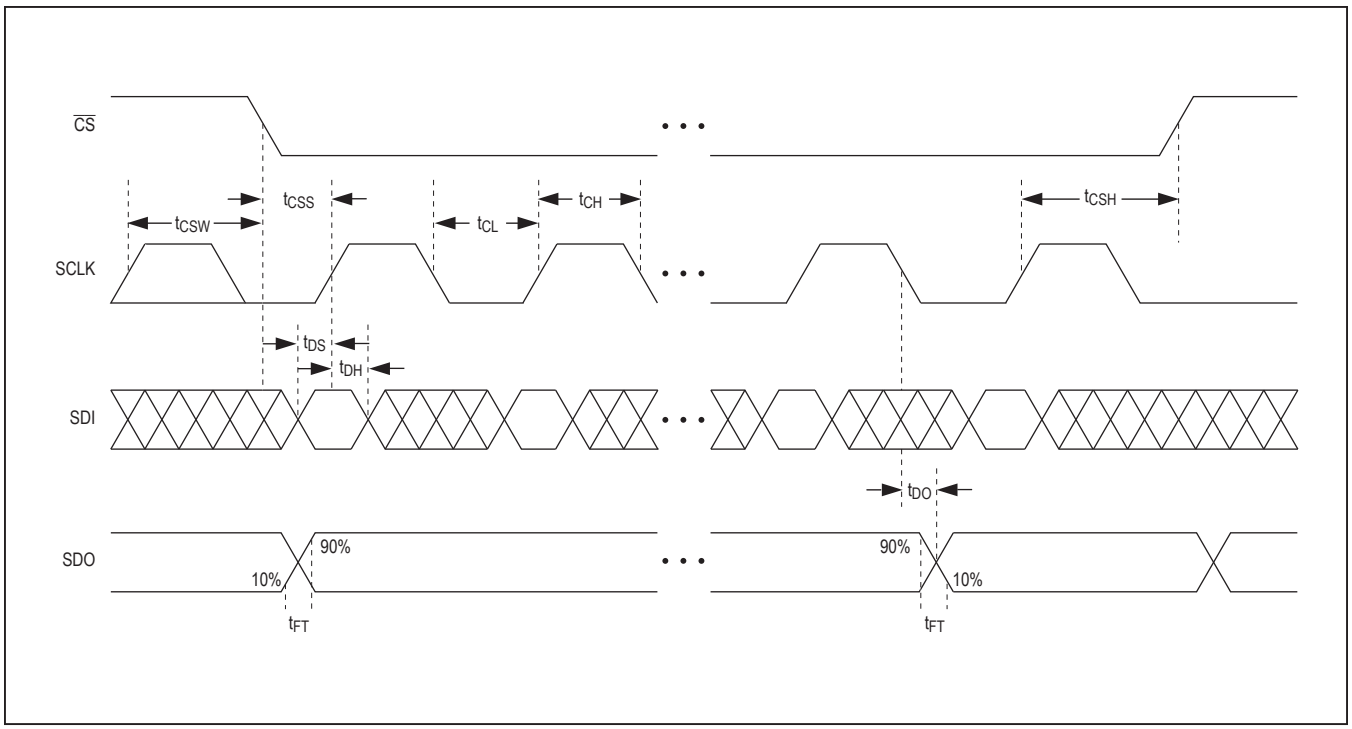
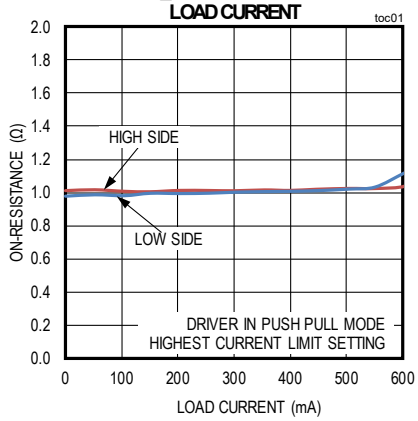


Figure 5. SPI Timing Diagram

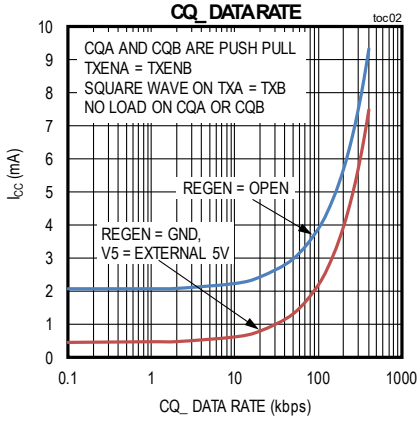
Typical Operating Characteristics

(V_{CC} = 24V, V_L = 3.3V, REGEN is unconnected, CQ_ is in push-pull configuration, T_A = +25°C, unless otherwise noted.)

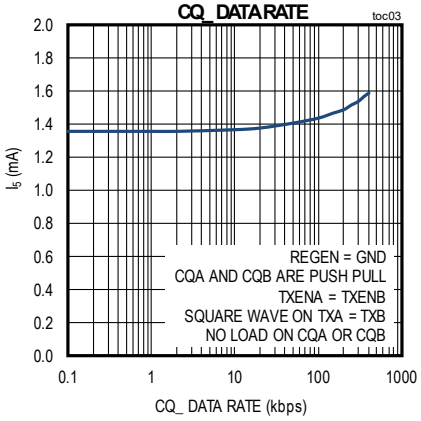
CQ_ ON-RESISTANCE vs LOAD CURRENT



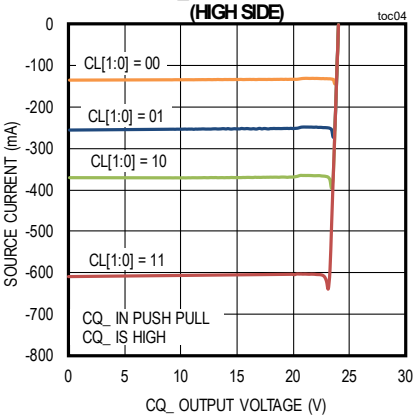
VCC SUPPLY CURRENT vs CQ_ DATA RATE



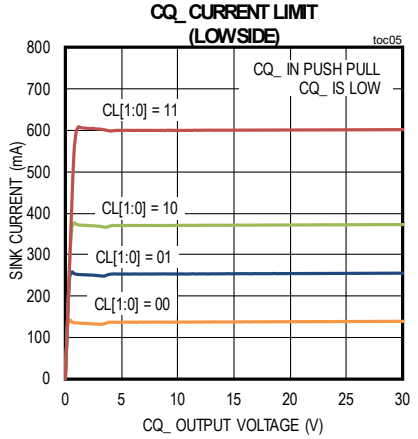
V5 SUPPLY CURRENT vs CQ_ DATA RATE



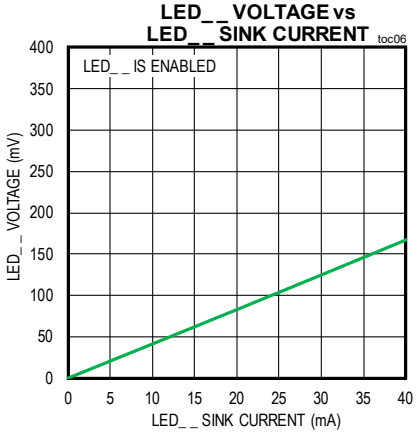
CQ_ CURRENT LIMIT (HIGH SIDE)



CQ_ CURRENT LIMIT (LOW SIDE)

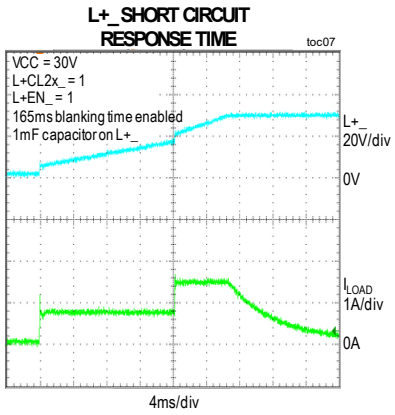


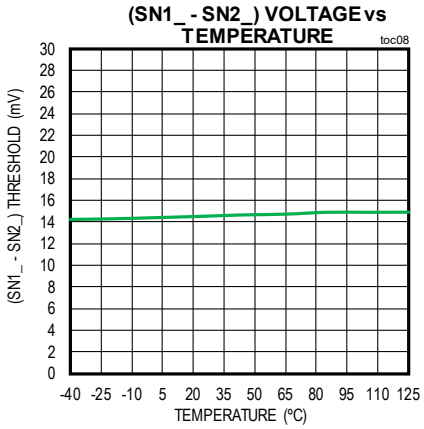
LED_ _ VOLTAGE vs LED_ _ SINK CURRENT

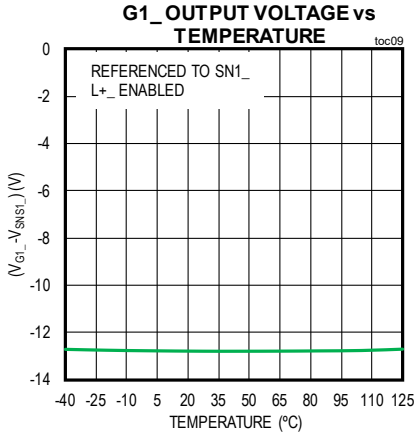


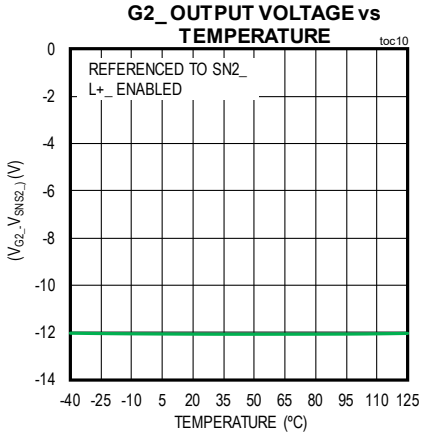
Typical Operating Characteristics (continued)

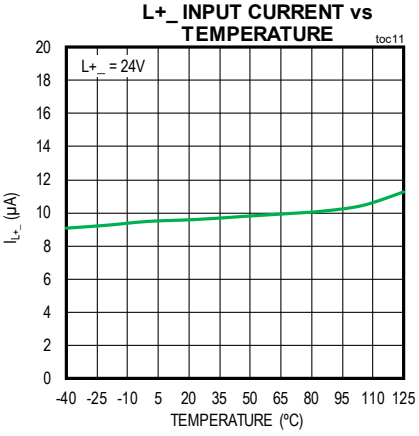
(V_{CC} = 24V, V_L = 3.3V, REGEN is unconnected, CQ_ is in push-pull configuration, T_A = +25°C, unless otherwise noted.)

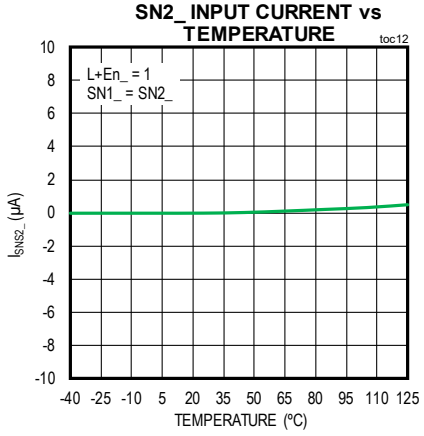




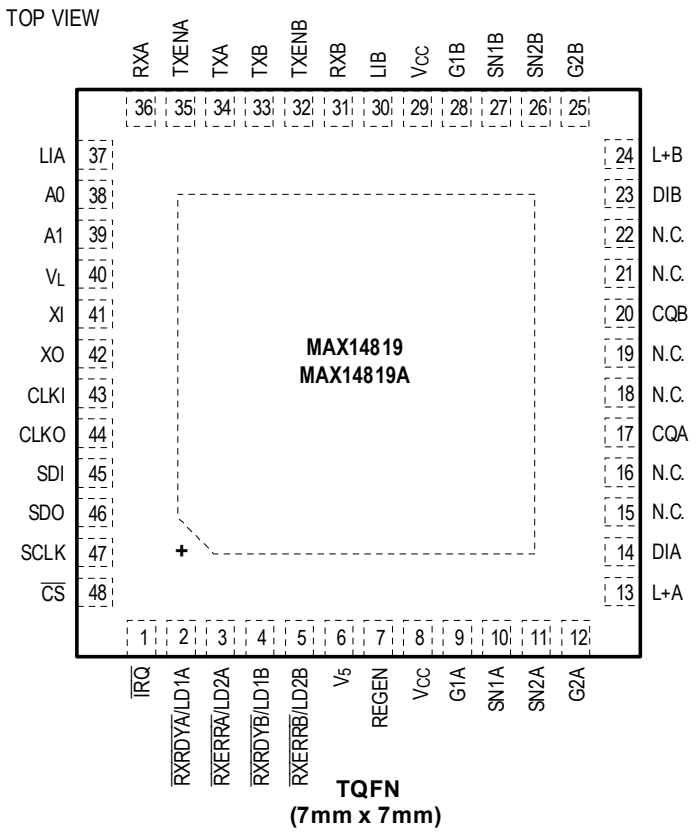








Pin Configuration



Pin Description

PIN	NAME	FUNCTION	REFERENCE
1	$\overline{IRQ}$	Open-drain Interrupt Output. Connect a pullup resistor to $\overline{IRQ}$. $\overline{IRQ}$ asserts whenever a bit that has been enabled in the InterruptEn register is set in the Interrupt register. See the *Register Description* for more information.	GND
2	$\overline{RXRDYA}$/LD1A	Channel A Configurable Open-Drain Receive Data Ready Output/LD1A Driver. Set the RxRdyEnA bit to 1 in the LEDCtrl register to enable $\overline{RXRDYA}$/LD1A as an interrupt output. In this configuration, $\overline{RXRDYA}$/LD1A asserts when the RxDataEnRdyA interrupt bit is set in the Interrupt register. Set the RxRdyA bit to 0 to configure $\overline{RXRDYA}$/LD1A as an open-drain LED driver. When configured as an LED driver, $\overline{RXRDYA}$/LD1A is controlled by the LEDEn1A bit in the LEDCtrl register. Connect a resistor in series to limit the LED current. See the *Register Description* for more information.	GND

Pin Description (continued)

PIN	NAME	FUNCTION	REFERENCE
3	$\overline{\text{RXERRA}}$/LD2A	Channel A Configurable Open-Drain Receive Error Output/LD2A Driver. Set the RxErrEnA bit in the LEDCtrl register to enable $\overline{\text{RXERRA}}$/LD2A as an interrupt output. In this configuration, $\overline{\text{RXERRA}}$/LD2A asserts when the RxErrorA bit in the Interrupt register is set. Set the RxErrEnA bit to 0 to configure $\overline{\text{RXERRA}}$/LD2A as an open-drain LED driver. When configured as a LED driver, $\overline{\text{RXERRA}}$/LD2A is controlled by the LEDEn2A bit in the LEDCtrl register. Connect a resistor in series to limit the LED current. See the *Register Description* for more information.	GND
4	$\overline{\text{RXRDYB}}$/LD1B	Channel B Configurable Open-Drain Receive Data Ready Output/LD1B Driver. Set the RxRdyEnB bit to 1 in the LEDCtrl register to enable $\overline{\text{RXRDYB}}$/LD1B as an interrupt output. In this configuration, $\overline{\text{RXRDYB}}$/LD1B asserts when the RxDataRdyB interrupt bit is set in the Interrupt register. Set the RxRdyEnB bit to 0 to configure $\overline{\text{RXRDYB}}$/LD1B as an open-drain LED driver. When configured as an LED driver, $\overline{\text{RXRDYB}}$/LD1B is controlled by the LEDEn1B bit in the LEDCtrl register. Connect a resistor in series to limit the LED current. See the *Register Description* for more information.	GND
5	$\overline{\text{RXERRB}}$/LD2B	Channel B Configurable Open-Drain Receive Error Output/LD2B Driver. Set the RxErrEnB bit in the LEDCtrl register to enable $\overline{\text{RXERRB}}$/LD2B as an interrupt output. In this configuration, $\overline{\text{RXERRB}}$/LD2B asserts when the RxErrorB bit in the Interrupt register is set. Set the RxErrEnB bit to 0 to configure $\overline{\text{RXERRB}}$/LD2B as an open-drain LED driver. When configured as an LED driver, $\overline{\text{RXERRB}}$/LD2B is controlled by the LEDEn2B bit in the LEDCtrl register. Connect a resistor in series to limit the LED current. See the *Register Description* for more information.	GND
6	V_5	5V Supply Input/Linear Regulator Voltage Output. Connect a 1µF bypass capacitor as close as possible to the IC. Apply an external 5V supply to V_5 if the internal 5V regulator is disabled (REGEN = GND). 5V must be present on V_5 at all times for normal operation.	GND
7	REGEN	5V Linear Regulator Enable Input. Leave REGEN unconnected to enable the internal 5V regulator. Connect REGEN to GND to disable the internal 5V regulator.	GND
8, 29	V_{CC}	V_{CC} Supply Input. Bypass V_{CC} to GND with a 1µF capacitor as close as possible to the device.	GND
9	G1A	Channel A Gate Drive Output 1. Connect G1A to the gate of the external PMOS1A to control the external reverse-current-blocking transistor of sensor supply A (L+A). Leave G1A unconnected if the external PMOS1A is not used.	SN1A
10	SN1A	Channel A Sense Input 1/PMOS1A Source Connection. Connect a current-limiting resistor between SN1A and SN2A. Leave SN1A unconnected when the channel A supply controller is not used.	GND
11	SN2A	Channel A Sense Input 2/PMOS2A Source Connection. Connect a current-limiting resistor between SN1A and SN2A. Connect SN2A to SN1A when current sensing is not used.	SN1A, GND
12	G2A	Channel A Gate Drive Output 2. Connect G2A to the gate of the external PMOS2A for the channel A sensor supply (L+A). Leave G2A unconnected if the external PMOS2A is not used.	SNA1, GND

Pin Description (continued)

PIN	NAME	FUNCTION	REFERENCE
13	L+A	Channel A L+ Sensor Supply Monitoring Input. Connect L+A to the drain of the external PMOS2A current-limiting transistor. Bypass L+A to GND with 0.47µF. Connect a 100Ω resistor in series with L+A (see *Typical Operating Circuit*). Connect L+A to GND or leave unconnected if not used.	GND
14	DIA	Channel A Auxiliary Digital Input. Connect a 100Ω resistor in series with DIA (see *Typical Operating Circuit*).	GND
15, 16, 18 ,19, 21, 22	N.C.	No Connection. Not internally connected.	—
17	CQA	Channel A C/Q Transceiver Input/Output	V_{CC}, GND
20	CQB	Channel B C/Q Transceiver Input/Output	V_{CC}, GND
23	DIB	Channel B Auxiliary Digital Input. Connect a 100Ω resistor in series with DIB (see *Typical Operating Circuit*).	GND
24	L+B	Channel B L+ Sensor Supply Monitoring Input. Connect L+B to the drain of the external PMOS2B transistor to limit the load current sourced by the channel B source supply. Bypass L+B to GND with 0.47µF. Connect a 100Ω resistor in series with L+B (see *Typical Operating Circuit*). Connect L+B to V_{CC} or GND, or leave unconnected if not used.	GND
25	G2B	Channel B Gate Drive Output 2. Connect G2B to the gate of the external PMOS2B for the channel B sensor supply (L+B). Leave G2B unconnected if the external PMOS2B is not used.	SN1B
26	SN2B	Channel B Sense Input 2/PMOS2B Drain Connection. Connect a current-limiting resistor between SN1B and SN2B. Connect SN2B to SN1B or leave unconnected when current sensing is not used.	SN1B
27	SN1B	Channel B Sense Input 1/PMOS1B Source Connection. Connect a current-limiting resistor between SN1B and SN2B. Leave SN1B unconnected when supply controller B is not used.	V_{CC}
28	G1B	Channel B Gate Drive Output 1. Connect G1B to the gate of the external PMOS1B to control the external reverse-current-blocking transistor of sensor supply B (L+B). Leave G1B unconnected if the external PMOS1B is not used.	SN1B
30	LIB	Channel B Logic Output of the Digital Input (DIB). LIB is the logic inverse of the signal on DIB.	V_L, GND
31	RXB	Channel B Logic Output of the CQB Receiver. RXB is the logic inverse of the signal on CQB (when InvCQB = 0).	V_L, GND
32	TXENB	Channel B CQB Transmitter Output Enable. Drive TXENB high to enable the CQB driver. Drive TXENB low at power-up.	V_L, GND
33	TXB	Channel B CQB Transmitter Logic Input. CQB is the logic inverse of the signal on TXB (when InvCQB = 0).	V_L, GND
34	TXA	Channel A CQA Transmitter Logic Input. CQA is the logic inverse of the signal on TXA (when InvCQA = 0).	V_L, GND
35	TXENA	Channel A CQA Transmitter Output Enable. Drive TXENA high to enable the CQA driver. Drive TXENA low at power-up.	V_L, GND

Pin Description (continued)

PIN	NAME	FUNCTION	REFERENCE
36	RXA	Channel A Logic Output of the CQA Receiver. RXA is the logic inverse of the signal on CQA (when InvCQA = 0).	V_L, GND
37	LIA	Channel A Logic Output of the Digital Input (DIA). LIA is the logic inverse of the signal on DIA.	V_L, GND
38	A0	SPI Chip Address Input A0. The MAX14819/MAX14819A is designed to allow up to 4 transceivers on the SPI at one time with a shared $\overline{CS}$ signal. Connect A1 and A0 high or low to set the individual IC SPI address. Do not leave A0 unconnected.	V_L, GND
39	A1	SPI Chip Address Input A1. The MAX14819/MAX14819A is designed to allow up to 4 transceivers on the SPI at one time with a shared $\overline{CS}$ signal. Connect A1 and A0 high or low to set the individual IC SPI address. Do not leave A1 unconnected.	V_L, GND
40	V_L	Logic Level Supply Input. V_L sets the logic level of all logic inputs and outputs (TXEN_, TX_, RX_, LI_, and the SPI interface). Bypass V_L to GND with a 0.1µF capacitor as close as possible to the device.	GND
41	XI	Crystal Oscillator Input for Internal Framer Operation. Connect a crystal between XI and XO to use crystal clocking. Leave XI unconnected if crystal clocking is not used.	V_5, GND
42	XO	Crystal Oscillator Output for Internal Framer Operation. Connect a crystal between XI and XO to use crystal clocking. Leave XO unconnected if crystal clocking is not used.	V_5, GND
43	CLKI	Logic Clock Input for Internal Framer Operation. When not using a crystal for framer operation, connect a 3.686MHz clock signal to CLKI. Connect CLKI to GND when not used.	V_5, GND
44	CLKO	Logic Clock Output for Internal Framer Operation. CLKO outputs a 3.686MHz clock signal when enabled (ClkOEn = 1). When using multiple MAX14819/MAX14819A ICs on a board, these can be clocked with a single crystal by connecting the CLKO output of one device to the CLKI inputs of the other(s).	V_5, GND
45	SDI	SPI Data Input. Connect SDI to the MOSI output of the microcontroller.	V_5, GND
46	SDO	SPI Data Output. Connect SDO to the MISO input of the microcontroller.	V_5, GND
47	SCLK	SPI Clock Input. Connect SCLK to the CLK output of the microcontroller.	V_5, GND
48	$\overline{CS}$	SPI Chip-Select Input. The SPI cycle begins when $\overline{CS}$ is driven low and ends when $\overline{CS}$ is driven high. Up to 4 MAX14819/MAX14819A ICs can share a single SPI bus and $\overline{CS}$ input using the A1 and A0 address inputs.	V_5, GND
EP	—	Exposed Pad. Connect to GND.	GND

Detailed Description

The MAX14819/MAX14819A low-power dual-channel industrial IO-Link master transceiver is fully compliant with the latest SDCI/ IO-Link standards and test specifications. The MAX14819/MAX14819A features two integrated framers but can alternatively operate with external UARTs.

The MAX14819/MAX14819A features a high-speed SPI interface for system-side data and control interfacing. Integrated IO-Link message frame handlers and FIFOs simplify time critical control and cycle time management of all IO-Link M-sequence communication, easing data link layer control. Autonomous cycle timers also reduce the need for accurate controller timing. Integrated establish-communication sequencers simplify wake-up management.

The MAX14819/MAX14819A further includes two sensor supply controllers (L+A, L+B) with current limiting and reverse current blocking. The current limit is set with external sense resistors.

POWER

Power-Up

The CQ_ driver outputs are high impedance when the V_{CC} supply, V_5, and V_L voltages are below their respective undervoltage thresholds during power-up.

The drivers are automatically disabled when the V_{CC} voltage falls below the 9V (typ) UVLO threshold. The SPI interface remains active while V_5 and V_L are present.

V_{CC} Low Voltage and Undervoltage Detection

The MAX14819/MAX14819A monitors the V_{CC} supply for low-voltage and undervoltage conditions. Low-voltage warnings are reported in the Status register and can be configured to generate an interrupt on the $\overline{IRQ}$ output.

When V_{CC} falls below the 18V (max) low-voltage warning threshold, the VCCWarn and VCCWarnCOR bits in the Status register are set. If VCCWarnCOR in the Clock register is set, a StatusInt interrupt is generated and $\overline{IRQ}$ asserts.

When V_{CC} falls below the 9V (max) undervoltage-lockout (UVLO) threshold, the VCCUV and VCCUVCOR bits in the Status register are set. A StatusInt interrupt is generated and IRQ asserts.

5V Linear Regulator

The MAX14819/MAX14819A includes an integrated regulator to generate 5V (V_5). To enable the internal regulator, leave REGEN unconnected and connect a 1µF bypass capacitor between V_5 and ground as close as possible to the device. The internal V_5 regulator is capable of driving external loads up to 20mA.

When the internal 5V linear regulator is not used, V_5 is the supply input for the internal analog and digital functions and must be supplied externally. Connect REGEN to ground to disable the internal regulator when applying an external 5V to V_5. Ensure that V_5 is present for normal operation.

An internal undervoltage lockout comparator detects when the V_5 voltage falls below the 3.5V (typ) V_{5_UVLO} threshold. When the V_5 voltage drops below this level, the device is under reset: SPI registers are reset to their power-up state, the CQ_ outputs and L+_ supplies are disabled, internal pullups/pulldowns are turned off, the CQ_ and DI_ receivers are disabled, and the LED outputs are high impedance. When the V_5 voltage rises above the UVLO threshold, the MAX14819/MAX14819A restarts in the default power-on configuration.

The internal V_5 regulator output is not protected against short circuits.

Logic Supply (V_L)

The V_L input is the logic-level supply for all the digital I/Os. Apply a voltage between 1.62V and 5.5V to V_L for normal operation.

Internal UVLO circuitry monitors the V_L supply. If V_L falls below the 0.7V (typ) V_L UVLO threshold, all the digital I/Os referred to V_L are ignored and either set to high impedance or are low.

L+ Sensor Supply Controllers

The MAX14819/MAX14819A includes one sensor/actuator supply controller for each IO-Link channel, L+A and L+B. Each sensor supply is configurable through the SPI interface and must be enabled by setting the L+En_ bit in the L+Cnfg_ register. Using external pMOS transistors, these controllers provide active current limiting, reverse current blocking, and undervoltage detection. The 24V V_{CC} field supply input is tolerant to reverse voltage and the L+A/L+B output is negative voltage capable down to V_{CC} - 60V.

Setting the L+_ Current Limit

The L+_ sensor supply current is limited by placing a sense resistor between the SN1_ and SN2_ current-sense inputs. When the voltage across the resistor reaches the V_{CL_T} (15mV, typ) threshold, the gate of the pMOS (G2_) is actively controlled to limit the load current such that:

$$I_{LIM} = V_{CL\_T/RSENSE}$$

If the L+_ voltage is pulled below ground (< -3V), the current limit is reduced to about 10% of normal value to reduce the power dissipated in the external pMOS.

L+_ Blanking Time and Autoretry Functionality

The L+_ controllers have programmable variables (set in the L+Cnfg_ registers) that allow the system to optimize turn-on and charging large loads while protecting the pMOS FETs in cases of shorts and challenging load conditions.

If the load current is in current limiting for a period exceeding the set blanking time, the gate drive (G2_) is turned off. The sensor supply is then either turned off until the controller reenables it, or is turned on again following the autoretry delay.

To further reduce the power dissipated in the pMOS transistors during turn-on of loads that require large inrush currents (e.g., capacitive loads), the current limiter includes a dynamic blanking time mode that reduces the blanking time when the voltage across the pMOS is high, limiting the pulse energy during the initial turn-on phase. Dynamic blanking time mode is operational when the L+_ output voltage is below 18V and must be enabled by setting the L+DynBl_ bit in the L+Cnfg_ register.

The MAX14819/MAX14819A current-limit circuitry also includes the option to double the L+_ load current when the L+_ supply voltage is above 18V. This functionality is enabled by setting the L+CL2x_ bit in the L+Cnfg_ register.

Bypassing the L+_ Sensor Supplies

When the internal L+_ supply controllers are not used, leave all the associated pins (G1_, G2_, SN1_, SN2_, L+_) unconnected. L+_ can also be connected to GND.

CQ_ Transceivers

The CQA and CQB drivers are independently configurable as push-pull, NPN, PNP mode outputs in the SPI registers. Set the bits in the CQCfgA and CQCfgB registers to configure the drivers, enable or disable internal pullup and pulldown current sources on the CQ_ I/Os, and to set the digital input thresholds. The CQ_ drivers can also be enabled/disabled in these registers.

CQ_ Current Limit and Thermal Protection

The MAX14819/MAX14819A features a selectable current limit for both CQ_ drivers ranging from 100mA to 500mA. Set the CL[1:0] bits in the DrvrCurrLim register to select the current limit for the drivers.

The CQ_ drivers are independently thermally protected. If one output driver temperature rises above the 160°C threshold, that output is disabled until the temperature drops below 145°C.

CQ_ Driver Fault Detection

The MAX14819/MAX14819A senses a fault condition on the CQ_ driver when an overcurrent event exists for longer than the blanking time. Both the current limit and blanking time can be configured in the DrvrCurrLim register.

When a short-circuit fault occurs on CQ_, the CQFault_ and CQFaultCOR_ bits in the ChanStat_ register are set and can trigger an interrupt.

When an overcurrent event occurs on CQ_, the driver can either be set to continue supplying the selected current until the device enters thermal shutdown (autoretry is disabled), or to enter autoretry mode. In autoretry mode, the driver is automatically disabled after the current blanking time and is then reenabled.

CQ_ Reverse-Polarity Protection

The CQ_ outputs are protected against reverse polarity vs. ground. If CQ_ is connected to a negative voltage, the driver is automatically disabled and CQ_ is set to high impedance.

When CQ_ is shorted to a voltage above V_{CC}, the driver is automatically disabled and the output is set to high impedance.

During a reverse condition, positive or negative, when no fault is detected on CQ_ but the internal diode begins to overheat, the L+_ supply is immediately disabled (turning off the external transistors) to protect the device.

Reverse conditions do not generate a fault or interrupt.

CQ_ Current Sources/Sinks

The MAX14819/MAX14819A features programmable internal 2.5mA/5.8mA pullup/pulldown current sources on the CQ_ receivers. Select the pullup/pulldown current for each CQ_ I/O by setting the SinkSel_[1:0] bits in the CQCfg_ register. The internal pullup/pulldown currents are automatically disabled when the CQ_ output is driven (i.e., push-pull not in high-impedance state, NPN mode is set low, or NPN mode is set high).

CQ_ Receiver Output (RXA/RXB)

RX_ is the output of the CQ_ receiver. By default, the RX_ output is the inverse logic of the CQ_ input. Setting the InvCQ_ bit in the MsgCtrl_ register inverts CQ_ so that the RX_ output is the same logic of the CQ_ input. RX_ cannot be disabled/three-stated.

CQ_ Receiver Threshold

The CQ_ receiver thresholds are compliant with the IO-Link standard by default. The receiver thresholds are also configurable to be compatible with the IEC 61131-2 type 1 and type 2/3 digital inputs. Set the IEC3Th_ bit in the CQCfg_ register to select the input thresholds for each receiver.

CQ_ Receiver Deglitch

The CQ_ receivers feature a selectable glitch filter for improved noise immunity. Enable/disable this filter by setting the CQFilterEn_ bit in the CQCfg_ register. Transients longer than 1.3µs (typ) are ignored when the glitch filter is enabled.

DI_ Receiver

The MAX14819/MAX14819A includes two auxiliary digital inputs: DIA and DIB. These inputs are protected against reverse polarity (referred to V_{CC} and/or GND).

DI_ inputs are configurable in the IOStCfg_ registers. Set the DiCSource__ bit to enable the internal 2.4mA source on the DI_ input. Set the DiCSink_ bit to enable the 2.4mA sink on the input.

Each DI_ input also features a selectable glitch filter for improved noise immunity. Transients longer than 1.3µs (typ) are ignored when the glitch filter is enabled. Set the DiFilterEn_ bit to enable or disable this filter. When the glitch filter is enabled, signal pulses less than 1µs are ignored on the DI_ input.

The DI_ receiver thresholds are configurable to be compatible with the IEC 61131-2 type 1, and type 2/3 digital inputs. Set the DiEC3Th_ bit in the IOStCfg_ register to select the input thresholds for each receiver.

SPI Interface

The MAX14819/MAX14819A is connected to a microcontroller or SPI-host through an SPI-compatible serial interface. The interface has three inputs: clock (SCLK), chip select (CS), and data in (SDI), and one output, data out (SDO). SDO is high impedance when CS is high, allowing multiple SPI slave devices to share a common bus. The SPI is not daisy-chainable. The maximum SPI clock rate is 20MHz when V_L > 2.5V.

The SPI interface logic complies with SPI clock polarity (CPOL = 0) and clock phase (CPHA = 0). The SPI interface supports both byte-by-byte cycle and burst mode read and write.

In both read and write cycles, the SDO signals the IRQ status, as well as the receive-data-ready and receive-data-error for both receivers A and B (Figure 6 and Figure 7).

The SPI interface is not available when the V_L voltage is below the 0.7V (typ) V_L UVLO threshold or when 5V is not present on V_5. The SPI registers are reset to their default state when the V_5 voltage falls below the 3.5V V_5 UVLO threshold.

SPI Chip Address (A1, A0)

The MAX14819/MAx14819A is designed to allow up to four master transceivers on a single bus with a single/shared CS. This is accomplished using SPI-addressable devices with logic address inputs A1 and A0. See Table 1. Do not leave the A1 or A0 address input unconnected. Each chip on the SPI bus should be assigned an individual chip address.

The MAX14819/MAX14819A monitors the SPI address in each read/write cycle and responds when the SPI address matches the pin-programmed address for that IC.

SPI trigger commands are global and are not filtered by the chip address. All MAX14819/MAX14819A devices connected to the SPI bus will react to a received trigger command.

SPI In-Band IRQ Interrupt

The addressed MAX14819/MAX14819A sends out an IRQ bit on SDO in every SPI cycle (both in single cycle as well as burst mode), beginning on the third SPI clock. This bit is equivalent to the IRQ interrupt output pin logic, but inverted (active high). The IRQ bit is set when the $\overline{IRQ}$ pin is asserted. Similarly, when the $\overline{IRQ}$ output is high impedance, the IRQ bit is 0. See Figure 6 and Figure 7.

The IRQ bit cannot be masked.

SPI In-Band Device-Message-Ready Signaling

In addition to sending IRQ status, the addressed MAX14819/MAX14819A can be enabled to also send out 2 bits per channel in every SPI cycle that provide information, whether the IO-Link device answer message was received correctly (RRDY_) or in error (RERR_) (Figure 6 and Figure 7). Set the RMessgRdy_ bits in the MesgCrtl_ register to enable this functionality.

Table 1. SPI MAX14819/MAX14819A Chip Address Select

A1	A0	DEVICE ADDRESS
LOW	LOW	00
LOW	HIGH	01
HIGH	LOW	10
HIGH	HIGH	11

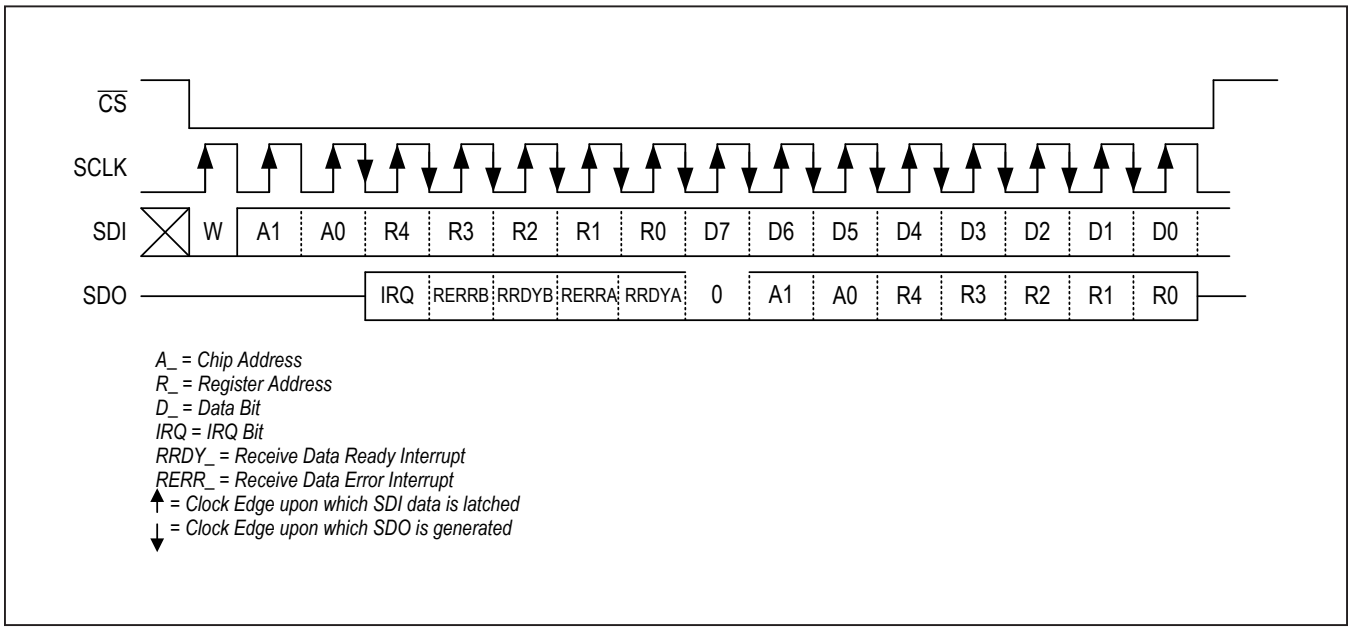


Figure 6. SPI Byte-by-Byte Write Cycle

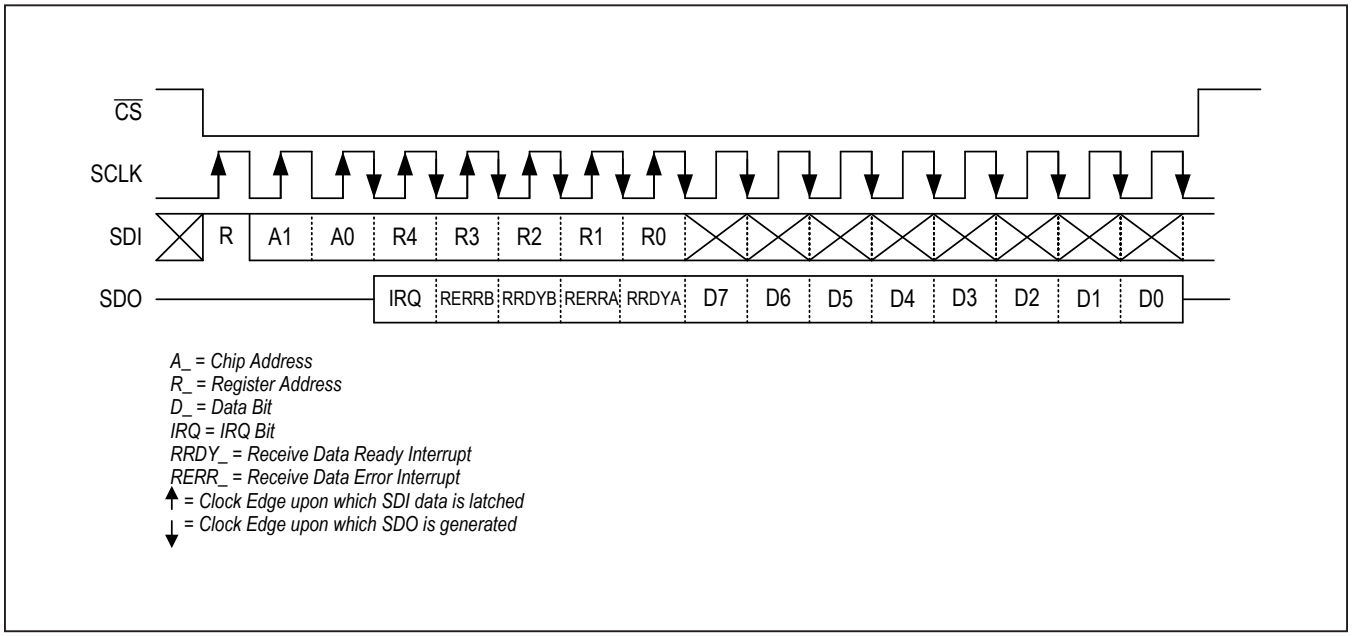


Figure 7. SPI Byte-by-Byte Read Cycle

The RRDY_ bits are equivalent to the DtaRdy_ hardware outputs. Similarly, the RERR_ bits are the equivalent to the RxErr_ hardware outputs. The SDO bit logic is the inverse of the pin logic: when the pin output is low, the associated bit is set to 1, and when the pin output is high, the associated bit is 0.

The RRDY_ bits and the $\overline{\text{RXRDY\_}}$ pins are cleared automatically when the device message is read out of the RxFIFO_.

SPI Burst Access

Burst access allows SPI reading/writing of two or more bytes in a single SPI cycle. The chip-select input ($\overline{\text{CS}}$) must be held low during the entire burst write/read cycle. The SPI clock must continue clocking throughout the burst access cycle. Only the initial register address is sent, followed by multiple bytes of data. The burst cycle ends when the SPI master pulls $\overline{\text{CS}}$ high. See Figure 8.

When performing a burst read or write of/to the TxRxData_ registers, the register address remains the same, allowing fast loading of a master message into the TxFIFO_ and reading of the device message out of the RxFIFO_.

When burst reading or writing of registers having a higher address than the TxRxData_ registers, the register address is automatically incremented, allowing reading and writing of a consecutive register block by only defining the initial register address in the SPI command byte.

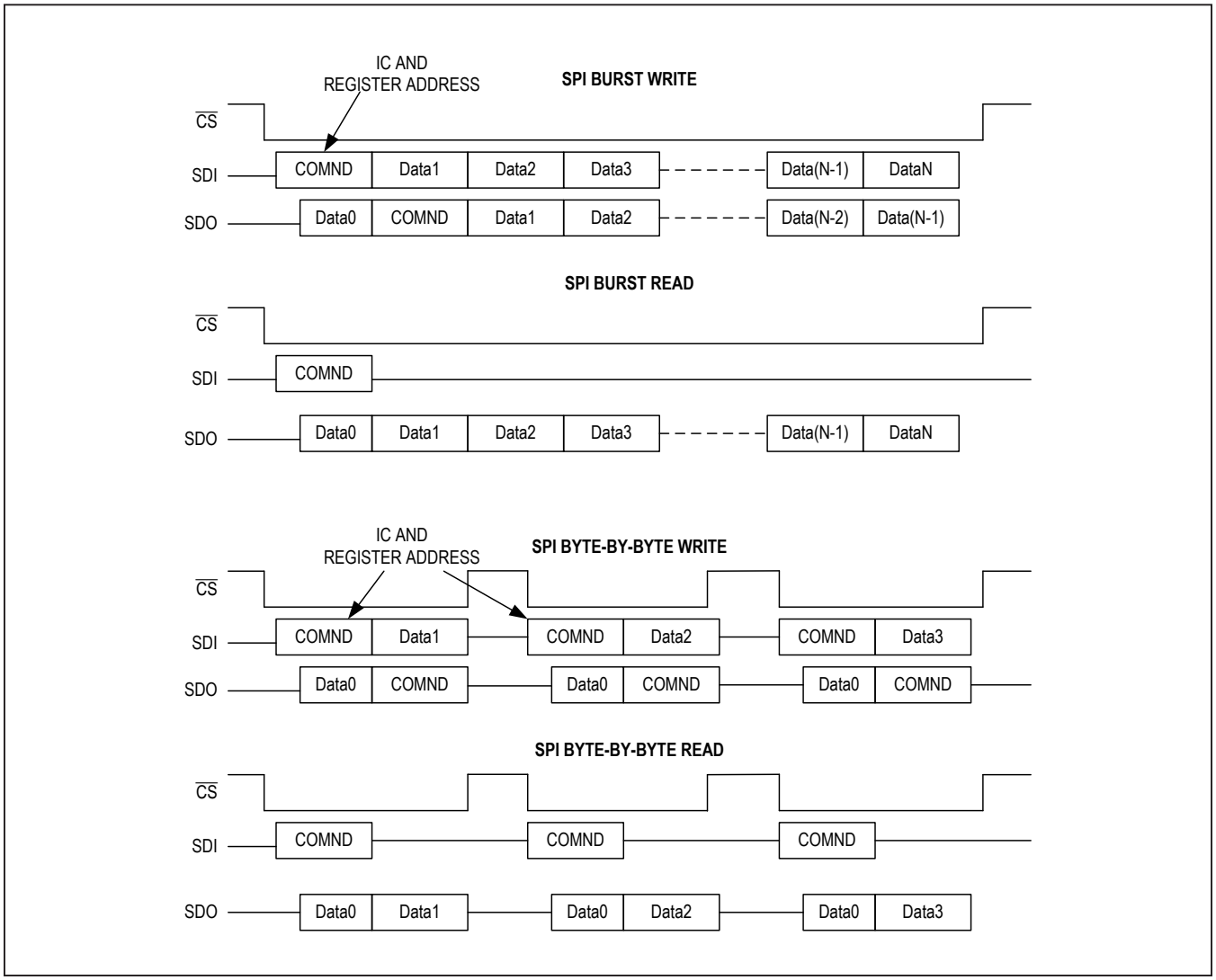


Figure 8. SPI Burst Read/Write and Byte-by-Byte Read/Write Overview

Wake-Up Pulse Generation

The MAX14819/MAX14819A can automatically generate a wake-up pulse to initiate IO-Link communication. Set the CQ_ driver into receive mode (TXEN = low or TxEn_ = 0), and drive TX_ low or set the Tx_ bit to 0 before the wake-up sequence begins. Set the WuPuls_ bit to begin the wake-up sequence. When the WuPuls_ bit is set, the MAX14819/MAX14819A samples the CQ_ voltage level and then automatically enables the CQ_ driver. A 500mA current pulse of opposite polarity is applied to the CQ_ line for 80µs (typ). During the wake-up pulse, the CQ_ current limit is temporarily set above 500mA internally, although the CL_ register bits are not changed. The driver remains enabled, the line returns to the original polarity, and after a 100µs (typ) delay the MAX14819/MAX14819A CQ_ driver is set to high impedance (Figure 9). The WuPuls_ bit is automatically cleared after the t_{ON_WU} delay.

Microcontroller Data Interface

The MAX14819/MAX14819A offers two interface options for IO-Link communication. When used as a transceiver, external UARTs are required in the microcontroller and these are interfaced to the TX_, RX_ and TXEN_ pins. If the IO-Link framers in the MAX14819/MAX14819A are used, then the SPI is used for interfacing to the microcontroller.

Framer Communication

The MAX14819/MAX14819A includes two independent IO-Link framers with UARTs, one for each CQ_ channel. Each framer operates in a Master-message (TX)/Device-message (RX) doublet, verifying communication timing and data transmitted/received. After a channel has completed transmission of a master message, the framer is automatically switched into receive mode. When the expected number of bytes has been received, the framer automatically exits from receive mode and any further received data is ignored.

Shortly before, during, and after the frame handler sends and receives messages, its transmitter must be disabled. Disable the transmitter by either driving the associated TXEN_ pin low, or by setting the TXTXENDis bit to 1. Note that the TXTXENDis bit is global and acts on both channels.

UART Framing

The UART frame is made up of one start bit, 8 data bits with 1 even parity bit and 1 STOP bit. When transmitting, the idle time between the STOP bit and the following START bit is less than 1 bit interval.

Frame Handler FIFOs (TxRxFIFOA/TxRxFIFOB)

Each IO-Link channel on the MAX14819/MAX14819A (CQA and CQB) has a transmit and receive FIFO for buffering the IO-Link M-sequence messages that are sent and received. These FIFOs have a depth (66 bytes) to buffer the largest M-sequence, Type 2.V, in addition to the two length bytes.

Transmit/Receive FIFO Data Structure

To ensure proper communication, the message from the SPI master to the TxFIFO_ must follow the sequence shown in Figure 10.

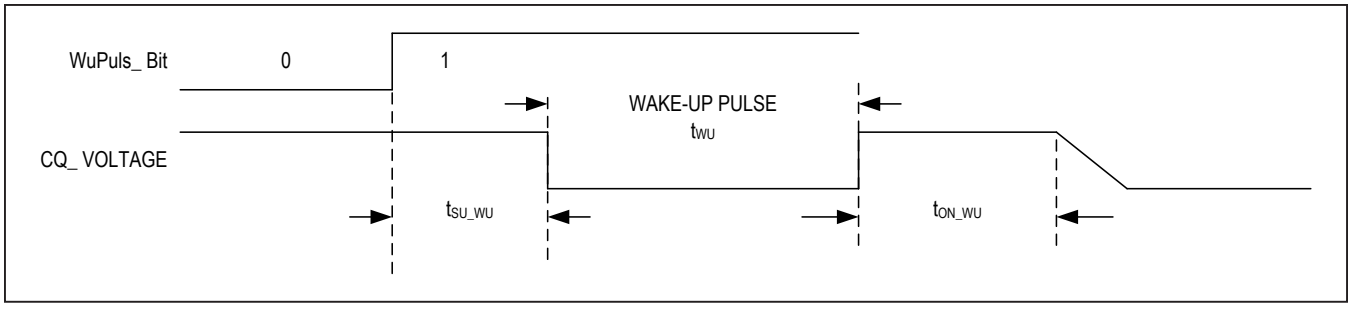


Figure 9. Wake-Up Timing

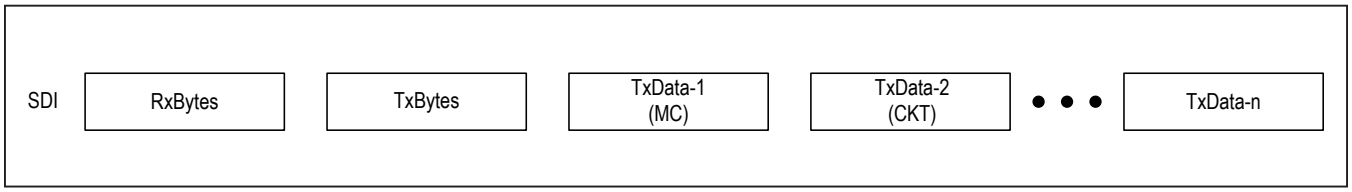


Figure 10. Transmit SPI Data Write Sequence

RxBytes is the number of octets the IO-Link device is expected to reply with after it receives this master message. TxBytes is the number of bytes that the master will send to the device in this message (the master message length).

The IO-Link device answers with the device message, which is stored in the RxFIFO_. When the RxFIFO_ on the MAX14819/MAX14819A is read, the data is formatted as shown in Figure 11. RxBytesAct is the actual number of bytes received from the device and available for readout from the RxFIFO_. This may differ from the expected number of receive bytes (RxBytes).

Loading the Transmit FIFO (TxFIFO_)

The master message is loaded into the transmit FIFO (TxFIFO_) through the SPI interface. The SPI master needs to send three pieces of information to the TxRxData_ register for a complete master message (Figure 12):

1) A byte describing the expected number of bytes of the IO-Link device reply message. This is RxBytes.
2) A byte describing the number of bytes in the master message (the length that will be transmitted). This is TxBytes.
3) The data for the master message.

The TxBytes byte signals the number of octets in the master message and the RxBytes indicates the number of octets expected from the device in the response message.

Set the TSizeEn_ bit in the MsgCtrl_ register to compare the TxBytes information to the number of octets loaded in the TxFIFO_ and verify that the full message has been received by the SPI master. The TSizeEn_ functionality can be used either for byte-by-byte FIFO loading or for burst loading. When a size error is detected, a TSizeErr_ interrupt is generated.

The TxFIFO_ can be written to using byte-by-byte write or a burst write. When loading the TxFIFO_ with byte-by-byte writing, the CQ_ transmission can be started before the complete master message is loaded into the TxFIFO_ (transmission and TxFIFO_ loading can be done in parallel). In this case, the SPI controller must set the InsChks bit in the MsgCtrl_ register to 0 and include the 6-bit checksum in the master message CKT octet, since the MAX14819/MAX14819A cannot calculate it. The MAX14819/MAX14819A can only generate a TChkSmEr_ interrupt after the whole message is loaded into the TxFIFO_; if transmission is started before the full message was loaded, it is possible that the IO-Link device will receive a message with a checksum in error.

When transmission starts after the TxFIFO_ is completely loaded, the MAX14819/MAX14819A can calculate and insert the checksum (when InsChk_= 1) into the CKT octet. Alternatively, the SPI master can insert the checksum in the master message and the MAX14819/MAX14819A will verify the data (SPIChks_ = 1). If a checksum error is detected, a TChksmEr_ interrupt is generated and the MAX14819/MAX14819A does one of

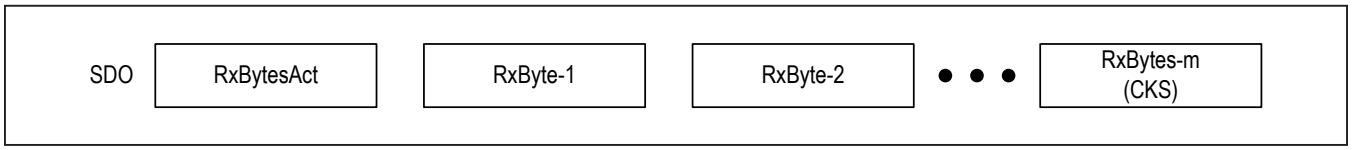


Figure 11. Receive SPI Data Read Sequence

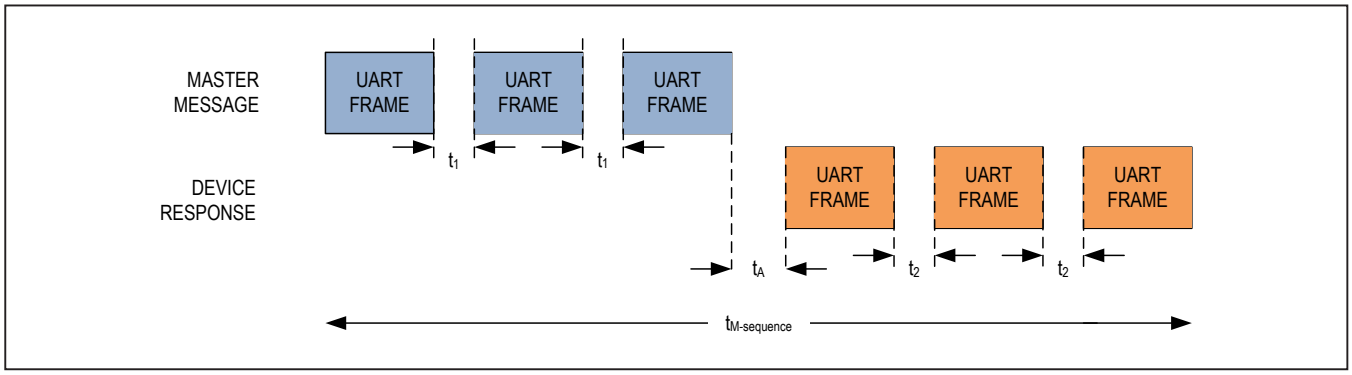


Figure 12. Message Timing

two things, depending on the state of the TxErDestroy_ bit in the MsgCtrl_ register:

- If TxErDestroy = 1: The MAX14819/MAX14819A will not send the message, so the SPI master must reload the message into the TxFIFO_ in time for the cycle time.
- If TxErDestroy = 0: The MAX14819/MAX14819A sends the message with the error.

Initiating Transmission

Transmission on CQ_ is initiated either by setting the CQSend_ bit in the CQCtrl_ register or by using a trigger command (see the TrigAssgn_ register for more information). Transmission can also be initiated cyclically when the internal cycle time is enabled (CyclTmrEn_=1).

When SPI burst write mode is used, transmission must be initiated after the TxFIFO_ is loaded or the MAX14819/MAX14819A generates a cycle error interrupt (TCycleErr_ = 1).

When using byte-by-byte SPI write mode, transmission can be initiated before the complete master message is loaded. When using this mode, ensure that the TxFIFO_ always has at least 1 data byte stored in it to avoid any idle time or errors. The TxFIFO_ transmission is halted and the CQ_ transceiver is configured to receive mode as soon as the TxFIFO_ is empty.

During transmission, the CQ_ transmitter is set to push-pull mode. CQ_ is restored to the previous state when transmission is complete.

Transmit Loopback Check

The internal framers automatically verify transmitted data through a loopback check. During transmission, the signal at CQ_ is automatically routed to the receiver and the message sent is checked against the data sent out. If inconsistencies are detected (e.g., when a CQ_ line is shorted), the TransmErr_ bit is set and a TxError_ interrupt can be generated.

Receiving the Device Message

When the MAX14819/MAX14819A completes transmission of the master message to the IO-Link device, the CQ_ transmitter is set to receive mode within 3µs (typ) and the master waits for the device reply message. The MAX14819/MAX14819A waits for 9 to 24 bit times (set by the DDelay_ bits in the DeviceDly_ register) for a valid START from the device.

From the RxBytes data in the master message, the MAX14819/MAX14819A already knows the number of bytes expected to be returned from the device. If the number of bytes received is not the expected number, a RSizeErr_ interrupt is generated. The receiver stops reception when the number of received bytes equals the value in RxBytes and any further data sent from the device is ignored. Reception is also terminated when less bytes are received than expected. The MAX14819/MAX14819A determines this to be the case when no START bit occurs within 2 to 5 bit times (as set in the BDelay_ bits in the DeviceDly_ register) after the last character's STOP bit.

When the device message is received successfully (without any errors), an RxDataRdy_ interrupt is signaled to the host SPI controller by asserting the $\overline{IRQ}$ pin (if (RDaRdyIntEn = 1) and/or by asserting the $\overline{RXRDY}$_/LD1_ pin when the received data (device message) is ready for readout from the RxFIFO_. The host controller can read out the message from the RxFIFO_ in byte-by-byte mode or in a single-burst SPI cycle. The $\overline{IRQ}$ and/or $\overline{RXRDY}$/LD1_ interrupts are automatically cleared when the first byte of the message is read out of the RxFIFO_, or alternatively, by reading the Interrupt register.

If the device message is not received successfully (i.e., received with an error), an RxError_ interrupt is signaled to the host controller by asserting the $\overline{IRQ}$ pin (if RxErrIntEn_ = 1) and/or by asserting the $\overline{RXERR}$_/LD2_ pin. Detected errors in the received data can include checksum, parity, UART framing, or size deviations. The RxError_ interrupt is cleared only when the Interrupt register is read.

Monitoring Message Timing

The IO-Link standard requires that the device reply message must be fully received within a time of $t_{M\text{-sequence}}$ after the start of the communication cycle:

$$t_{M\text{-sequence}} = (m+n) \times 11 \times T_{BIT} + t_A + (m-1) \times t_1 + (n-1) \times t_2$$

where m is the number of octets in the master message, n is the number of octets in the device message, T_{BIT} is the bit time at the present COM data rate, t_A (max) is 10 bits, t_1 is a maximum of 1 bit, and t_2 is a maximum of 3 bits (Figure 12).

The MAX14819/MAX14819A can be set to generate an error if the device message is not completely received in the expected $t_{M\text{-sequence}}$ window. Set the RspnsTmrEn_ bit in the DeviceDly_ register to enable the internal message timing monitor.

While the IO-Link standard specifies $t_{M\text{-sequence}}$ as the longest allowable delay, actual IO-Link devices may exhibit longer delays (e.g., a longer delay can occur when t_A exceeds more than 10 x T_{BIT}). The MAX14819/MAX14819A can be set to allow for these tolerances. Set the BDelay_[1:0] and DDelay_[3:0] bits in the DeviceDly_ register to add additional delay. For IO-Link compliance, set BDelay_[1:0] = 01b and DDelay_[3:0] = 0001b. If a device

message is not received or not completely received in this time, the RxErr_ interrupt is signaled.

Response Time Checking (MAX14819A Only)

When the RspnsTmrEn bit is 0 (RspnsTmrEn = 0), the MAX14819A does not check the message response delay (T_A) cycle time. This response time checking is not done whether the cycle timer is enabled or disabled. When RspnsTmrEn = 0, the receive FIFO waits for a device to answer the message with no time limit on the response. If the IO-Link device does not reply, the MAX14819A does not send a new message after the cycle timer expires (if the cycle timer is enabled). When this occurs, the SPI master must reset the RxFIFO by setting the RxFIFORst bit (RxFIFORst = 1). Setting RxFIFORst = 1 puts the receiver in idle mode and resumes normal cyclic operation.

Checksum Calculation and Checking

The MAX14819/MAX14819A can perform standard IO-Link 6-bit checksum calculation and checksum verification. This can be used to generate the master message checksum automatically, to check the integrity of the master message from the SPI master to the TxFIFO_, and to check the received device message.

Set the InsChks_ bit in the MsgCtrl_ register to enable master-message checksum generation. When enabled, the checksum bits from the SPI master are ignored and the MAX14819/MAX14819A inserts the calculated checksum bits into the CKT octet before transmission. The master message must be completely loaded into the TxFIFO_ before transmission for the MAX14819/MAX14819A to insert the calculated checksum into the message.

Set the SPIChks_ bit in the MsgCtrl_ register to enable the MAX14819/MAX14819A to verify the current checksum in the CKT octet in the TxFIFO_ with the calculated master-message checksum. If a difference is detected, a TChksmEr_ interrupt is generated. When the TxErDestroy_ bit in the MsgCtrl_ register is set, the master message is deleted in the TxFIFO_ and is not sent to the IO-Link device. In SPI byte-by-byte write mode, the master message is deleted only if the complete master message has been loaded into the TxFIFO before transmission is initiated.

Establish-Communication Sequencer

The MAX14819/MAX14819A features an integrated IO-Link establish-communication sequencer to autonomously perform the IO-Link establish-communication wake-up sequence. The wake-up sequence is the prerequisite for placing the device in IO-Link pre-operate and operate modes. Set the EstCom_ bit in the CQCtrl_ register to begin the autonomous establish-communication sequencer.

When the EstCom_ bit is set, the MAX14819/MAX14819A generates an 80µs (typ) wake-up pulse on the CQ_ line and then autonomously determines the COM rate and minimum cycle time of the attached IO-Link device. During this time, the microcontroller should not initiate driver activity on the CQ_ interface until the establish communication sequence is complete. Once the sequence is successfully completed, the COM rate of the IO-Link device is stored in the ComRt_ bits of the CQCtrl_ register. Similarly , the minimum cycle time of the device is stored in the CyclTmr_ register.

If the first establish-communication sequence fails, the MAX14819/MAX14819A repeats the sequence again after a 30ms delay. If the sequence fails again, a third attempt is made. If the third attempt fails, the MAX14819/MAX14819A stops attempting to establish communication with the device and a WURQInt interrupt is generated, the EstCom_ bit is reset, and the CQ_ driver is returned to SIO mode after 300ms (max). A new establish-communication sequence can then be initiated by the SPI controller by setting the EstCOM_ bit.

Transmitter Synchronization

The start of master-message transmission can be synchronized on multiple IO-Link ports, so that ports that operate with the same cycle time receive the master message simultaneously. Triggering allows synchronization of master ports on one or many MAX14819/MAX14819A devices being driven by a common SPI. Assign the same trigger value to ports that will be synchronized in the TrigAssgn_ registers and enable synchronization by setting the TrigEn_ bit.

Write an SPI trigger value to the Trigger register to initiate immediate transmission of the data in the TxFIFOs assigned to that trigger value. Trigger is a global SPI command and is not filtered by the SPI address bits, making it possible to synchronize the transmitters of multiple MAX14819/MAX14819A devices on a single SPI bus with a single trigger command.

Trigger functionality can also be used with the internal cycle timer. When configured for this, the cycle timer is immediately started when its trigger value is received.

Trigger Delay and Synchronization Accuracy

The delay between the time when the MAX14819/MAX14819A receives a trigger command and the time when the associated CQ_ transmitter starts transmission is made up of a fixed and a variable component, which depends on the UART data rate. The time (t_{TRIG}) between the last rising edge of the serial clock (SCLK) and the beginning of the CQ_ START bit is:

- COM3: 0.813µs ≤ t_{TRIG} ≤ 1.085µs
- COM2: 4.881µs ≤ t_{TRIG} ≤ 6.508µs
- COM1: 39.060µs ≤ t_{TRIG} ≤ 52.080µs

The reference point is the time when the trigger command is received by the MAX14819/MAX14819A. This occurs on the final (i.e., the 16th) SPI clock's low-to-high transition (Figure 13).

When synchronizing multiple CQ transmitters, the trigger delay skew of the CQ_ transmitter outputs is based on the triggering delays of each transmitter (see Figure 14). This skew has a baud-rate-dependent component, similar to the trigger accuracy equation for a single transmitter output. Calculate the CQ_ transmitter output skew using the following equation:

$$t_{TRIG\_SKEW}\ (max) \le (4BT_S - 3BT_F) / 16$$

Where BT is the bit time of the CQ_ data (= 1/COM rate), BT_S is the bit time of the lower bit rate (e.g., COM1), and BT_F is the bit time of the faster bit rate.

When synchronizing ports that use the internal cycle timers, the skew between channels will be larger, ranging from 0µs to (BT/16 + 101µs).

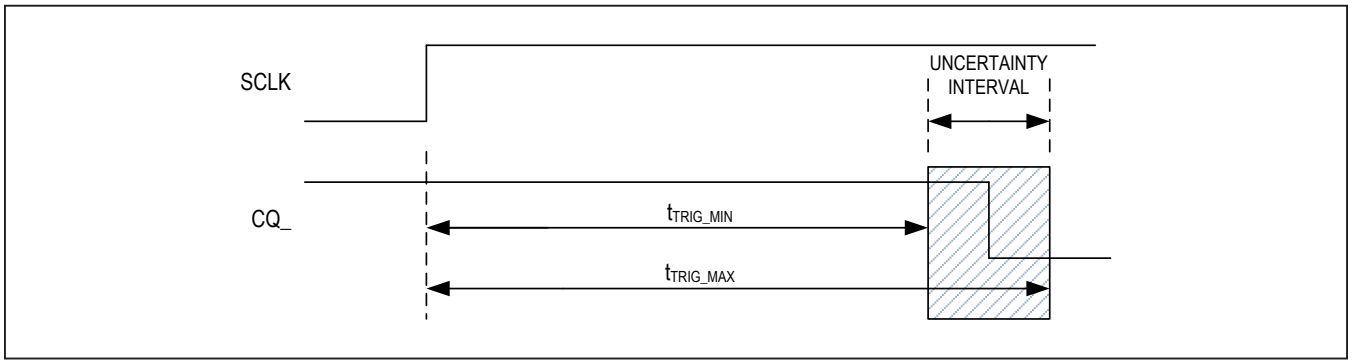


Figure 13. Trigger Delay

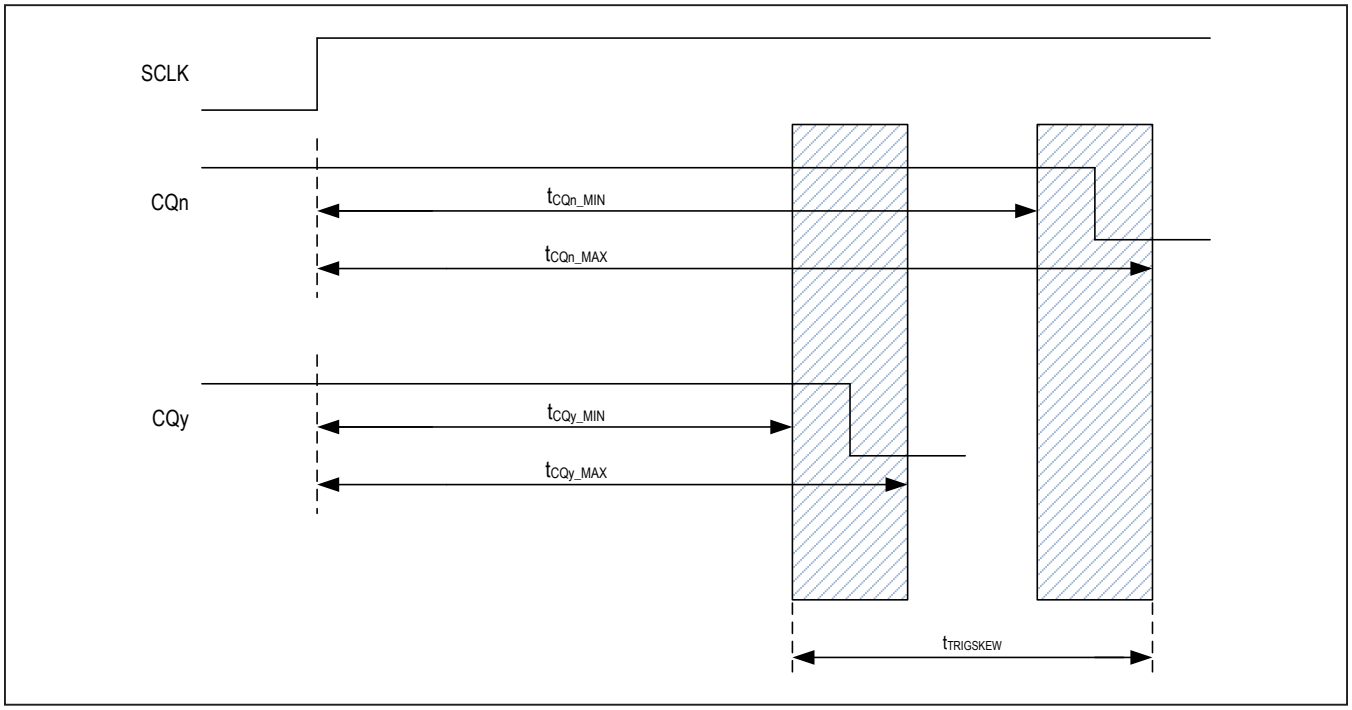


Figure 14. Master-Message Trigger Skew

Cycle Timer

The MAX14819/MAX14819A features two cycle timers (one for each CQ_ transceiver) that autonomously send the master message from the TxFIFO_ at predefined time intervals. The bits in the CyclTmr_ register set the time interval. The smallest cycle time supported by the cycle timer is 400µs.

The minimum cycle time of the attached IO-Link device is automatically determined during the establish-communication sequence and is stored in the CyclTmr_ register. If the device returns a minimum cycle time value of 0x03 or less, then this will be shown in the associated CycleTmr_ register, however the actual cycle time will be set to 400µs. The SPI master can overwrite these values with the cycle time required by the application.

Set the RspnsTmrEn bit to 1 (RspnsTmrEn = 1) for normal cycle timer operation. See the *Response Time Checking (MAX14819A Only)* section to operate the cycle timer without checking the message response delay, T_A.

To start the cycle timer sending the first master message, either send its trigger value or set the CQSend_ bit in the CQCtrl_ register.

At the start of each cycle, the CQ_ transmitter is enabled and the master message sent. The CQ_ transceiver is then automatically switched to receive mode (within 1 bit interval) and the MAX14819/MAX14819A waits for the IO-Link device response message. When the complete device message is received, an RxDataRdy_ interrupt is triggered.

When the data ready interrupt is triggered, the SPI master must read out the device message from the RxFIFO. The following master message must then be written into the TxFIFO, if the TxKeepMsg_ bit is not set. A TxError_ interrupt is generated due to TCycleErr_ if the SPI master does not load the next master message in time.

Clocking

If external UARTs of a microcontroller are used, external clock sources are not required since the MAX14819/MAX14819A has adequate internal clocking. If the internal framers are used instead of external UARTs, external clocking from a crystal or clock source is required to achieve the timing accuracy required for IO-Link communication (Figure 15). Set the ClkDiv[1:0] bits in the Clock register to select the input (crystal or clock) frequency: 3.686MHz, 7.372MHz, or 14.745MHz. Set the ComRt_[1:0] bits in the CQCtrl_ register to determine the COM rate on the CQ_ interface. Set the ExtClockEn bit in the Clock register to enable clocking from an external clock source on the CLKI input. Set the XtalEn bit and clear the ExtClkEn bit if a crystal is used for clocking.

Set the ClkOEn bit in the Clock register to enable the clock signal on the CLKO output. When ClkOEn is set, a 3.6864MHz clock output is routed to CLKO, allowing multiple MAX14819/MAX14819A transceivers to operate from a single crystal oscillator.

An internal oscillator is used for basic functionality when both the crystal oscillator and the external clock are disabled. SPI read/write functionality is also available when no valid external clock source is present.

LED Control

The MAX14819/MAX14819A features four logic outputs that can be used for driving LEDs: LD1A, LD1B, LD2A, LD2B. LED functionality is controlled by setting the bits in the LEDCtrl register.

Thermal Protection

Thermal Shutdown

The CQ_ drivers are automatically disabled when the driver temperature exceeds the +160°C (typ) thermal-shutdown threshold. Drivers are automatically switched on when the driver temperature falls below the thermal-shutdown threshold plus hysteresis. The MAX14819/MAX14819A generates a thermal-shutdown interrupt (ThShdnCOR = 1) in the Status register when thermal shutdown occurs.

Overtemperature Warning

When the junction temperature exceeds the +135°C (typ) overtemperature-warning threshold, the TempWarn bit in the Status register is set.

The TempWarn bit is cleared when the die temperature falls to +120°C (typ).

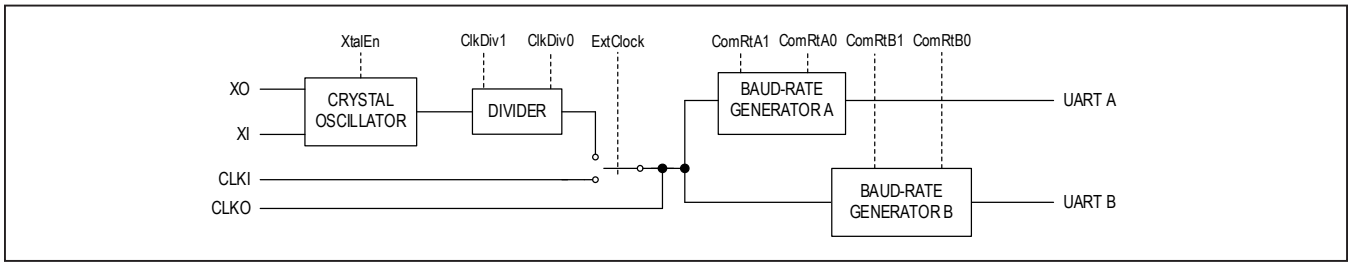


Figure 15. Clock Generation

Register Map

REGISTER NAME	CH/ GLOBAL	REG ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxRxDataA	A	0x00	DataA7	DataA6	DataA5	DataA4	DataA3	DataA2	DataA1	DataA0
TxRxDataB	B	0x01	DataB7	DataB6	DataB5	DataB4	DataB3	DataB2	DataB1	DataB0
Interrupt	G	0x02	StatusInt	WURQInt	TxErrorB	TxErrorA	RxErrorB	RxErrorA	RxDataRdyB	RxDataRdyA
InterruptEn	B	0x03	StatusIntEn	WURQIntEn	TxErrIntEnB	TxErrIntEnA	RxErrIntEnB	RxErrIntEnA	RDaRdyIntEnB	RxDaRdyIntEnA
RxFIFOLvlA	A	0x04	FifoLvlA7	FifoLvlA6	FifoLvlA5	FifoLvlA4	FifoLvlA3	FifoLvlA2	FifoLvlA1	FifoLvlA0
RxFIFOLvlB	B	0x05	FifoLvlB7	FifoLvlB6	FifoLvlB5	FifoLvlB4	FifoLvlB3	FifoLvlB2	FifoLvlB1	FifoLvlB0
CQCtrlA	A	0x06	ComRtA1	ComRtA0	EstComA	WuPulsA	TxFifoRstA	RxFifoRstA	CycleTmrEnA	CQSendA
CQCtrlB	B	0x07	ComRtB1	ComRtB0	EstComB	WuPulsB	TxFifoRstB	RxFifoRstB	CycleTmrEnB	CQSendB
CQErrA	A	0x08	TransmErrA	TCyclErrA	TChksmErA	TSizeErrA	RChksmErA	RSizeErrA	FrameErrA	ParityErrA
CQErrB	B	0x09	TransmErrB	TCyclErrB	TChksmErB	TSizeErrB	RChksmErB	RSizeErrB	FrameErrB	ParityErrB
MsgCtrlA	A	0x0A	TxErDestroyA	SPIChksA	InsChksA	TSizeEnA	TxKeepMsgA	RChksEnA	RMessgRdyEnA	InvCQA
MsgCtrlB	B	0x0B	TxErDestroyB	SPIChksB	InsChksB	TSizeEnB	TxKeepMsgB	RChksEnB	RMessgRdyEnA	InvCQB
ChanStatA	A	0x0C	RstA	FramerEnA	L+CLimCORA	UVL+CORA	CQFaultCORA	L+CLimA	UVL+A	CQFaultA
ChanStatB	B	0x0D	RstB	FramerEnB	L+CLimCORB	UVL+CORB	CQFaultCORB	L+CLimB	UVL+B	CQFaultB
LEDCtrl	G	0x0E	LEDEn2B	RxErrEnB	LEDEn1B	RxRdyEnB	LEDEn2A	RxErrEnA	LEDEn1A	RxRdyEnA
Trigger	G	0x0F	*	*	*	*	TrigInit3	TrigInit2	TrigInit1	TrigInit0
CQCfgA	A	0x10	IEC3ThA	SourceSinkA	SinkSelA1	SinkSelA0	NPNA	PushPulA	DrvDisA	CQFilterEnA
CQCfgB	B	0x11	IEC3ThB	SourceSinkB	SinkSelB1	SinkSelB0	NPNB	PushPulB	DrvDisB	CQFilterEnB
CyclTmrA	A	0x12	TCyclBsA1	TCyclBsA0	TCyclMA5	TCyclMA4	TCyclMA3	TCyclMA2	TCyclMA1	TCyclMA0
CyclTmrB	B	0x13	TCyclBsB1	TCyclBsB0	TCyclMB5	TCyclMB4	TCyclMB3	TCyclMB2	TCyclMB1	TCyclMB0
DeviceDlyA	A	0x14	DelayErrA	BDelayA1	BDelayA0	DDelayA3	DDelayA2	DDelayA1	DDelayA0	RspnsTmrEnA
DeviceDlyB	B	0x15	DelayErrB	BDelayB1	BDelayB0	DDelayB3	DDelayB2	DDelayB1	DDelayB0	RspnsTmrEnB
TrigAssgnA	A	0x16	TrigA3	TrigA2	TrigA1	TrigA0	*	*	*	TrigEnA
TrigAssgnB	B	0x17	TrigB3	TrigB2	TrigB1	TrigB0	*	*	*	TrigEnB
L+CnfgA	A	0x18	L+RTA1	L+RTA0	L+DynBLA	L+BLA1	L+BLA0	L+CL2xA	L+CLimDisA	L+EnA
L+CnfgB	B	0x19	L+RTB1	L+RTB0	L+DynBLB	L+BLB1	L+BLB0	L+CL2xB	L+ClimDisB	L+EnB
IOStCfgA	A	0x1A	DiLevelA	CQLevelA	TxEnA	TxA	DiFilterEnA	DiEC3ThA	DiCSourceA	DiCSinkA
IOStCfgB	B	0x1B	DiLevelB	CQLevelB	TxEnB	TxB	DiFilterEnB	DiEC3ThB	DiCSourceB	DiCSinkB
DrvrCurrLim	G	0x1C	CL1	CL0	CLDis	CLBL1	CLBL0	TAr1	TAr0	ArEn
Clock	G	0x1D	VCCWarnEn	TXTXENDis	ExtClkMis	ClkOEn	ClkDiv1	ClkDiv0	ExtClkEn	XtalEn
Status	G	x01E	ThShdnCOR	ThWarnCOR	VCCUVCOR	VCCWamCOR	ThShdn	TempWarn	VCCUV	VCCWarn
RevID	G	0x1F	*	*	*	*	ID3	ID2	ID1	ID0

**Bit is unused.*

Register Description

TxRxDataA Register [0x00]

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIT NAME	DataA7	DataA6	Data5	DataA4	DataA3	DataA2	DataA1	DataA0
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR STATE	X	X	X	X	X	X	X	X
RESET UPON READ	N	N	N	N	N	N	N	N

The TxRxDataA register allows writing data into the channel A TxFIFOA and reading data received out of the channel A RxFIFOA. Data can be written into the TxFIFOA and read out of the RxFIFOA in either byte-by-byte mode or burst mode. When using SPI burst mode, multiple bytes can be written to/read from the FIFOs in a single SPI cycle. Reading the RxFIFOA after it is empty results in random values.

RxFIFOA and TxFIFOA are available when framer A is enabled by setting the FramerEnA bit in the ChanStatA register.

BIT	NAME	DESCRIPTION
7:0	DataA	Channel A TxFIFO/RxFIFO data

TxRxDataB Register [0x01]

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIT NAME	DataB7	DataB6	DataB5	DataB4	DataB3	DataB2	DataB1	DataB0
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR STATE	X	X	X	X	X	X	X	X
RESET UPON READ	N	N	N	N	N	N	N	N

The TxRxDataB register allows writing data into the channel B TxFIFOB and reading data received out of the channel B RxFIFOB. Data can be written into the TxFIFOB and read out of the RxFIFOB in either byte-by-byte mode or burst mode. When using SPI burst mode, multiple bytes can be written to/read from the FIFOs in a single SPI cycle. Reading the RxFIFOB after it is empty results in random values. Reading the RxFIFOB after it is empty results in random values.

RxFIFOB and TxFIFOB are available when framer B is enabled by setting the FramerEnB bit in the ChanStatB register.

BIT	NAME	DESCRIPTION
7:0	DataB	Channel B TxFIFO/RxFIFO data

Interrupt Register [0x02]

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIT NAME	StatusInt	WURQInt	TxErrorB	TxErrorA	RxErrorB	RxErrorA	RxDataRdyB	RxDataRdyA
READ/WRITE	R	R	R	R	R	R	R	R
POR STATE	0	0	0	0	0	0	0	0
RESET UPON READ	Y	Y	Y	Y	Y	Y	N	N

BIT	NAME	DESCRIPTION
7	StatusInt	**Status Error Interrupt** This bit is set when a supply error or thermal error L+ supply error, or CQ_ driver error occurs. See Figure 16.
6	WURQInt	**Wake-Up Request Interrupt** This bit is set when the establish-communication sequencer is either successfully or unsuccessfully completed after an EstCom_ sequence is initiated. See the CQCntrl register for more information.
5	TxErrorB	**Channel B Transmitter Error Interrupt** This bit is set when an error is detected on the channel B transmitter (CQB). Details on the type of error can be read out of the CQErrB register. See Figure 17.
4	TxErrorA	**Channel A Transmitter Error Interrupt** This bit is set when an error is detected on the channel A transmitter (CQA). Details on the type of error can be read out of the CQErrA register. See Figure 17.
3	RxErrorB	**Channel B Receiver Error Interrupt** This bit is set when a receive error is detected on CQB. Details on the receive error can be read out of the CQErrB or DevicDelyB register. Optionally, the status of the RxErrorB bit can be made available on the $\overline{\text{RXERRB}}$/LD2B pin. Set the RxErrEnB bit in the LEDCtrl register to 1 to assert the $\overline{\text{RXERRB}}$/LD2B pin when RxErrorB is set. See Figure 18.
2	RxErrorA	**Channel A Receiver Error Interrupt** This bit is set when a receive error is detected on CQA. Details on the receive error can be read out of the CQErrA register. Optionally, the status of the RxErrorA bit can be made available on the $\overline{\text{RXERRA}}$/LD2A pin. Set the RxErrEnB bit in the LEDCtrl register to 1 to assert the $\overline{\text{RXERRA}}$/LD2A pin when RxErrorA is set. See Figure 18.
1	RxDataRdyB	**Channel B Receiver Data Ready Interrupt** RxDataRdyB is set when the first byte of data is received by the channel B RxFIFO. The RxDataRdyB interrupt is set when the RxFIFOB level changes from empty to at least one received word. If RMessgRdyEnB = 1, RxDataRdyB is set when a complete M-sequence frame was received correctly and is ready for SPI readout from TxRxDataB. Set the RxRdyEnB bit in the LEDCtrl register to 1 to assert the $\overline{\text{RXRDYB}}$/LD1B pin when RxDataRdyB is set. RxDataRdyB is cleared when the TxRxDataB register is read.
0	RxDataRdyA	**Channel A Receiver Data Ready Interrupt** RxDataRdyaA is set when the first byte of data is received by the channel A RxFIFO. The RxDataRdyA interrupt is set when the RxFIFOA level changes from empty to at least one received word. If RMessageRdyEnA = 1, RxDataRdyA is set when a complete M-sequence frame was received correctly and is ready for SPI readout from TxRxDataA. Set the RxRdyEnA bit in the LEDCtrl register to 1 to assert the $\overline{\text{RXRDYA}}$/LD1A pin when RxDataRdyA is set. RxDataRdyA is cleared when TxRxDataA is read.

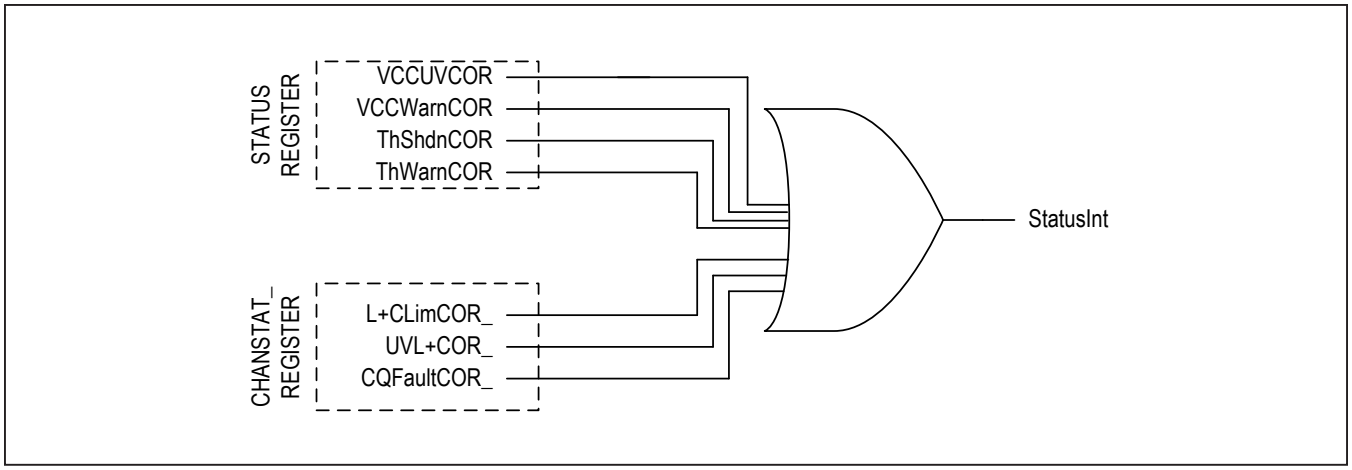


Figure 16. StatusInt Interrupt Triggers

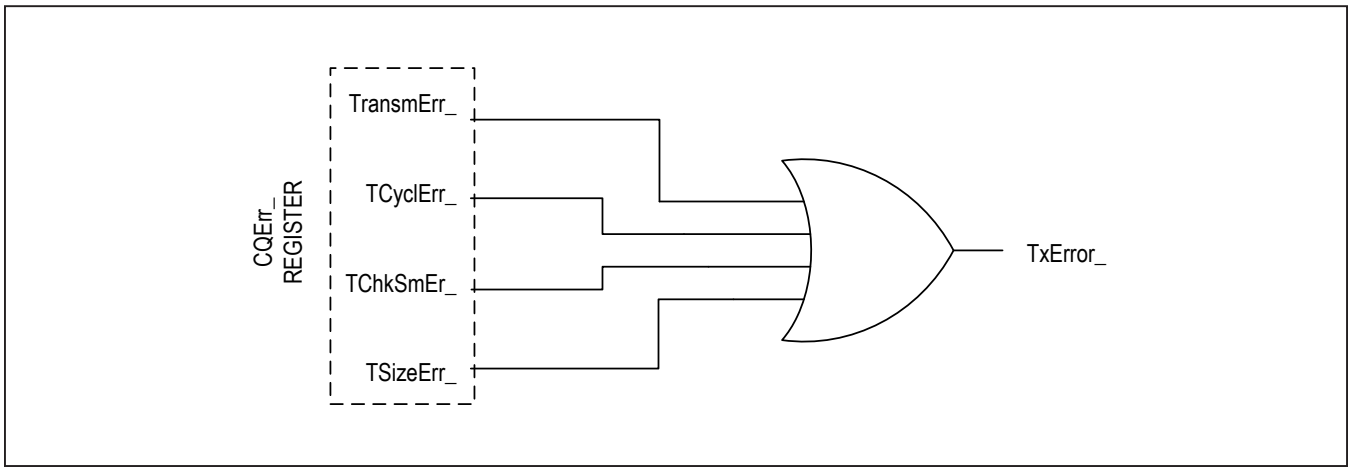


Figure 17. TxError_ Triggers

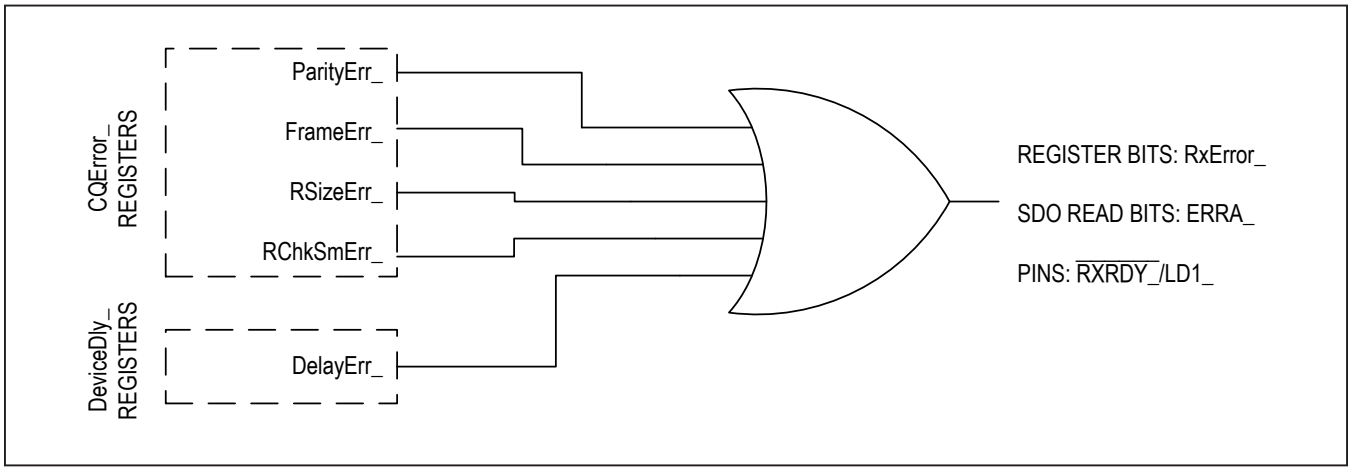


Figure 18. RxError_Triggers

InterruptEn Register [0x03]

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIT NAME	StatusIntEn	WURQIntEn	TxErrIntEnB	TxErrIntEnA	RxErrIntEnB	RxErrIntEnA	RDaRdyIntEnB	RDaRdyIntEnA
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR STATE	0	0	0	0	0	0	0	0
RESET UPON READ	N	N	N	N	N	N	N	N

BIT	NAME	DESCRIPTION
7	StatusIntEn	**Status Interrupt Enable** Set the StatIntEn bit to 1 to assert the $\overline{IRQ}$ output when a StatusInt interrupt is generated. Clear the StatusIntEn bit to disable/mask the $\overline{IRQ}$ output when a StatusInt interrupt is generated.
6	WURQIntEn	**Wake-Up Request Interrupt Enable** Set the WURQIntEn bit to 1 to assert the $\overline{IRQ}$ output when a WURQInt interrupt is generated. Clear the WURQIntEn bit to disable/mask the $\overline{IRQ}$ output when a WURQInt interrupt is generated.
5	TxErrIntEnB	**Channel B Transmitter Error Interrupt Enable** Set the TxErrIntEnB bit to 1 to assert the $\overline{IRQ}$ output when a TxErrorB interrupt is generated. Clear the TxErrIntEn bit to disable/mask the $\overline{IRQ}$ output when a TxErrorB interrupt is generated.
4	TxErrIntEnA	**Channel A Transmitter Error Interrupt Enable** Set the TxErrIntEnA bit to 1 to assert the $\overline{IRQ}$ output when a TxErrorA interrupt is generated. Clear the TxErrIntEn bit to disable/mask the $\overline{IRQ}$ output when a TxErrorA einterrupt is generated.
3	RxErrIntEnB	**Channel B Receiver Error Interrupt Enable** Set the RxErrIntEnB bit to 1 to assert the $\overline{IRQ}$ output when a RxErrorB interrupt is generated. Clear the RxErrIntEnB bit to disable/mask the $\overline{IRQ}$ output when a RxErrorB interrupt is generated. . The RxErrIntEnB bit does not mask or enable the $\overline{RXERRB}$/LD2B pin.

InterruptEn Register [0x03] (continued)

BIT	NAME	DESCRIPTION
2	RxErrIntEnA	**Channel A Receiver Error Interrupt Enable** Set the RxErrIntEnA bit to 1 to assert the $\overline{IRQ}$ output when a RxErrorA interrupt is generated. Clear the RxErrIntEnA bit to disable/mask the $\overline{IRQ}$ output when a RxErrorA interrupt is generated. The RxErrIntEnA bit does not mask or enable the $\overline{RXERRA}$/LD2A pin.
1	RDaRdyIntEnB	**Channel B Receiver Data Ready Interrupt Enable** Set the RDaRdyIntEnB bit to 1 to assert the $\overline{IRQ}$ output when a RxDataRdyB interrupt is generated. Clear the RDaRdyIntEnB bit to disable/mask the $\overline{IRQ}$ output when a RxDataRdyB interrupt is generated. The RDaRdyIntEnB bit does not mask or enable the $\overline{RXRDYB}$/LD1B pin.
0	RDaRdyIntEnA	**Channel A Receiver Data Ready Interrupt Enable** Set the RDaRdyIntEnA bit to 1 to assert the $\overline{IRQ}$ output when a RxDataRdyA interrupt is generated. Clear the RDaRdyIntEnA bit to disable/mask the $\overline{IRQ}$ output when a RxDataRdyA interrupt is generated. The RDaRdyIntEnA bit does not mask or enable the $\overline{RXRDYA}$/LD1A pin.

RxFIFOLvlA Register [0x04]

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIT NAME	FifoLvlA7	FifoLvlA6	FifoLvlA5	FifoLvlA4	FifoLvlA3	FifoLvlA2	FifoLvlA1	FifoLvlA0
READ/WRITE	R	R	R	R	R	R	R	R
POR STATE	0	0	0	0	0	0	0	1
RESET UPON READ	N	N	N	N	N	N	N	N

The RxFIFOLvlA register shows the current number of device message bytes in the RxFIFOA. This changes as data is read out of the RxFIFOA and as the RxFIFOA fills up. The MAX14819/MAX14819A adds one byte, at the start of the RxFIFOA data, which is the number of device message bytes that were received; the RxFIFOLvlA value does not include this added byte.

Note: Due to the limitations of simultaneous access, the value read from the RxFIFOLvlA register may be off by ±1 word while the receiver is receiving data. The value read from RxFIFOLvlA is correct while the receiver is not receiving data.

BIT	NAME	DESCRIPTION
7:0	FifoLvlA	Channel A Receive FIFO Device Message Level

RxFIFOLvlB Register [0x05]

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIT NAME	FifoLvlB7	FifoLvlB6	FifoLvlB5	FifoLvlB4	FifoLvlB3	FifoLvlB2	FifoLvlB1	FifoLvlB0
READ/WRITE	R	R	R	R	R	R	R	R
POR STATE	0	0	0	0	0	0	0	0
RESET UPON READ	N	N	N	N	N	N	N	N

The RxFIFOLvlB register shows the current number of device message bytes in the RxFIFOB. This changes as data is read out of the RxFIFOB and as the RxFIFOB fills up. The MAX14819/MAX14819A adds one byte, at the start of the RxFIFOB data, which is the number of device message bytes that were received; the RxFIFOLvlB value does not include this added byte.
Note: Due to the limitations of simultaneous access, the value read from the RxFIFOLvlB register may be off by ±1 word while the receiver is receiving data. The value read from RxFIFOLvlB is correct while the receiver is not receiving data.

BIT	NAME	DESCRIPTION
7:0	FifoLvlB	Channel B Receive FIFO Device Message Level

CQCtrlA Register [0x06]

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIT NAME	ComRtA1	ComRtA0	EstComA	WuPulsA	TxFifoRstA	RxFifoRstA	CycleTmrEnA	CQSendA
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR STATE	0	0	0	0	0	0	0	0
RESET UPON READ	N	N	N	N	N	N	N	N

BIT	NAME	DESCRIPTION
[7:6]	ComRtA1, ComRtA0	**Channel A CQ (CQA) COM Rate Setting** The ComRtA[1:0] bits set the COM data rate on the CQA interface. Once the establish-communication sequence, intiated with EstComA, is successfully completed, the COM rate of the IO-link device will be stored in these bits as follows: 00: Detection failure (230.4kbps) 01: COM1 = 4.8kbps 10: COM2 = 38.4kbps 11: COM3 = 230.4kbps

CQCtrlA Register [0x06] (continued)

BIT	NAME	DESCRIPTION
5	EstComA	**Channel A Establish-Communication Sequence Enable** Set the EstComA to 1 to initiate an IO-Link establish-communication sequence on CQA. After successful completion of the establish communication sequence, a WURQInt interrupt is generated and the EstComA bit changes to 0. During the generated wake-up pulse, the CQA current limit is temporarily set above 500mA internally, although the CL_ register bits are not changed. The COM rate of the IO-Link device is then reflected by the ComRt0A and ComRt1A bits and the device cycle time can be read out of the CyclTimeA register. If the establish-communication sequence was not successful, a WURQInt interrupt is generated and EstComA is 0 and the ComRt1A and ComRt0A bits both = 0. The FramerEnA bit must be 1 to use the EstComA function.
4	WuPulsA	**Channel A Wake-Up Pulse Generate** Set WuPulsA to 1 to immediately generate a wake-up pulse/request (WURQ) on CQA. Following the wake-up request, the CQA transceiver is set into receive mode. WuPulsA is reset to 0 after the WURQ is completed. WuPulsA is used when the microcontroller manages the establish communication sequence and the EstComA funciton is not used.
3	TxFifoRstA	**Channel A TX FIFO (TxFIFOA) Reset** Set TxFifoRstA to reset the TxFIFOA. This may be necessary if an SPI transmission error is detected when filling the TxFIFOA or if a CQA transmission error is detected.
2	RxFifoRstA	**Channel A RX FIFO (RxFIFOA) Reset** Set RxFifoRstA to reset the RxFIFOA. This may be necessary if an RSizeErrA event occurs.
1	CycleTmrEnA	**Channel A Cycle Timer Enable** Set CyclTmrEnA to 1 to enable the channel A cycle time. CyclTmrEnA does not start the cycle timer. Cycle timer A starts when the CQSendA bit is set to 1 (after the timer is enabled) or an associated trigger command is received. Set CyclTmrEnA to 0 to stop the cycle timer. The timer can be stopped at any time, even if the current cycle is not yet complete.
0	CQSendA	**Channel A Initiate Master Message** Set CQSendA to 1 to initiate transmission of the master message in the channel A transmit FIFO (TxFIFOA). The CQA transceiver is put into transmit mode and sends the master message/data in the TxFIFOA. When the master message is complete/TxFIFOA is empty, the CQA transceiver is set to receive mode to receive device messages. If CyclTmrEnA = 1, setting CQSendA to 1 also starts cycle timer A. CQSendA is automatically cleared.

CQCtrlB Register [0x07]

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIT NAME	ComRtB1	ComRtB0	EstComB	WuPulsB	TxFifoRstB	RxFifoRstB	CycleTmrEnB	CQSendB
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR STATE	0	0	0	0	0	0	0	0
RESET UPON READ	N	N	N	N	N	N	N	N

BIT	NAME	DESCRIPTION
[7:6]	ComRtB1, ComRtB0	**Channel B CQ (CQB) COM Rate Setting** The ComRtB[1:0] bits set the COM data rate on the CQB interface. Once the establish-communication sequence, intiated with EstComB, is successfully completed, the COM rate of the IO-link device will be stored in these bits as follows: 00: Detection failure (230.4kbps) 01: COM1 = 4.8kbps 10: COM2 = 38.4kbps 11: COM3 = 230.4kbps
5	EstComB	**Channel B Establish-Communication Sequence** Set the EstComB to 1 to initiate an IO-Link establish-communication sequence on CQB. After successful completion of the establish communication sequence, a WURQInt interrupt is generated and the EstComB bit changes to 0. During the generated wake-up pulse, the CQB current limit is temporarily set above 500mA internally, although the CL_ register bits are not changed. The COM rate of the IO-Link device is then reflected by the ComRt0A and ComRt1A bits and the device cycle time can be read out of the CyclTimeB register. If the establish-communication sequence was not successful, a WURQInt interrupt is generated and EstComB is 0 and the ComRt1B and ComRt0B bits both = 0. The FramerEnB bit must be 1 to use the EstComB function.
4	WuPulsB	**Channel B Wake-Up Pulse Generate** Set WuPulsB to 1 to immediately generate a wake-up pulse/request (WURQ) on CQB. Following the wake-up request, the CQB transceiver is set into receive mode. WuPulsB is reset to 0 after the WURQ is completed. WuPulsA is used when the microcontroller manages the establish-communication sequence and the EstComB function is not used.

CQCtrlB Register [0x07] (continued)

BIT	NAME	DESCRIPTION
3	TxFifoRstB	**Channel B TX FIFO (TxFIFOA) Reset** Set TxFifoRstB to reset the TxFIFOB. This may be necessary if an SPI transmission error is detected when filling the TxFIFOB or if a CQB transmission error is detected.
2	RxFifoRstB	**Channel B RX FIFO (RxFIFOA) Reset** Set RxFifoRstA to reset the RxFIFOA. This may be necessary if an RSizeErrA event occurs.
1	CyclTmrEnB	**Channel B Cycle Timer Enable** Set CyclTmrEnB to 1 to enable the channel B cycle time. CyclTmrEnB does not start the cycle timer. Cycle timer B starts when the CQSendB bit is set to 1 (after the timer is enabled) or an associated trigger command is received. Set CyclTmrEnB to 0 to stop the cycle timer. The timer can be stopped at any time, even if the current cycle is not yet complete.
0	CQSendB	**Channel B Initiate Master Message** Set CQSendB to 1 to initiate transmission of the master message in the channel B transmit FIFO (TxFIFOB). The CQB transceiver is put into transmit mode and sends the master message/data in the TxFIFOB. When the master message is complete/TxFIFOB is empty, the CQB transceiver is set to receive mode to receive device messages. If CyclTmrEnB = 1, setting CQSendB to 1 also starts cycle timer B. CQSendB is automatically cleared.

CQErrA Register [0x08]

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIT NAME	TransmErrA	TCyclErrA	TChksmErA	TSizeErrA	RChksmErA	RSizeErrA	FrameErrA	ParityErrA
READ/WRITE	R	R	R	R	R	R	R	R
POR STATE	0	0	0	0	0	0	0	0
RESET UPON READ	Y	Y	Y	Y	Y	Y	Y	Y

BIT	NAME	DESCRIPTION
7	TransmErrA	**Channel A Transmission Error** This bit is set when the message sent on Channel A was not properly sent. The bit is cleared when the CQErrA register is read.

CQErrA Register [0x08] (continued)

BIT	NAME	DESCRIPTION
6	TCyclErrA	**Channel A Transmission Cycle Error** This bit is set when when no data is loaded into the TxFIFOA before the start of the master message transmission. At least one octet must be loaded into TxFIFOA at the start of the transmission cycle. This bit is only active when the internal cycle timer is used (CycTmrEnA = 1). The bit is cleared when the CQErrA register is read.
5	TChksmErA	**Channel A Transmitter Checksum Error** This bit is set when the checksum calculated by the MAX14819/MAX14819A on the master message is different to the checksum written in the TxFIFOA by the SPI master. A checksum error indicates an SPI transmission error. This bit is only active when SPIChksA = 1. If TChksmErA = 1, the master message is not sent to the device when the autonomous cycle timer A is enabled. The bit is cleared when the CQErrA register is read.
4	TSizeErrA	**Channel A Transmitter Size Error** This bit is set when the number of octets in the master message differs from the TxBytes value written into the TxFIFOA. This can occur as a result of slow SPI master writing of the master message into TxFIFOA while CQA transmission has started, so that the master message cannot be sent in the allocated time. When this error occurs, it is recommended that the controller delete the TxFIFOA (TxFIFORstA = 1) and repeat the master message transmission. The bit is cleared when the CQErrA register is read.
3	RChksmErA	**Channel A Receiver Checksum Error** This bit is set when a 6-bit checksum calculated by the MAX14819/MAX14819A differs from the checksum in the received device message. The bit is cleared when the CQErrA register is read.
2	RSizeErrA	**Channel A Receiver Size Error** This bit is set when the number of octets received for the device differs from RxBytes previously loaded into TxFIFOA. The bit is cleared when the CQErrA register is read.
1	FrameErrA	**Channel A Frame Error** This bit is set when a UART frame error is detected on the data received on the CQA receiver. A FrameErrA error triggers a RxErrorA interrupt. The bit is cleared when the CQErrA register is read.
0	ParityErrA	**Channel A Parity Error** This bit is set when a UART parity error is detected on a word received by the CQA receiver. A ParityErrA interrupt triggers an RxErrorA interrupt in the Interrupt register. The bit is cleared when the CQErrA register is read.

CQErrB Register [0x09]

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIT NAME	TransmErrB	TCyclErrB	TChksmErB	TSizeErrB	RChksmErB	RSizeErrB	FrameErrB	ParityErrB
READ/WRITE	R	R	R	R	R	R	R	R
POR STATE	0	0	0	0	0	0	0	0
RESET UPON READ	Y	Y	Y	Y	Y	Y	Y	Y

BIT	NAME	DESCRIPTION
7	TransmErrB	**Channel B Transmission Error** This bit is set when the message sent on Channel B was not properly sent. The bit is cleared when the CQErrB register is read.
6	TCyclErrB	**Channel B Transmission Cycle Error** This bit is set when when no data is loaded into the TxFIFOB before the start of the master message transmission. At least one octet must be loaded into TxFIFOB at the start of the transmission cycle. This bit is only active when the internal cycle timer is used (CyclTmrEnB = 1). The bit is cleared when the CQErrB register is read.
5	TChksmErB	**Channel B Transmitter Checksum Error** This bit is set when the checksum calculated by the MAX14819/MAX14819A on the master message is different to the checksum written in the TxFIFOB by the SPI master. A checksum error indicates an SPI transmission error. This bit is only active when SPIChksB = 1. If TChksmErB = 1, the master message is not sent to the device when the autonomous cycle timer B is enabled. The bit is cleared when the CQErrB register is read.
4	TSizeErrB	**Channel B Transmitter Size Error** This bit is set when the number of octects in the master message differs from the TxBytes value written into the TxFIFOB. This can occur as a result of slow SPI master writing of the master message into TxFIFOB while CQB transmission has started, so that the master message cannot be sent in the allocated time. When this error occurs, it is recommended that the controller delete the TxFIFOB (TxFIFORstB = 1) and repeat the master message transmission. The bit is cleared when the CQErrB register is read.

CQErrB Register [0x09] (continued)

BIT	NAME	DESCRIPTION
3	RChksmErB	**Channel B Receiver Checksum Error** This bit is set when a 6-bit checksum calculated by the MAX14819/MAX14819A differs from the checksum in the received device message. The bit is cleared when the CQErrB register is read.
2	RSizeErrB	**Channel B Receiver Size Error** This bit is set when the number of octets received for the device differs from RxBytes previously loaded inot TxFIFOB. The bit is cleared when the CQErrB register is read.
1	FrameErrB	**Channel B Frame Error** This bit is set when a UART frame error is detected on the data received on the CQB receiver. A FrameErrB error triggers a RxErrorB interrupt. The bit is cleared when the CQErrBregister is read.
0	ParityErrB	**Channel B Parity Error** This bit is set when a UART parity error is detected on a word received by the CQB receiver. A ParityErrB interrupt triggers an RxErrorB interrupt in the Interrupt register. The bit is cleared when the CQErrB register is read.

MsgCtrlA Register [0x0A]

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIT NAME	TxErDestroyA	SPIChksA	InsChksA	TSizeEnA	TxKeepMsgA	RChksEnA	RMessgRdyEnA	InvCQA
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR STATE	0	0	0	0	0	0	0	0
RESET UPON READ	N	N	N	N	N	N	N	N

BIT	NAME	DESCRIPTION
7	TxErDestroyA	**Channel A TxFIFOA Message Delete on Error** Set TxErDestroyA = 1 to instruct the MAX14819 to automatically delete the message in the TxFIFOA (reset TxFIFOA) when a checksum or size error is detected in the message. This is only possible when a complete master message is loaded in the the TxFIFOA before transmission starts.

MsgCtrlA Register [0x0A] (continued)

BIT	NAME	DESCRIPTION
6	SPIChksA	**Channel A SPI Checksum Verify** Set SPIChksA = 1 to enable checking of the SPI checksum that the SPI master wrote into the CKT octet compared to the calculated checksum. This bit is independent of InsChksA. When a checksum disparity is found, the TChksmErA bit is set in the CQErrA register.
5	InsChksA	**Channel A Insert Checksum** Set InsChksA = 1 to instruct the MAX14819/MAX14819A to calculate the 6-bit checksum on the master message residing in TxFIFOA and insert this into the CKT byte. The bits written by the SPI master into these 6 bits are replaced.
4	TSizeEnA	**Channel A TxFIFOA Size Check Enable** Set TSizeEnA = 1 to require the MAX14819/MAX14819A to verify that the number of bytes in the TxFIFOA is equal to the TxBytes value written into the TxFIFOA. If the master message is loaded before transmission starts, a TxErrA interrupt is generated and the message can be deleted by the MAX14819/MAX14819A (when TxErDestroyA = 1). If the transmission has started before the whole message is loaded, then the message cannot be automatically deleted.
3	TxKeepMsgA	**Channel A Keep TxFIFO Message Enable** Set TxKeepMsgA = 1 to stop the MAX14819/MAX14819A from clearing the TxFIFOA after the message has been sent. This allows sending the same master message on the following cycle. When TxKeepMsgA = 0, the data in the TxFIFOA is automatically cleared after the message has been sent.
2	RChksEnA	**Channel A Device Message Checksum Enable** Set RChksEnA = 1 to enable the MAX14819/MAX14819A to check the device message checksum in the RxFIFOA. If an error is detected during the checksum check, the RChksmErA bit is set.
1	RMessgRdyEnA	**Channel A Received Message Ready** Set RMessgRdyEnA = 1 to generate a RxDataRdyA interrupt when the complete device response message is received and has no errors. When RMessgRdyEnA = 0, a RxDataRdyA interrupt is generated as soon as the first word is received in the RxFIFOA.
0	InvCQA	**Channel A Logic Invert** Set InvCQA = 1 to switch the polarity of the CQA output for transmission and reception. when InvCQA = 0, TXA and RXA are logic inverts of CQA. When InvCQA = 1, TXA and RXA follow CQA, logically.

MsgCtrlB [0x0B]

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIT NAME	TxErDestroyB	SPIChksB	InsChksB	TSizeEnB	TxKeepMsgB	RChksEnb	RMessgRdyEnb	InvCQB
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR STATE	0	0	0	0	0	0	0	0
RESET UPON READ	N	N	N	N	N	N	N	N

BIT	NAME	DESCRIPTION
7	TxErDestroyB	**Channel B TxFIFOB Message Delete on Error** Set TxErDestroyB = 1 to instruct the MAX14819/MAX14819A to automatically delete the message in the TxFIFOB (reset TxFIFOB) when a checksum or size error is detected in the message. This is only possible when a complete master message is loaded in the the TxFIFO before transmission starts.
6	SPIChksB	**Channel B SPI Checksum Verify** Set SPIChksB = 1 to enable checking of the SPI checksum that the SPI master wrote into the CKT octet compared to the calculated checksum. This bit is independent of InsChksB. When a checksum disparity is found, the TChksmErB bit is set in the CQErrB register.
5	InsChksB	**Channel B Insert Checksum** Set InsChksB = 1 to instruct the MAX14819/MAX14819A to calculate the 6-bit checksum on the master message residing in TxFIFOB and inster this into the CKT byte. The bits written by the SPI master into these 6 bits are replaced.
4	TSizeEnB	**Channel B TxFIFOB Size Check Enable** Set TSizeEnB = 1 to require the MAX14819/MAX14819A to verify that the number of bytes in the TxFIFOB is equal to the TxBytes value written into the TxFIFOB. If the master message is loaded before transmission starts, a TxErrB interrupt is generated and the message can be deleted by the MAX14819/MAX14819A (when TxErDestroyB = 1). If the transmission has started before the whole message is loaded, then the message cannot be automatically deleted.

MsgCtrlB [0x0B] (continued)

BIT	NAME	DESCRIPTION
3	TxKeepMsgB	**Channel B Keep TxFIFO Message Enable** Set TxKeepMsgB = 1 to stop the MAX14819/MAX14819A from clearing the TxFIFOB after the message has been sent. This allows sending the same master message on the following cycle. When TxKeepMsgB = 1, the TxFIFOB must be cleared by setting the TxFIFORstB bit. When TxKeepMsgB = 0, the data in the TxFIFOB is automatically cleared after the message has been sent.
2	RChksEnB	**Channel B Device Message Checksum Enable** Set RChksEnB = 1 to enable the MAX14819/MAX14819A to check the device message checksum in the RxFIFOB. If an error is detected during the checksum check, the RChksmErB bit is set.
1	RMessgRdyEnB	**Channel B Received Message Ready** Set RMessgRdyEnB = 1 to generate a RxDataRdyB interrupt when the complete device response message is received and has no errors. When RMessgRdyEnB = 0, a RxDataRdyB interrupt is generated as soon as the first word is received by the RxFIFOB.
0	InvCQB	**Channel B Logic Invert** Set InvCQB = 1 to switch the polarity of the CQB output for transmission and reception. when InvCQB = 0, TXB and RXB are logic inverts of CQB. When InvCQB = 1, TXB and RXB follow CQB, logically.

ChanStatA Register [0x0C]

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIT NAME	RstA	FramerEnA	L+CLimCORA	UVL+CORA	CQFaultCORA	L+CLimA	UVL+A	CQFaultA
READ/WRITE	R/W	R/W	R	R	R	R	R	R
POR STATE	0	0	X	X	0	X	X	0
RESET UPON READ	N	N	Y	Y	Y	N	N	N

BIT	NAME	DESCRIPTION
7	RstA	**Channel A Register Reset** Set RstA = 1 to reset all channel A register bits, the TxFIFOA, and RxFIFOA. Channel B registers and global register bits are not affected. RstA is cleared automatically when the channel A registers have been reset.
6	FramerEnA	**Channel A Framer Enable** Set FramerEnA = 1 to enable the internal message handler, RxFIFOA, and TxFIFOA. When an external UART is used (the internal framer is not used), set FramerEnA = 0 and connect the external UART to the TXENA, TXA, and RXA pins.
5	L+CLimCORA	**Channel A L+A Current Limit Latched** Clear-on-read flag of the L+ClimA bit. This bit is set only when the L+CLimA bit transitions from 0 to 1. This bit can generate a StatusInt interrupt.
4	UVL+CORA	**Channel A L+A UnderVoltage Latched** Clear-on-read flag of the UVL+A bit. This bit is set only when the UVL+A bit transitions from 0 to 1. This bit can generate a StatusInt interrupt.
3	CQFaultCORA	**Channel A CQ Driver Fault Latched** Clear-on-read flag of the CQFaultA bit. This bit is set only when the CQFaultA bit transitions from 0 to 1. This bit can generate a StatusInt interrupt.
2	L+CLimA	**Channel A L+A Current Limit Real Time** This bit is set when the L+A sensor supply load current exceeds the current-limit threshold set by the sense resistor for longer than the programmed current-limit blanking time (see the L+CnfgA register for more information). L+CLimA is cleared when the L+A supply exits autoretry current limiting.
1	UVL+A	**Channel A L+A Undervoltage Real Time** This bit is set when the L+A supply voltage falls below the L+ power-good falling threshold. The bit is cleared when the L+A voltage rises above the L+ power-good rising threshold.
0	CQFaultA	**Channel A CQ Driver Fault Real Time** This bit is set when a fault is detected on the CQA driver. The fault can be an overload condition, for example an overcurrent of thermal-shutdown event.

ChanStatB Register [0x0D]

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIT NAME	RstB	FramerEnB	L+CLimCORB	UVL+CORBr	CQFaultCORB	L+CLimB	UVL+B	CQFaultB
READ/WRITE	R/W	R/W	R	R	R	R	R	R
POR STATE	0	0	X	X	0	X	X	0
RESET UPON READ	N	N	Y	Y	Y	N	N	N

BIT	NAME	DESCRIPTION
7	RstB	**Channel B Register Reset** Set RstB = 1 to reset all channel B register bits, the TxFIFOB, and RxFIFOB. Channel A registers and global register bits are not affected. RstB is cleared automatically when the channel B registers have been reset.
6	FramerEnB	**Channel B Framer Enable** Set FramerEnB = 1 to enable the internal UARTB, message handler, RxFIFOB, and TxFIFOB. When an external UART is used (the internal framer is not used), set FramerEnA = 0 and connect the external UART to the TXENA, TXA, and RXA pins.
5	L+CLimCORB	**Channel B L+B Current Limit Latched** Clear-on-read flag of the L+ClimB bit. This bit is set when the L+CLimB bit transitions from 0 to 1. This bit can generate a StatusInt interrupt.
4	UVL+CORB	**Channel B L+B UnderVoltage Latched** Clear-on-read flag of the UVL+B bit. This bit is set only when the UVL+B bit transitions from 0 to 1. This bit can generate a StatusInt interrupt.
3	CQFaultCORB	**Channel B CQ Driver Fault Latched** Clear-on-read flag of the CQFaultB bit. This bit is set only when the CQ-FaultB bit transitions from 0 to 1. This bit can generate a StatusInt interrupt.
2	L+CLimB	**Channel B L+B Current Limit Real Time** This bit is set when the L+B sensor supply load current exceeds the current-limit threshold set by the sense resistor for longer than the programmed current-limit blanking time (see the LpCfgB register for more information). L+CLimB is cleared when the L+B supply exits autoretry current limiting.
1	UVL+B	**Channel B L+B Undervoltage Real Time** This bit is set when the L+B supply voltage falls below the L+ power-good falling threshold. The bit is cleared when the L+B voltage rises above the the L+ power-good rising threshold.
0	CQFaultB	**Channel B CQ Driver Fault Real Time** This bit is set when a fault is detected on the CQB driver. The fault can be an overload condition, for example an overcurrent of thermal-shutdown event.

LEDCtrl Register [0x0E]

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIT NAME	LEDEn2B	RxErrEnB	LEDEn1B	RxRdyEnB	LEDEn2A	RxErrEnA	LEDEn1A	RxRdyEnA
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR STATE	0	0	0	0	0	0	0	0
RESET UPON READ	N	N	N	N	N	N	N	N

BIT	NAME	DESCRIPTION
7	LEDEn2B	**Channel B LD2B LED Driver Control** Set LEDEn2B = 1 to turn on a LED connected to $\overline{\text{RXERRB}}$/LD2B. Set LEDEn2B = 0 to turn the LED off. LEDEn2B is only active when RxErrEnB = 0.
6	RxErrEnB	**Channel B $\overline{\text{RXERRB}}$/LD2B Pin Function Select** Set RxErrEnB = 1 to enable the receiver-error (RxErrorB) interrupt functionality on the $\overline{\text{RXERRB}}$/LD2B pin. In this mode, $\overline{\text{RXERRB}}$/LD2B asserts when the RxErrorB bit is set. The $\overline{\text{RXERRB}}$/LD2B pin functionality is not affected by the RxErrIntEnB interrupt mask. Set RxErrEnB = 0 to enable the LED driver function on the ERRB/LD2B output.
5	LEDEn1B	**Channel B LD1B LED Driver Control** Set LEDEn1B = 1 to turn on a LED connected to $\overline{\text{RXRDYB}}$/LD1B. Set LEDEn1B = 0 to turn the LED off. LEDEn1B is only active when RxRdyEnB = 0.
4	RxRdyEnB	**Channel B $\overline{\text{RXRDYB}}$/LD1B Pin Function Select** Set RxRdyEnB = 1 to enable the receiver-error (RxErrorB) interrupt functionality on the $\overline{\text{RXRDYB}}$/LD1B pin. In this mode, $\overline{\text{RXRDYB}}$/LD1B asserts when the RcDaRdyB bit is set. The $\overline{\text{RXRDYB}}$/LD1B pin functionality is not affected by the RxDaRdyIntEnB interrupt mask. Set RxRdyEnB = 0 to enable the LED driver function on the $\overline{\text{RXRDYB}}$/LD1B pin.
3	LEDEn2A	**Channel A LD2A LED Driver Control** Set LEDEn2A = 1 to turn on a LED connected to $\overline{\text{RXERRA}}$/LD2A. Set LEDEn2A = 0 to turn the LED off. LEDEn2A is only active when RxErrEnA = 0.

LEDCtrl Register [0x0E] (continued)

BIT	NAME	DESCRIPTION
2	RxErrEnA	**Channel A $\overline{\text{RXERRA}}$/LD2A Pin Function Select Bit** Set RxErrEnA = 1 to enable the receiver-error (RxErrorA) interrupt functionality on the $\overline{\text{RXERRA}}$/LD2A pin. In this mode, $\overline{\text{RXERRA}}$/LD2A asserts when the RxErrorA bit is set. The $\overline{\text{RXERRA}}$/LD2A pin functinoality is not affected by the RxErrIntEnA interrupt mask. Set RxErrEnA = 0 to enable the LED driver functiona on $\overline{\text{RXERRA}}$/LD2A.
1	LEDEn1A	**Channel A LD1A LED Driver Control Bit** Set LEDEn1A = 1 to turn on a LED connected to the $\overline{\text{RXRDYA}}$/LD1A pin. Set LEDEn1A = 0 to turn the LED off. LEDEn1A is only active when RxRdyEnA = 0.
0	RxRdyEnA	**Channel A $\overline{\text{RXRDYA}}$/LD1A Pin Function Select Bit** Set RxRdyEnA = 1 to enable the receiver-data-ready interrupt functionality on the $\overline{\text{RXRDYA}}$/LD1A pin. In this mode, $\overline{\text{RXRDYA}}$/LD1A asserts when the RDataRdyA bit is set. The $\overline{\text{RXRDYA}}$/LD1A pin is not affected by the RxDaRdyIntEnA interrupt mask. Set RxRdyEnA = 0 to enable the LED driver function on $\overline{\text{RXRDYA}}$/LD1A.

Trigger Register [0x0F]

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIT NAME	—	—	—	—	Trigger3	Trigger2	Trigger1	Trigger0
READ/WRITE	—	—	—	—	W	W	W	W
POR STATE	0	0	0	0	0	0	0	0
RESET UPON READ	—	—	—	—	N	N	N	N

BIT	NAME	DESCRIPTION
7:4	—	These bits are not used.
3:0	Trigger[3:0]	**SPI Trigger Start Transmission Bits** When the SPI master writes a vlue into the trigger register that matches the assigned value in the TrigAssignA/TrigAssignB registers, the MAX14819/MAX14819A immediately starts the cycle timer for the matching channel(s) (if enabled), and starts sending the master message. Note that writing to the trigger register is a global SPI write. Data written to the trigger register is not filtered by the SPI address and is written into the trigger reigster of each MAX14819/MAX14819A device connected to the common SPI bus.

CQCfgA Register [0x10]

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIT NAME	IEC3ThA	SourceSinkA	SinkSelA1	SinkSelA0	NPNA	PushPulA	DrvDisA	CQFilterEnA
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR STATE	0	0	0	0	0	0	0	0
RESET UPON READ	N	N	N	N	N	N	N	N

BIT	NAME	DESCRIPTION
7	IEC3ThA	**Channel A IEC61131-2 Type2/3 Threshold Select** Set IEC3ThA = 0 for IO-Link operation and to select IEC61131-2 type 1 thresholds in SIO digital input mode. Set IEC3ThA = 1 to enable type 2/3 thresholds on receiver CQA, if desired for SIO digital input operation.
6	SourceSinkA	**Channel A CQ Current Sink or Source Select** Set SourceSinkA = 1 to enable the internal current source on CQA. Set SourceSinkA = 0 to enable the internal current sink on CQA. Select the current level with the SinkSelA[1:0] bits.
5:4	SinkSelA[1:0]	**Channel A CQ Sink/Source Current Level Select** Set the SinkSelA[1:0] bits to enable/disable and select the current level of the internal current sink or source on CQA: 00: Current sink/source OFF 01: 5mA 10: 2mA 11: 150µA
3	NPNA	**Channel A CQ Driver NPN/PNP Mode Select** Set NPNA = 1 to configure the CQA driver in NPN mode. Set NPNA = 0 to configure the CQA driver in PNP mode. NPNA is ignored if PushPulA = 1.
2	PushPulA	**Channel A CQ Driver Push-Pull Mode Select** Set PushPulA = 1 to configure the CQA driver in push-pull mode required for IO-Link operation. Set PushPulA = 0 for open-drain operation (NPN or PNP) on the CQA driver.
1	DrvDisA	**Channel A CQ Driver Disable** Set DrvDisA = 1 to disable the CQA driver. CQA is high impedance when disabled. Set DrvDisA = 0 to enable the CQA driver.
0	CQFilterEnA	**Channel A CQ Glitch Filter Enable** Set CQFilterEnA = 1 to enable the glitch filter on the CQA receiver. This is useful for burst filtering. Transients longer than 1.3µs (typ) are ignored when the glitch filter is enabled.

CQCfgB Register [0x11]

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIT NAME	IEC3ThB	SourceSinkB	SinkSelB1	SinkSelB0	NPNB	PushPulB	DrvDisB	CQFilterEnB
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR STATE	0	0	0	0	0	0	0	0
RESET UPON READ	N	N	N	N	N	N	N	N

BIT	NAME	DESCRIPTION
7	IEC3ThB	**Channel B IEC61131-2 Type2/3 Threshold Select** Set IEC3ThB = 0 for IO-Link operation and to select IEC61131-2 type 1 thresholds in SIO digital input mode. Set IEC3ThB = 1 to enable type 2/3 thresholds on receiver CQB, if desired for SIO digital input operation.
6	SourceSinkB	**Channel B CQ Current Sink or Source Select** Set SourceSinkB = 1 to enable the internal current source on CQB. Set SourceSinkB = 0 to enable the internal current sink on CQB. Select the current level with the SinkSelB[1:0] bits.
5:4	SinkSelB[1:0]	**Channel B CQ Sink/Source Current Level Select** Set the SinkSelB[1:0] bits to enable/disable and select the current level of the internal current sink or source on CQB: 00: Current sink/source OFF 01: 5mA 10: 2mA 11: 150µA
3	NPNB	**Channel B CQ Driver NPN/PNP Mode Select** Set NPNB = 1 to configure the CQB driver in NPN mode. Set NPNB = 0 to configure the CQB driver in PNP mode. NPNB is ignored if PushPulB = 1.
2	PushPulB	**Channel B CQ Driver Push-Pull Mode Select** Set PushPulB = 1 to configure the CQB driver in push-pull mode required for IO-Link operation. Set PushPulB = 0 for open-drain operation (NPN or pnp) on the CQB driver.
1	DrvDisB	**Channel B CQ Driver Disable** Set DrvrDisB = 1 to disable the CQB driver. CQB is high impedance when disabled. Set DrvrDisB = 0 to enable the CQB driver.
0	CQFilterEnB	**Channel B CQ Glitch Filter Enable** Set CQFilterEnB = 1 to enable the glitch filter on the CQB receiver. This is useful for burst filtering. Transients longer than 1.3µs (typ) are ignored when the glitch filter is enabled.

CyclTmrA Register [0x12]

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIT NAME	TCyclBsA1	TCyclBsA0	TCyclMA5	TCyclMA4	TCyclMA3	TCyclMA2	TCyclMA1	TCyclMA0
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR STATE	0	0	0	0	0	0	0	0
RESET UPON READ	N	N	N	N	N	N	N	N

BIT	NAME	DESCRIPTION
7:6	TCyclBsA[1:0]	**Channel A Cycle Time-Base Select** Set the TCyclBsA[1:0] bits to select the cycle time base for channel A IO-Link communication. The cycle timer is enabled by setting the CyclTmrEnA bit in the CQCntrlA register. See Table 2.
5:0	TCyclMA[5:0]	**Channel A Cycle Time Multipler** Set the TCyclMA bits to select the cycle time multiplier for channel A communication. ee Table 2.

Table 2. Cycle Time-Base Selection

TCyclBs_[1:0]	TIME BASE	CALCULATION	CYCLE TIME
00	0.1ms	TCyclMA x Time Base	0.4ms to 6.3ms
01	0.4ms	6.4ms + TCyclMA x Time Base	6.4ms to 31.6ms
10	1.6ms	32ms + TCyclMA x Time Base	32ms to 132.8ms
11	N/A	N/A	N/A

CyclTmrB Register [0x13]

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIT NAME	TCyclBsB1	TCyclBsB0	TCyclMB5	TCyclMB4	TCyclMB3	TCyclMB2	TCyclMB1	TCyclMB0
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR STATE	0	0	0	0	0	0	0	0
RESET UPON READ	N	N	N	N	N	N	N	N

BIT	NAME	DESCRIPTION
7:6	TCyclBsB[1:0]	**Channel B Cycle Time-Base Select** Set the TCyclBsB[1:0] bits to select the cycle time base for channel B communication. The cycle timer is enabled by setting the CyclTmrEnB bit in the CQCntrlB register. See Table 2.
5:0	TCyclMB[5:0]	Channel B Cycle Time Multipler Set the TCyclMB bits to select the cycle time multiplier for channel B communication. See Table 2.

DeviceDlyA Register [0x14]

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIT NAME	DelayErrA	BDelayA1	BDelayA0	DDelayA3	DDelayA2	DDelayA1	DDelayA0	RspnsTmrEnA
READ/WRITE	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR STATE	0	0	0	0	0	0	0	0
RESET UPON READ	Y	N	N	N	N	N	N	N

BIT	NAME	DESCRIPTION
7	DelayErrA	**Channel A Delay Error** This bit is set when the device message is not received within the programmed delay time. DelayErrA triggers a RxErrorA interrupt when set. This bit is cleared when the DevDlyA register is read.
6:5	BDelayA[1:0]	**Channel A Additional Byte Delay** Set the BDelayA[1:0] bits to allow additional time between the device UART bytes, on top of the worst case delay defined by the IO-Link standard. The maximum additional delay is 3 bit intervals.
4:1	DDelayA[3:0]	**Channel A Additional Device Message Delay** Set the DDelayA[3:0] bits to allow additional time to the expected device message response delay, on top of the worst case delay defined in the IO-Link standard of 10 bits. The maximum additional delay is 15 bit intervals. Set DDelayA = 1 for IO-Link compliance.
0	RspnsTmrEnA	**Channel A Response Timer Enable** Set RspnsTmrEnA = 1 to enable monitoring of the device message delay from the last stop bit of the message transmitted by the master. If the delay is longer than the expected delay, an RxErrorA interrupt is generated. DelayErrA is set if the IO-Link device takes a longer than usual response time or interpacket delay. Set RspnsTmrEnA = 0 to disable this device message delay monitoring. When RspnsTmrEnA = 0, DelayErrA is always 0.

DeviceDlyB Register [0x15]

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIT NAME	DelayErrB	BDelayB1	BDelayB0	DDelayB3	DDelayB2	DDelayB1	DDelayB0	RspnsTmrEnB
READ/WRITE	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR STATE	0	0	0	0	0	0	0	0
RESET UPON READ	Y	N	N	N	N	N	N	N

BIT	NAME	DESCRIPTION
7	DelayErrB	**Channel B Delay Error** This bit is set when the device message is not received within the programmed delay time. DelayErrB triggers a RxErrorB interrupt when set. This bit is cleared when the DevDlyB register is read.
6:5	BDelayB[1:0]	**Channel B Additional Byte Delay** Set the BDelayB[1:0] bits to allow additional time b etween the device UART bytes, on top of the worst case delay defined by the IO-Link standard. The maximum additional delay is 3 bit intervals.
4:1	DDelayB[3:0]	**Channel B Additional Device Message Delay** Set the DDelayB[3:0] bits to allow additional time to the expected device message response delay, on top of the worst case delay defined in the IO-Link standard of 10 bits. The maximum additional delay is 15 bit intervals. Set DDelayB = 1 for Io-Link compliance.
0	RspnsTmrEnB	**Channel B Response Timer Enable** Set RspnsTmrEnB = 1 to enable monitoring of the device message delay from the last stop bit of the message transmitted by the master. If the delay is longer than the expected delay, an RxErrorB interrupt is generated. DelayErrB is set if the IO-Link device takes a longer than usual response time or interpacket delay. Set RspnsTmrEnB = 0 to disable this device message delay monitoring. When RspnsTmrEnB = 0, DelayErrB is always 0.

TrigAssgnA Register [0x16]

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIT NAME	TrigA3	TrigA2	TrigA1	TrigA0	—	—	—	TrigEnA
READ/WRITE	R/W	R/W	R/W	R/W	R	R	R	R/W
POR STATE	0	0	0	0	0	0	0	0
RESET UPON READ	N	N	N	N	—	—	—	N

BIT	NAME	DESCRIPTION
7:4	TrigA[3:0]	**Channel A Transmission Trigger** Set the TrigA[3:0] bits to assign one of 16 possible trigger values to the CQA transmitter. When the same trigger value is subsequently written by the SPI master to the trigger register, the master message is immediately sent from TxFIFOA and the cycle timer is started (if previously enabled). Trigger 0000 is a global trigger value and is associated with both CQA and CQB by default, this cannot be changed.
6:1	—	These bits are not used
0	TrigEnA	**Channel A Tranmission Triggering Enable** Set TrigEnA = 1 to enable SPI based master message triggering/ synchronization on Channel A. Set TrigEnA = 0 to disable transmitter triggering. When TrigEnA = 0, the bits in TrigA[3:0] are ignored.

TrigAssgnB Register [0x17]

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIT NAME	TrigB3	TrigB2	TrigB1	TrigB0	—	—	—	TrigEnB
READ/WRITE	R/W	R/W	R/W	R/W	R	R	R	R/W
POR STATE	0	0	0	0	0	0	0	0
RESET UPON READ	N	N	N	N	—	—	—	N

BIT	NAME	DESCRIPTION
7:4	TrigB[3:0]	**Channel B Transmission Trigger** Set the TrigB[3:0] bits to assign one of 16 possible trigger values to the CQB transmitter. When the same trigger value is subsequently written by the SPI master to the trigger register, the master message is immediately sent from TxFIFOB and the cycle timer is started (if previously enabled). Trigger 0000 is a global trigger value and is associated with both CQA and CQB by default, this cannot be changed.
6:1	—	These bits are not used.
0	TrigEnB	**Channel B Tranmission Triggering Enable** Set TrigEnB = 1 to enable SPI based master message triggering/ synchronization on Channel B. Set TrigEnB = 0 to disable transmitter triggering. When TrigEnB = 0, the bits in TrigB[3:0] are ignored.

L+CnfgA Register [0x18]

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIT NAME	L+RTA1	L+RTA0	L+DynBLA	L+BLA1	L+BLA0	L+CL2xA	L+CLimDisA	L+EnA
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR STATE	0	0	0	0	0	0	0	0
RESET UPON READ	N	N	N	N	N	N	N	N

BIT	NAME	DESCRIPTION
7:6	L+RTA[1:0]	**Channel A L+ Sensor Supply Current-Limit Autoretry Period** Set the L+RTA[1:0] bits to select the current-limit autoretry period: 00: Latchoff, no autoretry 01: 400ms 10: 4s 11: 12s Latchoff is used for controller-managed timing.

L+CnfgA Register [0x18] (continued)

BIT	NAME	DESCRIPTION
5	L+DynBLA	**Channel A L+ Dynamic Blanking Time Enable/Disable** Set L+DynBLA = 1 to enable the blanking time reduction when the L+A voltage is below the L+ power-good falling threshold. This option allows the circuit to reduce the energy dissipated in the external PMOS2 in case of a shorted output, keeping the current constant. The dynamic blanking time is limited, dependent on the L+ voltage: • Blanking time is reduced to 1/2 programmed time when 9V (typ) ≤ V_L+ ≤ 17V (typ) • Blanking time is reduced to 1/4 programmed time when V_L+ < 9V (typ)
4:3	L+BLA[1:0]	**Channel A L+ Sensor Supply Current Blanking Time** Set the L+BLA[1:0] bits to set the current-limit blanking time for the L+A sensor supply: 00: 5.5ms 01: 16.5ms 10: 55ms 11: 165ms Longer blanking times allow for charging of larger capacitive loads. When selecting the blanking time, consider the power ratings of the external PMOS2 transistors used in the L+A supply line. The V_{DS} on these transistors linearly reduces during capacitive load charge-up. The time to charge a capacitive load is proportional to the maximum current during blanking time.
2	L+CL2xA	**Channel A L+Double Current Limit Enable/Disable** Set L+CL2xA = 1 to enable twice the current set by the current-limit resistor when the L+A voltage is higher than 18V. Set L+CL2xA = 0 to operate the L+A sensor supply with the normal current-limit threshold.
1	L+CLimDisA	**Channel A L+Supply Current Limit Enable/Disable** Set L+CLimDisA = 1 to disable current limiting on the L+A sensor supply. This disables the internal current-sense amplifier. Set L+CLimDisA = 0 to enable current limiting on L+A. The current limit is set by the sense resistor connected between the Channel A pMOSFETs.
0	L+EnA	**Channel A L+Supply Enable** Set the L+EnA = 1 to enable the L+A sensor supply. This turns on the PMOS2 G2A gate driver. When L+EnA is set to 0, the current-limit timers (autoretry, latchoff, and blanking timers) are reset. Set L+EnA = 0 long enough to allow the external PMOS to cool, if needed. Short pulses on L+EnA (less than 200µs) are ignored.

L+CnfgB Register [0x19]

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIT NAME	L+RTB1	L+RTB0	L+DynBLB	L+BLB1	L+BLB0	L+CL2xB	L+CLimDisB	L+EnB
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR STATE	0	0	0	0	0	0	0	0
RESET UPON READ	N	N	N	N	N	N	N	N

BIT	NAME	DESCRIPTION
7:6	L+RTB[1:0]	**Channel B L+ Sensor Supply Current-Limit Autoretry Period** Set the L+RTB[1:0] bits to select the current-limit autoretry period: 00: Latchoff, no autoretry 01: 400ms 10: 4s 11: 12s Latchoff is used for controller-managed timing.
5	L+DynBLB	**Channel B L+ Dynamic Blanking Time Enable/Disable** Set L+DynBLB = 1 to enable the blanking time reduction when the L+B voltage is below the L+ power-good falling threshold. This option allows the circuit to reduce the engery dissipated in the external PMOS2 in case of a shorted output, keeping the current constant. The dynamic blanking time is limited, dependent on the L+ voltage: • Blanking time is reduced to 1/2 programmed time when 9V (typ) ≤ V_L+ ≤ 17V (typ) • Blanking time is reduced to 1/4 programmed time when V_L+ < 9V (typ)
4:3	L+BLB[1:0]	**Channel B L+ Sensor Supply Current Blanking Time** Set the L+BLB[1:0] bits to set the current-limit blanking time for the L+B sensor supply: 00: 5.5ms 01: 16.5ms 10: 55ms 11: 165ms Longer blanking times allow for charging of larger capacitive loads. When selecting the blanking time, consider the power ratings of the external PMOS2 transistors used in the L+B supply line. The V_{DS} on these transistors linearly reduces during capacitive load charge-up. The time to charge a capacitive load is proportional to the maximum current during blanking time.

L+CnfgB Register [0x19] (continued)

BIT	NAME	DESCRIPTION
2	L+CL2xB	**Channel B L+ Double Current-Limit Enable/Disable** Set L+CL2xB = 1 to enable twice the current set by the current-limit resistor when the L+B voltage is higher than 18V. Set L+CL2xB = 0 to operate the L+B sensor supply with the normal current-limit threshold.
1	L+CLimDisB	**Channel B L+ Supply Current-Limit Enable/Disable** Set L+CLimDisB = 1 to disable current limiting on the L+B sensor supply. This disables the internal current-sense amplifier. Set L+CLimDisB = 0 to enabled current limiting on L+B. The current limit is set by the sense resistor connected between the Channel B pMOSFETs.
0	L+EnB	**Channel B L+ Supply Enable** Set the L+EnB = 1 to enable the L+B sensor supply. This turns on the G2B gate driver. When L+EnB is set to 0, the current-limit timers (autoretry, latchoff, and blanking timers) are reset. Set L+EnB = 0 long enough to allow the external PMOS to cool, if needed. Short pulses on L+EnB (less than 200µs) are ignored.

IOStCfgA Register [0x1A]

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIT NAME	DiLevelA	CQLevelA	TxEnA	TxA	DiFilterEnA	DiEC3ThA	DiCSourceA	DiCsinkA
READ/WRITE	R	R	R/W	R/W	R/W	R/W	R/W	R/W
POR STATE	0	0	0	0	0	0	0	0
RESET UPON READ	N	N	N	N	N	N	N	N

BIT	NAME	DESCRIPTION
7	DiLevelA	**Channel A DIA Logic Level** This bit is set when DIA = high. This bit is 0 when DIA = low.
6	CQLevelA	**Channel A CQA Logic Level** This bit is set when CQA = high. This bit is 0 when CQA = low.
5	TxEnA	**Channel A CQ Transmitter Enable Input** When TXTXENDis = 1, this bit has the same functionality as the TXENA input. When TXTXENDis = 0, this bit is ignored.
4	TxA	**Channel A CQ Transmitter Input** When TXTXENDis = 1, this bit has the same functionality as the TXA input. When TXTXENDis = 0, this bit is ignored.
3	DiFilterEnA	**Channel A DI Glitch Filter Enable/Disable** Set DiFilterEnA = 1 to enable the glitch filter on DIA. Set DiFilterEnA = 0 to disable the glitch filter. Transients longer than 1.3µs (typ) are ignored when the glitch filter is enabled.
2	DiEC3ThA	**Channel A IEC61131-2 Type2/3 Threshold Select** Set DiEC3ThA = 1 to enable type 2/3 thresholds on the DIA receiver. Set DiEC3ThA = 0 to enable type 1 threholds on the DIA receiver.
1	DiCSourceA	**Channel A DI Current Source Enable/Disable** Set DiCSourceA = 1 to enable the 2mA (typ) current source on DIA. Set DiCSourceA = 0 to disable the current source.
0	DiCSinkA	**Channel A DI Current Sink EnableDisable** Set DiCSinkA = 1 to enable the 2mA (typ) current sink on DIA. Set DiCSinkA = 0 to disable to current sink.

IOStCfgB Register [0x1B]

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIT NAME	DiLevelB	CQLevelB	TxEnB	TxB	DiFilterEnA	DiEC3ThA	DiCSourceA	DiCsinkB
READ/WRITE	R	R	R/W	R/W	R/W	R/W	R/W	R/W
POR STATE	0	0	0	0	0	0	0	0
RESET UPON READ	N	N	N	N	N	N	N	N

BIT	NAME	DESCRIPTION
7	DiLevelB	**Channel A DIA Logic Level** This bit is set when DIB = high. This bit is 0 when DIB = low.
6	CQLevelB	**Channel A CQA Logic Level** This bit is set when CQB = high. This bit is 0 when CQB = low.
5	TxEnB	**Channel A CQ Transmitter Enable Input** When TXTXENDis = 1, this bit has the same functionality as the TXENB input. When TXTXENDis = 0, this bit is ignored.
4	TxB	**Channel B CQ Transmitter Input** When TXTXENDis = 1, this bit has the same functionality as the TXB input. When TXTXENDis = 0, this bit is ignored.
3	DiFilterEnB	**Channel B DI Glitch Filter Enable/Disable** Set DiFilterEnB = 1 to enable the glitch filter on DIB. Set DiFilterEnB = 0 to disable the glitch filter. Transients longer than 1.3µs (typ) are ignored when the glitch filter is enabled.
2	DiEC3ThB	**Channel B IEC61131-2 Type2/3 Threshold Select** Set DiEC3ThB = 1 to enable type 2/3 thresholds on the DIB receiver. Set DiEC3ThB = 0 to enable type 1 thresholds on the DIB receiver.
1	DiCSourceB	**Channel B DI Current Source Enable/Disable** Set DiCSourceB = 1 to enable the 2mA (typ) current source on DIB. Set DiCSourceB = 0 to disable the current source.
0	DiCSinkB	**Channel B DI Current Sink EnableDisable** Set DiCSinkB = 1 to enable the 2mA (typ) current sink on DIB. Set DiCSinkB = 0 to disable to current sink.

DrvrCurrLim Register [0x1C]

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	CL1	CL0	CLDis	CLBL1	CLBL0	TAr1	TAr0	ArEn
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	0	0	0	0	0	0	0	0
Reset Upon Read	N	N	N	N	N	N	N	N

BIT	NAME	DESCRIPTION
7:6	CL[1:0]	**CQA and CQB Driver Current-Limit Selection** Set the CL[1:0] bits to set the current limit for the CQA and CQB drivers when CLDis = 0: 00: 100mA 01: 200mA 10: 300mA 11: 500mA
5	CLDis	**CQA and CQB Driver Current Enable/Disable** Set CLDis = 1 to disable current limiting on the CQA and CQB drivers. Set CLDis = 0 to enable current limiting on the CQA and CQB driver. When CLDis = 0, the CQA and CQB driver current limit is set by the CL[1:0] bits.
4:3	CLBL[1:0]	**Blanking Time Selection** Set the CLBL[1:0] bits to set the blanking time on the CQA and CQB drivers before a fault is indicated: 00: 128µs 01: 500µs 10: 1ms 11: 5ms The blanking time affects the maximum capacitive and incandescent lamp load that can be driven without triggering the fault signal. In order to drive very large capacitive or lamp loads, increase the blanking time and/or disable the autoretry timeout.
2:1	TAr[1:0]	**Autoretry Timeout Selection** When a fault is detected on a driver output, the driver is disabled for the autoretry timeout. The driver is reenabled following the autoretry timeout. Set the TAr[1:0] bits to select the autoretry timeout: 00: 50ms 01: 100ms 10: 200ms 11: 500ms
0	ArEn	**Autoretry Enable/Disable** Set ArEn = 1 to enable autoretry functionality when a fault condition occurs on CQA or CQB. When a fault is detected on a driver, the driver is disabled for the autoretry fixed off time (set in the TAr[1:0] bits). The driver is reenabled and, following the blanking time, is rechecked. If the fault persists, the fault bit is left set and the driver is disabled again. When the fault is removed, the status bit is reset and the driver returns to normal operation.

Clock Register [0x1D]

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIT NAME	VCCWarnEn	TXTXENDis	ExtClkMis	ClkOEn	ClkDiv1	ClkDiv0	ExtClkEn	XtalEn
READ/WRITE	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W
POR STATE	0	0	0	0	0	0	0	0
RESET UPON READ	N	N	N	N	N	N	N	N

BIT	NAME	DESCRIPTION
7	VCCWarnEn	**V_{CC} Warning Interrupt Enable** Set VCCWarnEn = 1 to enable the StatusInt interrupt when V_{CC} drops below the 18V (typ) V_{CC} warning threshold. When VCCWarnEn = 0, the VCCWarn bit in the Status register is active, but does not generate a StatErrInt interrupt when the V_{CC} voltage drops below 18V (typ).
6	TXTXENDis	**CQ_ Pin Control Enable/Disable** Set TXTXENDis = 1 to disable the external TX_ and TXEN_ input pins and to enable control of the CQ_ outputs through the Tx_ and TxEn_ bits in the IOStCfgA and IOStCfgB registers.
5	ExtClkMis	This bit is set when the external clock or crystal oscillator is not operational. When the external clock source (either crystal oscillator or the external clock on CLKI) fails, the internal clock takes over and the ExtClkMis bit is set. Wait 100ms after startup before reading ExtClkMis.
4	ClkOEn	**Clock Output Pin (CLKO) Enable/Disable** Set ClkOEn = 1 to enable the 3.686MHz output clock on the CLKO pin.
3:2	ClkDiv[1:0]	**External Crystal Frequency Divider** Set the ClkDiv[1:0] bits to select the frequency divider quotient related to the external crystal frequency: 00: 14.745MHz 01: 7.373MHz 10 and 11: 3.686MHz
1	ExtClkEn	**External Clock Input Enable/Disable** Set ExtClkEn = 1 to enable clocking from the CLKI input. XtalEn must be set to 0 when ExtClkEn is 1. Set ExtClkEn = 0 and XtalEn = 0 when the internal framer and neither the external clock, nor external crystal, are not used.
0	XtalEn	**Crystal Oscillator Enable/Disable** Set XtalEn = 1 to enable the internal crystal oscillator. ExtClkEn must be set to 0 when XtalEn is 1. Set XtalEn = 0 and ExtClkEn = 0 when the internal framer and neither the external clock, nor external crystal, are not used.

Status Register [0x1E]

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIT NAME	ThShdnCOR	ThWarnCOR	VCCUVCOR	VCCWarnCOR	ThShdn	ThWarn	VCCUV	VCCWarn
READ/WRITE	R	R	R	R	R	R	R	R
POR STATE	0	0	0	0	0	0	0	0
RESET UPON READ	Y	Y	Y	Y	N	N	N	N

BIT	NAME	DESCRIPTION
7	ThShdnCOR	**Clear-On-Read Thermal Shutdown** Clear-on-read version of the ThShdn bit. This bit is set only when the ThShdn bit transitions from 0 to 1. A StatusInt interrupt is generated when this bit is set. This bit is cleared when Status register is read.
6	ThWarnCOR	**Clear-On-Read Die Temperature Warning** Clear-on-read version of the ThWarn bit. This bit is set only when the ThWarn bit transitions from 0 to 1. A StatusInt interrupt is generated when this bit is set. This bit is cleared when the Status register is read.
5	VCCUVCOR	**Clear-On-Read V_{CC} Undervoltage Warning** Clear-on-read version of the VCCUV bit. This bit is set only when the VCCUV bit transitions from 0 to 1. A StatusInt interrupt is generated when this bit is set. This bit is cleared when the Status register is read.
4	VCCWarnCOR	**Clear-On-Read V_{CC} Supply Voltage Warning** Clear-on-read version of the VCCWarn bit. This bit is set only when the VCCWarn bit transitions from 0 to 1. A StatusInt interrupt is generated when this bit is set, if enabled by setting the VccWarnEn bit. This bit is cleared when the Status register is read.
3	ThShdn	**Thermal Shutdown** This bit is set when the die temperature reaches 150°C and the die enters thermal shutdown. This bit is cleared when the die temperature falls and the part is no longer in thermal shutdown.
2	ThWarn	**Die Temperature Warning** This bit is set when the die junction temperature exceeds the 135°C warning threshold. This bit is cleard when the die temperature falls below 120°C.
1	VCCUV	**V_{CC} Undervoltage** This bit is set when the V_{CC} voltage falls below 9V (typ). It is cleared when the V_{CC} voltage rises above 9V (typ).
0	VCCWarn	**V_{CC} Supply Voltage Warning** This bit is set when the V_{CC} voltage falls below 18V (max). It is cleared when the V_{CC} voltage rises above 15.5V (min).

RevID Register [0x1F]

BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIT NAME	—	—	—	—	ID3	ID2	ID1	ID0
READ/WRITE	R	R	R	R	R	R	R	R
POR STATE (MAX14819)	0	0	0	0	1	0	1	0
POR STATE (MAX14819A)	0	0	0	0	1	1	1	0
RESET UPON READ	N	N	N	N	N	N	N	N

BIT	NAME	DESCRIPTION
[7:4]	—	These bits are not used.
[3:0]	ID[3:0]	**CHIP ID Bits** These bits are ready only. They reflect the current revision of the MAX14819/MAX14819A. The RevID register is meant for use during system/chip initialization and should not be used during IO-Link communication, since a byte may be lost in the RxFIFOA. The RevID register is 0b00001010 for the MAX14819 and 0b00001110 for the MAX14819A.

The MAX14819/MAX14819A continues to operate normally unless the die temperature reaches the +160°C (typ) thermal-shutdown threshold, at which time the device enters thermal shutdown.

Applications Information

The Microcontroller Interface

Logic-Level I/Os

The logic levels of the microcontroller interface I/Os are defined by V_L. Apply a supply voltage between 1.62V and 5.5V to V_L for normal operation. Logic outputs are supplied by V_L.

Efficient Microcontroller Interface Management

When the MAX14819/MAX14819A receives the device responsemessage completely and error-free, an SPI RxDataRdy_ interrupt is generated and $\overline{IRQ}$ asserts. If enabled, the hardware interrupt ($\overline{RXRDY}$_/LD1_) also asserts. When the SPI master receives the interrupt and then reads out the device message from the RxFIFO_, the RxDataRdy_ bit and $\overline{RXRDY}$_/LD1_ pin interrupts are then automatically cleared.

If the device message is received by the MAX14819/MAX14819A with errors or not in time, then an RxError_ interrupt occurs ($\overline{IRQ}$ asserts) and optionally, the $\overline{RXERR}$_/LD2_ hardware interrupt also asserts if enabled. The MAX14819/MAX14819A can be configured to delete the device message under these circumstances and resend the master message with the SPI controller managing the process. The SPI controller is required only when the device message is ready and the MAX14819/MAX14819A is ready for the next master message (Figure 19).

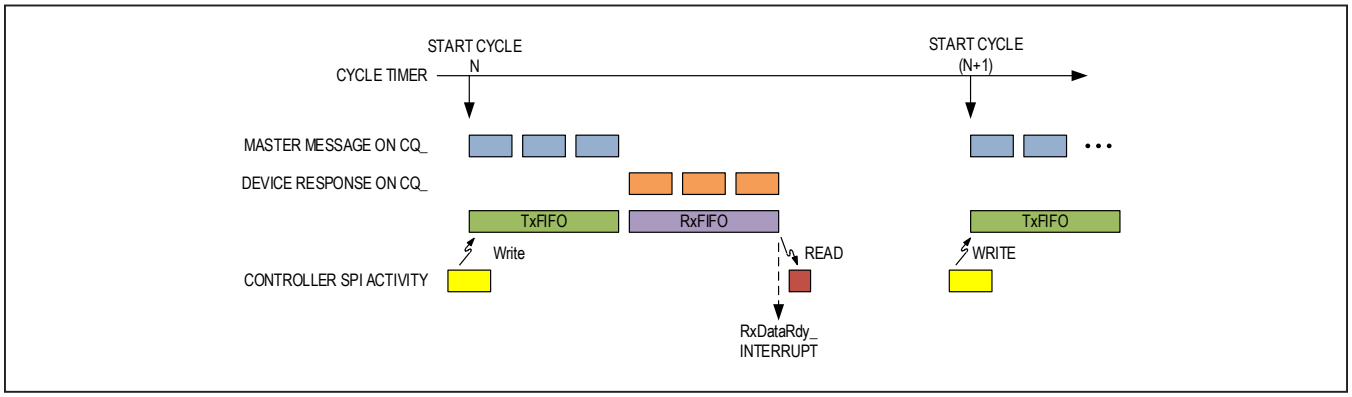


Figure 19. IO-Link Cycle Timing

Quartz Crystal Selection

The crystal should have a frequency of either 3.6864MHz, 7.3728MHz, or 14.7456MHz. Select a crystal with an equivalent series resistance (ESR), including stray resistances, less than 75Ω (max).

The crystal oscillator drives the crystal with a power limited to 70µW (max) power dissipation in the crystal based on a 14.7456MHz frequency, 8pF (max) shunt capacitance, and 75Ω equivalent series resistance.

The input capacitance of the MAX14819/MAX14819A XIN and XOUT pins is 10pF, so no external capacitors are needed if the crystal's load capacitance is in this range. If the selected crystal requires higher load capacitance, connect capacitors at XIN and XOUT to GND to make up for the difference.

Selecting the pMOS Transistors for the L+A/L+B Supplies

Select PMOS1_ and PMOS2_ transistors whose drain-to-source current (I_{DS}) carrying capability is higher than the maximum load current. The maximum load current for an application is set by the selected current limit resistor and the L+CL2x_ bits.

It is important to select pMOS FETs with low $R_{DS(ON)}$ to minimize the I^2R heat generation in the module. When turned on, the PMOS1_ and PMOS2_ gate-to-source voltage (V_{GS}) is driven to -12.5V (typ). Use this bias condition for selecting the $R_{DS(ON)}$ of the pMOS.

The pMOS transistors need to support the minimum and maximum voltages expected at the V_{CC} and L+_ terminals. Select the transistor such that the drain-to-source voltage (V_{DS}) of PMOS1_ FET is able to support the most negative V_{CC} voltage, while the L+_ supply maintains a positive voltage (e.g., 28V) due to capacitance on the line. Similarly, ensure that the V_{DS} of the PMOS2_ FET is large enough to support the maximum V_{CC} voltage while L+_ is shorted to the most negative voltage.

When the L+ supply output is shorted to ground or a negative voltage, the PMOS2_ FET dissipates the maximum heat. The heat energy is determined by the current-limit current, the on-to-off duty cycle (i.e., blanking time/autoretry time), and the V_{DS} voltage. Select a PMOS2_ transistor with a low thermal impedance to efficiently conduct away the heat.

The IO-Link specification requires the L+ sensor supply be able to supply a minimum of 400mA load current for 50ms after L+ supply turn-on. Hence the blanking time should be programmed to 55ms or larger. PMOS2 must be able to dissipate the transient heat pulse produced as a result of L+ output short-circuit for the length of the programmed blanking time.

Because the PMOS1_ transistor is not a part of the current-limiting circuitry, it does not dissipate as much heat as PMOS2_ during a short-circuit event.

Ensure that the PMOS1_ and PMOS2_ FETs have gate-source threshold voltages less than 0.8V ($V_{GS(th)}$ < -0.8V).

Examples of suitable pMOS FETs (depending on desired current limits) are NVMFS5113PL, NTTFS5116PL, and Si7415DN.

Transient Protection

Inductive Loads

Both the CQ_ drivers and the L+_ supplies can drive and switch inductive loads. External TVS/zener-clamping diodes are required to clamp the kickback voltage and absorb energy when inductive loads are driven and fast turn-off is needed. The clamping voltage must be less than the Absolute Maximum voltage ratings of the CQA and CQB pins. In some cases, the EMC protection devices may be adequate for this purpose.

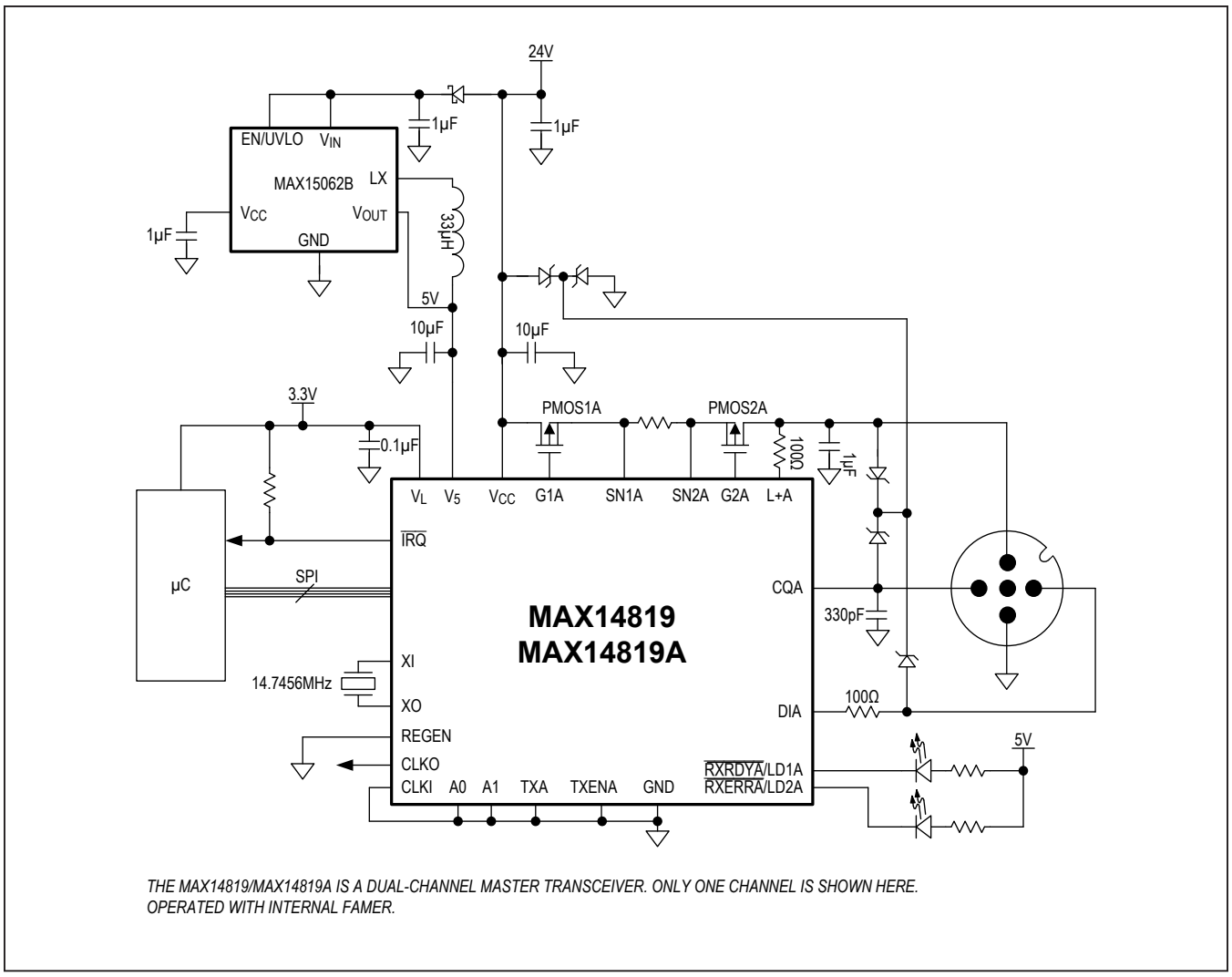
Surge, Burst, and ESD Protection

The CQ_, DI_, L+, and V_{CC} pins need to be protected against electrostatic discharge (ESD), electrical fast transients (EFT), and possible surges. The *Absolute Maximum Ratings* for these pins is (V_{CC} - 70V) to +65V, providing significant headroom to allow the use of physically small protection diodes and higher protection voltages. For standard ESD and burst protection demanded by the IO-Link specification, small package TVS (like the uClamp3603T or the SPT01-335) can be used to protect the CQ_, DI, and L+_ lines. If higher level surge ratings need to be achieved, such as IEC 61000-4-5 ±1kV/42Ω, PDFN3-32, SPT02-236, or SMCJ48A, TVS protectors can be used on CQ_, DI_ and L+. 48V TVS diodes allow for high negative voltages, making these pins tolerant to negative short circuits and reverse polarity.

For ±500V/2Ω IEC 61000-4-5 surge protection on the V_{CC} input, Maxim recommends the SM30TY47AY and SM30TY33AY.

Using a Step-Down Regulator with the 5V Regulator

To decrease power dissipation in the MAX14819/MAX14819A, V_5 can be powered by an external step-down regulator. Connect the external regulator's output to the V_5 input and disable the internal 5V regulator by connecting REGEN to ground (Figure 20).



THE MAX14819/MAX14819A IS A DUAL-CHANNEL MASTER TRANSCEIVER. ONLY ONE CHANNEL IS SHOWN HERE. OPERATED WITH INTERNAL FAMER.

Figure 20. Using an External 5V Step-Down Regulator

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14819ATM+	-40°C to +125°C	48 TQFN-EP*
MAX14819ATM+T	-40°C to +125°C	48 TQFN-EP*
MAX14819AATM+	-40°C to +125°C	48 TQFN-EP*
MAX14819AATM+T	-40°C to +125°C	48 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
T = Tape and reel.

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/17	Initial release	—
1	8/17	Updated/corrected figures and text	1, 2, 8, 23, 26, 28, 39, 40, 45, 46, 52, 53, 62, 63, 69
2	8/18	Updated *Absolute Maximum Ratings* section, *Electrical Characteristics* table, *Pin Description* table, *Framer Communication* section, *Establish-Communication Sequencer* section, *Cycle Timer* section, *Register Map*, and registers	3, 8, 19, 26, 29, 31, 52, 53, 58–60, 65, 66, 68
2.1		Corrected typos	22
3	3/30	Updated title and added the MAX14819A to all part references in text and figures; updated *General Description*, *Functional Diagram*, *Electrical Characteristics*, Figure 1, Figure 2, Figure 3, Figure 4, Figure 5, *Pin Description*, *Detailed Description*, V_{CC} *Low Voltage and Undervoltage Detection*, *5V Linear Regulator*, *L+ Sensor Supply Controllers*, *L+_ Blanking Time and Autoretry Functionality*, CQ_ *Current Limit and Thermal Protection*, *CQ_ Current Sources/Sinks*, *DI_ Receiver*, *SPI Interface*, *SPI Chip Address (A1, A0)*, *SPI Interface*, *SPI Chip Address (A1, A0)*, *SPI In-Band IRQ Interrupt*, *SPI In-Band Device-Message-Ready Signaling*, Table 1, *Wake-Up Pulse Generation*, *Microcontroller Data Interface*, *Framer Communication*, *Frame Handler FIFOs (TxRxFIFOA/TxRxFIFOB)*, *Transmit/Receive FIFO Data Structure*, *Loading the Transmit FIFO (TxFIFO_)*, *Initiating Transmission*, *Transmit Loopback Check*, *Receiving the Device Message*, *Monitoring Message Timing*, *Checksum Calculation and Checking*, *Establish-Communication Sequencer*, *Transmitter Synchronization*, *Trigger Delay and Synchronization Accuracy*, *Cycle Timer*, *Clocking*, *LED Control*, *Thermal Protection*, sections; Added *Response Time Checking (MAX14819A Only), and Applications Information*, *Efficient Microcontroller Interface Management*, *Quartz Crystal Selection*, *Surge, Burst, and ESD Protection*, *Using a Step-Down Regulator with the 5V Regulator* section, replaced Figure 20 and the *Typical Operating Circuit*; added the *Response Time Checking (MAX14819A Only)*; updated *Registers RxFIFOLvlA Register [0x04]*, *RxFIFOLvlB Register [0x05]*,*CQErrA Register [0x08]*, *CQErrB Register [0x09]*, *MsgCtrlB [0x0B]*, *ChanStatA Register [0x0C]*, *ChanStatB Register [0x0D]*, *Trigger Register [0x0F]*, *DeviceDlyB Register [0x15]*, *L+CnfgA Register [0x18]*, *L+CnfgB Register [0x19]* and *RevID Register [0x1F]*	1–71

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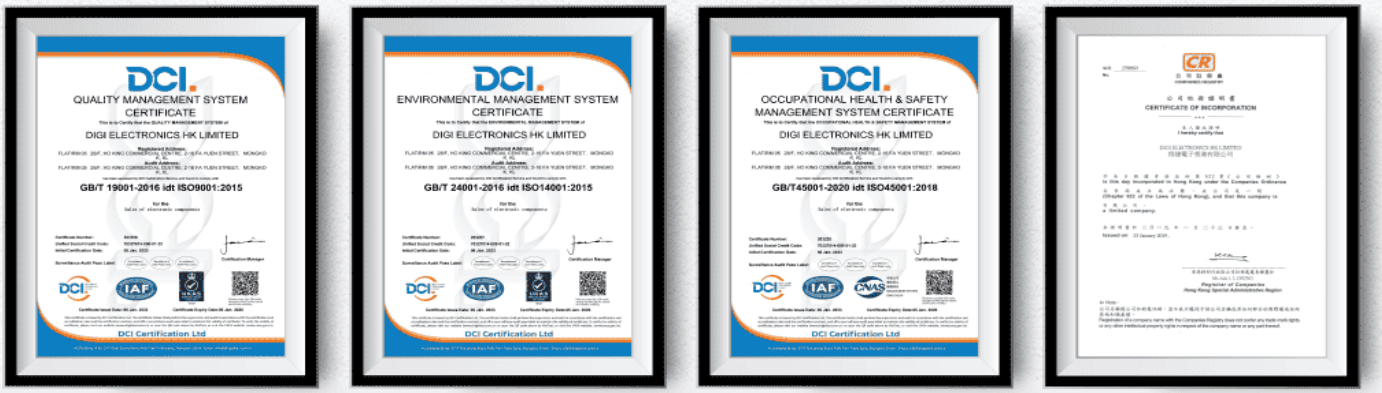

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