MAX14882AWE+ Datasheet

https://www.DiGi-Electronics.com

DiGi Electronics Part Number	MAX14882AWE+-DG
Manufacturer	Analog Devices Inc./Maxim Integrated
Manufacturer Product Number	MAX14882AWE+
Description	IC TXRX/ISO 1/1 16SOIC
Detailed Description	1/1 Transceiver, Isolated CANbus 16-SOIC

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Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
MAX14882AWE+	Analog Devices Inc./Maxim Integrated
Series:	Product Status:
-	Active
Type:	Protocol:
Transceiver, Isolated	CANbus
Number of Drivers/Receivers:	Duplex:
1/1	-
Receiver Hysteresis:	Data Rate:
125 mV	1Mbps
Voltage - Supply:	Operating Temperature:
3V ~ 5.5V	-40°C ~ 125°C
Mounting Type:	Package / Case:
Surface Mount	16-SOIC (0.295", 7.50mm Width)
Supplier Device Package:	Base Product Number:
16-SOIC	MAX14882

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8542.39.0001	

EVALUATION KIT AVAILABLE

*Click **here** for production status of specific part numbers.*

MAX14882

5kV$_{RMS}$ Isolated CAN Transceiver with Integrated Transformer Driver

General Description

The MAX14882 isolated high-speed CAN transceiver improves communication and safety by integrating galvanic isolation between the CAN-protocol controller-side (TDX, RXD) of the device and the physical wires of the CAN network (CANH, CANL) cable-side/bus-side of the transceiver. Isolation improves communication by breaking ground loops and reduces noise where large differences in ground potentials exists between ports. The MAX14882 provides up to 5000V$_{RMS}$ (60s) of galvanic isolation and a continuous working voltage of up to 848V$_{RMS}$, while operating at the maximum high-speed CAN data rate of 1Mbps.

The MAX14882 features additional integrated protection for robust communication. The ±25V receiver input common-mode range exceeds the ISO 11898 specification requirement of -2V to +7V. Additionally, the CANH and CANL IOs are fault tolerant up to ±54V and are protected from electrostatic discharge (ESD) up to ±15kV to GNDB on the bus-side, as specified by the Human Body Model (HBM).

Interfacing with CAN-protocol controllers is simplified by the wide 3.0V to 5.5V supply voltage range (V$_{DDA}$) on the controller-side of the device. The supply voltage range for the CAN bus-side of the device is 4.5V to 5.5V (V$_{DDB}$). An integrated transformer driver and LDO can be used, with an external transformer, to generate the isolated supply for V$_{DDB}$.

Field installation and troubleshooting are simplified by the polarity select (POL) input. POL swaps the functions of the CANH and CANL IOs, allowing for simple software correction of cross-wired bus cables in the field.

The MAX14882 operates over the -40°C to +125°C temperature range and is available in a 16-pin wide SOIC (W SOIC) package with 8mm of creepage and clearance.

Applications

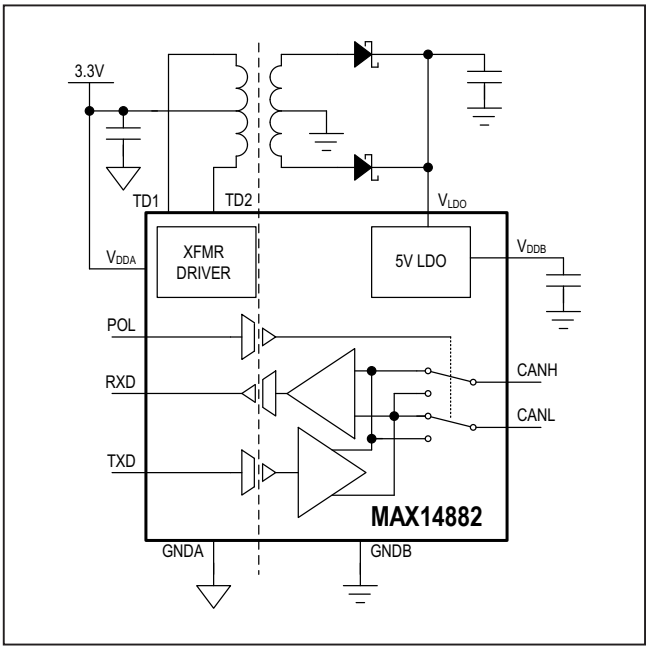
- Building Automation
- Industrial Controls
- HVAC
- Switching Gear

Benefits and Features

- Integrated Protection for More Robust Communication
  - 5kV$_{RMS}$ Withstand Galvanic Isolation (60s)
  - ±25V Common Mode Range
  - ±54V Fault Protection
  - ±15kV ESD (HBM) Protection on Driver Outputs/ Receiver Inputs
- High-Performance Transceiver Enables Flexible Designs
  - Wide 3.0V to 5.5V Supply Voltage Range for CAN Controller Interface
  - Field Bus Polarity Control (POL)
  - Integrated Transformer Driver for Power Transfer to Bus-Side
  - Integrated LDO for Powering CAN Bus-Side
- Safety Regulatory Approvals (Pending)
  - UL1577 (Basic Insulation)
  - cUL According to CSA Bulletin 5A

***Ordering Information** appears at end of data sheet.*

Simplified Block Diagram



19-100246; Rev 1; 7/19

Absolute Maximum Ratings

V_{DDA} to GNDA ..... -0.3V to +6V
V_{DDB} to GNDB ..... -0.3V to +6V
V_{LDO} to GNDB ..... -0.3V to +16V
TD1,TD2 to GNDA ..... -0.3V to +12V
TXD, POL to GNDA ..... -0.3V to +6V
RXD to GNDA ..... -0.3V to (V_{DDA} + 0.3V)
I.C. to GNDB ..... -0.3V to (V_{DDB} + 0.3V)
CANH or CANL to GNDB (Continuous) ..... -54V to +54V
Short-Circuit Duration (CANH to CANL) ..... Continuous
Short Circuit Duration (CAN_ to GNDB or V_{DDB}) ..... Continuous
Short-Circuit Duration (RXD to GNDA or V_{DDA}) ..... Continuous
TD1, TD2 Continuous Current ..... ±1.4A
Continuous Power Dissipation (T_A = +70°C)
16-pin W SOIC (Derate 14.1mW/°C above +70°C) ... 1126.8mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -60°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

Wide 16-SOIC

PACKAGE CODE	W16+10
Outline Number	21-0042
Land Pattern Number	90-0107
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	107 °C/W
Junction to Case (θ_{JC})	22 °C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	71 °C/W
Junction to Case (θ_{JC})	23 °C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{DDA} = 3.0V to 5.5V, V_{DDB} = 4.5V to 5.5V, POL =GNDA, I.C. = GNDB, T_A = -40°C to +125°C. Typical values are at V_{DDA} = 3.3V, V_{DDB} = 5V, GNDA = GNDB, and T_A = +25°C, unless otherwise noted. (Notes 1, 2))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER							
Controller-Side (A-Side) Voltage Supply	V_{DDA}			3		5.5	V
Bus-Side (B-Side) Voltage Supply	V_{DDB}			4.5		5.5	V
Controller Side (A-Side) Supply Current	I_{DDA}	POL = TXD = high or low, RXD unconnected, TD1/TD2 unconnected	V_{DDA} = 5V		4.7	7.7	mA
			V_{DDA} = 3.3V		4.5	7.5	

Electrical Characteristics (continued)

(V_{DDA} = 3.0V to 5.5V, V_{DDB} = 4.5V to 5.5V, POL =GNDA, I.C. = GNDB, T_A = -40°C to +125°C. Typical values are at V_{DDA} = 3.3V, V_{DDB} = 5V, GNDA = GNDB, and T_A = +25°C, unless otherwise noted. (Notes 1, 2))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Bus-Side (B-Side) Supply Current	I_{DDB}	V_{DDB} = 5V	TXD = GNDA, R_L = open		9.4	15.5	mA
			TXD = GNDA, R_L = 60Ω		52	76	
			TXD = V_{DDA}, R_L = 60Ω		8.5		
			TXD = GNDA, CANH shorted to CANL		98	130	
			TXD = V_{DDA}, CANH shorted to CANL		8.5		
Controller-Side (A-Side) Undervoltage Lockout Threshold	V_{UVLOA}	V_{DDA} rising	RXD, TXD, POL			1.66	V
			TD1, TD2			2.85	
Controller-Side (A-Side) UVLO Hysteresis	V_{UVLOA_HYST}	V_{DDA} falling	RXD, TXD, POL		50		mV
			TD1, TD2		200		
Bus-Side (B-Side) Under-voltage Lockout Threshold	V_{UVLOB}	V_{DDB} rising				4.25	V
		V_{DDB} falling		3.45			
TRANSFORMER DRIVER							
TD1, TD2 Output Resistance	R_O	TD1/TD2 = low, $I_{TD\_}$ = 300mA			0.6	1.5	Ω
TD1, TD2 Current Limit	I_{LIM}	4.5V ≤ V_{DDA} ≤ 5.5V		540	785	1300	mA
		3.0V ≤ V_{DDA} ≤ 3.6V		485	730	1170	
Switching Frequency	f_{SW}			350	450	550	kHz
Duty Cycle	D				50		%
Crossover Dead Time	t_{DEAD}				50		ns
LDO							
LDO Supply Voltage	V_{LDO}	(Note 3)		4.68		14	V
LDO Output Voltage	V_{DDB}			4.5	5	5.5	V
LDO Current Limit					300		mA
Load Regulation		V_{LDO} = 6V, I_{LOAD} = 20mA to 40mA			0.19		mV/mA
Line Regulation		V_{LDO} = 6V to 9.5V, I_{LOAD} = 20mA			0.12	1.8	mV/V
Dropout Voltage		V_{LDO} = 4.68V, I_{DDB} = -120mA			100	180	mV
Load Capacitance		Nominal value (Notes 4, 5)		1		10	µF
CAN BUS DRIVER							
Dominant Output Voltage High	V_{CAN_DH}	TXD = GNDA, 50Ω ≤ R_L ≤ to 65Ω	CANH, POL = GNDA	2.75		4.5	V
			CANL, POL = V_{DDA}	2.75		4.5	
Dominant Output Voltage Low	V_{CAN_DL}	TXD = GNDA, 50Ω ≤ R_L ≤ to 65Ω	CANH, POL = GNDA	0.5		2.25	V
			CANL, POL = V_{DDA}	0.5		2.25	
Dominant Output Voltage, Differential	V_{OD}	50Ω ≤ R_L ≤ 65Ω, Figure 1	R_{CM} = Open	1.5		3	V
			R_{CM} = 1.25kΩ, -17V ≤ V_{CM} ≤ +17V	1.5		3	
			R_{CM} = 1.25kΩ, -25V ≤ V_{CM} ≤ +25V	1.1		3	

Electrical Characteristics (continued)

(V_{DDA} = 3.0V to 5.5V, V_{DDB} = 4.5V to 5.5V, POL =GNDA, I.C. = GNDB, T_A = -40°C to +125°C. Typical values are at V_{DDA} = 3.3V, V_{DDB} = 5V, GNDA = GNDB, and T_A = +25°C, unless otherwise noted. (Notes 1, 2))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CANH Recessive Output Voltage	V_{CAN_HR}	TXD = V_{DDA}, no load		2		3	V
CANL Recessive Output Voltage	V_{CAN_RL}	TXD = V_{DDA}, no load		2		3	V
Recessive Output Voltage, Differential		TXD = V_{DDA}	R_L = 60Ω	-12		+12	mV
			R_L = Open	-50		+50	
High-Side Short-Circuit Current	I_{SHORT_H}	TXD = GNDA	POL = GNDA, CANH = GNDB	50	75	100	mA
			POL = V_{DDA}, CANL = GNDB	50	75	100	
Low-Side Short-Circuit Current	I_{SHORT_L}	TXD = GNDA	POL = GNDA, CANL = V_{DDB}	50	75	100	mA
			POL = V_{DDA}, CANH = V_{DDB}	50	75	100	
RECEIVER							
Common Mode Input Range		CANH or CANL to GNDB, RXD output valid		-25		+25	V
Differential Input Voltage (Recessive)	V_{ID_R}	$\lvert V_{CANH} - V_{CANL} \rvert$, TXD = V_{DDA}		0.5			V
Differential Input Voltage (Dominant)	V_{ID_D}	$\lvert V_{CANH} - V_{CANL} \rvert$, TXD = V_{DDA}				0.9	V
Differential Input Hysteresis					125		mV
Common-Mode Input Resistance	R_{IN}	TXD = V_{DDA}, R_{IN} = ΔV/ΔI, ΔV = +300mV		10		50	kΩ
Differential Input Resistance	R_{DIFF_IN}	TXD = V_{DDA}, R_{IN} = ΔV/ΔI, ΔV = +300mV		20		100	kΩ
Input Leakage Current		V_{DDB} = GNDB, V_{CANH} = V_{CANL} = 5V				310	µA
Input Capacitance		CANH or CANL to GNDB, T_A = +25ºC (Note 4)			14.4	20	pF
Differential Input Capacitance		CANH to CANL, T_A = +25°C (Note 4)			7.2	10	pF
LOGIC INTERFACE (RXD, TXD, POL)							
Input High Voltage	V_{IH}	POL, TXD to GNDA		0.7 x V_{DDA}			V
Input Low Voltage	V_{IL}	POL, TXD to GNDA				0.8	V
Input Hysteresis	V_{HYS}				220		mV
Output High Voltage	V_{OH}	RXD, I_{OUT} = -4mA		V_{DDA} - 0.4			V
Output Low Voltage	V_{OL}	RXD, I_{OUT} = 4mA				0.4	V
Input Pullup Current	I_{PU}	TXD		-10	-4.5	-1.5	µA
Input Pulldown Current	I_{PD}	POL		1.5	4.5	10	µA
Input Capacitance	C_{IN}				2		pF

Electrical Characteristics (continued)

(V_{DDA} = 3.0V to 5.5V, V_{DDB} = 4.5V to 5.5V, POL =GNDA, I.C. = GNDB, T_A = -40°C to +125°C. Typical values are at V_{DDA} = 3.3V, V_{DDB} = 5V, GNDA = GNDB, and T_A = +25°C, unless otherwise noted. (Notes 1, 2))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PROTECTION							
Fault Protection Range		CANH, CANL to GNDB		-54		+54	V
ESD Protection (CANH and CANL to GNDB)		IEC 61000-4-2 Air-Gap Discharge			±10		kV
		IEC 61000-4-2 Contact Discharge			±5		
		Human Body Model (HBM)			±15		
ESD Protection (CANH and CANL to GNDA)		IEC 61000-4-2 Contact Discharge			±3		kV
		IEC 61000-4-2 Air Gap Discharge. 470pF capacitor connected between GNDA and GNDB			±10		
ESD Protection (All Other Pins)		Human Body Model (HBM)			±2		kV
Thermal Shutdown	T_{SHDN}	Junction temperature rising			+160		°C
Thermal Shutdown Hysteresis	T_{SH_HYST}				13		°C
SWITCHING CHARACTERISTICS							
Common-Mode Transient Immunity	CMTI	(Note 6)			35		kV/µs
Driver Rise Time	t_R	R_{CM} is open, R_L = 60Ω, C_L = 100pF, 10% to 90% of transition on $\|V_{CANH} - V_{CANL}\|$, Figure 1				23	ns
Driver Fall Time	t_F	R_{CM} is open, R_L = 60Ω, C_L = 100pF, 90% to 10% of transition on $\|V_{CANH} - V_{CANL}\|$, Figure 1				31	ns
TXD to RXD Loop Delay	t_{LOOP}	Dominant to recessive and recessive to dominant, R_L= 60Ω, C_L = 100pF, C_{LR} = 15pF, Figure 2				215	ns
TXD Propagation Delay	t_{PDTXD_RD}, t_{PDTXD_DR}	R_{CM} is open, R_L = 60Ω, C_L = 100pF, Figure 1	Recessive to dominant			80	ns
			Dominant to recessive			80	
RXD Propagation Delay	t_{PDRXD_RD}, t_{PDRXD_DR}	C_{LR} = 15pF, Figure 3	Recessive to dominant			135	ns
			Dominant to recessive			135	
TXD Dominant Timeout	t_{DOM}	(Note 7)		1.4		4.8	ms
Undervoltage Threshold Detection Time to Normal Operation						120	µs
INSULATION CHARACTERISTICS							
Partial Discharge Voltage	V_{PR}	Method B1 = V_{IORM} x 1.875 (t = 1s, partial discharge < 5pC)			2250		V_P
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	(Note 8)			1200		V_P
Maximum Working Isolation Voltage	V_{IOWM}	(Note 8)			848		V_{RMS}
Maximum Transient Isolation Voltage	V_{IOTM}	t = 1s			8400		V_P

Electrical Characteristics (continued)

(V_{DDA} = 3.0V to 5.5V, V_{DDB} = 4.5V to 5.5V, POL =GNDA, I.C. = GNDB, T_A = -40°C to +125°C. Typical values are at V_{DDA} = 3.3V, V_{DDB} = 5V, GNDA = GNDB, and T_A = +25°C, unless otherwise noted. (Notes 1, 2))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Withstand Isolation Voltage	V_{ISO}	t = 60s, f = 60Hz (Notes 8, 9)		5000		V_{RMS}
Maximum Surge Isolation Voltage	V_{IOSM}	Basic Insulation		10		kV
Insulation Resistance	R_S	T_A = +150°C, V_{IO} = 500V		>10^9		Ω
Barrier Capacitance Input-to-Output	CIO	f = 1MHz		2		pF
Minimum Creepage Distance	CPG	Wide SOIC		8		mm
Minimum Clearance Distance	CLR	Wide SOIC		8		mm
Internal Clearance		Distance through insulation		0.015		mm
Comparative Tracking Resistance Index	CTI	Material Group II (IEC 60112)		575		
Climatic Category				40/125/21		
Pollution Degree (DIN VDE 0110, Table 1)				2		

Note 1: All devices 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design. Specifications marked "GBD" are guaranteed by design and not production tested.

Note 2: All currents into the device are positive. All currents out of the device are negative. All voltages referenced to their respective ground (GNDA or GNDB), unless otherwise noted.

Note 3: The maximum V_{LDO} voltage listed in the *Electrical Characteristics* table indicates the voltage capability of the MAX14882. Ambient temperature and power dissipation requirements of a given circuit may limit the allowable maximum V_{LDO} to a lower value during operation.

Note 4: Not production tested. Guaranteed by design (GBD) and characterization.

Note 5: Capacitance range for a stable output. Values are nominal and allow for normal capacitor tolerance.

Note 6: CMTI is the maximum sustainable common-mode voltage slew rate while maintaining the correct output states. CMTI applies to both rising and falling common-mode voltage edges. Tested with the transient generator connected between GNDA and GNDB.

Note 7: The dominant timeout feature releases the bus when TXD is held low longer than t_{DOM}. CAN protocol guarantees a maximum of 11 successive dominant bits in any transmission. The minimum data rate allowed by the dominant timeout, then, is 11/t_{DOM}(min)

Note 8: V_{IORM}, V_{IOWM}, and V_{ISO} are defined by the IEC 60747-5-5 standard

Note 9: Product is qualified V_{ISO} for 60 seconds. 100% production tested at 120% of V_{ISO} for 1 second.

Test Circuits and Timing Diagrams

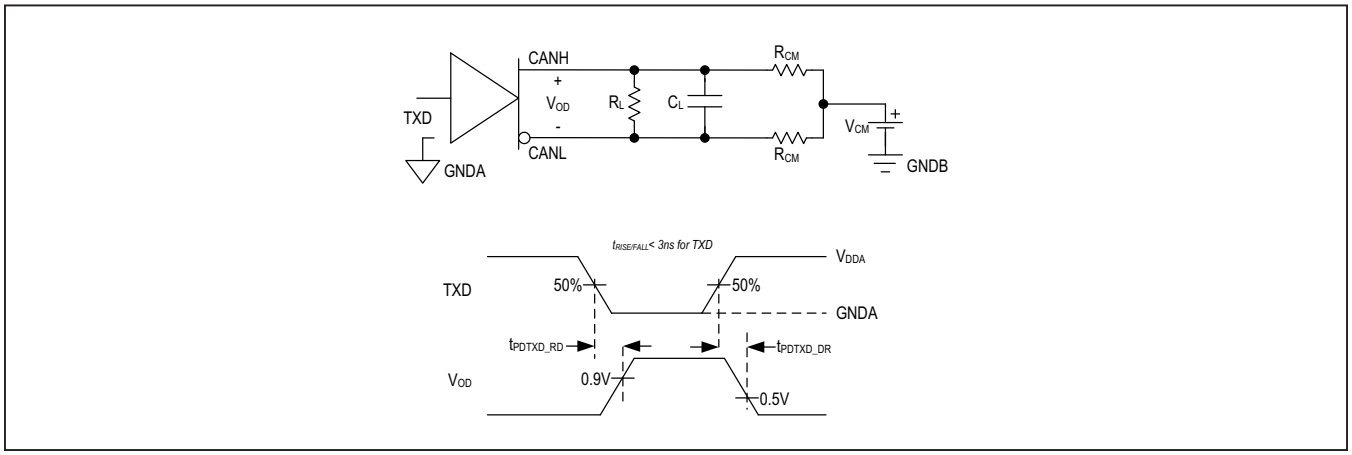


Figure 1. Transmitter Test Circuit and Timing Diagram

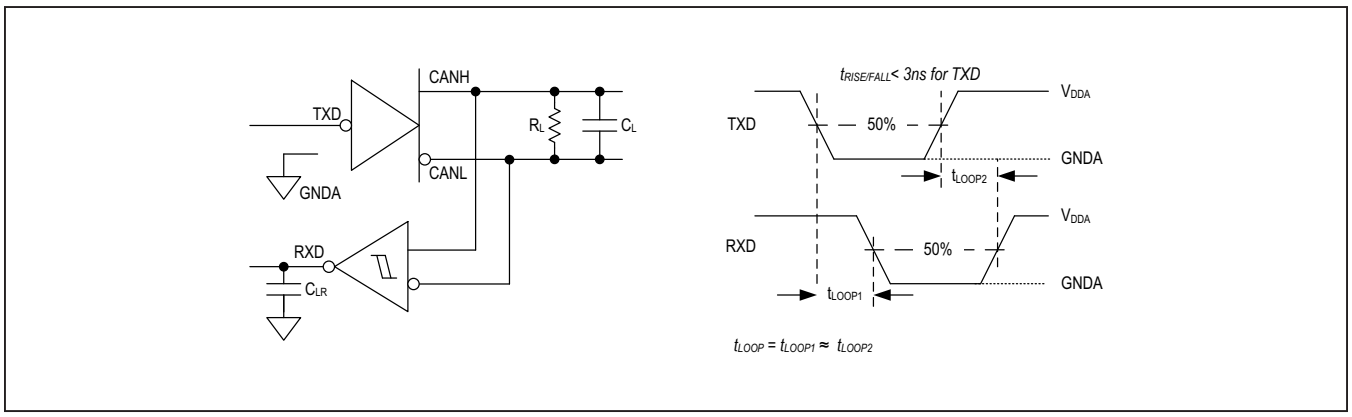


Figure 2. Loop Delay Timing Diagram

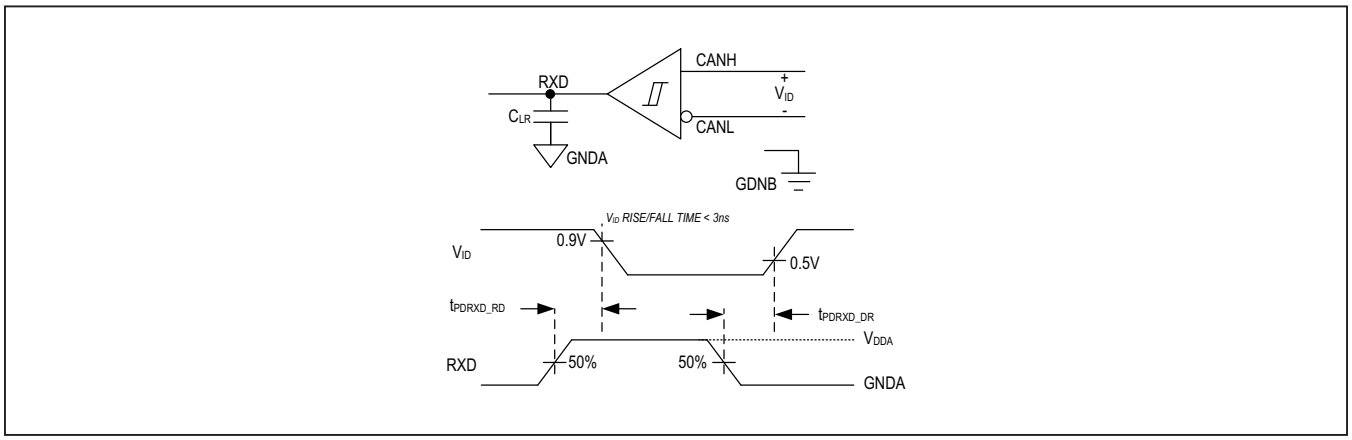
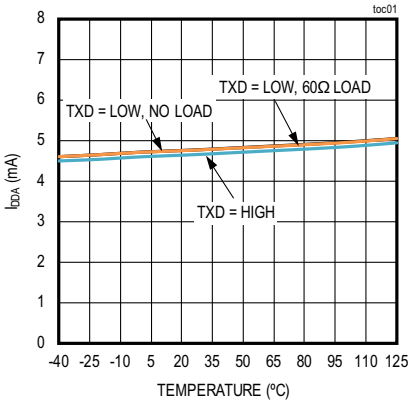


Figure 3. Receiver Timing Diagram

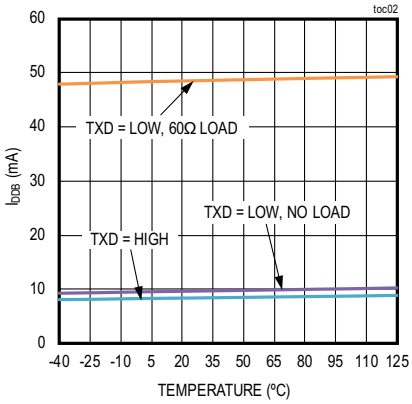
Typical Operating Characteristics

V_{DDA} = 3.3V to GNDA, 60Ω load between CANH and CANL, GNDA = GNDB, T_A = 25ºC, unless otherwise noted.

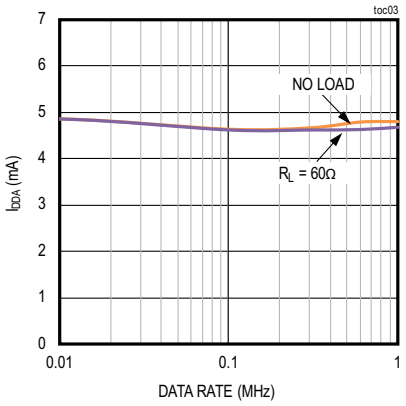
V_{DDA} SUPPLY CURRENT vs. TEMPERATURE



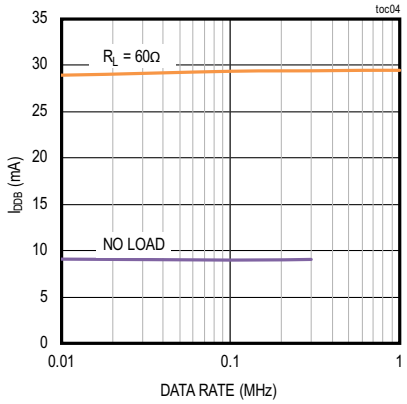
V_{DDB} SUPPLY CURRENT vs. TEMPERATURE



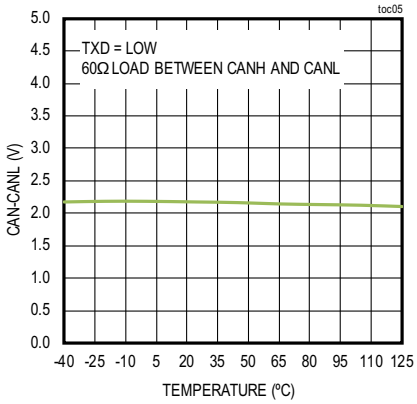
V_{DDA} SUPPLY CURRENT vs. DATA RATE



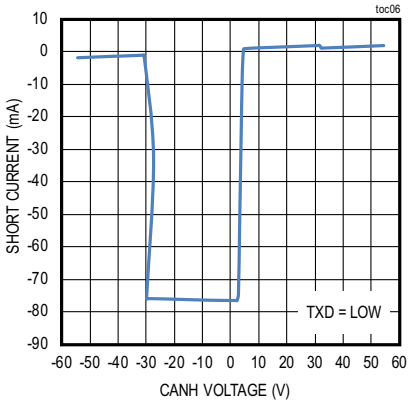
V_{DDB} SUPPLY CURRENT vs. DATA RATE



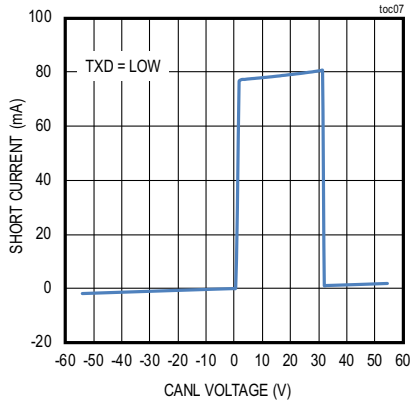
(CANH-CANL) OUTPUT VOLTAGE vs. TEMPERATURE



CANH SHORT-CIRCUIT CURRENT vs. VOLTAGE



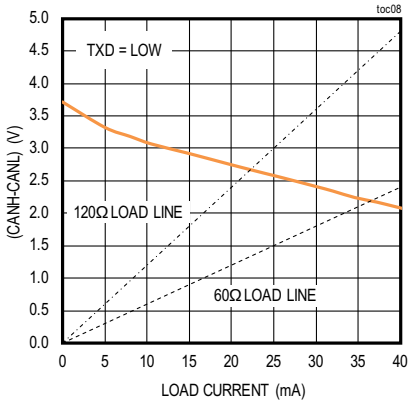
CANL SHORT CIRCUIT CURRENT vs. VOLTAGE



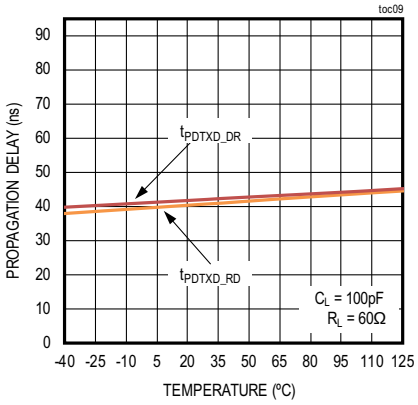
Typical Operating Characteristics (continued)

V_{DDA} = 3.3V to GNDA, 60Ω load between CANH and CANL, GNDA = GNDB, T_A = 25ºC, unless otherwise noted.

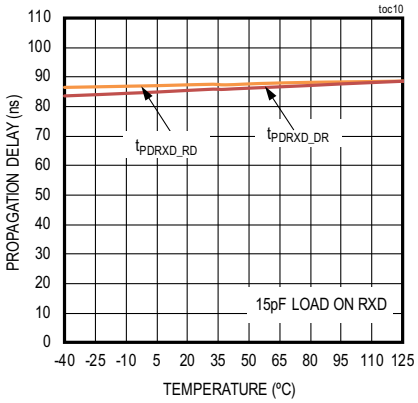
(CANH-CANL) VOLTAGE vs. LOAD RESISTANCE



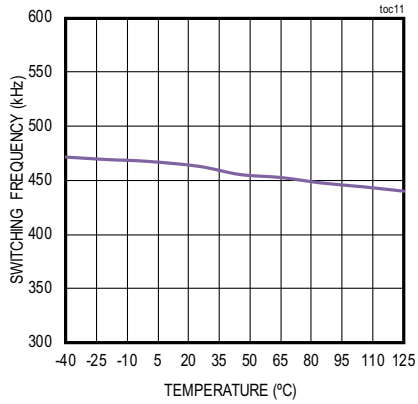
TXD PROPAGATION DELAY vs. TEMPERATURE



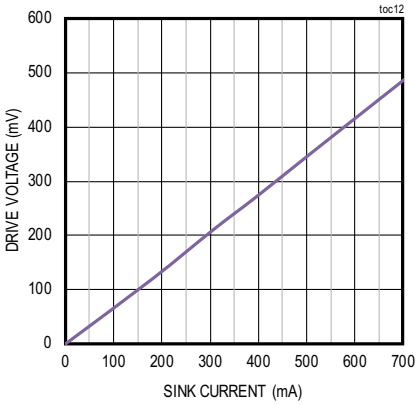
RXD PROPAGATION DELAY vs. TEMPERATURE



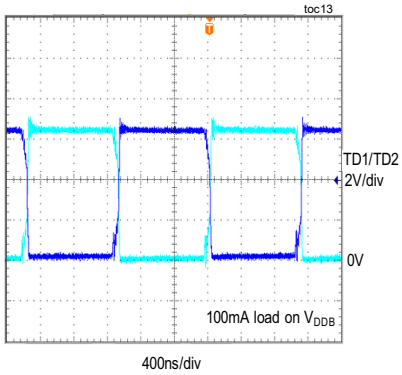
TRANSFORMER SWITCHING FREQUENCY vs.TEMPERATURE



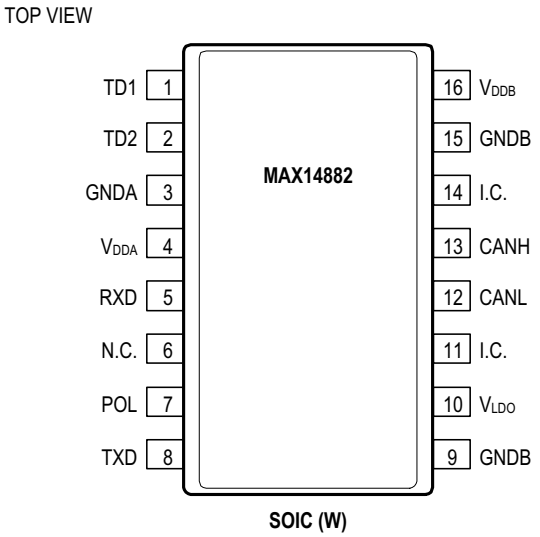
TD1/TD2 VOLTAGE vs. LOAD CURRENT



TRANSFORMER DRIVER



Pin Configuration



Pin Description

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
CONTROLLER-SIDE (A-SIDE)				
1	TD1	Transformer Driver Output 1	GNDA	Analog
2	TD2	Transformer Driver Output 2	GNDA	Analog
3	GNDA	Controller-Side/A-Side Ground. GNDA is the ground reference for POL, TXD, and RXD.	—	Ground
4	V_{DDA}	Power Supply Input for the Controller-Side/A-Side. Bypass V_{DDA} to GNDA with both a 0.1µF and a 1µF capacitor as close to the device as possible.	GNDA	Power
5	RXD	Receiver Output. RXD is high when the bus is in the recessive state. RXD is low when the bus is in the dominant state.	GNDA	Digital Output
6	N.C.	No Connection. Not internally connected. Connect to GNDA, V_{DDA}, or leave unconnected.	GNDA	
7	POL	Polarity Set Input. Drive POL low for normal CANH, CANL operation (CANH is high and CANL is low when TXD is low). Drive POL high to swap the functions of CANH and CANL (CANH is low and CANL is high when TXD is low). See Table 1for more information.	GNDA	Digital Input
8	TXD	Transmit Data Input. CANH and CANL are in the dominant state when TXD is low. CANH and CANL are in the recessive state when TXD is high.	GNDA	Digital Input

Pin Description (continued)

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
CAN BUS-SIDE (B-SIDE)				
9, 15	GNDB	Bus-Side/B-Side Ground. GNDB is the ground reference for V_{LDO}, V_{DDB}, CANH, and CANL.	—	Ground
10	V_{LDO}	LDO Power Input. Connect a minimum voltage of 4.68V to V_{LDO} to power the bus-side of the transceiver. Bypass V_{LDO} to GNDB with both 0.1µF and 1µF capacitors as close as possible to the device. To disable the internal LDO, leave V_{LDO} unconnected or connect to GNDB.	GNDB	Power Input
11, 14	I.C.	Internally Connected. Connect to GNDB.	GNDB	
12	CANL	Low-Level CAN Differential Bus Line	GNDB	Differential I/O
13	CANH	High-Level CAN Differential Bus Line	GNDB	Differential I/O
16	V_{DDB}	Bus-Side Power Input/LDO Power Output. Bypass V_{DDB} to GNDB with both 0.1µF and 1µF capacitors as close as possible to the device. V_{DDB} is the output of the internal LDO when power is applied to V_{LDO}. When the internal LDO is not used (V_{LDO} is unconnected or connected to GNDB), V_{DDB} is the positive supply input for the bus-side of the IC.	GNDB	Power

Detailed Description

The MAX14882 isolated controller area network (CAN) transceiver provides 5000V$_{RMS}$ (60s) of galvanic isolation between the cable-side (B-side) of the transceiver and the controller-side (A-side). This device allows up to 1Mbps communication across the isolation barrier when a large potential exists between grounds on each side of the barrier. CANH and CANL outputs are short-circuit current-limited and are protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs in a high-impedance state.

Isolation

Both data and power can be transmitted across the isolation barrier. Data isolation is achieved using integrated capacitive isolation that allows data transmission between the controller-side and the cable-side of the transceiver.

To achieve power isolation, the MAX14882 features an integrated transformer driver to drive an external center-tapped transformer, allowing the transfer of operating power from the controller-side, across the isolation barrier, to the cable-side. Connect the primary side of the external transformer to the MAX14882's transformer driver outputs (TD1 and TD2).

Fault Protection

The MAX14882 features ±54V fault protection on the CANH and CANL bus lines. When CANH or CANL is pulled above +30V (typ) or below -30V (typ), the I/O is set to high-impedance. This wide fault protection range simplifies selecting external TVS components for surge protection.

Transmitter

The transmitter converts a single-ended input signal (TXD) from the CAN controller to differential outputs for the bus lines (CANH, CANL). The truth table for the transmitter and receiver is given in Table 1.

Transmitter Dominant Timeout

The MAX14882 features a transmitter-dominant timeout (t_{DOM}) that prevents erroneous CAN controllers from clamping the bus to a dominant level by maintaining a continuous low TXD signal. When TXD remains in the dominant state (low) for greater than t_{DOM}, the transmitter is disabled, releasing the bus to a recessive state (Table 1).

After a dominant timeout fault, normal transmitter function is re-enabled on the rising edge of a TXD. The transmitter-dominant timeout limits the minimum possible data rate to 7.86kbps for standard CAN protocol.

Transmitter and Receiver Functionality When Not Connected to the Bus

Table 1. Transmitter and Receiver Functionality when Not Connected to the Bus

POL	TXD	TXD LOW TIME	CANH	CANL	BUS STATE	RXD
L	L	< t_{DOM}	H	L	Dominant	L
L	L	≥ t_{DOM}	$V_{DDB}/2$	$V_{DDB}/2$	Recessive	H
L	H	X	$V_{DDB}/2$	$V_{DDB}/2$	Recessive	H
H	L	< t_{DOM}	L	H	Dominant	L
H	L	≥ t_{DOM}	$V_{DDB}/2$	$V_{DDB}/2$	Recessive	H
H	H	X	$V_{DDB}/2$	$V_{DDB}/2$	Recessive	H
X = Don't care						

Driver Output Protection

The MAX14882 features integrated circuitry to protect the transmitter output stage against a short-circuit to a positive or negative voltage by limiting the driver current. The transmitter returns to normal operation once the short is removed.

Thermal shutdown further protects the transceiver from excessive temperatures that may result from a short by setting the transmitter outputs to high impedance when the junction temperature exceeds +160°C (typ). The transmitter returns to normal operation when the junction temperature falls below the thermal shutdown hysteresis.

Receiver

The receiver reads the differential input from the bus (CANH, CANL) and transfers this data as a single-ended output (RXD) to the CAN controller. During normal operation, a comparator senses the difference between CANH and CANL, $V_{DIFF} = |V_{CANH} - V_{CANL}|$, with respect to an internal threshold of 0.7V (typ). If V_{DIFF} > 0.9V, a logic-low is present on RXD. If V_{DIFF} < 0.5V, a logic-high is present.

The CANH and CANL common-mode range is ±25V. RXD is logic-high when CANH and CANL are shorted or terminated and undriven.

Transformer Driver

Overcurrent Limiting

The MAX14882 features overcurrent limiting to protect the integrated transformer driver from excessive currents when charging large capacitive loads or driving into short-circuits. Current limiting is achieved in two stages: internal circuitry monitors the output current and detects when the peak current rises above 1.2A.

When the 1.2A threshold is exceeded, internal circuitry reduces the output current to the 730mA current-limit. The MAX14882 monitor the driver current on a cycle-by-cycle basis and limit the current until the short is removed.

The transformer driver on the MAX14882 can dissipate large amounts of power during overcurrent limiting,causing the IC to enter thermal shutdown. When the junction temperature exceeds the thermal shutdown threshold, the TD1 and TD2 driver outputs are disabled. The driver resumes normal operation when the temperature falls below the thermal shutdown temperature minus the hysteresis.

Transformer Selection

The integrated push-pull transformer driver allows the transmission of operating power from the logic side, across the isolation barrier, to the isolated field side of the device. The 450kHz (typ) transformer driver operates with center-tapped primary transformers. Select a transformer with an ET product greater than or equal to the ET of the driver to ensure that the transformer does not enter saturation. E is the voltage applied to the transformer and T is the maximum time it is applied during any one cycle. Calculate the minimum ET product for the transformer primary as:

$$ET = V_{MAX}/(2 \times f_{MIN})$$

where V_{MAX} is the worst-case maximum supply voltage on V_{DDA} and f_{MIN} is the minimum frequency at that supply voltage. For example, using 5.5V and 350kHz, the required minimum ET product is 7.9Vµs.

Table 2 shows a list of recommended transformers to use with the MAX14882.

Applications Information

Reduced EMI and Reflections

In multidrop CAN applications, it is important to maintain a single linear bus, of uniform impedance, that is properly terminated at each end. Do not use a star configuration.

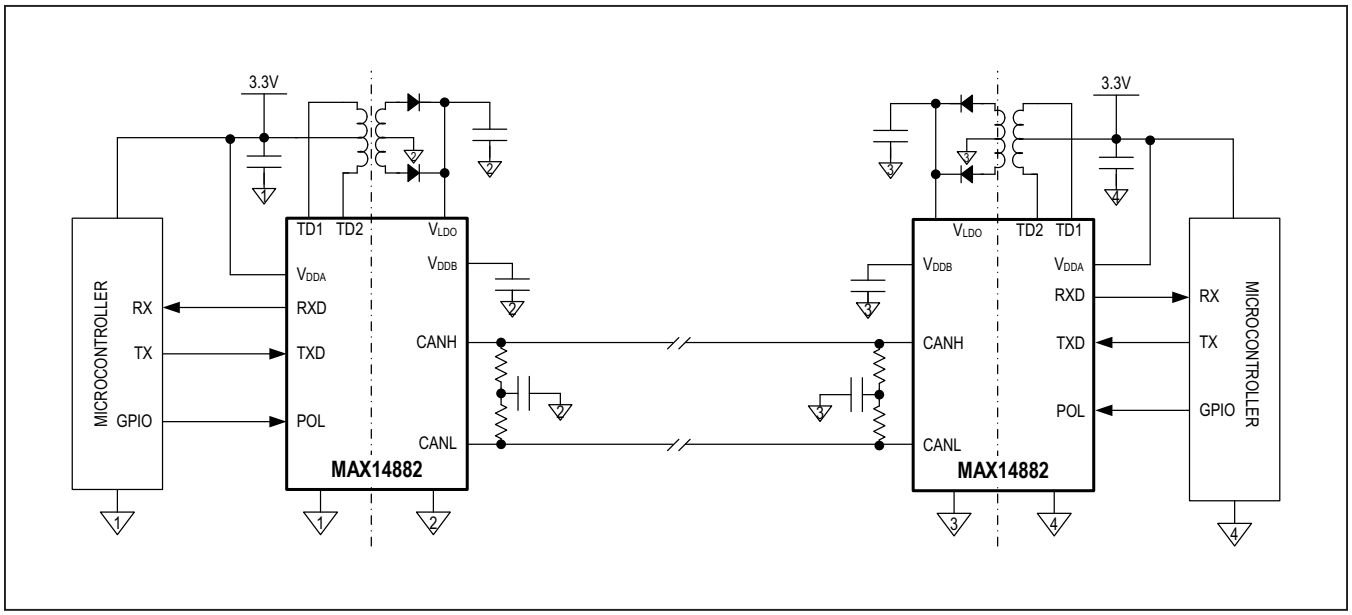
Any deviation from the end-to-end wiring scheme creates a stub. High-speed data edges on a stub can create reflections back down the bus and can cause data errors, by eroding the noise margin of the system. Although stubs are unavoidable in a multidrop system, care should be taken to keep these stubs as short as possible, especially when operating with high data rates.

Recommended Transformers

Table 2. Recommended Transformers

MANUFACTURER	PART NUMBER	APPLICATION	TURNS RATIO	ISOLATION (V_{RMS})	OPERATING TEMP	ET CONSTANT (V x µs, MIN)	OPERATING CURRENT (mA)	DIMENSIONS (L x W x H) (mm)
Wurth	750315225	5V to 5V	1CT:1.1CT	2750	-40°C to +125°C	9.44	200	6.73 x 7.14 x 4.19
Wurth	750315226	5V to 5V	1CT:1.3CT	2750		9.44	200	6.73 x 7.14 x 4.19
Wurth	750315227	3.3V to 5V	1CT:1.7CT	2750		9.44	200	6.73 x 7.14 x 4.19
Wurth	750315228	3.3V to 5V	1CT:2CT	2750		9.44	160	6.73 x 7.14 x 4.19
Wurth	750315229	5V to 5V	1CT:1.13CT	5000	-40°C to +125°C	10.7	200	9.14 x 8.00 x 7.62
Wurth	750315230	5V to 5V	1CT:1.38CT	5000		10.7	150	9.14 x 8.00 x 7.62

Typical Application Circuit



Ordering Information

PART	ISOLATION RATING	V_{DDA} SUPPLY	POL	V_{DDB} LDO VOLTAGE	TRANSFORMER DRIVER	PACKAGE
MAX14882AWE+	5kV$_{RMS}$	3.0V to 5.5V	YES	5V	YES	16 SOIC (W)
MAX14882AWE+T	5kV$_{RMS}$	3.0V to 5.5V	YES	5V	YES	16 SOIC (W)

+Denotes a lead (Pb)-free/RoHS-compliant package
T = Tape and Reel

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/18	Initial release	—
1	7/19	Updated the *Electrical Characteristics* table	5–6

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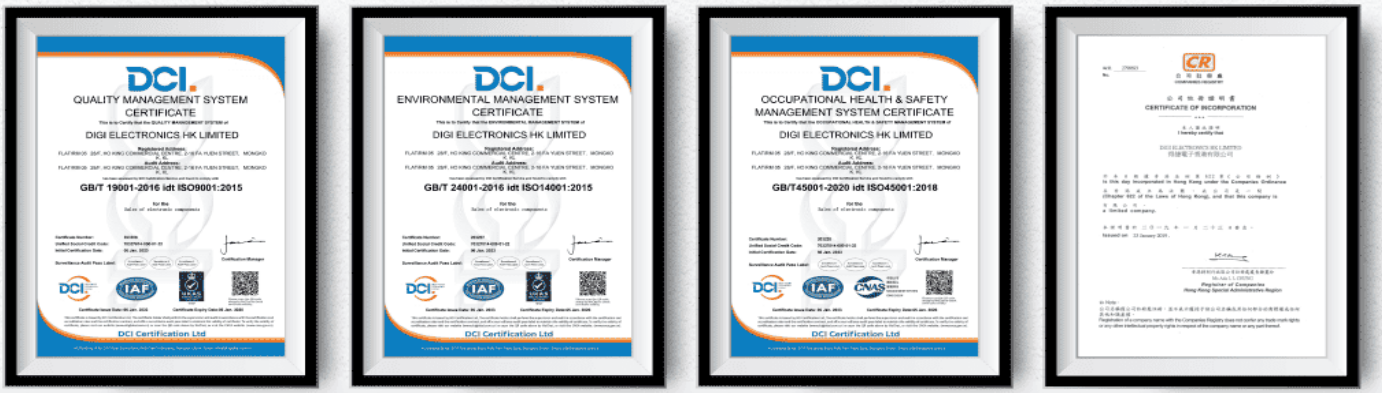

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