# MAX5541ESA+T Datasheet

www.digi-electronics.com

https://www.DiGi-Electronics.com

| | |
|---|---|
| DiGi Electronics Part Number | MAX5541ESA+T-DG |
| Manufacturer | Analog Devices Inc./Maxim Integrated |
| Manufacturer Product Number | MAX5541ESA+T |
| Description | IC DAC 16BIT V-OUT 8SOIC |
| Detailed Description | 16 Bit Digital to Analog Converter 1 8-SOIC |

# Purchase and inquiry

| | |
|---|---|
| Manufacturer Product Number: | Manufacturer: |
| MAX5541ESA+T | Analog Devices Inc./Maxim Integrated |
| Series: | Product Status: |
| - | Active |
| DiGi-Electronics Programmable: | Number of Bits: |
| Not Verified | 16 |
| Number of D/A Converters: | Settling Time: |
| 1 | 1µs (Typ) |
| Output Type: | Differential Output: |
| Voltage - Unbuffered | No |
| Data Interface: | Reference Type: |
| SPI | External |
| Voltage - Supply, Analog: | Voltage - Supply, Digital: |
| 5V | 5V |
| INL/DNL (LSB): | Architecture: |
| ±4, ±0.5 | R-2R |
| Operating Temperature: | Package / Case: |
| -40°C ~ 85°C | 8-SOIC (0.154", 3.90mm Width) |
| Supplier Device Package: | Mounting Type: |
| 8-SOIC | Surface Mount |
| Base Product Number: | |
| MAX5541 | |

# Environmental & Export classification

| | |
|---|---|
| RoHS Status: | Moisture Sensitivity Level (MSL): |
| ROHS3 Compliant | 1  (Unlimited) |
| REACH Status: | ECCN: |
| REACH Unaffected | EAR99 |
| HTSUS: | |
| 8542.39.0001 | |

*MAXIM*

# Low-Cost, +5V, Serial-Input, Voltage-Output, 16-Bit DAC
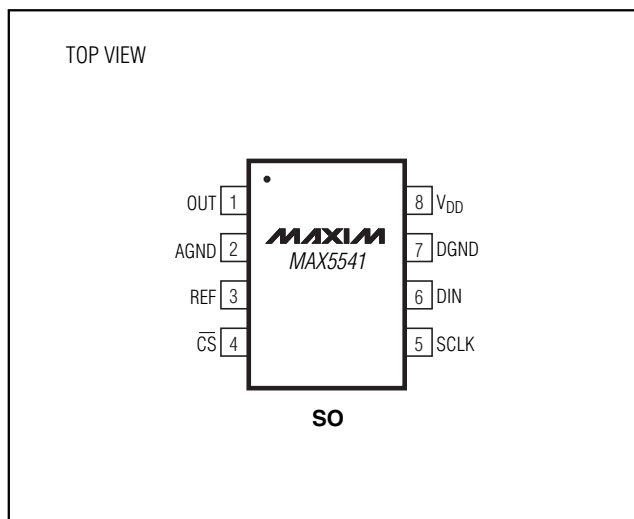
**MAX5541**

## General Description

The MAX5541 serial-input, voltage-output, 16-bit monotonic digital-to-analog converter (DAC) operates from a single +5V supply. The DAC output is unbuffered, resulting in a low 0.3mA supply current and low 1LSB offset error. The DAC output range is 0V to $V_{REF}$. The DAC latch accepts a 16-bit serial word. A power-on reset (POR) circuit clears the DAC output to 0V (unipolar mode) when power is initially applied.

The 10MHz 3-wire serial interface is SPI™/QSPI™/MICROWIRE™-compatible and interfaces directly with optocouplers for applications requiring isolation. The MAX5541 is available in an 8-pin SO package. For the 1LSB (max) INL version, refer to the MAX541 data sheet.

## Features

♦ **Full 16-Bit Performance Without Adjustments**

♦ **+5V Single-Supply Operation**

♦ **Low Power: 1.5mW**

♦ **1µs Settling Time**

♦ **Unbuffered Voltage Output Directly Drives 60kΩ Loads**

♦ **SPI/QSPI/MICROWIRE-Compatible Serial Interface**

♦ **Power-On Reset Circuit Clears DAC Output to 0V (unipolar mode)**

♦ **Schmitt Trigger Inputs for Direct Optocoupler Interface**

♦ **Choose MAX541 as a 1LSB (max) INL Upgrade to the MAX5541**

## Applications

High-Resolution Offset and Gain Adjustment

Industrial Process Control

Automated Test Equipment

Data Acquisition Systems

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|------|------------|-------------|
| MAX5541CSA | 0°C to +70°C | 8 SO |
| MAX5541ESA | -40°C to +85°C | 8 SO |

## Pin Configuration



## Functional Diagram



*SPI and QSPI are trademarks of Motorola, Inc.*
*MICROWIRE is a trademark of National Semiconductor Corp.*

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# Low-Cost, +5V, Serial-Input, Voltage-Output, 16-Bit DAC

**MAX5541**
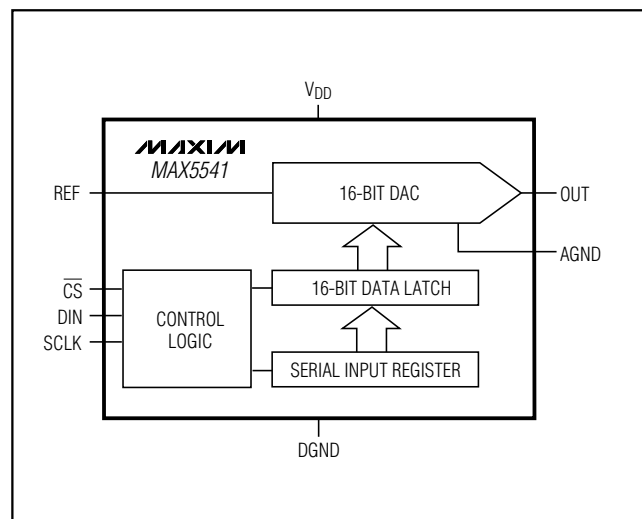
## ABSOLUTE MAXIMUM RATINGS

$V_{DD}$ to DGND............................................-0.3V to +6V
$\overline{CS}$, SCLK, DIN to DGND.......................................-0.3V to +6V
REF to AGND, DGND .................................-0.3V to ($V_{DD}$ +0.3V)
AGND to DGND.....................................-0.3V to +0.3V
OUT to AGND, DGND.................................... .............-0.3V to $V_{DD}$
Maximum Current into Any Pin...........................................50mA
Continuous Power Dissipation ($T_A$ = +70°C)
    8-Pin SO (derate 5.88mW/°C above +70°C)................471mW

Operating Temperature Ranges
    MAX5541CSA ......................................................0°C to +70°C
    MAX5541ESA ...................................................-40°C to +85°C
Junction Temperature...................................................+150°C
Storage Temperature Range ...........................-65°C to +150°C
Lead Temperature (soldering, 10s) ................................ +300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{DD}$ = +5V ±5%, $V_{REF}$ = +2.5V, $V_{AGND}$ = $V_{DGND}$ = 0, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **STATIC PERFORMANCE—ANALOG SECTION** ($R_L = \infty$) | | | | | | |
| Resolution | N | | | 16 | | Bits |
| Differential Nonlinearity | DNL | Guaranteed monotonic | | ±0.5 | ±1.0 | Bits |
| Integral Nonlinearity | INL | $V_{DD}$ = 5V (Note 1) | | ±4 | ±16 | LSB |
| Zero-Code Offset Error | ZSE | $T_A$ = +25°C | | | ±1 | LSB |
| | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | ±2 | |
| Zero-Code Tempco | $ZS_{TC}$ | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | ±0.05 | | ppm/°C |
| Gain Error (Note 2) | | $T_A$ = +25°C | | | ±5 | LSB |
| | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | ±10 | |
| Gain-Error Tempco | | | | ±0.1 | | ppm/°C |
| DAC Output Resistance | $R_{OUT}$ | (Note 3) | | 6.25 | | kΩ |
| Power-Supply Rejection | PSR | 4.75V ≤ $V_{DD}$ ≤ 5.25V | | | ±1.0 | LSB |
| **REFERENCE INPUT** | | | | | | |
| Reference Input Range | $V_{REF}$ | (Note 4) | 2.0 | | 3.0 | V |
| Reference Input Resistance | $R_{REF}$ | (Note 5) | 11.5 | | | kΩ |
| **DYNAMIC PERFORMANCE—ANALOG SECTION** ($R_L = \infty$) | | | | | | |
| Voltage Output Slew-Rate | SR | $C_L$ = 10pF (Note 6) | | 25 | | V/µs |
| Output Settling Time | | To ±$\frac{1}{2}$LSB of FS, $C_L$ = 10pF | | 1 | | µs |
| DAC Glitch Impulse | | Major-carry transition | | 10 | | nVs |
| Digital Feedthrough | | Code = 0000 hex, $\overline{CS}$ = $V_{DD}$, SCLK = $V_{DIN}$ = 0 to $V_{DD}$ levels | | 10 | | nVs |
| **DYNAMIC PERFORMANCE—REFERENCE SECTION** | | | | | | |
| Reference -3dB Bandwidth | BW | Code = FFFF hex | | 1 | | MHz |
| Reference Feedthrough | | Code = 0000 hex, $V_{REF}$ = 1$V_{P-P}$ at 100kHz | | 1 | | $mV_{P-P}$ |
| Signal-to-Noise Ratio | SNR | | | 92 | | dB |
| Reference Input Capacitance | $C_{IN}$ | Code = 0000 hex | | 75 | | pF |
| | | Code = FFFF hex | | 120 | | |

**MAXIM**

# Low-Cost, +5V, Serial-Input, Voltage-Output, 16-Bit DAC

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = +5V ±5%, $V_{REF}$ = +2.5V, $V_{AGND}$ = $V_{DGND}$ = 0, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **STATIC PERFORMANCE—DIGITAL INPUTS** | | | | | | |
| Input High Voltage | $V_{IH}$ | | 2.4 | | | V |
| Input Low Voltage | $V_{IL}$ | | | | 0.8 | V |
| Input Current | $I_{IN}$ | $V_{IN}$ = 0 | | | ±1 | µA |
| Input Capacitance | $C_{IN}$ | (Note 7) | | | 10 | pF |
| Hysteresis Voltage | $V_H$ | | | 0.40 | | V |
| **POWER SUPPLY** | | | | | | |
| Positive Supply Range | $V_{DD}$ | | 4.75 | | 5.25 | V |
| Positive Supply Current | $I_{DD}$ | | | 0.3 | 1.1 | mA |
| Power Dissipation | PD | | | 1.5 | | mW |

## TIMING CHARACTERISTICS

($V_{DD}$ = +5V ±5%, $V_{REF}$ = +2.5V, $V_{AGND}$ = $V_{DGND}$ = 0, CMOS inputs, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| SCLK Frequency | $f_{CLK}$ | | | | 10 | MHz |
| SCLK Pulse Width High | $t_{CH}$ | | 45 | | | ns |
| SCLK Pulse Width Low | $t_{CL}$ | | 45 | | | ns |
| $\overline{CS}$ Low to SCLK High Setup | $t_{CSS0}$ | | 45 | | | ns |
| $\overline{CS}$ High to SCLK High Setup | $t_{CSS1}$ | | 45 | | | ns |
| SCLK High to $\overline{CS}$ Low Hold | $t_{CSH0}$ | (Note 7) | 30 | | | ns |
| SCLK High to $\overline{CS}$ High Hold | $t_{CSH1}$ | | 45 | | | ns |
| DIN to SCLK High Setup | $t_{DS}$ | | 40 | | | ns |
| DIN to SCLK High Hold | $t_{DH}$ | | 0 | | | ns |
| $V_{DD}$ High to $\overline{CS}$ Low (power-up delay) | | | | 20 | | µs |

**Note 1:** Refer to the MAX541 for the 1LSB (max) INL version.
**Note 2:** Gain error tested at $V_{REF}$ = +2.0V, +2.5V, and +3.0V.
**Note 3:** $R_{OUT}$ tolerance is typically ±20%.
**Note 4:** Min/max ranges guaranteed by gain-error test. Operation outside min/max limits will result in degraded performance.
**Note 5:** Reference input resistance is code dependent, minimum at 8555 hex.
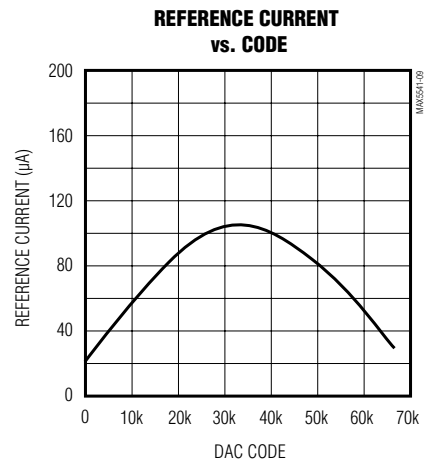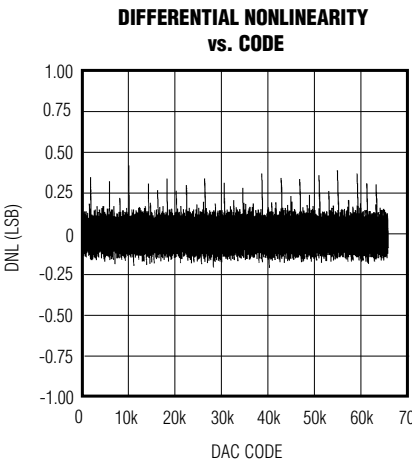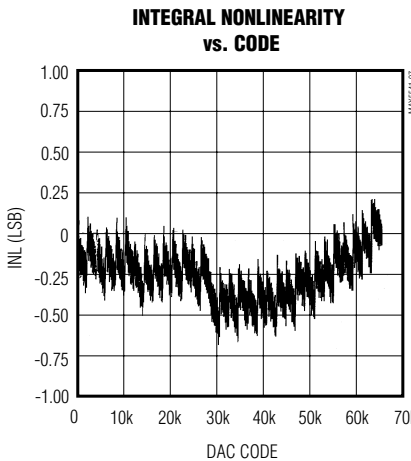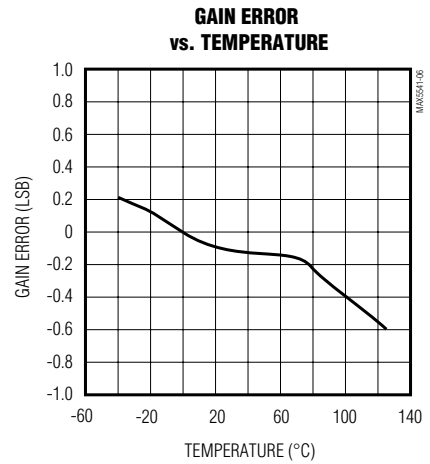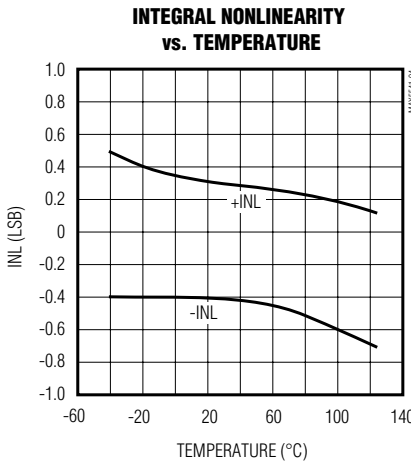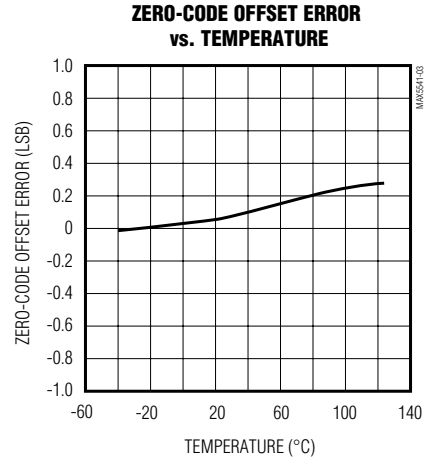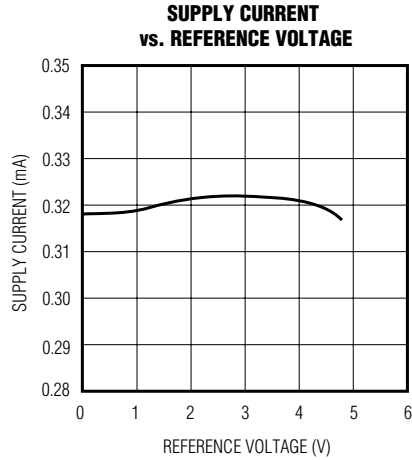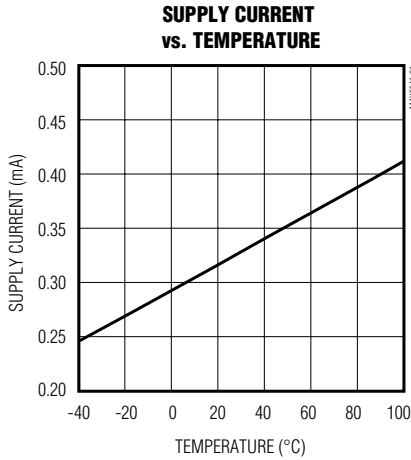**Note 6:** Slew-rate value is measured from 0% to 63%.
**Note 7:** Guaranteed by design. Not production tested.

# Low-Cost, +5V, Serial-Input, Voltage-Output, 16-Bit DAC

**MAX5541**

_____**Typical Operating Characteristics**

(V_DD = +5V, V_REF = +2.5V, T_A = +25°C, unless otherwise noted.)
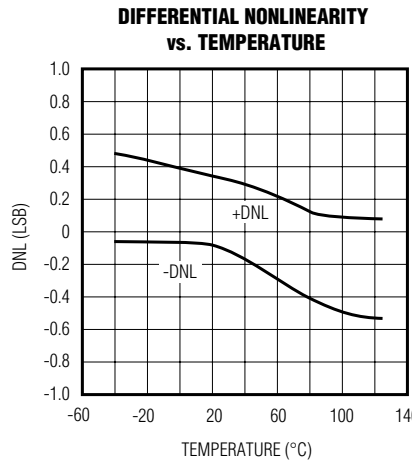
**SUPPLY CURRENT vs. TEMPERATURE**

**SUPPLY CURRENT vs. REFERENCE VOLTAGE**

**ZERO-CODE OFFSET ERROR vs. TEMPERATURE**

**INTEGRAL NONLINEARITY vs. TEMPERATURE**

**DIFFERENTIAL NONLINEARITY vs. TEMPERATURE**

**GAIN ERROR vs. TEMPERATURE**

**INTEGRAL NONLINEARITY vs. CODE**

**DIFFERENTIAL NONLINEARITY vs. CODE**

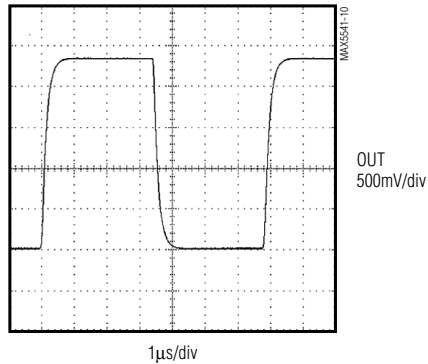**REFERENCE CURRENT vs. CODE**

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**MAXIM**

# Low-Cost, +5V, Serial-Input, Voltage-Output, 16-Bit DAC
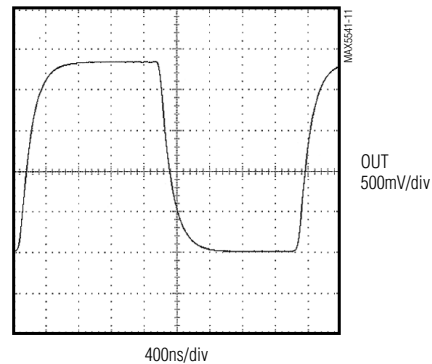
**MAX5541**

## _____Typical Operating Characteristics (continued)

($V_{DD}$ = +5V, $V_{REF}$ = +2.5V, $T_A$ = +25°C, unless otherwise noted.)
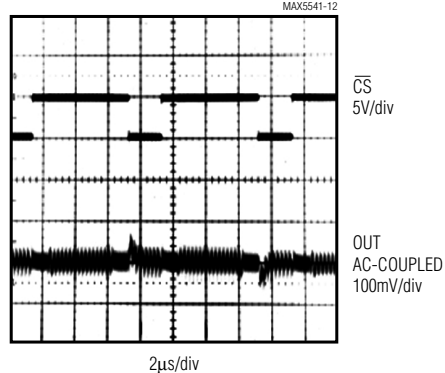
**FULL-SCALE STEP RESPONSE**
**($f_{SCLK}$ = 10MHz)**

OUT
500mV/div

1µs/div

$C_L$ = 13pF, $R_L$ = ∞

**FULL-SCALE STEP RESPONSE**
**($f_{SCLK}$ = 20MHz)**

OUT
500mV/div

400ns/div

$C_L$ = 13pF, $R_L$ = ∞

**MAJOR-CARRY OUTPUT GLITCH**

$\overline{CS}$
5V/div

OUT
AC-COUPLED
100mV/div

2µs/div

**DIGITAL FEEDTHROUGH**

SCLK
5V/div

OUT
AC-COUPLED
50mV/div

2µs/div
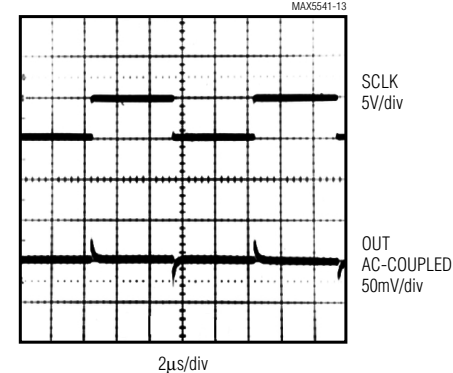
CODE = 0000 hex

## _____Pin Description

| PIN | NAME | FUNCTION |
|-----|------|----------|
| 1 | OUT | DAC Output Voltage |
| 2 | AGND | Analog Ground |
| 3 | REF | Voltage Reference Input. Connect to external +2.5V reference. |
| 4 | $\overline{CS}$ | Chip-Select Input |
| 5 | SCLK | Serial-Clock Input. Duty cycle must be between 40% and 60%. |
| 6 | DIN | Serial-Data Input |
| 7 | DGND | Digital Ground |
| 8 | $V_{DD}$ | +5V Supply Voltage |

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# Low-Cost, +5V, Serial-Input, Voltage-Output, 16-Bit DAC

*MAX5541*

## Detailed Description

The MAX5541 voltage-output, 16-bit digital-to-analog converter (DAC) offers 16-bit monotonicity with less than 1LSB differential linearity error. Serial-data transfer minimizes the number of package pins required.

The MAX5541 is composed of two matched DAC sections, with a 12-bit inverted R-2R DAC forming the twelve LSBs and the four MSBs derived from fifteen identically matched resistors. This architecture allows the lowest glitch energy to be transferred to the DAC output on major-carry transitions. It also decreases the DAC output impedance by a factor of eight compared to a standard R-2R ladder, allowing unbuffered operation in medium-load applications. Figure 1 is the *Timing Diagram*.

### Digital Interface

The MAX5541 digital interface is a standard 3-wire connection compatible with SPI/QSPI/MICROWIRE interfaces. The chip-select input ($\overline{CS}$) frames the serial data loading at the data input pin (DIN). Immediately following $\overline{CS}$s high-to-low transition, the data is shifted synchronously and latched into the input register on the rising edge of the serial-clock input (SCLK). After 16 data bits have been loaded into the serial input register, it transfers its contents to the DAC latch on $\overline{CS}$s low-to-high transition (Figure 2). Note that if $\overline{CS}$ does not remain low during the entire sixteen SCLK cycles, data will be corrupted. In this case, reload the DAC latch with a new 16-bit word.

### External Reference

The MAX5541 operates with external voltage references from 2V to 3V. The reference voltage determines the DACs full-scale output voltage.

### Power-On Reset

The MAX5541 has a power-on reset (POR) circuit to set the DACs output to 0V in unipolar mode when $V_{DD}$ is first applied. This ensures that unwanted DAC output voltages will not occur immediately following a system power-up, such as after power loss. In bipolar mode, the DAC output is set to -$V_{REF}$.
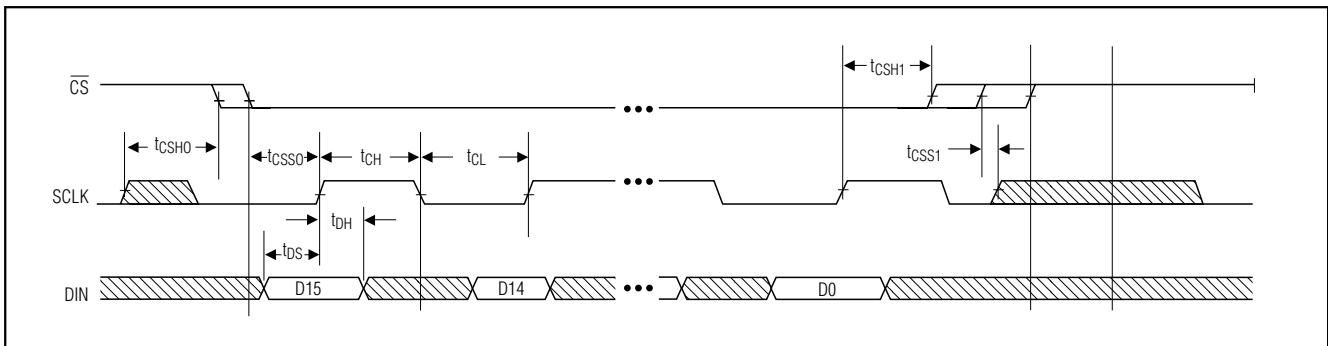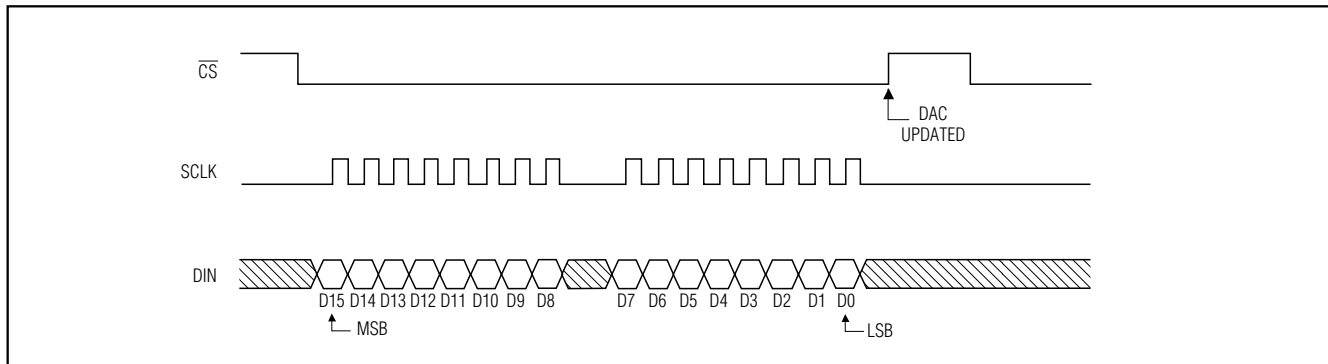


Figure 1.  Timing Diagram



Figure 2.  3-Wire Interface Timing Diagram

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# Low-Cost, +5V, Serial-Input, Voltage-Output, 16-Bit DAC

## Applications Information

### Reference and Analog Ground Inputs

The MAX5541 operates with external voltage references from 2V to 3V, and maintains 16-bit performance with proper reference selection and application. Ideally, the reference's temperature coefficient should be less than 0.4ppm/°C to maintain 16-bit accuracy to within 1LSB over the commercial (0°C to +70°C) temperature range. Since this converter is designed as an inverted R-2R voltage-mode DAC, the input resistance seen by the voltage reference is code dependent. The worst-case input-resistance variation is from 11.5k$\Omega$ (at code 8555 hex) to 200k$\Omega$ (at code 0000 hex). The maximum change in load current for a 2.5V reference is 2.5V/ 11.5k$\Omega$ = 217µA; therefore, the required load regulation is 7ppm/mA for a maximum error of 0.1LSB. This implies a reference output impedance of <18m$\Omega$. In addition, the impedance of the signal path from the voltage reference to the reference input must be kept low because it contributes directly to the load-regulation error.

The requirement for a low-impedance voltage reference is met with capacitor bypassing at the reference inputs and ground. A 0.1µF ceramic capacitor with short leads between REF and AGND provides high-frequency bypassing. A surface-mount ceramic chip capacitor is preferred because it has the lowest inductance. An additional 10µF between REF and AGND provides low-frequency bypassing. A low-ESR tantalum, film, or organic semiconductor capacitor works well. Leaded capacitors are acceptable because impedance is not as critical at lower frequencies. The circuit can benefit from even larger bypassing capacitors, depending on the stability of the external reference with capacitive loading. If separate force and sense lines are not used, connect the appropriate force and sense pins together close to the package.

AGND must also be low impedance, as load-regulation errors will be introduced by excessive AGND resistance. As in all high-resolution, high-accuracy applications, separate analog and digital ground planes yield the best results. Connect DGND to AGND at the AGND pin to form the "star" ground for the DAC system. For the best possible performance, always refer remote DAC loads to this system ground.

### Unbuffered Operation

Unbuffered operation reduces power consumption as well as offset error contributed by the external output buffer. The R-2R DAC output is available directly at OUT, allowing 16-bit performance from +$V_{REF}$ to AGND without degradation at zero-scale. The DAC's output impedance is also low enough to drive medium loads ($R_L$ > 60k$\Omega$) without degradation of INL or DNL, only the gain error is increased by externally loading the DAC output.

### External Output Buffer Amplifier

In unipolar mode, the output amplifier is used in a voltage-follower connection. The DAC's output resistance is constant and is independent of input code; however, the output amplifier's input impedance should still be as high as possible to minimize gain errors. The DAC's output capacitance is also independent of input code, thus simplifying stability requirements on the external amplifier.

In single-supply applications, precision amplifiers with input common-mode ranges including AGND are available; however, their output swings do not normally include the negative rail (AGND) without significant performance degradation. A single-supply op amp, such as the MAX495, is suitable if the application does not use codes near zero.

Since the LSBs for a 16-bit DAC are extremely small (38.15µV for $V_{REF}$ = 2.5V), pay close attention to the external amplifier's input specification. The input offset voltage can degrade the zero-scale error and might require an output offset trim to maintain full accuracy if the offset voltage is greater than 1/2LSB. Similarly, the input bias current multiplied by the DAC output resistance (typically 6.25k$\Omega$) contributes to the zero-scale error. Temperature effects also must be taken into consideration. Over the commercial temperature range, the offset voltage temperature coefficient (referenced to +25°C) must be less than 0.42µV/°C to add less than 1/2LSB of zero-scale error. The external amplifier's input resistance forms a resistive divider with the DAC output resistance, which results in a gain error. To contribute less than 1/2LSB of gain error, the input resistance typically must be greater than:

$$6.25\text{k}\Omega \; / \frac{1}{2}\left[\frac{1}{2^{14}}\right] = 205\text{M}\Omega$$

The settling time is affected by the buffer input capacitance, the DAC's output capacitance, and PC board capacitance. The typical DAC output voltage settling time is 1µs for a full-scale step. Settling time can be significantly less for smaller step changes. Assuming a single time-constant exponential settling response, a full-scale step takes twelve time constants to settle to within 1/2LSB of the final output voltage. The time constant is equal to the DAC output resistance multiplied by the total output capacitance. The DAC output capacitance is typically 10pF. Any additional output capacitance will increase the settling time.

# Low-Cost, +5V, Serial-Input, Voltage-Output, 16-Bit DAC

**MAX5541**

The external buffer amplifier's gain-bandwidth product is important because it increases the settling time by adding another time constant to the output response. The effective time constant of two cascaded systems, each with a single time-constant response, is approximately the root square sum of the two time constants. The DAC output's time constant is 1µs/12 = 83ns, ignoring the effect of additional capacitance. If the time constant of an external amplifier with 1MHz bandwidth is $1/2\pi$ (1MHz) = 159ns, then the effective time constant of the combined system is:

$$\sqrt{\left[\left(83ns\right)^2 + \left(159ns\right)^2\right]} = 180ns$$

This suggests that the settling time to within 1/2LSB of the final output voltage, including the external buffer amplifier, will be approximately $12 \times 180ns = 2.15\mu s$.

### Digital Inputs and Interface Logic

The digital interface for the 16-bit DAC is based on a 3-wire standard that is SPI/QSPI/MICROWIRE–compatible. The three digital inputs ($\overline{CS}$, DIN, and SCLK) load the digital input data serially into the DAC.

All of the digital inputs include Schmitt-trigger buffers to accept slow-transition interfaces. This means that optocouplers can interface directly to the MAX5541 without additional external logic. The digital inputs are TTL/CMOS-logic compatible.

### Unipolar Configuration

Figure 3 shows the MAX5541 configured for unipolar operation with an external op amp. The op amp is set for unity gain, and Table 1 shows the codes for this circuit.
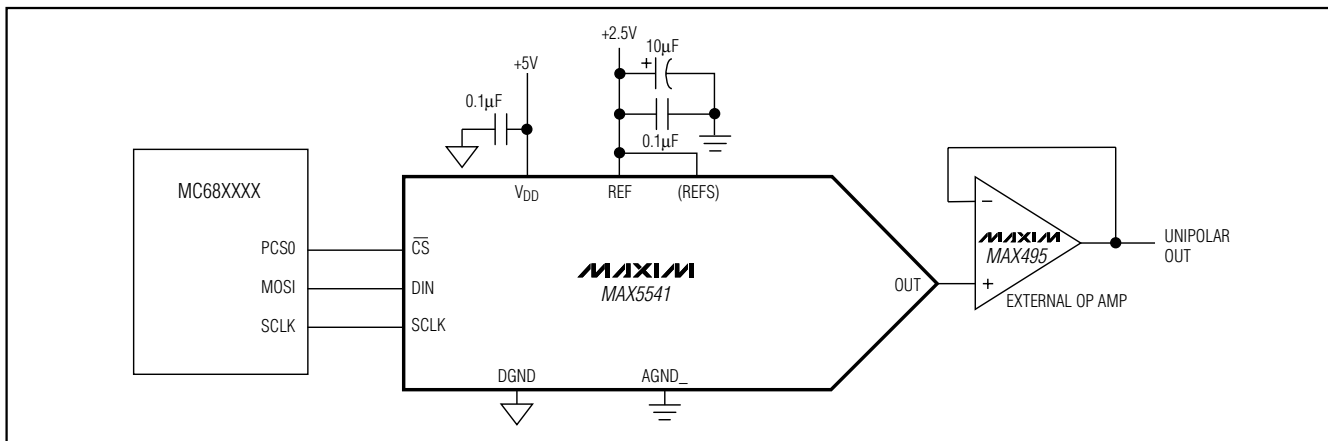
## Table 1. Unipolar Code Table

| DAC LATCH CONTENTS | | ANALOG OUTPUT, $V_{OUT}$ |
|---|---|---|
| **MSB** | **LSB** | |
| 1111 1111 1111 1111 | | $V_{REF} \times (65,535 / 65,536)$ |
| 1000 0000 0000 0000 | | $V_{REF} \times (32,768 / 65,536) = 1/2 V_{REF}$ |
| 0000 0000 0000 0001 | | $V_{REF} \times (1 / 65,536)$ |
| 0000 0000 0000 0000 | | 0V |

### Power-Supply Bypassing and Ground Management

For optimum system performance, use PC boards with separate analog and digital ground planes. Wire-wrap boards are not recommended. Connect the two ground planes together at the low-impedance power-supply source. Connect DGND and AGND together at the IC. The best ground connection can be achieved by connecting the DACs DGND and AGND pins together and connecting that point to the system analog ground plane. If the DACs DGND is connected to the system digital ground, digital noise may get through to the DACs analog portion.

Bypass $V_{DD}$ with a 0.1µF ceramic capacitor connected between $V_{DD}$ and AGND. Mount it with short leads close to the device. Ferrite beads can also be used to further isolate the analog and digital power supplies.
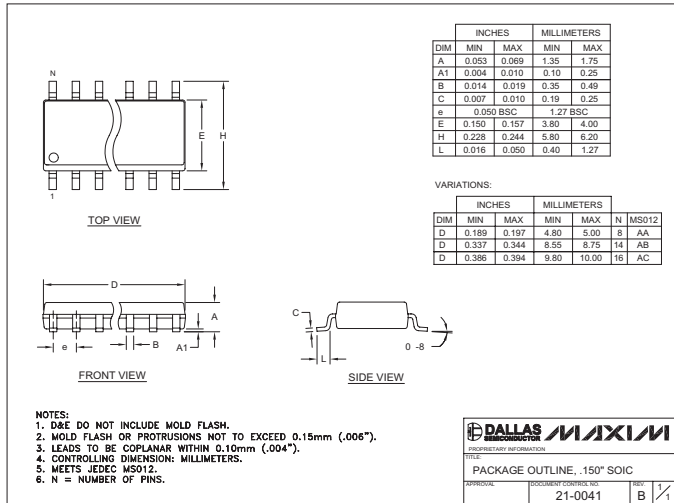
## Chip Information

TRANSISTOR COUNT: 2209

SUBSTRATE CONNECTED TO DGND



Figure 3. Typical Operating Circuit

**MAXIM**

# Low-Cost, +5V, Serial-Input, Voltage-Output, 16-Bit DAC

**MAX5541**

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



| DIM | INCHES MIN | INCHES MAX | MILLIMETERS MIN | MILLIMETERS MAX |
|---|---|---|---|---|
| A | 0.053 | 0.069 | 1.35 | 1.75 |
| A1 | 0.004 | 0.010 | 0.10 | 0.25 |
| B | 0.014 | 0.019 | 0.35 | 0.49 |
| C | 0.007 | 0.010 | 0.19 | 0.25 |
| e | 0.050 BSC | | 1.27 BSC | |
| E | 0.150 | 0.157 | 3.80 | 4.00 |
| H | 0.228 | 0.244 | 5.80 | 6.20 |
| L | 0.016 | 0.050 | 0.40 | 1.27 |

VARIATIONS:

| DIM | INCHES MIN | INCHES MAX | MILLIMETERS MIN | MILLIMETERS MAX | N | MS012 |
|---|---|---|---|---|---|---|
| D | 0.189 | 0.197 | 4.80 | 5.00 | 8 | AA |
| D | 0.337 | 0.344 | 8.55 | 8.75 | 14 | AB |
| D | 0.386 | 0.394 | 9.80 | 10.00 | 16 | AC |

TOP VIEW

FRONT VIEW

SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR /VI/IXI/VI

PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, .150" SOIC

| APPROVAL | DOCUMENT CONTROL NO. | REV. | |
|---|---|---|---|
| | 21-0041 | B | 1/1 |

SOICN.EPS

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