

# 74ABT08PW,118 Datasheet

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DiGi Electronics Part Number	74ABT08PW,118-DG
Manufacturer	<a href="#">Nexperia USA Inc.</a>
Manufacturer Product Number	74ABT08PW,118
Description	IC GATE AND 4CH 2-INP 14TSSOP
Detailed Description	AND Gate IC 4 Channel 14-TSSOP



Tel: +00 852-30501935

RFQ Email: [Info@DiGi-Electronics.com](mailto:Info@DiGi-Electronics.com)

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## Purchase and inquiry

**Manufacturer Product Number:**

74ABT08PW,118

**Series:**

74ABT

**Logic Type:**

AND Gate

**Number of Inputs:**

2

**Voltage - Supply:**

4.5V ~ 5.5V

**Current - Output High, Low:**

15mA, 20mA

**Input Logic Level - High:**

2V

**Operating Temperature:**

-40°C ~ 85°C

**Supplier Device Package:**

14-TSSOP

**Base Product Number:**

74ABT08

**Manufacturer:**

Nexperia USA Inc.

**Product Status:**

Active

**Number of Circuits:**

4

**Features:**

-

**Current - Quiescent (Max):**

50 µA

**Input Logic Level - Low:**

0.8V

**Max Propagation Delay @ V, Max CL:**

3.4ns @ 5V, 50pF

**Mounting Type:**

Surface Mount

**Package / Case:**

14-TSSOP (0.173", 4.40mm Width)

## Environmental & Export classification

**RoHS Status:**

ROHS3 Compliant

**REACH Status:**

REACH Unaffected

**HTSUS:**

8542.39.0001

**Moisture Sensitivity Level (MSL):**

1 (Unlimited)

**ECCN:**

EAR99

# 74ABT08

## Quad 2-input AND gate

Rev. 5.1 — 18 January 2024

Product data sheet

### 1. General description

The 74ABT08 is a quad 2-input AND gate. This device is fully specified for partial power down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

### 2. Features and benefits

- Supply voltage range from 4.5 V to 5.5 V
- BiCMOS high speed and output drive
- Direct interface with TTL levels
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- Latch-up protection exceeds 500 mA per JESD78B class II level A
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
<a href="#">74ABT08D</a>	-40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	<a href="#">SOT108-1</a>
<a href="#">74ABT08PW</a>	-40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	<a href="#">SOT402-1</a>

## 4. Functional diagram

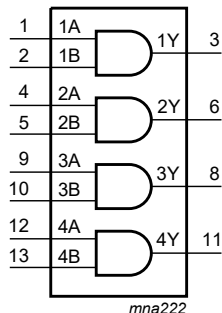


Fig. 1. Logic symbol

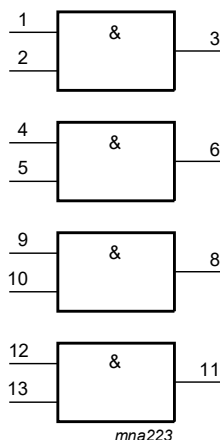


Fig. 2. IEC logic symbol

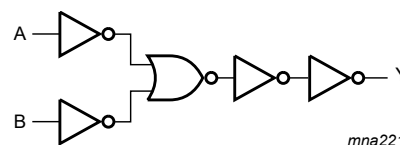
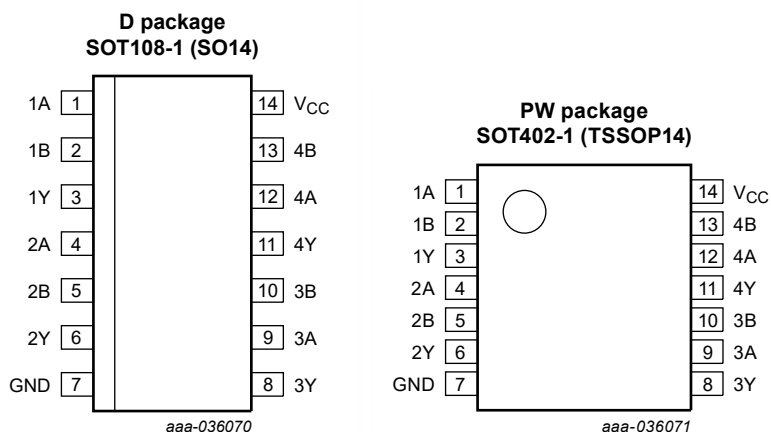


Fig. 3. Logic diagram (one gate)

## 5. Pinning information

### 5.1. Pinning



### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A	1, 4, 9, 12	data input
1B, 2B, 3B, 4B	2, 5, 10, 13	data input
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V <sub>CC</sub>	14	supply voltage

## 6. Functional description

**Table 3. Function table**

*H = HIGH voltage level; L = LOW voltage level; X = don't care.*

Input		Output
nA	nB	nY
L	X	L
X	L	L
H	H	H

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		[1]	+7.0	V
$V_O$	output voltage	output HIGH or LOW	[1]	+5.5	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-18	-	mA
$I_{OK}$	output clamping current	$V_O < 0$ V	-50	-	mA
$I_O$	output current	output in LOW-state	-	40	mA
$T_j$	junction temperature		-	150	°C
$T_{stg}$	storage temperature		-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 8. Recommended operating conditions

**Table 5. Operating conditions**

*Voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		4.5	-	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$V_{IH}$	HIGH-level input voltage		2.0	-	-	V
$V_{IL}$	LOW-level input voltage		-	-	0.8	V
$I_{OH}$	HIGH-level output current		-15	-	-	mA
$I_{OL}$	LOW-level output current		-	-	20	mA
$\Delta t/\Delta V$	input transition rise and fall rate		0	-	5	ns/V
$T_{amb}$	ambient temperature	in free air	-40	-	+85	°C

## 9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
V <sub>IK</sub>	input clamping voltage	V <sub>CC</sub> = 4.5 V; I <sub>IK</sub> = -18 mA	-1.2	-0.9	-	-1.2	-	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>CC</sub> = 4.5 V; I <sub>OH</sub> = -15 mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	2.5	2.9	-	2.5	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>CC</sub> = 4.5 V; I <sub>OL</sub> = 20 mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	-	0.35	0.5	-	0.5	V
I <sub>I</sub>	input leakage current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = GND or 5.5 V	-	±0.01	±1.0	-	±1.0	µA
I <sub>OFF</sub>	power-off leakage current	V <sub>CC</sub> = 0 V; V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V	-	±5.0	±100	-	±100	µA
I <sub>CEX</sub>	output high leakage current	HIGH-state; V <sub>O</sub> = 5.5 V; V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = GND or V <sub>CC</sub>	-	5.0	50	-	50	µA
I <sub>O</sub>	output current	V <sub>CC</sub> = 5.5 V; V <sub>O</sub> = 2.5 V [1]	-50	-75	-180	-50	-180	mA
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = GND or V <sub>CC</sub>	-	2	50	-	50	µA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>CC</sub> = 5.5 V; one input at 3.4 V; other inputs at V <sub>CC</sub> or GND [2]	-	0.25	500	-	500	µA
C <sub>I</sub>	input capacitance	V <sub>I</sub> = 0 V or V <sub>CC</sub>	-	3	-	-	-	pF

[1] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[2] This is the increase in supply current for each input at 3.4 V.

## 10. Dynamic characteristics

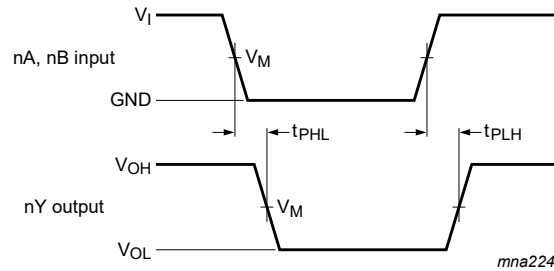
Table 7. Dynamic characteristics

GND = 0 V; for test circuit, see Fig. 5.

Symbol	Parameter	Conditions	25 °C; V <sub>CC</sub> = 5.0 V			-40 °C to +85 °C; V <sub>CC</sub> = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	LOW to HIGH propagation delay	nA, nB to nY; see Fig. 4	1.0	2.4	3.4	1.0	4.0	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	nA, nB to nY; see Fig. 4	1.0	1.9	2.8	1.0	3.0	ns
t <sub>sk(o)</sub>	output skew time [1]		-	0.4	0.5	-	0.5	ns

[1] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

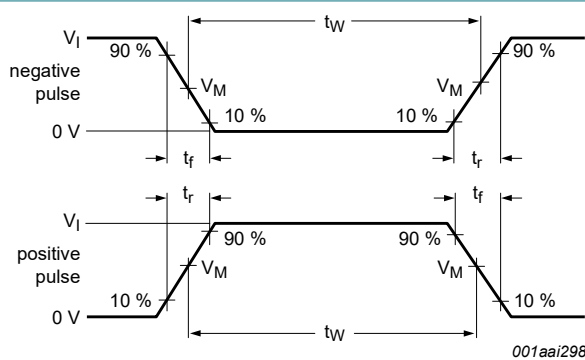
## 10.1. Waveforms and test circuit



$$V_M = 1.5 \text{ V}$$

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig. 4. Propagation delay input (nA, nB) to output (nY) and output skew time**



a. Input pulse definition

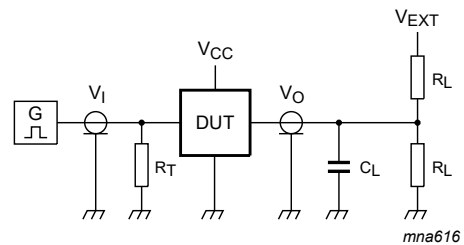
Test data is given in [Table 8](#).

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.



b. Test circuit

**Fig. 5. Test circuit for measuring switching times**

**Table 8. Test data**

Input				Load		$V_{EXT}$
$V_I$	$f_i$	$t_W$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHL}, t_{PLH}$
3.0 V	1 MHz	500 ns	$\leq 2.5 \text{ ns}$	50 pF	500 $\Omega$	open

## 11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

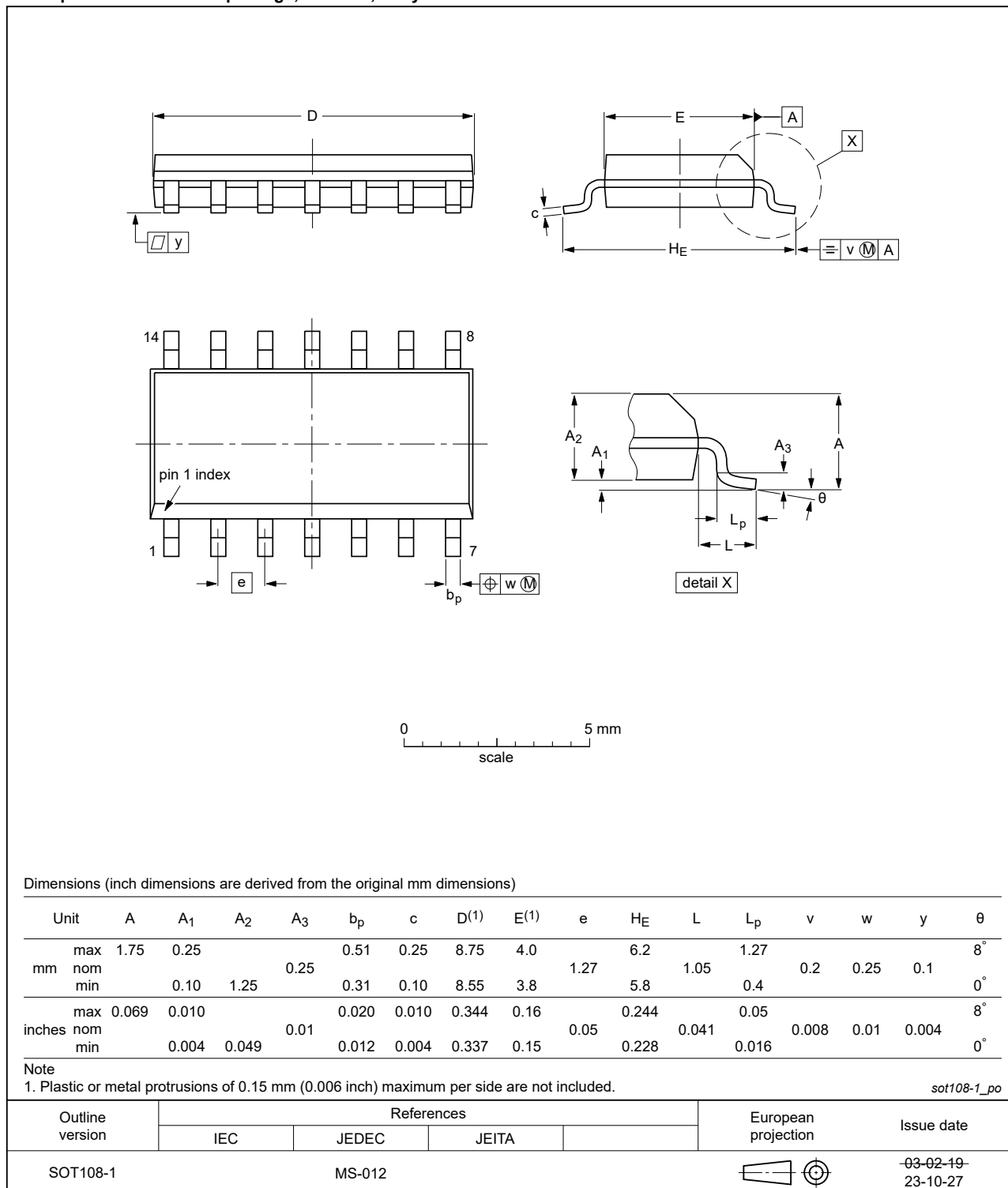


Fig. 6. Package outline SOT108-1 (SO14)



TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

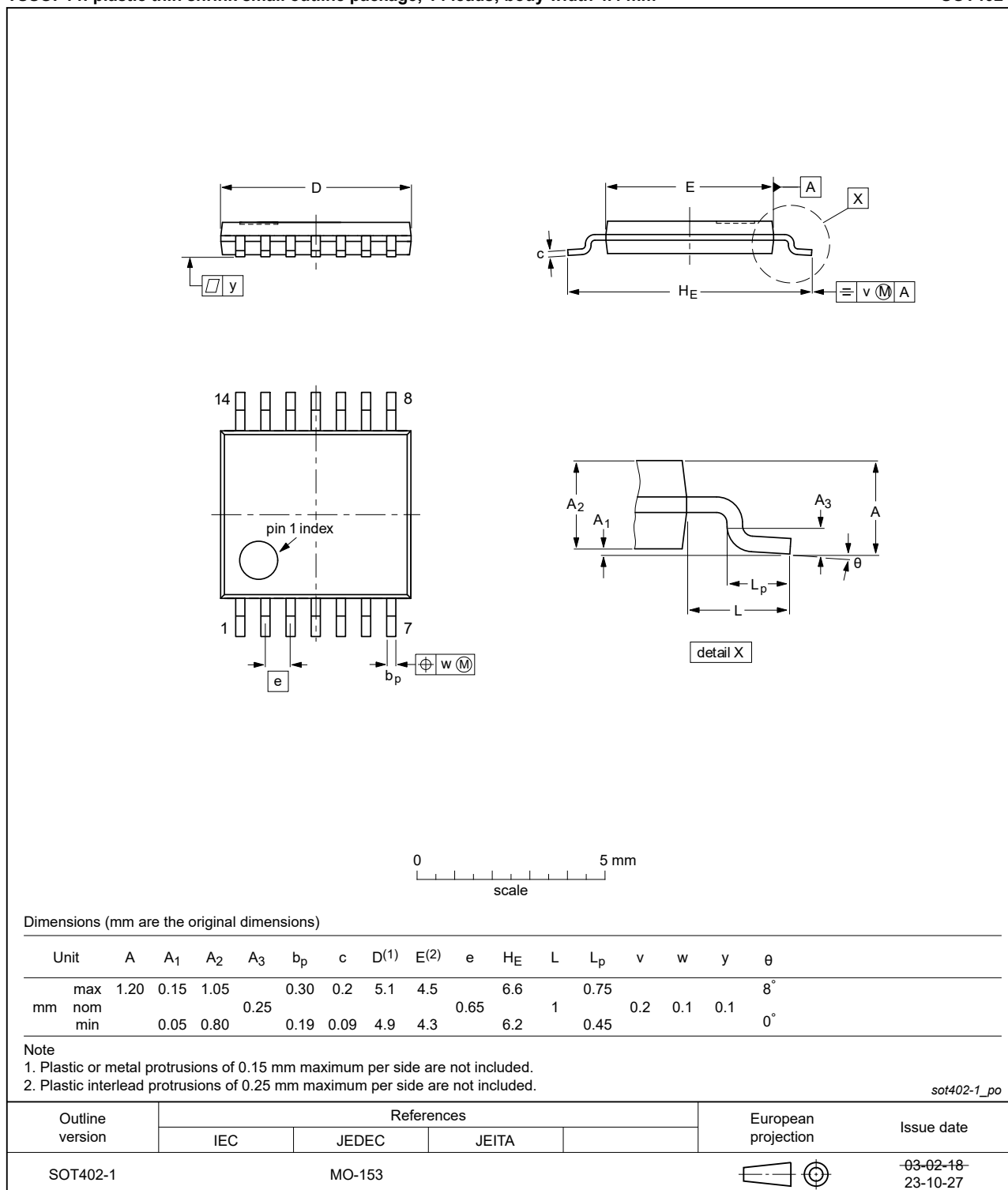


Fig. 7. Package outline SOT402-1 (TSSOP14)

## 12. Abbreviations

Table 9. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal-Oxide Semiconductor
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT08 v.5.1	20240118	Product data sheet	-	74ABT08 v.4
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li> <li>• <a href="#">Fig. 6</a>, <a href="#">Fig. 7</a>: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.</li> </ul>			
74ABT08 v.4	20201007	Product data sheet	-	74ABT08 v.3
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• <a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> <li>• Type number 74ABT08DB (SOT337-1 / SSOP14) removed.</li> </ul>			
74ABT08 v.3	20151120	Product data sheet	-	74ABT08 v.2
Modifications:	<ul style="list-style-type: none"> <li>• Type number 74ABT08N (SOT27-1) removed.</li> </ul>			
74ABT08 v.2	20140314	Product data sheet	-	74ABT08 v.1
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
74ABT08 v.1	19950918	Product specification	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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