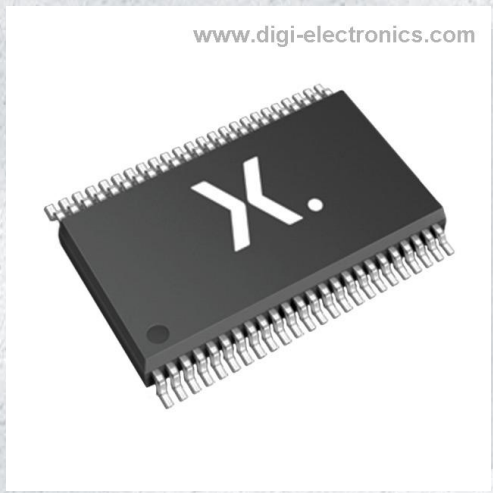
74ABT16245BDGG,512 Datasheet



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DiGi Electronics Part Number	74ABT16245BDGG,512-DG
Manufacturer	Nexperia USA Inc.
Manufacturer Product Number	74ABT16245BDGG,512
Description	IC TXRX NON-INVERT 5.5V 48TSSOP
Detailed Description	Transceiver, Non-Inverting 2 Element 8 Bit per Element 3-State Output 48-TSSOP

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
74ABT16245BDGG,512	Nexperia USA Inc.
Series:	Product Status:
74ABT	Obsolete
Logic Type:	Number of Elements:
Transceiver, Non-Inverting	2
Number of Bits per Element:	Input Type:
8	-
Output Type:	Current - Output High, Low:
3-State	32mA, 64mA
Voltage - Supply:	Operating Temperature:
4.5V ~ 5.5V	-40°C ~ 85°C (TA)
Mounting Type:	Package / Case:
Surface Mount	48-TFSOP (0.240", 6.10mm Width)
Supplier Device Package:	Base Product Number:
48-TSSOP	74ABT16245

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8542.39.0001	

74ABT16245B

16-bit bus transceiver; 3-state

Rev. 8 — 24 June 2024 Product data sheet

1. General description

The 74ABT16245B is a 16-bit transceiver with 3-state outputs. The device can be used as two 8-bit transceivers or one 16-bit transceiver. The device features two output enables (1$\overline{OE}$ and 2$\overline{OE}$) each controlling eight outputs, and two send/receive (1DIR and 2DIR) inputs for direction control. A HIGH on n$\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Supply voltage range from 4.5 to 5.5 V
- BiCMOS high speed and output drive
- Direct interface with TTL levels
- 16-bit bidirectional bus interface
- Multiple V_{CC} and GND pins minimize switching noise
- Power-up 3-state
- 3-state buffers
- Output capability: +64 mA and -32 mA
- Live insertion/extraction permitted
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 500 mA per JESD 78 Class II Level B
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to 85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ABT16245BDGG	-40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1

4. Functional diagram

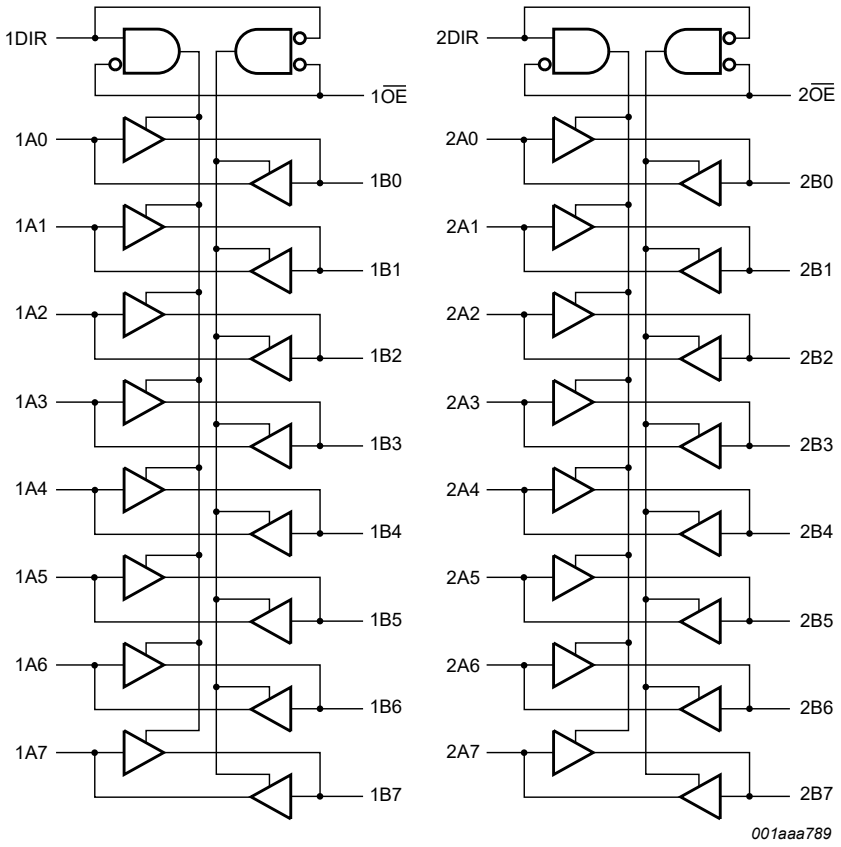


Fig. 1. Logic symbol

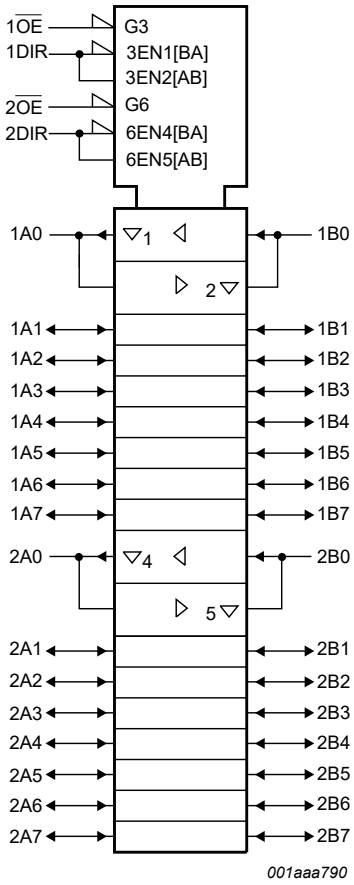
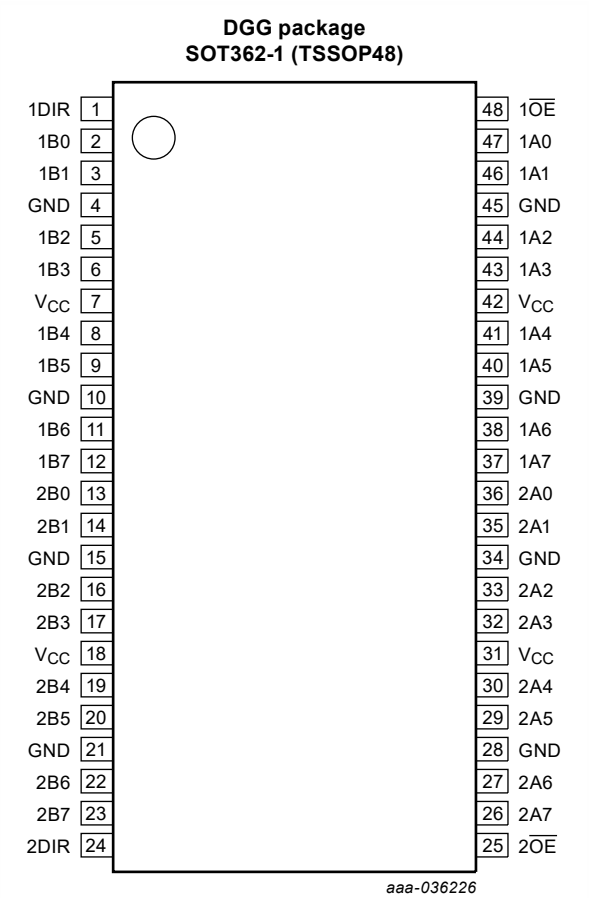


Fig. 2. IEC logic symbol

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1DIR, 2DIR	1, 24	direction control input
1B0, 1B1, 1B2, 1B3, 1B4, 1B5, 1B6, 1B7	2, 3, 5, 6, 8, 9, 11, 12	data input/output
2B0, 2B1, 2B2, 2B3, 2B4, 2B5, 2B6, 2B7	13, 14, 16, 17, 19, 20, 22, 23	data input/output
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V_{CC}	7, 18, 31, 42	supply voltage
$1\overline{OE}$, $2\overline{OE}$	48, 25	output enable input (active LOW)
1A0, 1A1, 1A2, 1A3, 1A4, 1A5, 1A6, 1A7	47, 46, 44, 43, 41, 40, 38, 37	data input/output
2A0, 2A1, 2A2, 2A3, 2A4, 2A5, 2A6, 2A7	36, 35, 33, 32, 30, 29, 27, 26	data input/output

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Inputs		Outputs	
n$\overline{OE}$	**nDIR**	**nAn**	**nBn**
L	L	nAn = nBn	inputs
L	H	inputs	nBn = nAn
H	X	Z	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+7.0	V
V_I	input voltage		[1]	-1.2	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state	[1]	-0.5	+5.5	V
I_{IK}	input clamping current	V_I < 0 V		-18	-	mA
I_{OK}	output clamping current	V_O < 0 V		-50	-	mA
I_O	output current	output in LOW-state		-	128	mA
		output in HIGH-state		-64	-	mA
T_j	junction temperature		[2]	-	150	°C
T_{stg}	storage temperature			-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

8. Recommended operating conditions

Table 5. Operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		4.5	5.5	V
V_I	input voltage		0	V_{CC}	V
V_{IH}	HIGH-level input voltage		2.0	-	V
V_{IL}	LOW-level input voltage		-	0.8	V
I_{OH}	HIGH-level output current		-32	-	mA
I_{OL}	LOW-level output current		-	64	mA
$\Delta t/\Delta V$	input transition rise and fall rate		-	10	ns/V
T_{amb}	ambient temperature	in free air	-40	+85	°C

9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
V_{IK}	input clamping voltage	V_{CC} = 4.5 V; I_{IK} = -18 mA	-1.2	-0.9	-	-1.2	-	V
V_{OH}	HIGH-level output voltage	V_I = V_{IL} or V_{IH}						
		V_{CC} = 4.5 V; I_{OH} = -3 mA	2.5	2.9	-	2.5	-	V
		V_{CC} = 5.0 V; I_{OH} = -3 mA	3.0	3.4	-	3.0	-	V
		V_{CC} = 4.5 V; I_{OH} = -32 mA	2.0	2.4	-	2.0	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 4.5 V; I_{OL} = 64 mA; V_I = V_{IL} or V_{IH}	-	0.42	0.55	-	0.55	V
I_I	input leakage current	control pins; V_{CC} = 5.5 V; V_I = V_{CC} or GND	-	±0.01	±1.0	-	±1.0	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O ≤ 4.5 V	-	±5.0	±100	-	±100	µA
$I_{O(pu/pd)}$	power-up/ power-down output current	V_{CC} = 2.0 V; V_O = 0.5 V; V_I = GND or V_{CC}; $n\overline{OE}$ = HIGH [1]	-	±5.0	±50	-	±50	µA
I_{OZ}	OFF-state output current	V_{CC} = 5.5 V; V_I = V_{IL} or V_{IH}						
		output HIGH-state at V_O = 5.5 V	-	0.1	10	-	10	µA
		output LOW-state at V_O = 0 V	-	-0.1	-10	-	-10	µA
I_{CEX}	output high leakage current	HIGH-state; V_O = 5.5 V; V_{CC} = 5.5 V; V_I = GND or V_{CC}	-	5.0	50	-	50	µA
I_O	output current	V_{CC} = 5.5 V; V_O = 2.5 V [2]	-50	-92	-180	-50	-180	mA
I_{CC}	supply current	V_{CC} = 5.5 V; V_I = GND or V_{CC}						
		outputs HIGH-state	-	0.30	0.7	-	0.7	mA
		outputs LOW-state	-	10	19	-	19	mA
		outputs 3-state	-	0.30	0.7	-	0.7	mA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 5.5 V; one data input at 3.4 V and other inputs at V_{CC} or GND [3]						
		outputs enabled	-	400	700	-	700	µA
		outputs disabled	-	100	250	-	250	µA
		control pins; outputs disabled; one enable input at 3.4 V and other inputs at V_{CC} or GND	-	400	700	-	700	µA
C_I	input capacitance	V_I = 0 V or V_{CC}	-	4	-	-	-	pF
$C_{I/O}$	input/output capacitance	outputs disabled; V_O = 0 V or V_{CC}	-	7	-	-	-	pF

[1] This parameter is valid for any V_{CC} between 0 V and 2.1 V, with a transition time of up to 10 ms. From V_{CC} = 2.1 V to V_{CC} = 5 V ± 10 %, a transition time of up to 100 µs is permitted.
[2] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
[3] This is the increase in supply current for each input at 3.4 V.

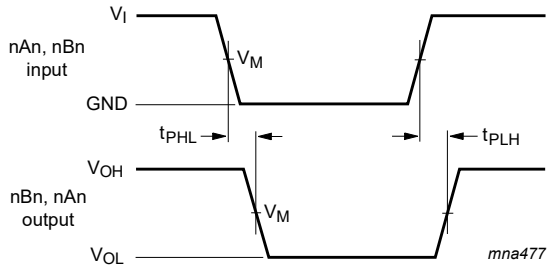
10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V. For test circuit, see Fig. 5.

Symbol	Parameter	Conditions	25 °C; V_{CC} = 5.0 V			-40 °C to +85 °C; V_{CC} = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	LOW to HIGH propagation delay	nAn to nBn; see Fig. 3	1.0	2.0	3.2	1.0	3.5	ns
t_{PHL}	HIGH to LOW propagation delay	nAn to nBn; see Fig. 3	1.0	2.3	3.5	1.0	4.0	ns
t_{PZH}	OFF-state to HIGH propagation delay	$n\overline{OE}$ to nAn or nBn; see Fig. 4	1.0	3.0	4.4	1.0	5.1	ns
t_{PZL}	OFF-state to LOW propagation delay	$n\overline{OE}$ to nAn or nBn; see Fig. 4	1.7	4.0	5.2	1.7	6.1	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$n\overline{OE}$ to nAn or nBn; see Fig. 4	1.7	3.5	4.9	1.7	5.4	ns
t_{PLZ}	LOW to OFF-state propagation delay	$n\overline{OE}$ to nAn or nBn; see Fig. 4	1.5	3.2	4.4	1.5	5.0	ns

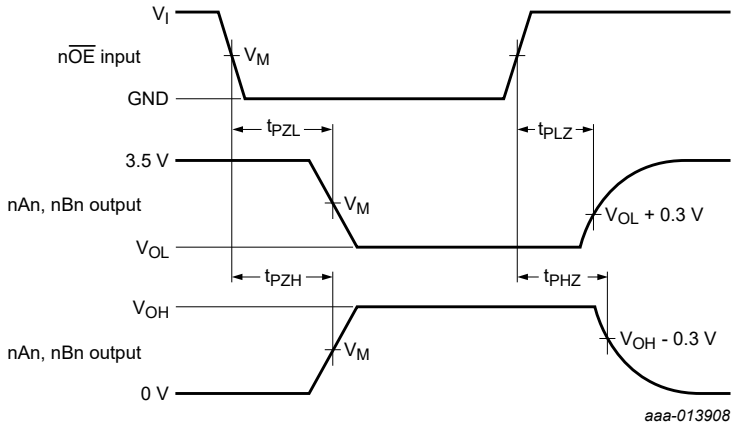
10.1. Waveforms and test circuit



V_M = 1.5 V

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

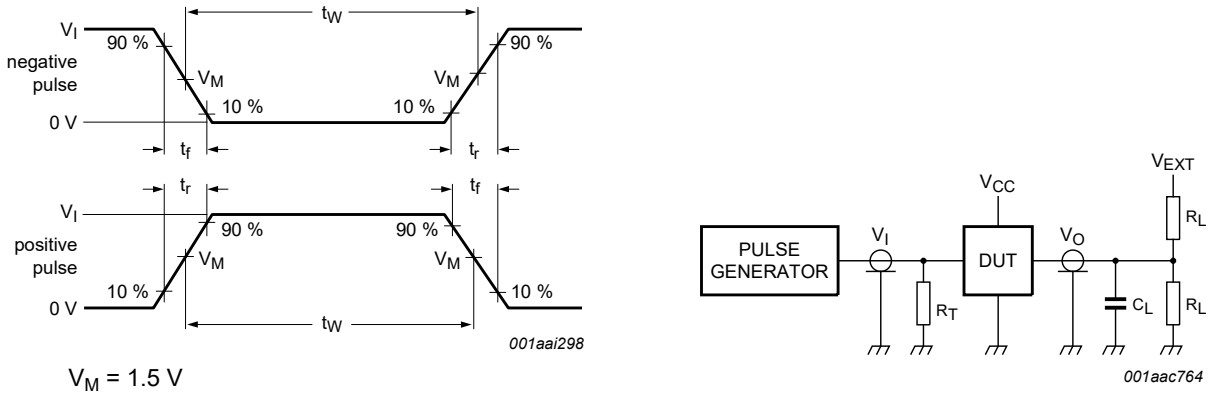
Fig. 3. Input (nAn) to output (nBn) propagation delay times



V_M = 1.5 V

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 4. 3-state output enable and disable times



V_M = 1.5 V

a.Input pulse definition

b.Test circuit

Test data is given in Table 8.

Definitions test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator

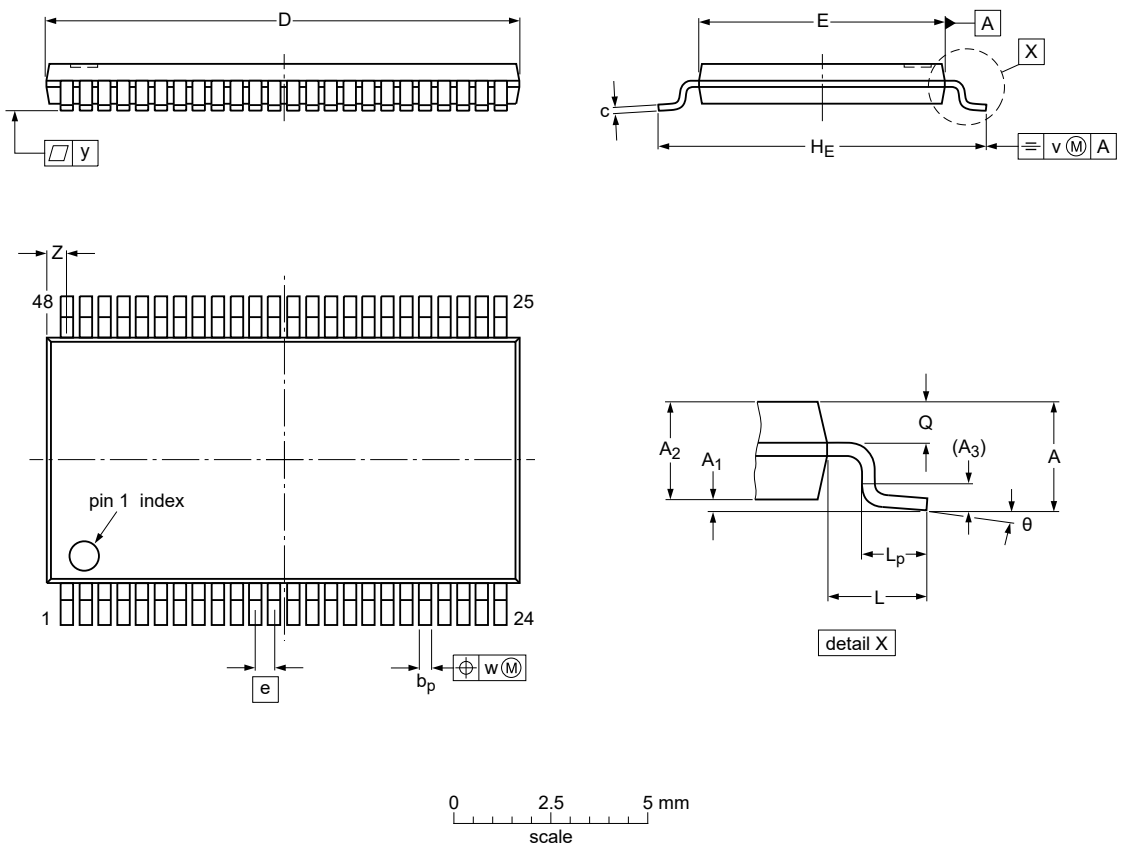
Fig. 5. Test circuit for measuring switching times

Table 8. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
3.0 V	1 MHz	500 ns	2.5 ns	50 pF	500 Ω	open	7.0 V	open

11. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	max	1.2	0.15	1.05		0.28	0.2	12.6	6.2		8.3		0.8	0.50				0.8	8°
	nom				0.25					0.5		1			0.25	0.08	0.1		
	min		0.05	0.85		0.17	0.1	12.4	6.0		7.9		0.4	0.35				0.4	0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot362-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				~~13-08-05~~ 24-01-05

Fig. 6. Package outline SOT362-1 (TSSOP48)

12. Abbreviations

Table 9. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

13. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT16245B v.8	20240624	Product data sheet	-	74ABT16245B v.7
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard.			
74ABT16245B v.7	20240424	Product data sheet	-	74ABT16245B v.6
Modifications:	• Fig. 6: Updated package outline drawing SOT362-1 (TSSOP48).			
74ABT16245B v.6	20210714	Product data sheet	-	74ABT16245B v.5
Modifications:	• Section 1 and Section 2 updated. • Type number 74ABT16245BDL (SOT370-1/SSOP48) removed.			
74ABT16245B v.5	20170410	Product data sheet	-	74ABT16245B v.4
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
74ABT16245B v.4	20140819	Product data sheet	-	74ABT_H16245B v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Type number 74ABTH16245BDL removed.			
74ABT_H16245B v.3	20021213	Product data sheet	-	74ABT_H16245B v.2
74ABT_H16245B v.2	19980225	Product data sheet	-	74ABT_H16245B v.1
74ABT_H16245B v.1	19961120	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 24 June 2024

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