

# 74AHC1G09GW,125 Datasheet

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DiGi Electronics Part Number	74AHC1G09GW,125-DG
Manufacturer	<a href="#">Nexperia USA Inc.</a>
Manufacturer Product Number	74AHC1G09GW,125
Description	IC GATE AND 1CH 2-INP 5TSSOP
Detailed Description	AND Gate IC 1 Channel Open Drain 5-TSSOP



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## Purchase and inquiry

**Manufacturer Product Number:**

74AHC1G09GW,125

**Series:**

74AHC

**Logic Type:**

AND Gate

**Number of Inputs:**

2

**Voltage - Supply:**

2V ~ 5.5V

**Current - Output High, Low:**

-, 8mA

**Input Logic Level - High:**

1.5V ~ 3.85V

**Operating Temperature:**

-40°C ~ 125°C

**Supplier Device Package:**

5-TSSOP

**Base Product Number:**

74AHC1G09

**Manufacturer:**

Nexperia USA Inc.

**Product Status:**

Active

**Number of Circuits:**

1

**Features:**

Open Drain

**Current - Quiescent (Max):**1  $\mu$ A**Input Logic Level - Low:**

0.5V ~ 1.65V

**Max Propagation Delay @ V, Max CL:**

7.5ns @ 5V, 50pF

**Mounting Type:**

Surface Mount

**Package / Case:**

5-TSSOP, SC-70-5, SOT-353

## Environmental & Export classification

**RoHS Status:**

ROHS3 Compliant

**REACH Status:**

REACH Unaffected

**HTSUS:**

8542.39.0001

**Moisture Sensitivity Level (MSL):**

1 (Unlimited)

**ECCN:**

EAR99



# 74AHC1G09

2-input AND gate with open-drain output

Rev. 5 — 19 September 2024

Product data sheet

## 1. General description

The 74AHC1G09 is a single 2-input AND gate with open-drain output. Inputs are overvoltage tolerant. This feature allows the use of these devices as translators in mixed voltage environments.

## 2. Features and benefits

- Wide supply voltage range from 2.0 to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- CMOS low power dissipation
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level A
- CMOS input levels
- Multiple package options
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C.

## 3. Ordering information

Table 1. Ordering information

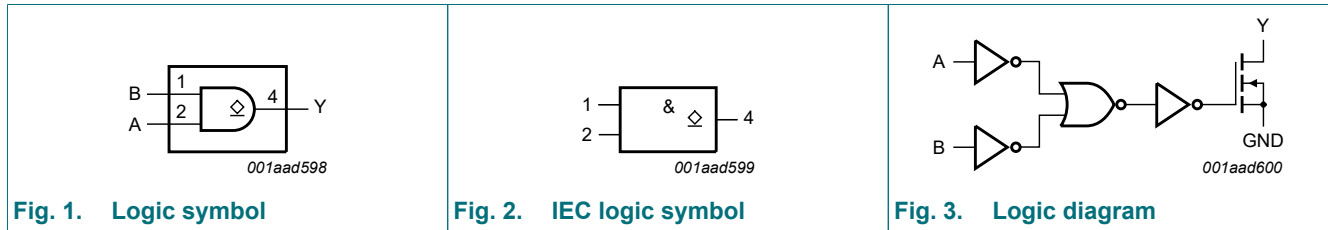
Type number	Package			
	Temperature range	Name	Description	Version
<a href="#">74AHC1G09GW</a>	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	<a href="#">SOT353-1</a>
<a href="#">74AHC1G09GV</a>	-40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	<a href="#">SOT753</a>
<a href="#">74AHC1G09GZ</a>	-40 °C to +125 °C	XSON5	plastic thermal enhanced extremely thin small outline package with side-wettable flanks (SWF); no leads; 5 terminals; body 1.1 × 0.85 × 0.5 mm	<a href="#">SOT8065-1</a>

## 4. Marking

Table 2. Marking

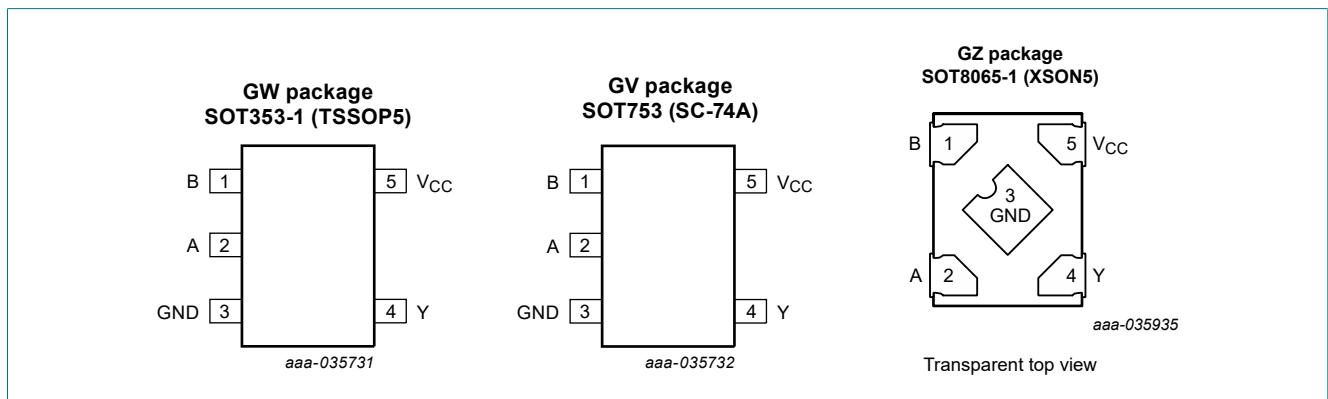
Type number	Marking code
74AHC1G09GW	A9
74AHC1G09GV	A09
74AHC1G09GZ	tbd

## 5. Functional diagram



## 6. Pinning information

### 6.1. Pinning



### 6.2. Pin description

**Table 3. Pin description**

Symbol	Pin	Description
B	1	data input B
A	2	data input A
GND	3	ground (0 V)
Y	4	data output Y
V <sub>CC</sub>	5	supply voltage

## 7. Functional description

**Table 4. Function table**

*H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.*

Input		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	Z

## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit	
$V_{CC}$	supply voltage		-0.5	+7.0	V	
$V_I$	input voltage	[1]	-0.5	+7.0	V	
$V_O$	output voltage	active mode	[1]	-0.5	+7.0	V
		high-impedance mode	[1]	-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5$ V	[1]	-	-20	mA
$I_{OK}$	output clamping current	$V_O < -0.5$ V	[1]	-	±20	mA
$I_O$	output current	$V_O > -0.5$ V	-	25	mA	
$I_{CC}$	supply current		-	±75	mA	
$I_{GND}$	GND current		-	±75	mA	
$T_{stg}$	storage temperature		-65	+150	°C	
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT353-1 (TSSOP5) package:  $P_{tot}$  derates linearly with 3.3 mW/K above 74 °C.

For SOT753 (SC-74A) package:  $P_{tot}$  derates linearly with 3.8 mW/K above 85 °C.

For SOT8065-1 (XSON5) package:  $P_{tot}$  derates linearly with 3.2 mW/K above 72 °C.

## 9. Recommended operating conditions

**Table 6. Recommended operating operations**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		2.0	5.0	5.5	V
$V_I$	input voltage		0	-	5.5	V
$V_O$	output voltage	active mode	0	-	$V_{CC}$	V
		high-impedance mode	0	-	6.0	V
$T_{amb}$	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.0$ V to 3.6 V	-	-	100	ns/V
		$V_{CC} = 4.5$ V to 5.5 V	-	-	20	ns/V

## 10. Static characteristics

**Table 7. Static characteristics**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0$ V	1.5	-	-	1.5	-	1.5	-	V
		$V_{CC} = 3.0$ V	2.1	-	-	2.1	-	2.1	-	V
		$V_{CC} = 5.5$ V	3.85	-	-	3.85	-	3.85	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0$ V	-	-	0.5	-	0.5	-	0.5	V
		$V_{CC} = 3.0$ V	-	-	0.9	-	0.9	-	0.9	V
		$V_{CC} = 5.5$ V	-	-	1.65	-	1.65	-	1.65	V

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I <sub>O</sub> = 8.0 mA; V <sub>CC</sub> = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	±0.1	-	±1.0	-	±2.0	μA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	±0.25		±2.5		±10.0	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	1.0	-	10	-	20	μA
C <sub>I</sub>	input capacitance		-	1.5	10	-	10	-	10	pF

## 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

GND = 0 V; for test circuit see Fig. 5.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t <sub>pd</sub>	propagation delay	A and B to Y; see Fig. 4 [1]								
		V <sub>CC</sub> = 3.0 V to 3.6 V [2]								
		C <sub>L</sub> = 15 pF	-	4.6	7.5	1.0	8.5	1.0	9.0	ns
		C <sub>L</sub> = 50 pF	-	6.5	11.0	1.5	12.0	1.5	12.5	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V [3]								
		C <sub>L</sub> = 15 pF	-	3.2	5.5	1.0	6.5	1.0	7.0	ns
		C <sub>L</sub> = 50 pF	-	4.6	7.5	1.5	8.0	1.5	8.5	ns
C <sub>PD</sub>	power dissipation capacitance	C <sub>L</sub> = 50 pF; f <sub>i</sub> = 1 MHz; [4] V <sub>I</sub> = GND to V <sub>CC</sub>	-	5	-	-	-	-	-	pF

[1] t<sub>pd</sub> is the same as t<sub>PZL</sub> and t<sub>PLZ</sub>.

[2] Typical values are measured at V<sub>CC</sub> = 3.3 V.

[3] Typical values are measured at V<sub>CC</sub> = 5.0 V.

[4] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

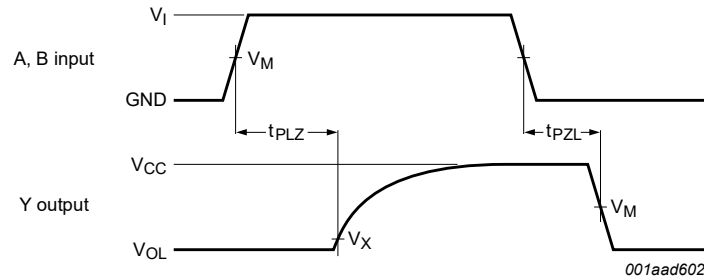
C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = dissipation due to the output if the combination of the pull up voltage and resistance results in V<sub>CC</sub> at the output.

### 11.1. Waveform and test circuit



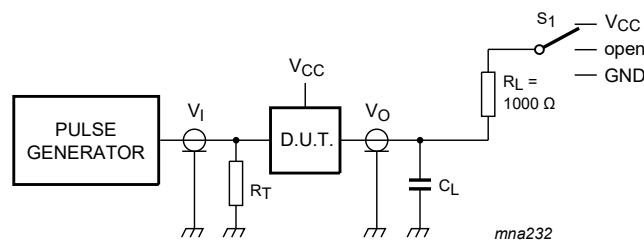
Measurement points are given in [Table 9](#).

$V_{OL}$  is the typical voltage output level that occur with the output load.

**Fig. 4.** The data input (A, B) to output (Y) propagation delays

**Table 9.** Measurement points

Input	Output	
$V_M$	$V_M$	$V_X$
$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.3 V$



Test data is given in [Table 10](#).

Definitions for test circuit:

$C_L$  = Load capacitance including jig and probe capacitance;

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

**Fig. 5.** Test circuit for measuring switching times

**Table 10.** Test data

Input		Load		$S_1$		
$V_I$	$t_r, t_f$	$R_L$	$C_L$	$t_{PHZ}, t_{PZH}$	$t_{PLZ}, t_{PZL}$	$t_{PLH}, t_{PHL}$
GND to $V_{CC}$	$\leq 3.0$ ns	$1000 \Omega$	15 pF	GND	$V_{CC}$	open
GND to $V_{CC}$	$\leq 3.0$ ns	$1000 \Omega$	50 pF	GND	$V_{CC}$	open

## 12. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1

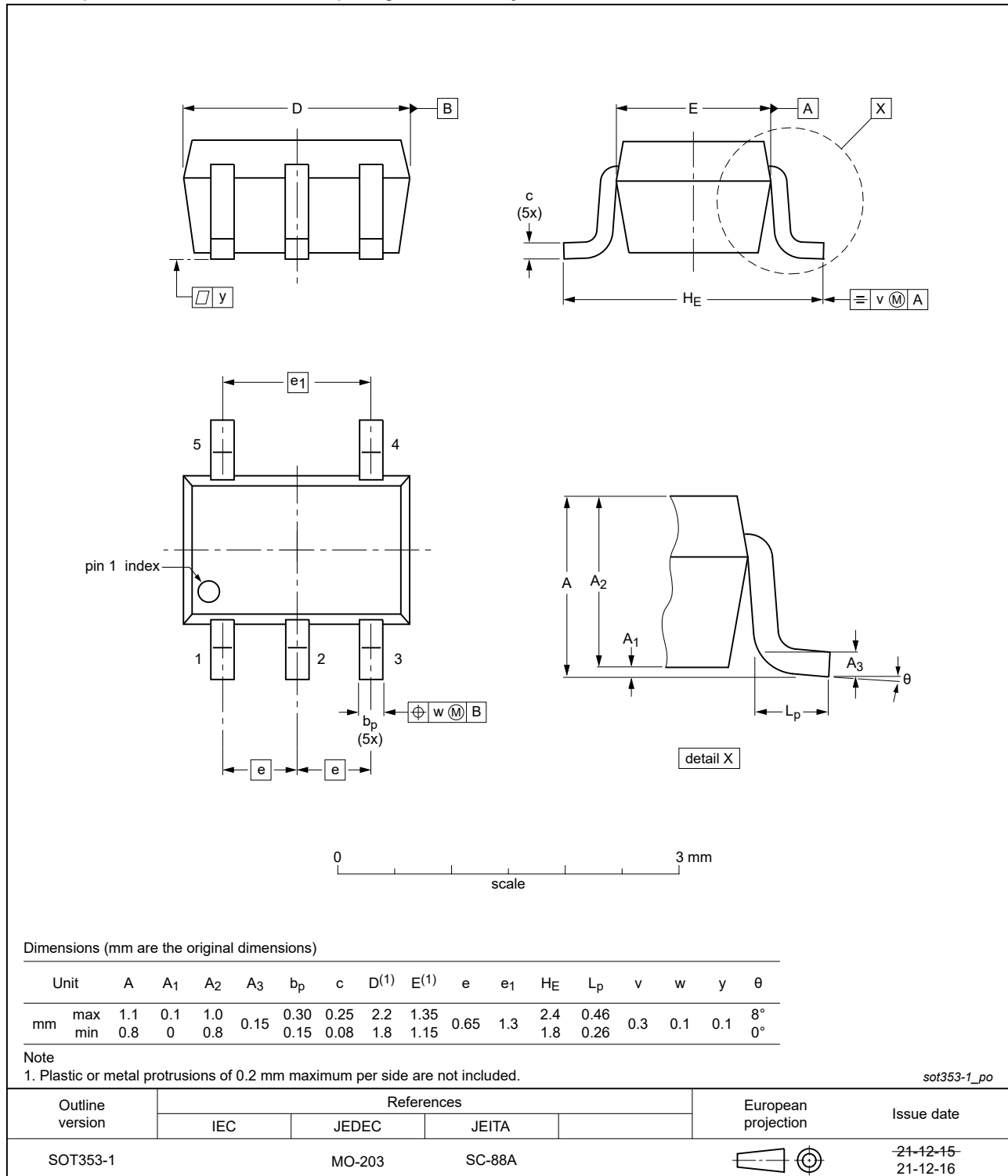


Fig. 6. Package outline SOT353-1 (TSSOP5)



Plastic surface-mounted package; 5 leads

SOT753

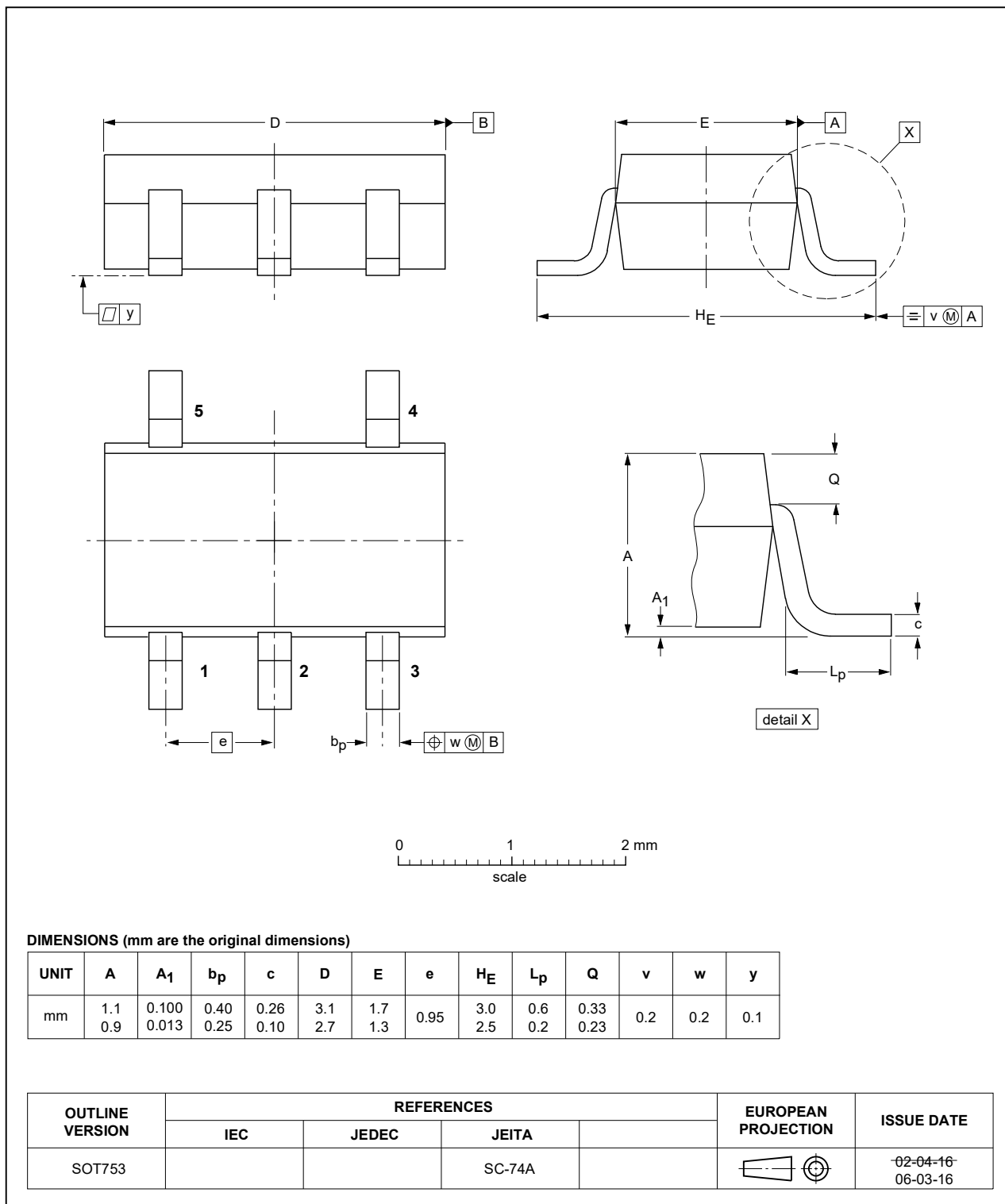
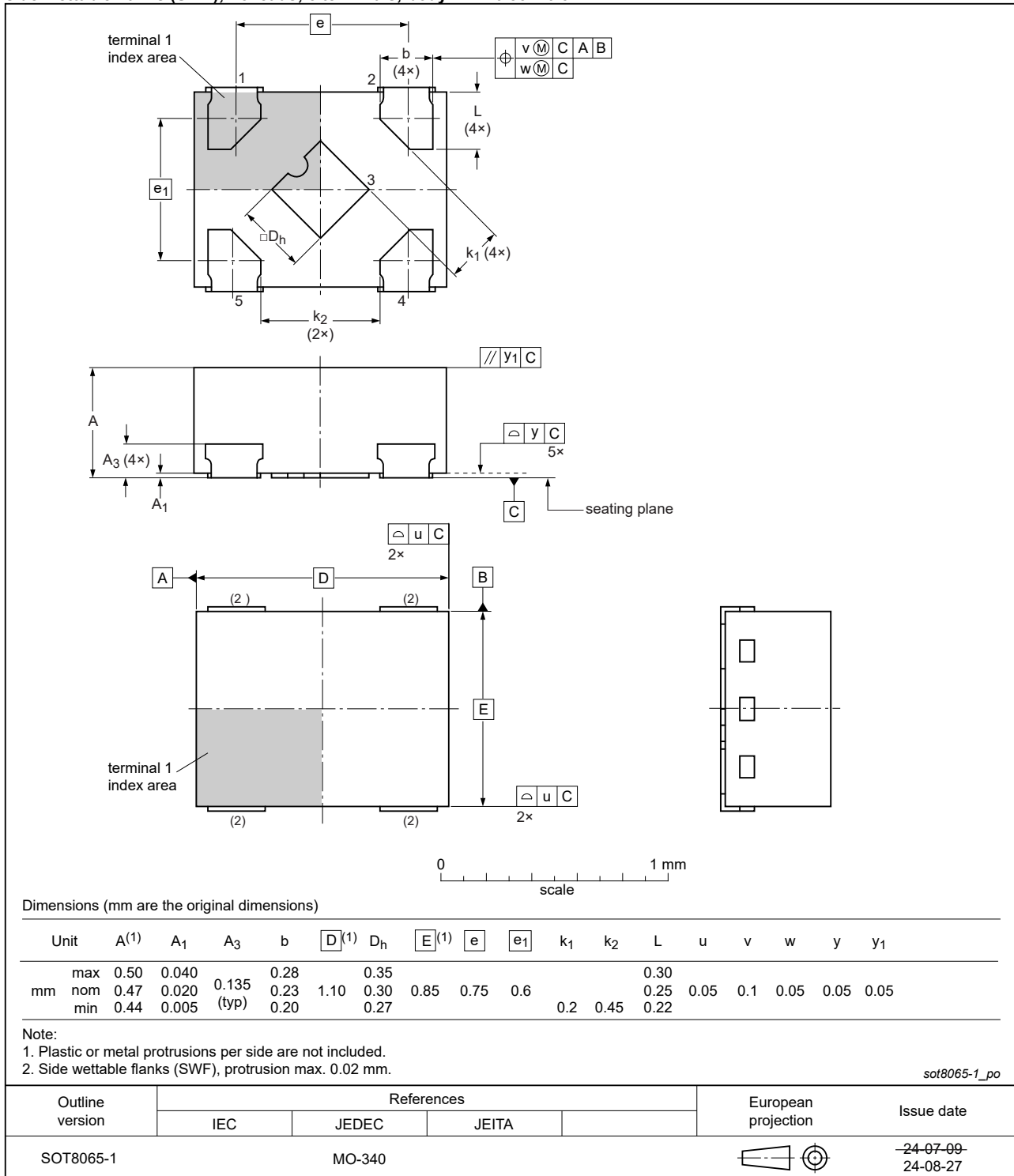


Fig. 7. Package outline SOT753 (SC-74A)

**XSON5: Plastic thermal enhanced extremely thin small outline package with side-wettable flanks (SWF); no leads; 5 terminals; body 1.1 × 0.85 × 0.5 mm**

SOT8065-1



**Fig. 8. Package outline SOT8065-1 (XSON5)**

## 13. Abbreviations

Table 11. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council

## 14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC1G09 v.5	20240919	Product data sheet	-	74AHC1G09 v.4
Modifications:	<ul style="list-style-type: none"> <li>Type number 74AHC1G09GZ (SOT8065-1/XSON5) added.</li> </ul>			
74AHC1G09 v.4	20231005	Product data sheet	-	74AHC1G09 v.3
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li> </ul>			
74AHC1G09 v.3	20220111	Product data sheet	-	74AHC1G09 v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> <li>SOT353-1 (TSSOP5) package outline drawing has changed.</li> <li><a href="#">Section 8</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> </ul>			
74AHC1G09 v.2	20071218	Product data sheet	-	74AHC1G09 v.1
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Package SOT753 added to <a href="#">Section 3</a>, <a href="#">Section 4</a> and <a href="#">Section 12</a>.</li> <li>Quick reference data section removed.</li> </ul>			
74AHC1G09 v.1	20050926	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
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Date of release: 19 September 2024

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