

# 74AHCT00PW-Q100J Datasheet

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DiGi Electronics Part Number	74AHCT00PW-Q100J-DG
Manufacturer	<a href="#">Nexperia USA Inc.</a>
Manufacturer Product Number	74AHCT00PW-Q100J
Description	IC GATE NAND 4CH 2-INP 14TSSOP
Detailed Description	NAND Gate IC 4 Channel 14-TSSOP



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## Purchase and inquiry

**Manufacturer Product Number:**

74AHCT00PW-Q100J

**Series:**

74AHCT

**Logic Type:**

NAND Gate

**Number of Inputs:**

2

**Voltage - Supply:**

4.5V ~ 5.5V

**Current - Output High, Low:**

8mA, 8mA

**Input Logic Level - High:**

2V

**Operating Temperature:**

-40°C ~ 125°C

**Qualification:**

AEC-Q100

**Supplier Device Package:**

14-TSSOP

**Base Product Number:**

74AHCT00

**Manufacturer:**

Nexperia USA Inc.

**Product Status:**

Active

**Number of Circuits:**

4

**Features:**

-

**Current - Quiescent (Max):**2  $\mu$ A**Input Logic Level - Low:**

0.8V

**Max Propagation Delay @ V, Max CL:**

7.9ns @ 5V, 50pF

**Grade:**

Automotive

**Mounting Type:**

Surface Mount

**Package / Case:**

14-TSSOP (0.173", 4.40mm Width)

## Environmental & Export classification

**RoHS Status:**

ROHS3 Compliant

**REACH Status:**

REACH Unaffected

**HTSUS:**

8542.39.0001

**Moisture Sensitivity Level (MSL):**

1 (Unlimited)

**ECCN:**

EAR99

# 74AHC00-Q100; 74AHCT00-Q100

## Quad 2-input NAND gate

Rev. 4 — 15 January 2024

Product data sheet

## 1. General description

The 74AHC00-Q100; 74AHCT00-Q100 are quad 2-input NAND gates. Inputs are overvoltage tolerant. This feature allows the use of these devices as translators in mixed voltage environments.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 2.0 V to 5.5 V
- Input levels:
  - For 74AHC00-Q100: CMOS level
  - For 74AHCT00-Q100: TTL level
- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- CMOS low power dissipation
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level A
- Multiple package options
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

## 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
<a href="#">74AHC00D-Q100</a> <a href="#">74AHCT00D-Q100</a>	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	<a href="#">SOT108-1</a>
<a href="#">74AHC00PW-Q100</a> <a href="#">74AHCT00PW-Q100</a>	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	<a href="#">SOT402-1</a>
<a href="#">74AHC00BQ-Q100</a> <a href="#">74AHCT00BQ-Q100</a>	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	<a href="#">SOT762-1</a>

## 4. Functional diagram

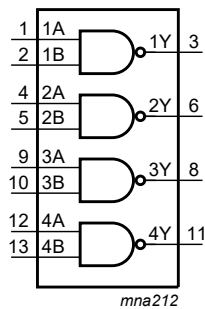


Fig. 1. Logic symbol

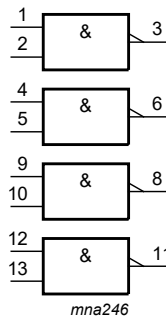


Fig. 2. IEC logic symbol

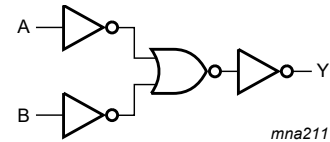
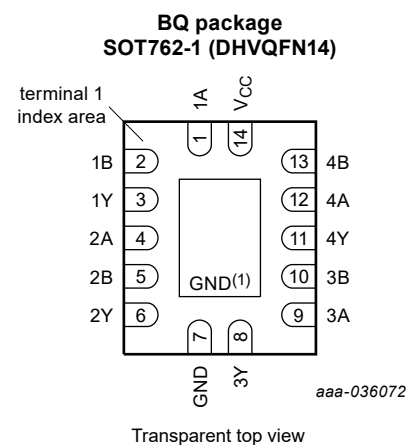
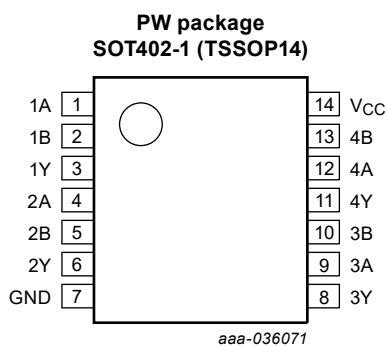
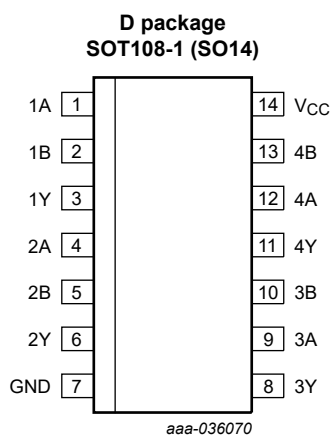


Fig. 3. Logic diagram (one gate)

## 5. Pinning information

### 5.1. Pinning



(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A	1, 4, 9, 12	data inputs
1B, 2B, 3B, 4B	2, 5, 10, 13	data inputs
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data outputs
GND	7	ground (0 V)
V <sub>CC</sub>	14	supply voltage

## 6. Functional description

**Table 3. Function selection**

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input		Output
nA	nB	nY
L	X	H
X	L	H
H	H	L

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		-0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < -0.5$ V [1]	-20	-	mA
$I_{OK}$	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V [1]	-20	+20	mA
$I_O$	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5$ V)	-25	+25	mA
$I_{CC}$	supply current		-	+75	mA
$I_{GND}$	ground current		-75	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT108-1 (SO14) package:  $P_{tot}$  derates linearly with 10.1 mW/K above 100 °C.

For SOT402-1 (TSSOP14) package:  $P_{tot}$  derates linearly with 7.3 mW/K above 81 °C.

For SOT762-1 (DHVQFN14) package:  $P_{tot}$  derates linearly with 9.6 mW/K above 98 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74AHC00-Q100			74AHCT00-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
$V_{CC}$	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
$V_I$	input voltage		0	-	5.5	0	-	5.5	V
$V_O$	output voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.3$ V $\pm$ 0.3 V	-	-	100	-	-	-	ns/V
		$V_{CC} = 5.0$ V $\pm$ 0.5 V	-	-	20	-	-	20	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74AHC00-Q100</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V <sub>CC</sub> = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V <sub>CC</sub> = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V <sub>CC</sub> = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -50 µA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -50 µA; V <sub>CC</sub> = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I <sub>O</sub> = -50 µA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 50 µA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 µA; V <sub>CC</sub> = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 50 µA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
		I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	2.0	-	20	-
C <sub>I</sub>	input capacitance	V <sub>I</sub> = V <sub>CC</sub> or GND	-	3.0	10	-	10	-	10	pF
<b>74AHCT00-Q100</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = -50 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -8.0 mA	3.94	-	-	3.80	-	3.70	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 50 µA	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	2.0	-	20	-	40	µA

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
$\Delta I_{CC}$	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}$ ; $I_O = 0 \text{ A}$ ; other pins at $V_{CC}$ or GND; $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	1.35	-	1.5	-	1.5	mA
$C_I$	input capacitance	$V_I = V_{CC}$ or GND	-	3.0	10	-	10	-	10	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
<b>74AHC00-Q100</b>										
$t_{pd}$	propagation delay	nA, nB to nY; see Fig. 4 [2]								
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$								
		$C_L = 15 \text{ pF}$	-	4.5	7.9	1.0	9.5	1.0	10.0	ns
		$C_L = 50 \text{ pF}$	-	6.0	11.4	1.0	13.0	1.0	14.5	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$								
		$C_L = 15 \text{ pF}$	-	3.2	5.5	1.0	6.5	1.0	7.0	ns
		$C_L = 50 \text{ pF}$	-	4.5	7.5	1.0	8.5	1.0	9.5	ns
$C_{PD}$	power dissipation capacitance	$C_L = 50 \text{ pF}$ ; $f_i = 1 \text{ MHz}$ ; $V_I = \text{GND to } V_{CC}$ [3]	-	7.0	-	-	-	-	-	pF
<b>74AHCT00-Q100</b>										
$t_{pd}$	propagation delay	nA, nB to nY; see Fig. 4 [2]								
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$								
		$C_L = 15 \text{ pF}$	-	3.3	6.9	1.0	8.0	1.0	9.0	ns
		$C_L = 50 \text{ pF}$	-	4.5	7.9	1.0	9.0	1.0	10.0	ns
$C_{PD}$	power dissipation capacitance	$C_L = 50 \text{ pF}$ ; $f_i = 1 \text{ MHz}$ ; $V_I = \text{GND to } V_{CC}$ [3]	-	7.0	-	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage ( $V_{CC} = 3.3 \text{ V}$  and  $V_{CC} = 5.0 \text{ V}$ ).

[2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .

[3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

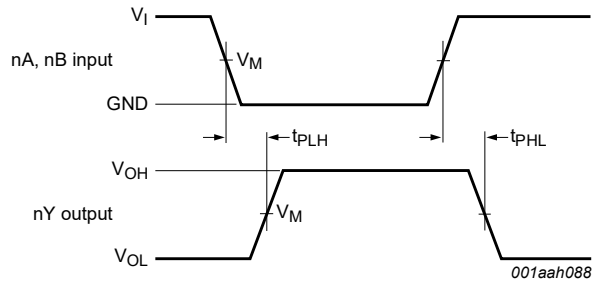
$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V;

$N$  = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

## 10.1. Waveforms



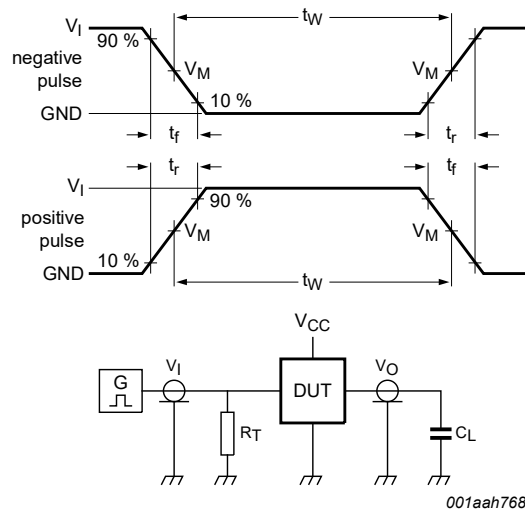
Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig. 4. Input to output propagation delays**

**Table 8. Measurement points**

Type	Input	Output
	$V_M$	$V_M$
74AHC00-Q100	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74AHCT00-Q100	1.5 V	$0.5 \times V_{CC}$



Test data is given in [Table 9](#).

Definitions test circuit:

$R_T$  = termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = load capacitance including jig and probe capacitance.

**Fig. 5. Test circuit for measuring switching times**

**Table 9. Test data**

Type	Input		Load	Test
	$V_I$	$t_r, t_f$	$C_L$	
74AHC00-Q100	$V_{CC}$	$\leq 3.0$ ns	15 pF, 50 pF	$t_{PLH}, t_{PHL}$
74AHCT00-Q100	3.0 V	$\leq 3.0$ ns	15 pF, 50 pF	$t_{PLH}, t_{PHL}$



## 11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

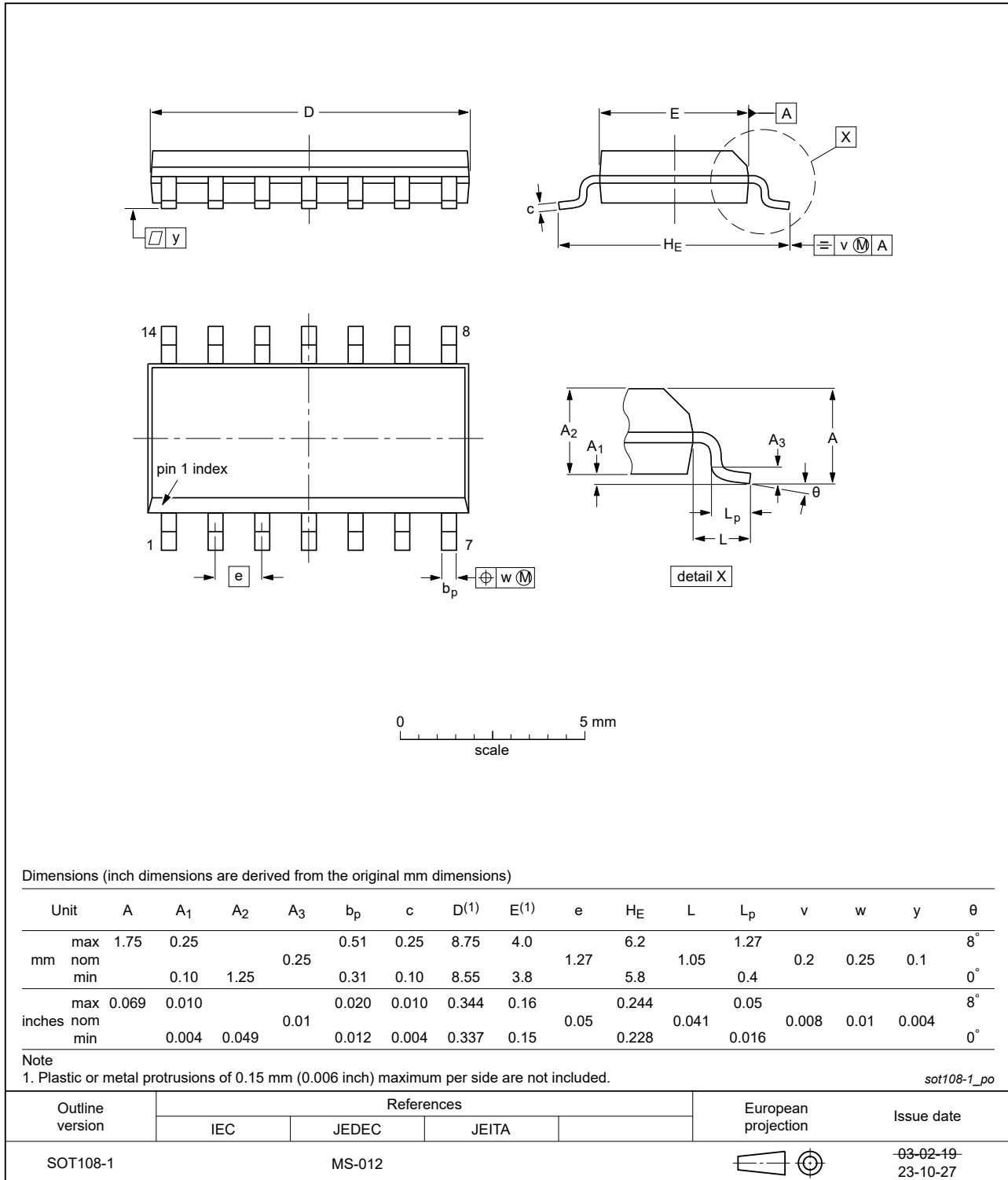


Fig. 6. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

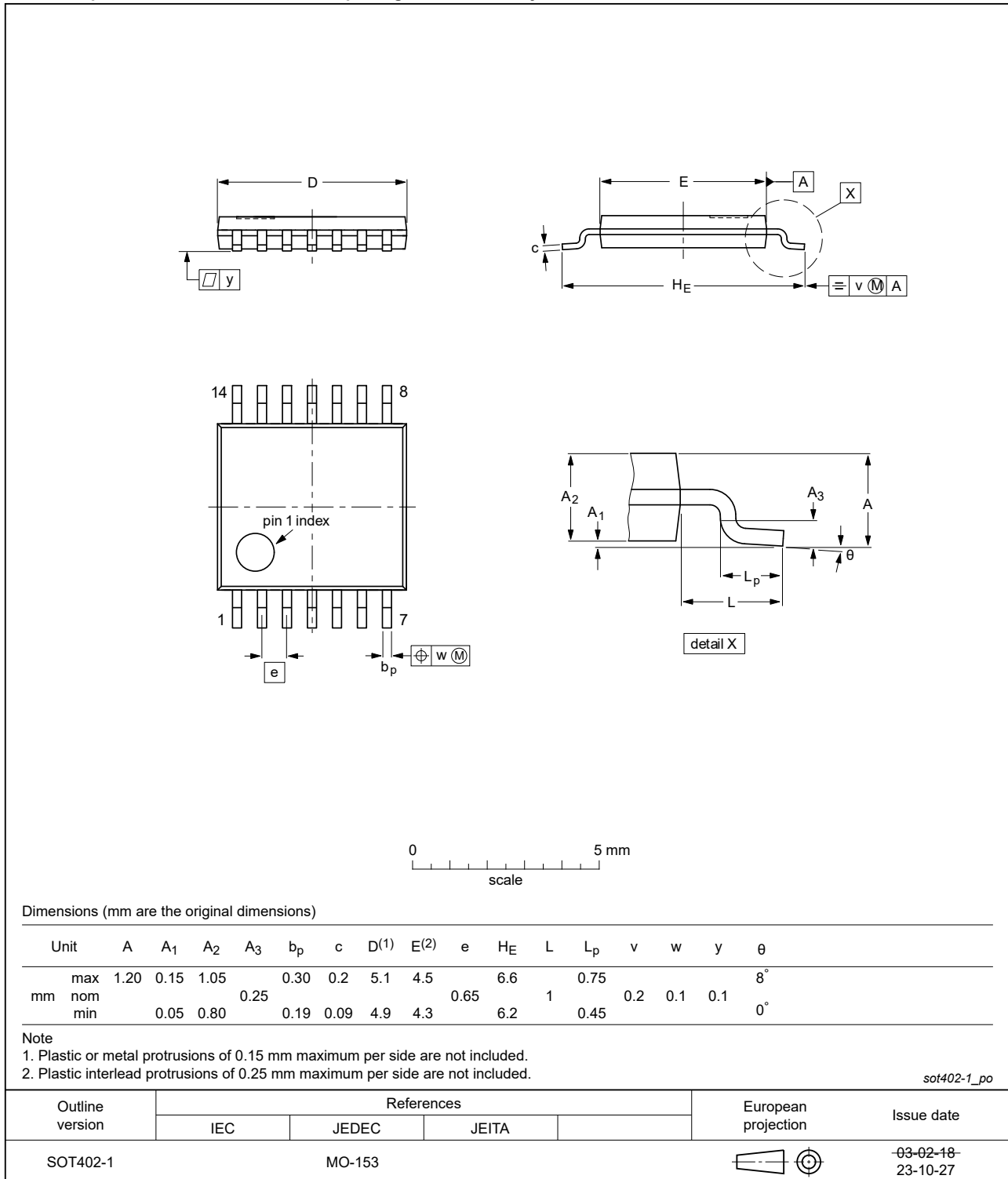


Fig. 7. Package outline SOT402-1 (TSSOP14)



## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charge Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT00_Q100 v.4	20240115	Product data sheet	-	74AHC_AHCT00_Q100 v.3
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li> <li><a href="#">Fig. 6</a>, <a href="#">Fig. 7</a>: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.</li> </ul>			
74AHC_AHCT00_Q100 v.3	20230901	Product data sheet	-	74AHC_AHCT00_Q100 v.2
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li> </ul>			
74AHC_AHCT00_Q100 v.2	20200526	Product data sheet	-	74AHC_AHCT00_Q100 v.1
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> <li><a href="#">Table 4</a>: Derating values for <math>P_{tot}</math> total power dissipation have been updated.</li> <li>Package outline drawing of SOT762-1 (<a href="#">Fig. 8</a>) updated.</li> </ul>			
74AHC_AHCT00_Q100 v.1	20130416	Product specification	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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Date of release: 15 January 2024

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