74AHCV07APWJ Datasheet

DiGi Electronics Part Number	74AHCV07APWJ-DG
Manufacturer	Nexperia USA Inc.
Manufacturer Product Number	74AHCV07APWJ
Description	IC BUFFER INVERT 5.5V 14TSSOP
Detailed Description	Buffer, Inverting 1 Element 6 Bit per Element Open Drain Output 14-TSSOP

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
74AHCV07APWJ	Nexperia USA Inc.
Series:	Product Status:
74AHCV	Active
Logic Type:	Number of Elements:
Buffer, Inverting	1
Number of Bits per Element:	Input Type:
6	-
Output Type:	Current - Output High, Low:
Open Drain	-, 16mA
Voltage - Supply:	Operating Temperature:
1.8V ~ 5.5V	-40°C ~ 125°C (TA)
Mounting Type:	Package / Case:
Surface Mount	14-TSSOP (0.173", 4.40mm Width)
Supplier Device Package:	Base Product Number:
14-TSSOP	74AHCV07

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8542.39.0001	

74AHCV07A
Hex buffer with open-drain outputs
Rev. 3 — 23 January 2024   **Product data sheet**

1. General description

The 74AHCV07A is a hex buffer with open-drain outputs. The outputs are open-drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions.

Inputs are overvoltage tolerant. This feature allows the use of these devices as translators in mixed voltage environments.

The data (nA) inputs include Schmitt trigger inputs capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.
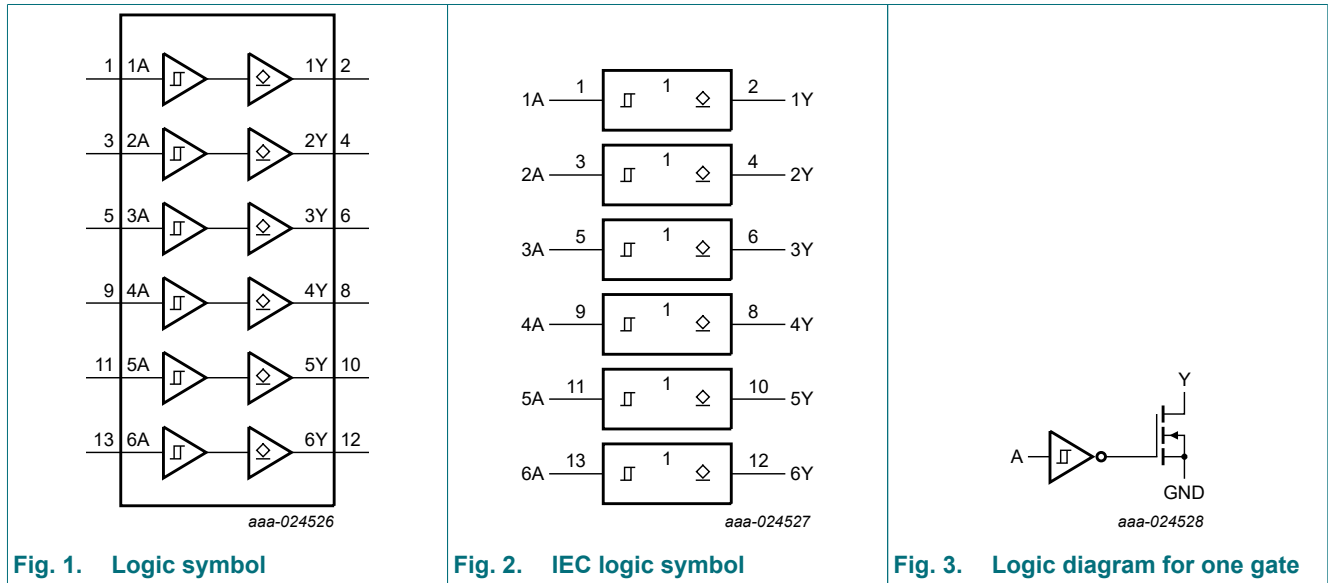
2. Features and benefits

- Wide supply voltage range from 1.8 V to 5.5 V
- Typical t_{PZL} of 3 ns at 5 V
- Typical $V_{OL(p)}$ < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C
- Supports mixed-mode voltage operation on all ports
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 250 mA per JESD 78 Class II
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 3000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 2000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

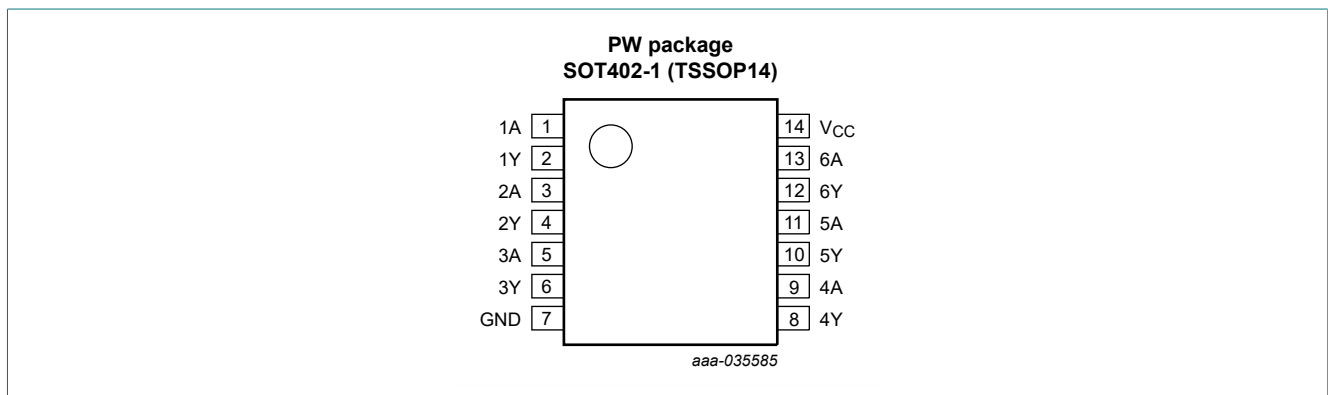| Type number	Package			
	Temperature range	Name	Description	Version
74AHCV07APW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

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4. Functional diagram

Fig. 1.   Logic symbol

Fig. 2.   IEC logic symbol

Fig. 3.   Logic diagram for one gate

5. Pinning information

5.1. Pinning

PW package
SOT402-1 (TSSOP14)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V_{CC}	14	supply voltage

6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state

Input	Output
nA	**nY**
L	L
H	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+7.0	V
V_I	input voltage		[1]	-0.5	+7.0	V
V_O	output voltage	output LOW state, 3-state or power-down	[2]	-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < 0$ V		-50	-	mA
I_{OK}	output clamping current	$V_O < 0$ V		-50	-	mA
I_O	output current	$V_O = 0$ V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			-100	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[3]	-	500	mW

[1]   The minimum input voltage ratings may be exceeded if the input current ratings are observed.
[2]   The output voltage ratings may be exceeded if the output current ratings are observed.
[3]   For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.8	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	output LOW state, 3-state or power-down	0	-	5.5	V
T_{amb}	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.3$ V to 2.7 V	-	-	50	ms/V
		$V_{CC} = 3.0$ V to 3.6 V	-	-	20	ms/V
		$V_{CC} = 4.5$ V to 5.5 V	-	-	1	ms/V

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9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{T+}	positive-going threshold voltage	V_{CC} = 1.8 V	-	-	1.65	-	1.65	-	1.65	V
		V_{CC} = 2.3 V	-	-	1.85	-	1.85	-	1.85	V
		V_{CC} = 3.0 V	-	-	2.2	-	2.2	-	2.2	V
		V_{CC} = 4.5 V	-	-	3.15	-	3.15	-	3.15	V
		V_{CC} = 5.5 V	-	-	3.85	-	3.85	-	3.85	V
V_{T-}	negative-going threshold voltage	V_{CC} = 1.8 V	0.15	-	-	0.15	-	0.15	-	V
		V_{CC} = 2.3 V	0.45	-	-	0.45	-	0.45	-	V
		V_{CC} = 3.0 V	0.9	-	-	0.9	-	0.9	-	V
		V_{CC} = 4.5 V	1.35	-	-	1.35	-	1.35	-	V
		V_{CC} = 5.5 V	1.65	-	-	1.65	-	1.65	-	V
V_H	hysteresis voltage	V_{CC} = 1.8 V	0.15	-	1.05	0.15	1.05	0.15	1.05	V
		V_{CC} = 2.3 V	0.2	-	1.1	0.2	1.1	0.2	1.1	V
		V_{CC} = 3.0 V	0.3	-	1.2	0.3	1.2	0.3	1.2	V
		V_{CC} = 4.5 V	0.4	-	1.4	0.4	1.4	0.4	1.4	V
		V_{CC} = 5.5 V	0.5	-	1.6	0.5	1.6	0.5	1.6	V
V_{OL}	LOW-level output voltage	$V_I = V_{T+}$ or V_{T-}								
		I_O = 50 µA; V_{CC} = 1.8 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 50 µA; V_{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 50 µA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 8 mA; V_{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.44	V
		I_O = 16 mA; V_{CC} = 4.5 V	-	-	0.44	-	0.55	-	0.55	V
I_{OZ}	OFF-state output current	V_{CC} = 5.5 V; $V_I = V_{IH}$ or V_{IL}; V_O = GND to 5.5 V	-	-	±0.25	-	±2.5	-	±2.5	µA
I_{OFF}	power-off leakage current	V_I or V_O = GND to 5.5 V; V_{CC} = 0 V	-	-	0.5	-	5	-	5	µA
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 0 V to 5.5 V	-	-	±0.1	-	±1	-	±1	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	2	-	20	-	20	µA

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9.1. Transfer characteristics waveforms
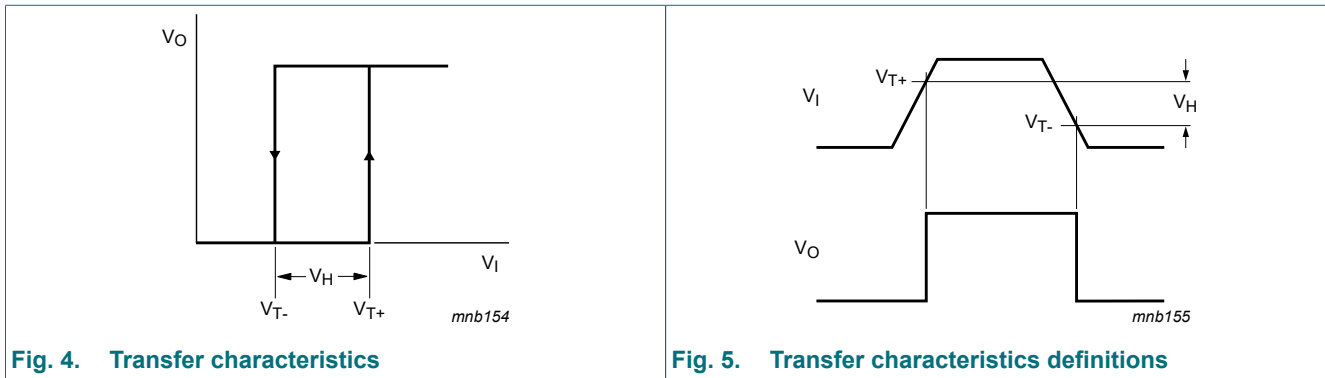
Fig. 4.   Transfer characteristics

Fig. 5.   Transfer characteristics definitions

a. V_CC = 3.0 V
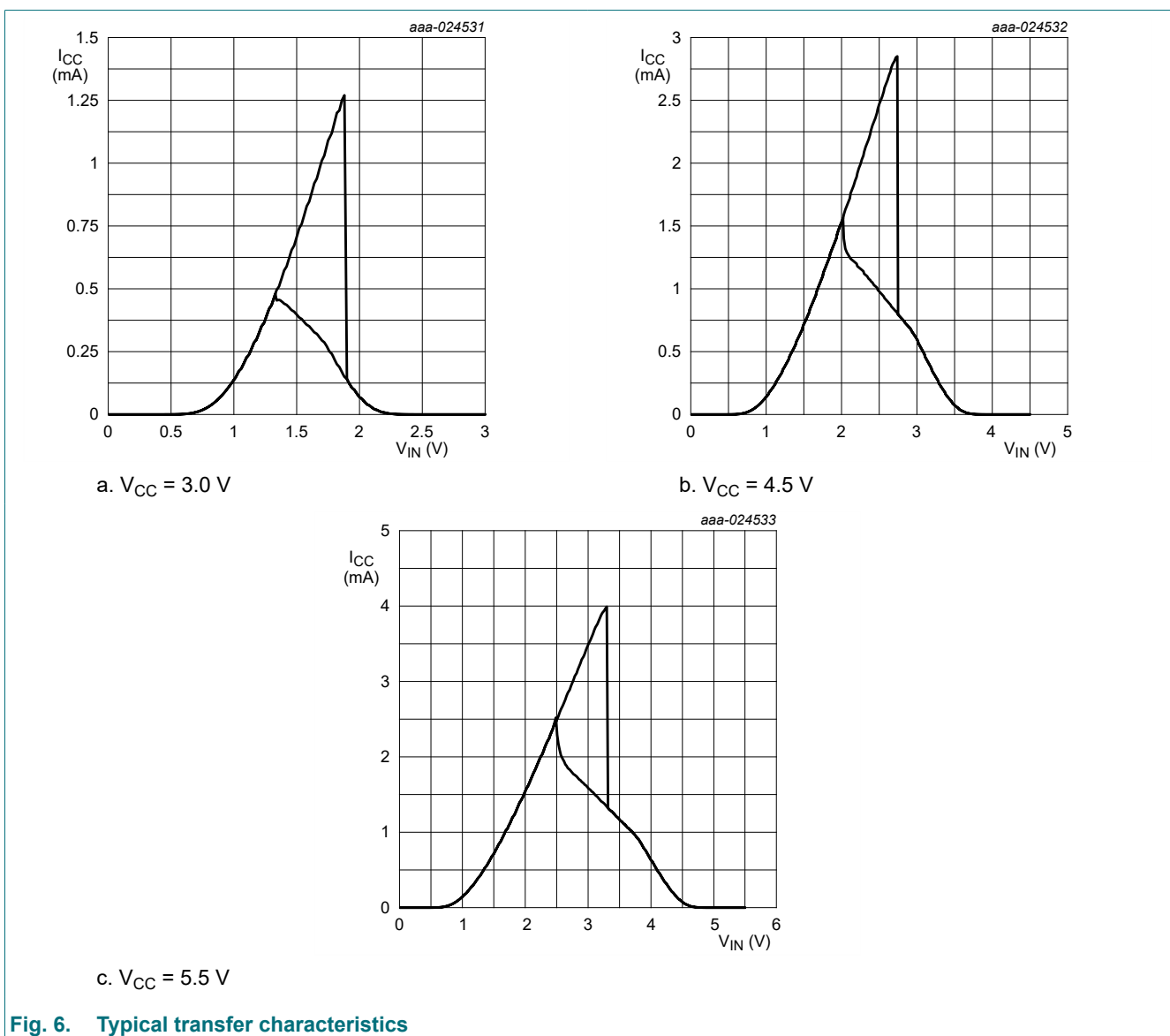
b. V_CC = 4.5 V

c. V_CC = 5.5 V

Fig. 6.   Typical transfer characteristics

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10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V. For test circuit see Fig. 8.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
t_{PZL}	OFF-state to LOW propagation delay	nA to nY; see Fig. 7								
		V_{CC} = 2.3 V to 2.7 V								
		C_L = 15 pF	-	5.2	10.4	1	13	1	13.9	ns
		C_L = 50 pF	-	7.5	15.2	1	18	1	19.6	ns
		V_{CC} = 3.0 V to 3.6 V								
		C_L = 15 pF	-	3.9	7.1	1	8.5	1	9.2	ns
		C_L = 50 pF	-	5.8	10.6	1	12	1	13	ns
		V_{CC} = 4.5 V to 5.5 V								
		C_L = 15 pF	-	3	5.5	1	6.5	1	7.0	ns
		C_L = 50 pF	-	4.6	7.5	1	8.5	1	9.2	ns
t_{PLZ}	LOW to OFF-state propagation delay	nA to nY; see Fig. 7								
		V_{CC} = 2.3 V to 2.7 V								
		C_L = 15 pF	-	5.8	9.1	1	11.1	1	11.6	ns
		C_L = 50 pF	-	10.4	15.2	1	18	1	18.6	ns
		V_{CC} = 3.0 V to 3.6 V								
		C_L = 15 pF	-	4.7	6.5	1	7.6	1	8.1	ns
		C_L = 50 pF	-	8.1	10.6	1	12	1	12.5	ns
		V_{CC} = 4.5 V to 5.5 V								
		C_L = 15 pF	-	3.8	5	1	5.8	1	6.1	ns
		C_L = 50 pF	-	6.0	7.5	1	8.5	1	8.8	ns
C_I	input capacitance	V_I = V_{CC} or GND; V_{CC} = 3.3 V	-	2	6	-	6	-	6	pF
C_O	output capacitance	V_O = V_{CC} or GND; V_{CC} = 3.3 V	-	5	-	-	-	-	-	pF
C_{PD}	power dissipation capacitance	per buffer; C_L = 0 pF; [2] f = 10 MHz; V_{CC} = 5 V; V_I = GND to V_{CC}	-	3	-	-	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 2.5 V, 3.3 V, and 5 V respectively, unless otherwise specified.

[2] C_{PD} is used to determine the dynamic power dissipation P_D (µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;
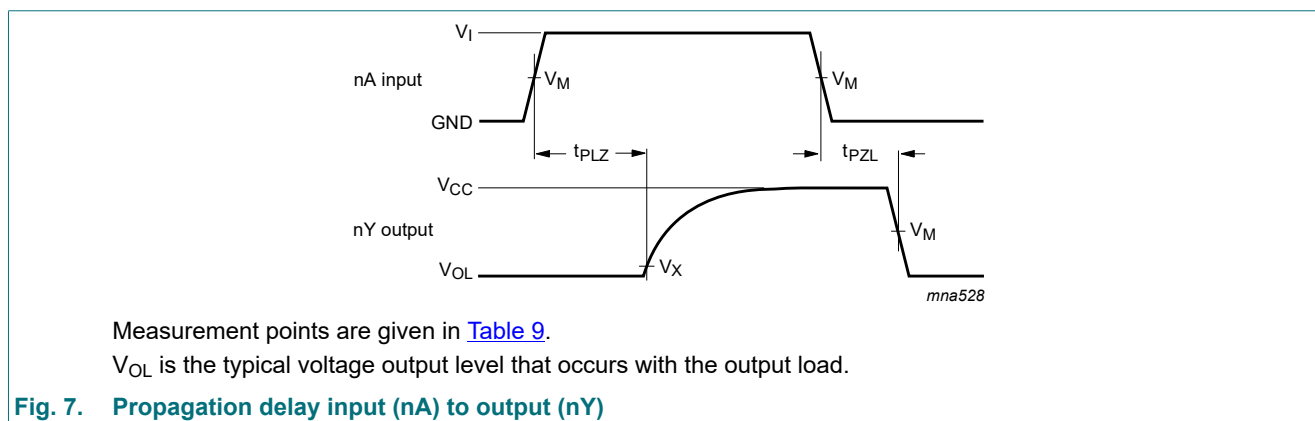
V_{CC} = supply voltage in V.

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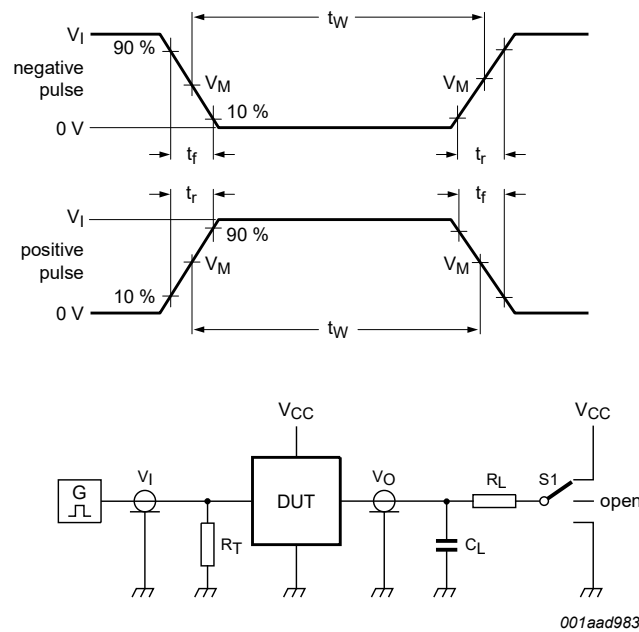
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Table 8. Noise characteristics

GND = 0 V. For test circuit see Fig. 8.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			Unit
			Min	Typ	Max	
V_{CC} = 3.3 V; C_L = 50 pF						
$V_{OL(p)}$	LOW-level output voltage (peak)		-	0.3	0.8	V
$V_{OL(v)}$	LOW-level output voltage (valley)		-0.8	-0.1	-	V
$V_{IH(AC)}$	AC HIGH-level input voltage (dynamic)		2.31	-	-	V
$V_{IL(AC)}$	AC LOW-level input voltage (dynamic)		-	-	0.99	V
V_{CC} = 5.0 V; C_L = 50 pF						
$V_{OL(p)}$	LOW-level output voltage (peak)		-	0.6	-	V
$V_{OL(v)}$	LOW-level output voltage (valley)		-	-0.4	-	V
$V_{IH(AC)}$	AC HIGH-level input voltage (dynamic)		3.5	-	-	V
$V_{IL(AC)}$	AC LOW-level input voltage (dynamic)		-	-	1.5	V

10.1. Waveforms and test circuit

Measurement points are given in Table 9.

V_{OL} is the typical voltage output level that occurs with the output load.

Fig. 7. Propagation delay input (nA) to output (nY)

Table 9. Measurement points

Input	Output	
V_M	V_M	V_X
0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.3 V

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Test data is given in Table 10.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

C_L = Load capacitance including jig and probe capacitance;

R_L = Load resistor;

S1 = Test selection switch.

Fig. 8. Test circuit for measuring switching times

Table 10. Test data

Input		Load			S1 position
V_I	t_r, t_f	C_L	R_L		t_{PLZ}, t_{PZL}
GND to V_{CC}	3.0 ns	15 pF, 50 pF	1 kΩ		V_{CC}

11. Package outline

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm   **SOT402-1**
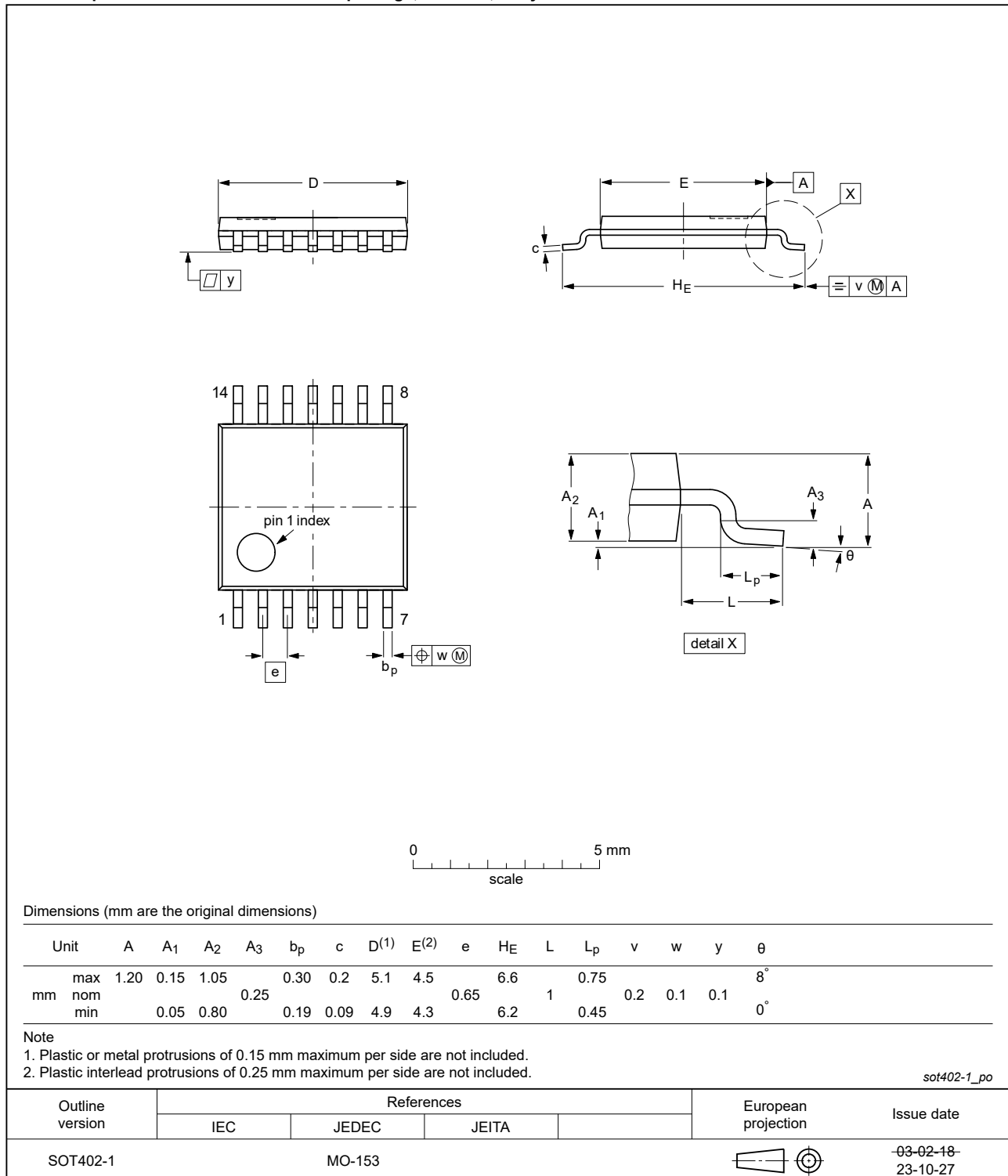

Dimensions (mm are the original dimensions)

Unit		A	A1	A2	A3	bp	c	D(1)	E(2)	e	HE	L	Lp	v	w	y	θ
mm	max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
	nom				0.25					0.65		1		0.2	0.1	0.1	
	min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot402-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 9.   Package outline SOT402-1 (TSSOP14)

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12. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charge Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHCV07A v.3	20240123	Product data sheet	-	74AHCV07A v.2
Modifications:		• Fig. 9: Aligned TSSOP package outline drawings to JEDEC MO-153.		
74AHCV07A v.2	20230927	Product data sheet	-	74AHCV07A v.1
Modifications		• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 2: ESD specification updated according to the latest JEDEC standard. • Table 4: Derating values for P_{tot} total power dissipation updated.		
74AHCV07A v.1	20161219	Product data sheet	-	-

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14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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