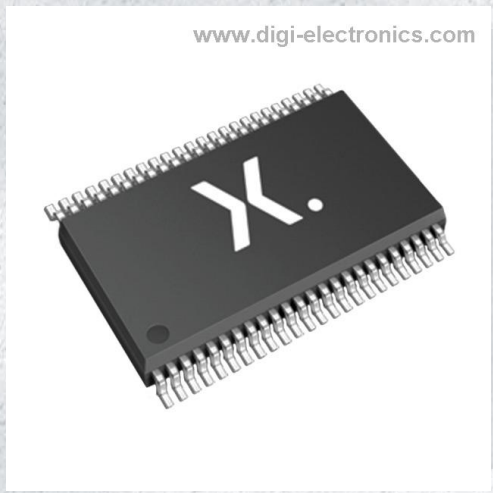
74ALVC16245DGG,512 Datasheet



https://www.DiGi-Electronics.com

DiGi Electronics Part Number	74ALVC16245DGG,512-DG
Manufacturer	Nexperia USA Inc.
Manufacturer Product Number	74ALVC16245DGG,512
Description	IC TXRX NON-INVERT 3.6V 48TSSOP
Detailed Description	Transceiver, Non-Inverting 2 Element 8 Bit per Element 3-State Output 48-TSSOP

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
74ALVC16245DGG,512	Nexperia USA Inc.
Series:	Product Status:
74ALVC	Obsolete
Logic Type:	Number of Elements:
Transceiver, Non-Inverting	2
Number of Bits per Element:	Input Type:
8	-
Output Type:	Current - Output High, Low:
3-State	24mA, 24mA
Voltage - Supply:	Operating Temperature:
1.2V ~ 3.6V	-40°C ~ 85°C (TA)
Mounting Type:	Package / Case:
Surface Mount	48-TFSOP (0.240", 6.10mm Width)
Supplier Device Package:	Base Product Number:
48-TSSOP	74ALVC16245

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8542.39.0001	

74ALVC16245; 74ALVCH16245

16-bit transceiver with direction pin; 3-state

Rev. 8 — 26 June 2024 Product data sheet

1. General description

The 74ALVC16245; 74ALVCH16245 is a 16-bit transceiver with 3-state outputs. The device can be used as two 8-bit transceivers or one 16-bit transceiver. The device features two output enables (1OE and 2OE) each controlling eight outputs, and two send/receive (1DIR and 2DIR) inputs for direction control. A HIGH on nOE causes the outputs to assume a high-impedance OFF-state.

Schmitt trigger action on all inputs makes the device tolerant of slow rise and fall times.

This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

The 74ALVCH16245 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

2. Features and benefits

- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins for minimum noise and ground bounce
- Overvoltage tolerant inputs to 5.5 V(74ALVC16245 only)
- Direct interface with TTL levels
- I_{OFF} circuitry provides partial Power-down mode operation
- Bushold on all data inputs(74ALVCH16245 only)
- Output drive capability 50 Ω transmission lines at 85 °C
- Current drive ±24 mA at 3.0 V
- Latch-up performance exceeds 2500 mA per JESD 78 Class II.A
- Complies with JEDEC standards:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ALVC16245DGG 74ALVCH16245DGG	-40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1

4. Functional diagram

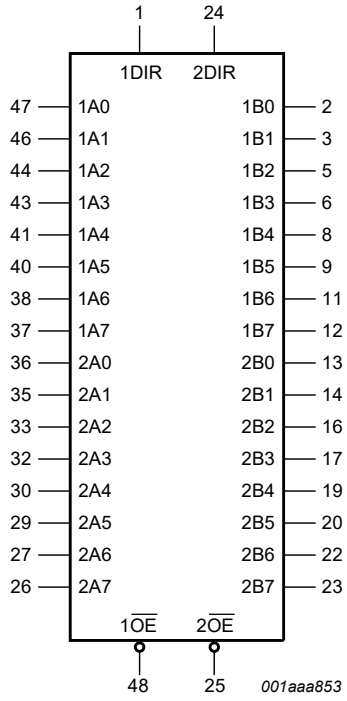


Fig. 1. Logic symbol

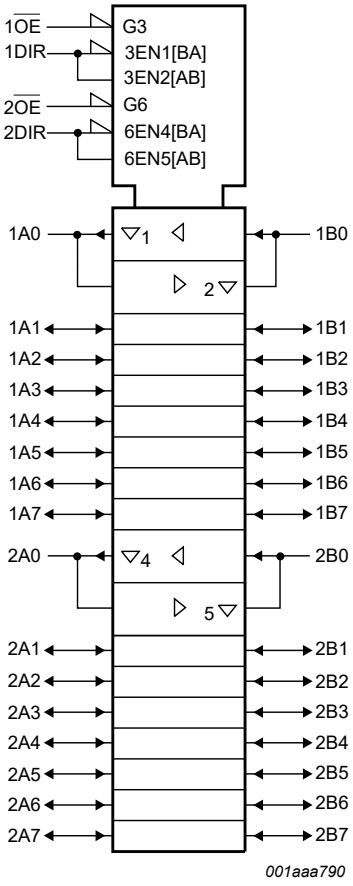


Fig. 2. IEC logic symbol

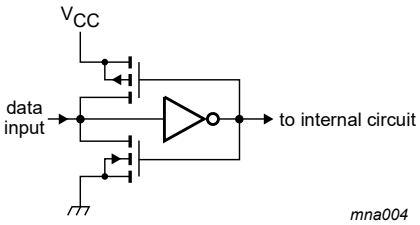


Fig. 3. Bushold circuit

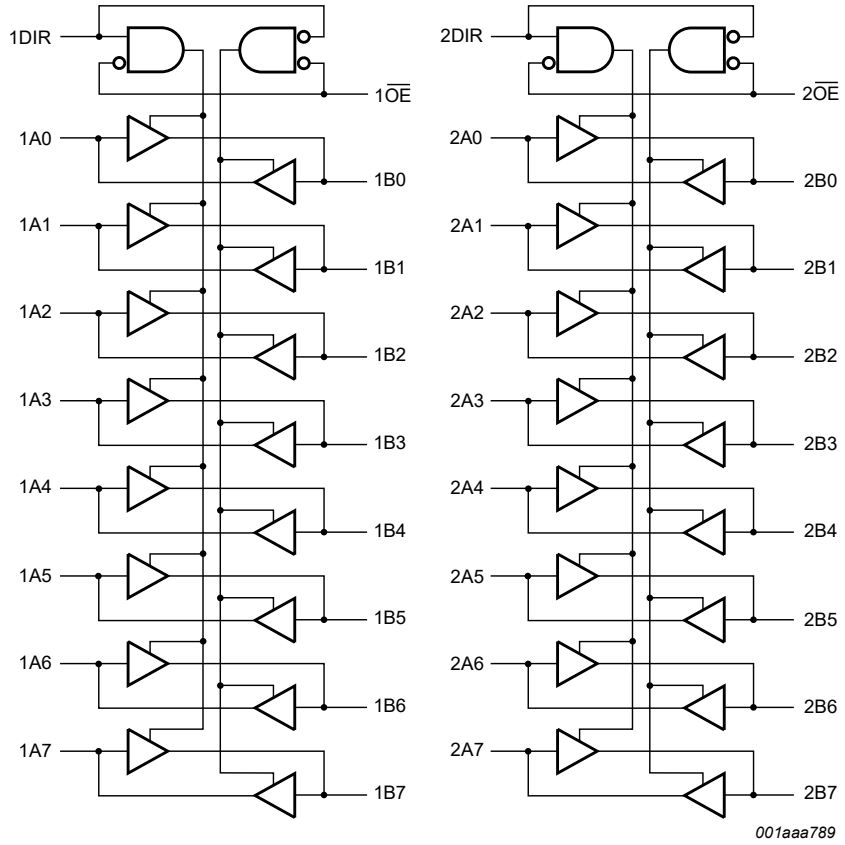
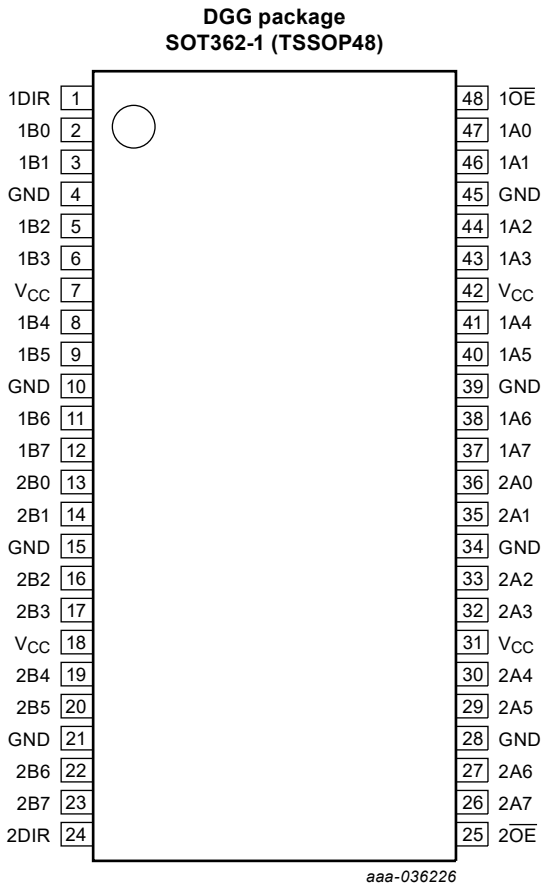


Fig. 4. Logic diagram

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1DIR, 2DIR	1, 24	direction control inputs
1B0, 1B1, 1B2, 1B3, 1B4, 1B5, 1B6, 1B7	2, 3, 5, 6, 8, 9, 11, 12	data output or input
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V_{CC}	7, 18, 31, 42	positive supply voltage
2B0, 2B1, 2B2, 2B3, 2B4, 2B5, 2B6, 2B7	13, 14, 16, 17, 19, 20, 22, 23	data output or input
$1\overline{OE}$, $2\overline{OE}$	48, 25	output enable input (active LOW)
2A0, 2A1, 2A2, 2A3, 2A4, 2A5, 2A6, 2A7	36, 35, 33, 32, 30, 29, 27, 26	data input or output
1A0, 1A1, 1A2, 1A3, 1A4, 1A5, 1A6, 1A7	47, 46, 44, 43, 41, 40, 38, 37	data input or output

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Input		Input or output	
$n\overline{OE}$	nDIR	nAn	nBn
L	L	output nAn = nBn	input
L	H	input	output nBn = nAn
H	X	Z	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+4.6	V
V_I	input voltage	74ALVCH16245; data inputs	[1]	-0.5	V_{CC} + 0.5	V
		74ALVC16245; data inputs	[1]	-0.5	+4.6	V
		control pins	[1]	-0.5	+4.6	V
V_O	output voltage		[1]	-0.5	V_{CC} + 0.5	V
I_{IK}	input clamping current	V_I < 0 V		-50	-	mA
I_{OK}	output clamping current	V_O > V_{CC} or V_O < 0 V		-	±50	mA
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			-100	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +85 °C		-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	maximum speed performance				
		C_L = 30 pF	2.3	-	2.7	V
		C_L = 50 pF	3.0	-	3.6	V
		low-voltage applications	1.2	-	3.6	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.3 V to 3.0 V	-	-	20	ns/V
		V_{CC} = 3.0 V to 3.6 V	-	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			
			Min	Typ[1]	Max	Unit
V_{IH}	HIGH-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7	1.2	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	1.5	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.3 V to 2.7 V	-	1.2	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	1.5	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = -100 µA; V_{CC} = 2.3 V to 3.6 V	V_{CC} - 0.2	V_{CC}	-	V
		I_O = -6 mA; V_{CC} = 2.3 V	V_{CC} - 0.3	V_{CC} - 0.08	-	V
		I_O = -12 mA; V_{CC} = 2.3 V	V_{CC} - 0.6	V_{CC} - 0.26	-	V
		I_O = -12 mA; V_{CC} = 2.7 V	V_{CC} - 0.5	V_{CC} - 0.14	-	V
		I_O = -12 mA; V_{CC} = 3.0 V	V_{CC} - 0.6	V_{CC} - 0.09	-	V
		I_O = -24 mA; V_{CC} = 3.0 V	V_{CC} - 1.0	V_{CC} - 0.28	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 100 µA; V_{CC} = 2.3 V to 3.6 V	-	GND	0.20	V
		I_O = 6 mA; V_{CC} = 2.3 V	-	0.07	0.40	V
		I_O = 12 mA; V_{CC} = 2.3 V	-	0.15	0.70	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	0.14	0.40	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	0.27	0.55	V
I_I	input leakage current	V_{CC} = 2.3 V to 3.6 V; V_I = V_{CC} or GND	-	0.1	5	µA
I_{OZ}	OFF-state output current	V_{CC} = 2.3 V to 3.6 V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND	-	0.1	10	µA
I_{CC}	supply current	V_{CC} = 2.3 V to 3.6 V; V_I = V_{CC} or GND; I_O = 0 A	-	0.2	40	µA
ΔI_{CC}	additional supply current	74ALVCH16245; per data I/O pin; V_{CC} = 2.3 V to 3.6 V; V_I = V_{CC} - 0.6 V; I_O = 0 A	-	150	750	µA
I_{BHL}	bus hold LOW current	V_{CC} = 2.3 V; V_I = 0.7 V [2]	45	-	-	µA
		V_{CC} = 3.0 V; V_I = 0.8 V [2]	75	150	-	µA
I_{BHH}	bus hold HIGH current	V_{CC} = 2.3 V; V_I = 1.7 V [2]	-45	-	-	µA
		V_{CC} = 3.0 V; V_I = 2.0 V [2]	-75	-175	-	µA
I_{BHLO}	bus hold LOW overdrive current	V_{CC} = 3.6 V [2]	500	-	-	µA
I_{BHHO}	bus hold HIGH overdrive current	V_{CC} = 3.6 V [2]	-500	-	-	µA
C_I	input capacitance		-	4.0	-	pF
$C_{I/O}$	input/output capacitance		-	8.0	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.
[2] Valid for data inputs of bushold parts.

10. Dynamic characteristics

Table 7. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7.

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
t_{pd}	propagation delay	nAn to nBn; nBn to nAn; see Fig. 5 [2]				
		V_{CC} = 2.3 V to 2.7 V	1.0	2.0	3.7	ns
		V_{CC} = 2.7 V	1.0	2.1	3.6	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	1.9	3.0	ns
t_{en}	enable time	$n\overline{OE}$ to nAn; $n\overline{OE}$ to nBn; see Fig. 6 [3]				
		V_{CC} = 2.3 V to 2.7 V	1.0	2.7	5.7	ns
		V_{CC} = 2.7 V	1.0	3.0	5.4	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.3	4.4	ns
t_{dis}	disable time	$n\overline{OE}$ to nAn; $n\overline{OE}$ to nBn; see Fig. 6 [4]				
		V_{CC} = 2.3 V to 2.7 V	1.0	2.2	5.2	ns
		V_{CC} = 2.7 V	1.0	3.1	4.6	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.8	4.1	ns
C_{PD}	power dissipation capacitance	per buffer; V_I = GND to V_{CC} [5]				
		outputs enabled	-	29	-	pF
		outputs disabled	-	5	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.
Typical values for V_{CC} = 2.3 V to 2.7 V are measured at V_{CC} = 2.5 V.
Typical values for V_{CC} = 3.0 V to 3.6 V are measured at V_{CC} = 3.3 V.

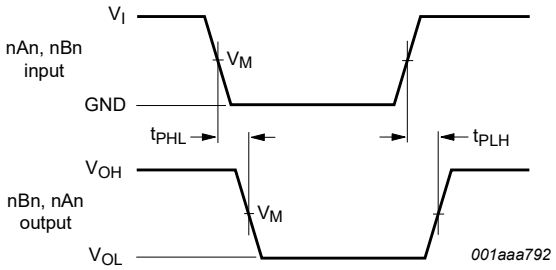
[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] t_{en} is the same as t_{PZL} and t_{PZH}.

[4] t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in Volts;
N = total load switching outputs;
$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

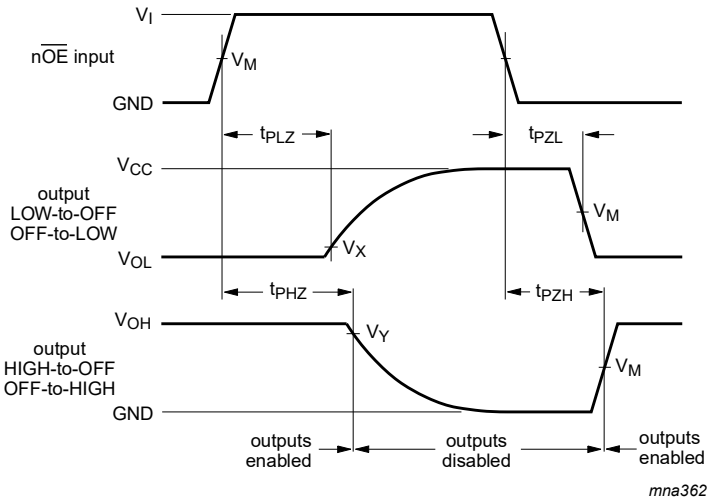
10.1. Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. Input (nAn, nBn) to output (nBn, nAn) propagation delay times



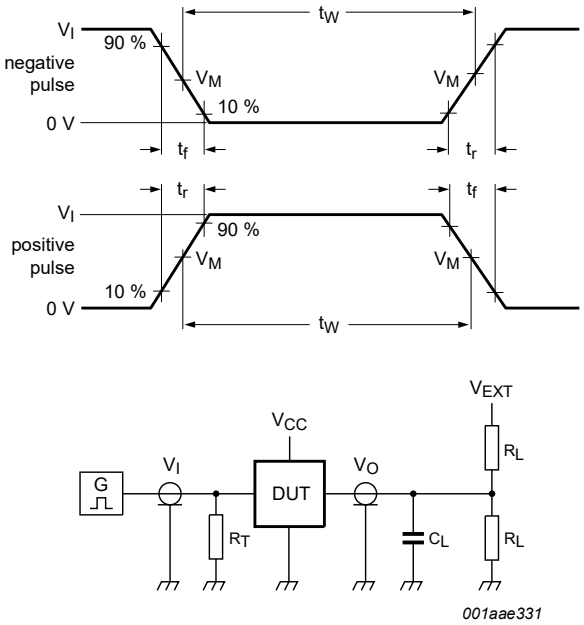
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 6. 3-state enable and disable times

Table 8. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
< 2.7 V	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.15 V	V_{OH} - 0.15 V
≥ 2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 9.

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance includes jig and probe capacitance.

R_T = Termination resistance should be equal to Z_o of pulse generator.

V_{EXT} = Test voltage for switching times.

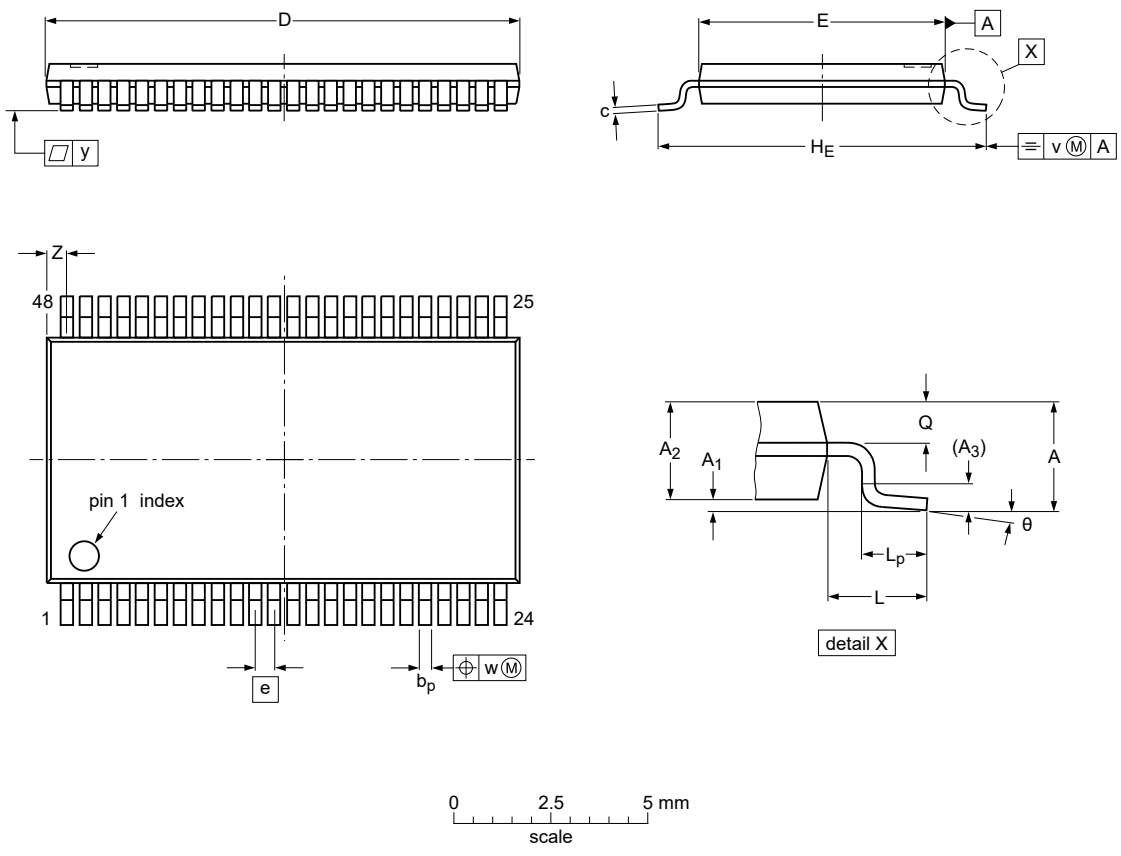
Fig. 7. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}
< 2.7 V	V_{CC}	≤2.0 ns	30 pF	500 Ω	open	GND	2 × V_{CC}
2.7 V to 3.6 V	2.7 V	≤2.5 ns	50 pF	500 Ω	open	GND	2 × V_{CC}

11. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	max	1.2	0.15	1.05		0.28	0.2	12.6	6.2		8.3		0.8	0.50				0.8	8°
	nom				0.25					0.5		1			0.25	0.08	0.1		
	min		0.05	0.85		0.17	0.1	12.4	6.0		7.9		0.4	0.35				0.4	0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot362-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				~~13-08-05~~ 24-01-05

Fig. 8. Package outline SOT362-1 (TSSOP48)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVC_ALVCH16245 v.8	20240626	Product data sheet	-	74ALVC_ALVCH16245 v.7
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard.			
74ALVC_ALVCH16245 v.7	20240603	Product data sheet	-	74ALVC_ALVCH16245 v.6
Modifications:	• Section 1 updated. • Section 2 updated. • Fig. 8: Updated package outline drawing SOT362-1 (TSSOP48).			
74ALVC_ALVCH16245 v.6	20210805	Product data sheet	-	74ALVC_ALVCH16245 v.5
Modifications:	• Type number 74ALVC16245DL (SOT370-1/SSOP48) removed.			
74ALVC_ALVCH16245 v.5	20201016	Product data sheet	-	74ALVC_ALVCH16245 v.4
Modifications:	• Type number 74ALVCH16245DL (SOT370-1/SSOP48) removed. • Section 1 and Section 2 updated. • Table 4: Derating values for P_{tot} total power dissipation updated.			
74ALVC_ALVCH16245 v.4	20171121	Product data sheet	-	74ALVC_ALVCH16245 v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
74ALVC_ALVCH16245 v.3	20040512	Product data sheet	-	74ALVCH16245 v.2 74ALVC16245_ 74ALVCH16245 v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the current presentation and information standard of Philips Semiconductors. • Section 1: General description updated.			
74ALVCH16245 v.2	19980629	Product specification	-	74ALVCH16245 v.1
74ALVC16245_ 74ALVCH16245 v.1	19980325	Product specification	-	-
74ALVCH16245 v.1	19950102	Preliminary specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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