

74AUP1G06GW,125 Datasheet

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DiGi Electronics Part Number 74AUP1G06GW,125-DG

Manufacturer Nexperia USA Inc.

Manufacturer Product Number 74AUP1G06GW,125

Description IC INVERTER 1CH 1-INP 5TSSOP

Detailed Description Inverter IC 1 Channel Open Drain 5-TSSOP



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Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
74AUP1G06GW,125	Nexperia USA Inc.
Series:	Product Status:
74AUP	Active
Logic Type:	Number of Circuits:
Inverter	1
Number of Inputs:	Features:
1	Open Drain
Voltage - Supply:	Current - Quiescent (Max):
0.8V ~ 3.6V	500 nA
Current - Output High, Low:	Input Logic Level - Low:
-, 4mA	0.7V ~ 0.9V
Input Logic Level - High:	Max Propagation Delay @ V, Max CL:
1.6V ~ 2V	10.5ns @ 3.3V, 30pF
Operating Temperature:	Mounting Type:
-40°C ~ 125°C	Surface Mount
Supplier Device Package:	Package / Case:
5-TSSOP	5-TSSOP, SC-70-5, SOT-353
Base Product Number:	
74AUP1G06	

Environmental & Export classification

8542.39.0001

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	

74AUP1G06

Low-power inverter with open-drain output

Rev. 12 — 13 November 2024

Product data sheet

1. General description

The 74AUP1G06 is a single inverter with open-drain output. Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device ensures very low static and dynamic power consumption across the entire V_{CC} range from 0.8 V to 3.6 V.

This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 0.8 V to 3.6 V
- High noise immunity
- · CMOS low power dissipation
- Low static power consumption; I_{CC} = 0.9 μA (maximum)
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Overvoltage tolerant inputs to 3.6 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- I_{OFF} circuitry provides partial Power-down mode operation
- Complies with JEDEC standards:
 - JESD8-12 (0.8 V to 1.3 V)
 - JESD8-11 (0.9 V to 1.65 V)
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8C (2.7 V to 3.6 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 3A exceeds 5000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C



3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AUP1G06GW	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74AUP1G06GM	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886
74AUP1G06GN	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 0.9 × 1.0 × 0.35 mm	<u>SOT1115</u>
74AUP1G06GS	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 1.0 × 1.0 × 0.35 mm	SOT1202
74AUP1G06GX	-40 °C to +125 °C	X2SON5	plastic thermal enhanced extremely thin small outline package; no leads; 5 terminals; body 0.8 × 0.8 × 0.32 mm	SOT1226-3
74AUP1G06GZ	-40 °C to +125 °C	XSON5	plastic thermal enhanced extremely thin small outline package with side-wettable flanks (SWF); no leads; 5 terminals; body 1.1 × 0.85 × 0.5 mm	SOT8065-1

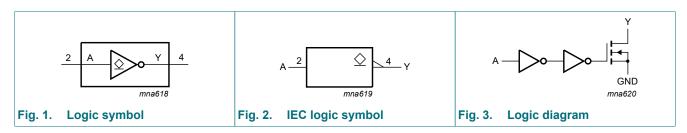
4. Marking

Table 2. Marking

Marking code [1]
pR

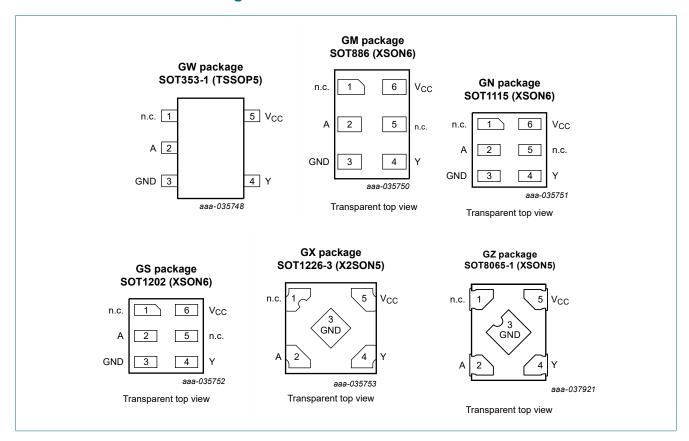
^[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram



6. Pinning information

6.1. Pinning



6.2. Pin description

Table 3. Pin description

Symbol	Pin	Pin		
	TSSOP5, XSON5 and X2SON5	XSON6		
n.c.	1	1	not connected	
A	2	2	data input	
GND	3	3	ground (0 V)	
Υ	4	4	data output	
n.c.	-	5	not connected	
V _{CC}	5	6	supply voltage	

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF state.

Input	Output
A	Υ
L	Z
Н	L

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
VI	input voltage	[1]	-0.5	+4.6	V
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
V_{O}	output voltage	Active mode and Power-down mode [1]	-0.5	+4.6	V
Io	output current	$V_O = 0 \text{ V to } V_{CC}$	-	+20	mA
I _{CC}	supply current		-	+50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C to } +125 ^{\circ}\text{C}$ [2]	-	250	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

For SOT886 (XSON6) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.

For SOT1115 (XSON6) package: Ptot derates linearly with 3.2 mW/K above 71 °C.

For SOT1202 (XSON6) package: Ptot derates linearly with 3.3 mW/K above 74 °C.

For SOT1226-3 (X2SON5) package: Ptot derates linearly with 3.0 mW/K above 67 °C.

For SOT8065-1 (XSON5) package: P $_{\rm tot}$ derates linearly with 3.2 mW/K above 72 $^{\circ}\text{C}.$

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		0.8	3.6	V
VI	input voltage		0	3.6	V
Vo	output voltage	Active mode	0	V _{CC}	V
		Power-down mode; V _{CC} = 0 V	0	3.6	V
T _{amb}	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 0.8 V to 3.6 V	0	200	ns/V

4/18

^[2] For SOT353-1 (TSSOP5) package: Ptot derates linearly with 3.3 mW/K above 74 °C.

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
T _{amb} = 2	25 °C					
V _{IH}	HIGH-level input	V _{CC} = 0.8 V	0.70 × V _{CC}	-	-	V
	voltage	V _{CC} = 0.9 V to 1.95 V	0.65 × V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V _{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 0.8 V	-	-	0.30 × V _{CC}	V
		V _{CC} = 0.9 V to 1.95 V	-	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V _{OL}	LOW-level output	$V_I = V_{IH}$ or V_{IL}				
	voltage	I _O = 20 μA; V _{CC} = 0.8 V to 3.6 V	-	-	0.1	V
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	-	0.3 × V _{CC}	V
		I _O = 1.7 mA; V _{CC} = 1.4 V	-	-	0.31	V
		I _O = 1.9 mA; V _{CC} = 1.65 V	-	-	0.31	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.31	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.44	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.31	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.44	V
I _I	input leakage current	V_I = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.1	μΑ
l _{OZ}	OFF-state output current	$V_I = V_{IL}$; $V_O = 0 \text{ V to } 3.6 \text{ V}$; $V_{CC} = 0 \text{ V to } 3.6 \text{ V}$	-	-	±0.1	μΑ
I _{OFF}	power-off leakage current	V_{I} or $V_{O} = 0$ V to 3.6 V; $V_{CC} = 0$ V			±0.2	μΑ
ΔI _{OFF}	additional power-off leakage current	V_1 or $V_0 = 0 V$ to 3.6 V; $V_{CC} = 0 V$ to 0.2 V			±0.2	μΑ
I _{CC}	supply current	$V_I = GND \text{ or } V_{CC}; I_O = 0 \text{ A};$ $V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$	-	-	0.5	μΑ
ΔI _{CC}	additional supply current	$V_I = V_{CC} - 0.6 \text{ V}; I_O = 0 \text{ A}; V_{CC} = 3.3 \text{ V}$	-	-	40	μΑ
Cı	input capacitance	V_{CC} = 0 V to 3.6 V; V_{I} = GND or V_{CC}	-	8.0	-	pF
Co	output capacitance	output enabled; $V_O = GND$; $V_{CC} = 0 V$	-	1.7	-	pF
		output disabled; V _O = GND; V _{CC} = 0 V	-	1.1	-	pF
T _{amb} = -	40 °C to +85 °C				<u>'</u>	
V _{IH}	HIGH-level input	V _{CC} = 0.8 V	0.70 × V _{CC}	-	-	V
	voltage	V _{CC} = 0.9 V to 1.95 V	0.65 × V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V _{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 0.8 V	-	-	0.30 × V _{CC}	V
		V _{CC} = 0.9 V to 1.95 V	-	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.9	V

74AUP1G06

Low-power inverter with open-drain output

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{OL}	LOW-level output	V _I = V _{IH} or V _{IL}				
V _{OL} L V _{OL} V _{OL} L V _{OL} V _{OL} L V _{OL} V _{OL} V _{OL} L V _{OL} V _{OL}	voltage	I _O = 20 μA; V _{CC} = 0.8 V to 3.6 V	-	-	0.1	V
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	-	0.3 × V _{CC}	V
		I _O = 1.7 mA; V _{CC} = 1.4 V	-	-	0.37	V
		I _O = 1.9 mA; V _{CC} = 1.65 V	-	-	0.35	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.33	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.45	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.33	V
l		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.45	V
I _I	input leakage current	V _I = GND to 3.6 V; V _{CC} = 0 V to 3.6 V	-	-	±0.5	μΑ
l _{OZ}	OFF-state output current	V _I = V _{IL} ; V _O = 0 V to 3.6 V; V _{CC} = 0 V to 3.6 V	-	-	±0.5	μΑ
I _{OFF}	power-off leakage current	V_{1} or $V_{0} = 0$ V to 3.6 V; $V_{CC} = 0$ V		±0.5	μΑ	
ΔI _{OFF}	additional power-off leakage current	V_{I} or $V_{O} = 0$ V to 3.6 V; $V_{CC} = 0$ V to 0.2 V	-			μΑ
I _{CC}	supply current	$V_{I} = GND \text{ or } V_{CC}; I_{O} = 0 \text{ A};$ - $V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$		-	0.9	μΑ
ΔI _{CC}	additional supply current	$V_I = V_{CC} - 0.6 \text{ V}; I_O = 0 \text{ A}; V_{CC} = 3.3 \text{ V}$	-	-	50	μΑ
T _{amb} = -	40 °C to +125 °C					
V _{IH}	HIGH-level input	V _{CC} = 0.8 V	0.75 × V _{CC}	-	-	V
	voltage	V _{CC} = 0.9 V to 1.95 V	0.70 × V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V _{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 0.8 V	-	-	0.25 × V _{CC}	V
		V _{CC} = 0.9 V to 1.95 V	-	-	0.30 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V _{OL}	LOW-level output	$V_I = V_{IH}$ or V_{IL}				
	voltage	I _O = 20 μA; V _{CC} = 0.8 V to 3.6 V	-	-	0.11	V
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	-	0.33 × V _{CC}	V
		I _O = 1.7 mA; V _{CC} = 1.4 V	-	-	0.41	V
		I _O = 1.9 mA; V _{CC} = 1.65 V	-	-	0.39	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.36	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.50	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.36	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.50	V

74AUP1G06

Low-power inverter with open-drain output

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
I _I	input leakage current	V _I = GND to 3.6 V; V _{CC} = 0 V to 3.6 V	-	-	±0.75	μΑ
I _{OZ}	OFF-state output current	$V_I = V_{IL}$; $V_O = 0 \text{ V to } 3.6 \text{ V}$; $V_{CC} = 0 \text{ V to } 3.6 \text{ V}$	-	-	±0.75	μΑ
I _{OFF}	power-off leakage current	V_1 or $V_0 = 0$ V to 3.6 V; $V_{CC} = 0$ V	-	-	±0.75	μΑ
ΔI _{OFF}	additional power-off leakage current	V_1 or $V_0 = 0$ V to 3.6 V; $V_{CC} = 0$ V to 0.2 V	-	-	±0.75	μΑ
I _{CC}	supply current	$V_I = GND \text{ or } V_{CC}; I_O = 0 \text{ A};$ $V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$	-	-	1.4	μΑ
ΔI _{CC}	additional supply current	$V_1 = V_{CC} - 0.6 \text{ V}; I_O = 0 \text{ A}; V_{CC} = 3.3 \text{ V}$	-	-	75	μΑ

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5.

Symbol	Parameter	Conditions	25 °C		-40 °C to +85 °C		-40 °C to +125 °C		Unit	
			Min	Typ [1]	Max	Min	Max	Min	Max	
$C_L = 5 p$	F									
P	propagation	A to Y; see <u>Fig. 4</u> [2]								
	delay	V _{CC} = 0.8 V	-	12.8	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	2.3	4.3	9.9	2.0	10.9	2.0	12.0	ns
		V _{CC} = 1.4 V to 1.6 V	1.8	3.1	6.1	1.5	7.1	1.5	7.8	ns
		V _{CC} = 1.65 V to 1.95 V	1.5	2.8	4.7	1.2	5.7	1.2	6.3	ns
		V _{CC} = 2.3 V to 2.7 V	1.2	2.2	3.2	1.0	3.9	1.0	4.3	ns
		V _{CC} = 3.0 V to 3.6 V	1.1	2.2	3.3	0.8	3.6	8.0	4.0	ns
C _L = 10	pF							,		<u>'</u>
t _{pd}	propagation	A to Y; see <u>Fig. 4</u> [2]								
	delay	V _{CC} = 0.8 V	-	15.8	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	2.7	5.4	11.2	2.5	13.2	2.5	15.0	ns
		V _{CC} = 1.4 V to 1.6 V	2.2	3.9	7.0	2.0	8.5	2.0	9.4	ns
		V _{CC} = 1.65 V to 1.95 V	1.9	3.6	5.4	1.7	6.7	1.7	7.4	ns
		V _{CC} = 2.3 V to 2.7 V	1.7	2.9	3.8	1.4	4.5	1.4	5.0	ns
		V _{CC} = 3.0 V to 3.6 V	1.6	3.2	4.6	1.2	4.9	1.2	5.4	ns
C _L = 15	pF	1							'	1
t _{pd}	propagation	A to Y; see <u>Fig. 4</u> [2]								
	delay	V _{CC} = 0.8 V	-	18.8	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	3.2	6.4	12.2	2.9	15.2	2.9	17.0	ns
		V _{CC} = 1.4 V to 1.6 V	2.6	4.6	7.7	2.3	9.4	2.3	10.0	ns
		V _{CC} = 1.65 V to 1.95 V	2.3	4.5	6.6	2.1	7.3	2.1	8.1	ns
		V _{CC} = 2.3 V to 2.7 V	2.1	3.5	4.6	1.7	5.1	1.7	5.7	ns
		V _{CC} = 3.0 V to 3.6 V	2.0	4.0	6.0	1.5	6.5	1.5	7.2	ns

74AUP1G06

Low-power inverter with open-drain output

Symbol	Parameter	Conditions	25 °C		-40 °C to +85 °C		-40 °C to +125 °C		Unit	
			Min	Typ [1]	Max	Min	Max	Min	Max	
C _L = 30	pF									
t _{pd}	propagation delay	A to Y; see <u>Fig. 4</u> [2]								
		V _{CC} = 0.8 V	-	27.8	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	4.4	9.3	16.5	3.9	19.3	3.9	21.3	ns
		V _{CC} = 1.4 V to 1.6 V	3.6	6.8	10.1	3.2	12.0	3.2	13.2	ns
		V _{CC} = 1.65 V to 1.95 V	3.2	6.8	10.7	2.9	11.0	2.9	12.1	ns
		V _{CC} = 2.3 V to 2.7 V	2.9	5.3	7.2	2.6	7.8	2.6	8.6	ns
		V _{CC} = 3.0 V to 3.6 V	2.9	6.5	10.5	2.5	10.8	2.5	11.9	ns
C _L = 5 p	F, 10 pF, 15 p	F and 30 pF								
C _{PD}	power dissipation capacitance	$f_i = 1 \text{ MHz}; V_I = \text{GND to } V_{CC}$ [3]								
		V _{CC} = 0.8 V	-	0.5	-	-	-	-	-	pF
		V _{CC} = 1.1 V to 1.3 V	-	0.6	-	-	-	-	-	pF
		V _{CC} = 1.4 V to 1.6 V	-	0.7	-	-	-	-	-	pF
		V _{CC} = 1.65 V to 1.95 V	-	0.7	-	-	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V	-	1.0	-	-	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V	-	1.2	-	-	-	-	-	pF

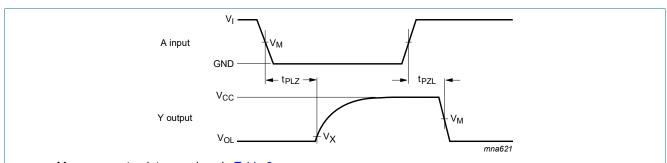
- All typical values are measured at nominal V_{CC}.
- t_{pd} is the same as t_{PZL} and t_{PLZ} . C_{PD} is used to determine the dynamic power dissipation (P_D in μW). $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N$ where:

 f_i = input frequency in MHz;

V_{CC} = supply voltage in V;

N = number of inputs switching.

11.1. Waveforms and test circuit



Measurement points are given in Table 9.

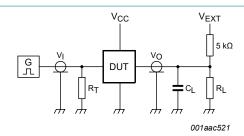
Logic level: V_{OL} is the typical output voltage level that occurs at the output load.

The data input (A) to output (Y) propagation delays Fig. 4.

Table 9. Measurement points

Supply voltage	Input			Output		
V _{cc}	V _M	V _I	$t_r = t_f$	V _M	V _X	
0.8 V to 1.6 V	0.5 × V _{CC}	V _{CC}	≤ 3.0 ns	0.5 × V _{CC}	V _{OL} + 0.1 V	
1.65 V to 2.7 V	0.5 × V _{CC}	V _{CC}	≤ 3.0 ns	0.5 × V _{CC}	V _{OL} + 0.15 V	
3.0 V to 3.6 V	0.5 × V _{CC}	V _{CC}	≤ 3.0 ns	0.5 × V _{CC}	V _{OL} + 0.3 V	

Low-power inverter with open-drain output



Test data is given in Table 10.

Definitions for test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

Fig. 5. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Load	V _{EXT}			
V _{CC}	CL	R _L [1]	t _{PLH} , t _{PHL}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}
0.8 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 k Ω or 1 M Ω	open	GND	2 × V _{CC}

[1] For measuring enable and disable times R_L = 5 k Ω . For measuring propagation delays, setup and hold times and pulse width R_L = 1 M Ω .

74AUP1G06

Low-power inverter with open-drain output

12. Package outline

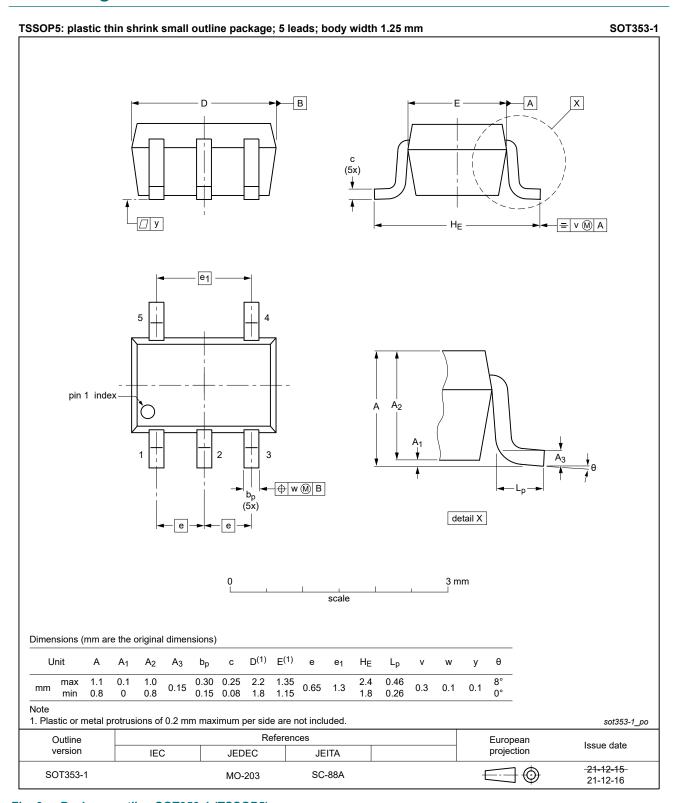


Fig. 6. Package outline SOT353-1 (TSSOP5)

Low-power inverter with open-drain output

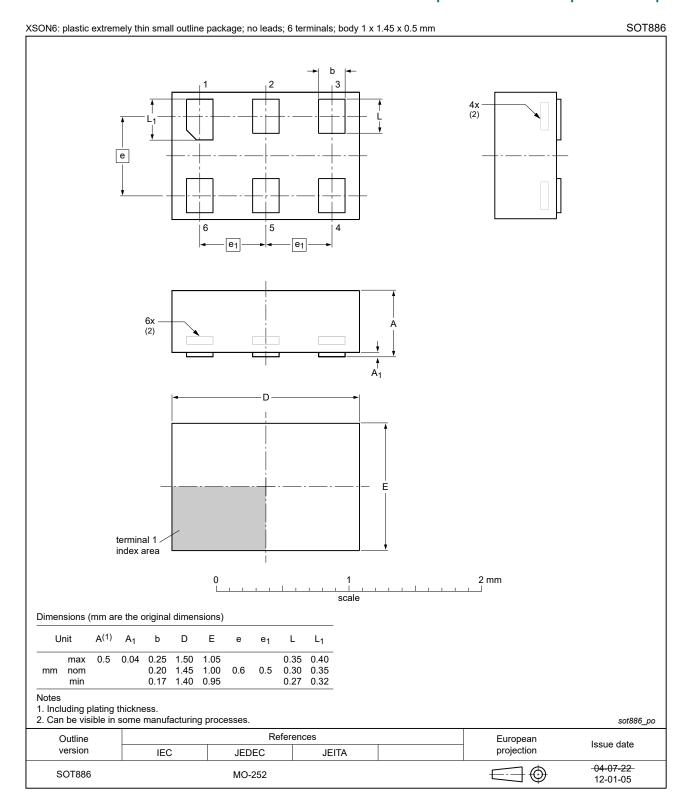


Fig. 7. Package outline SOT886 (XSON6)

Low-power inverter with open-drain output

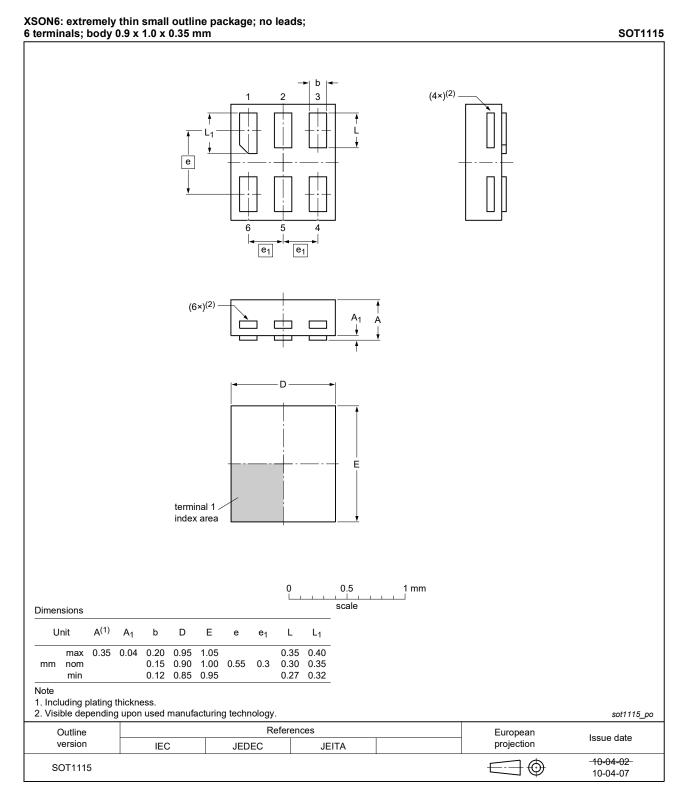


Fig. 8. Package outline SOT1115 (XSON6)

12 / 18

Low-power inverter with open-drain output

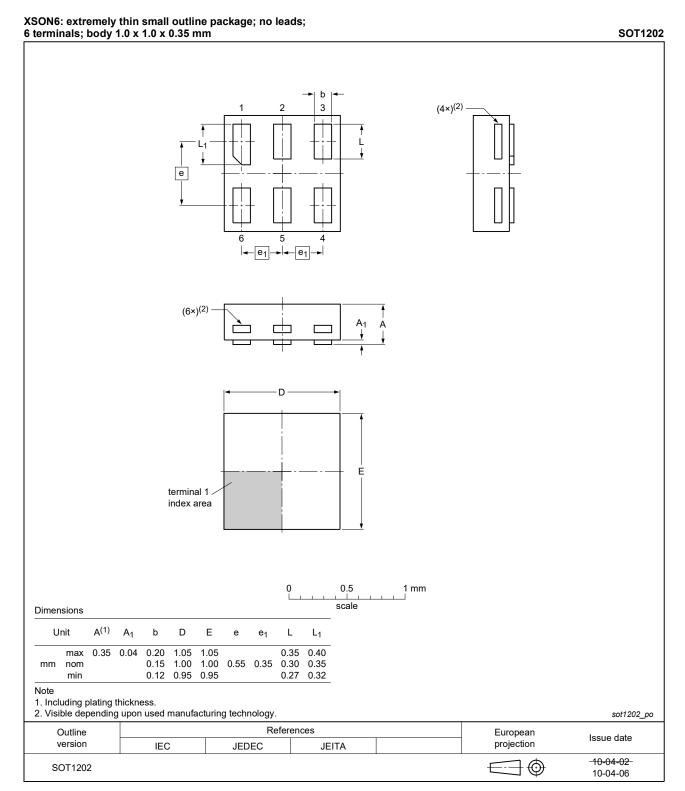


Fig. 9. Package outline SOT1202 (XSON6)

Low-power inverter with open-drain output

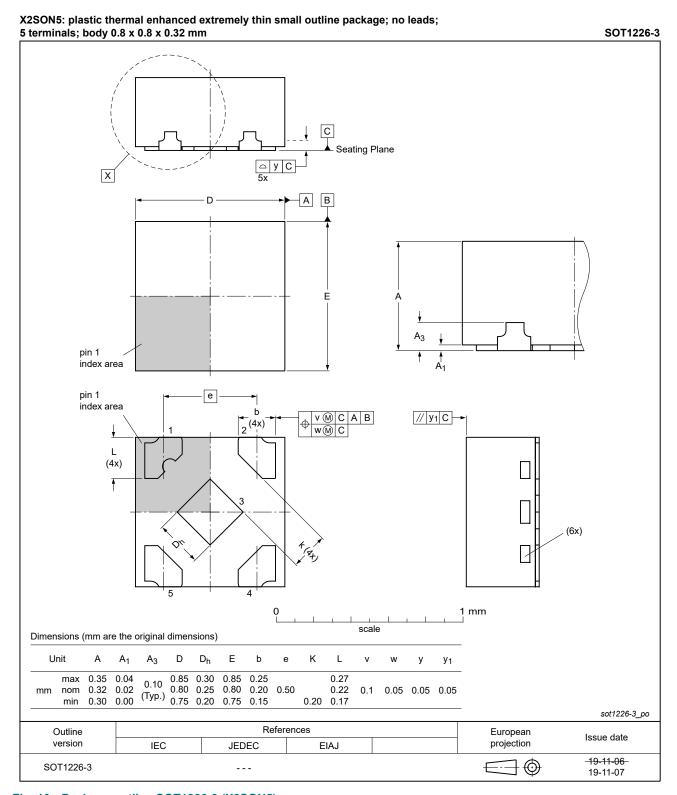


Fig. 10. Package outline SOT1226-3 (X2SON5)

Low-power inverter with open-drain output

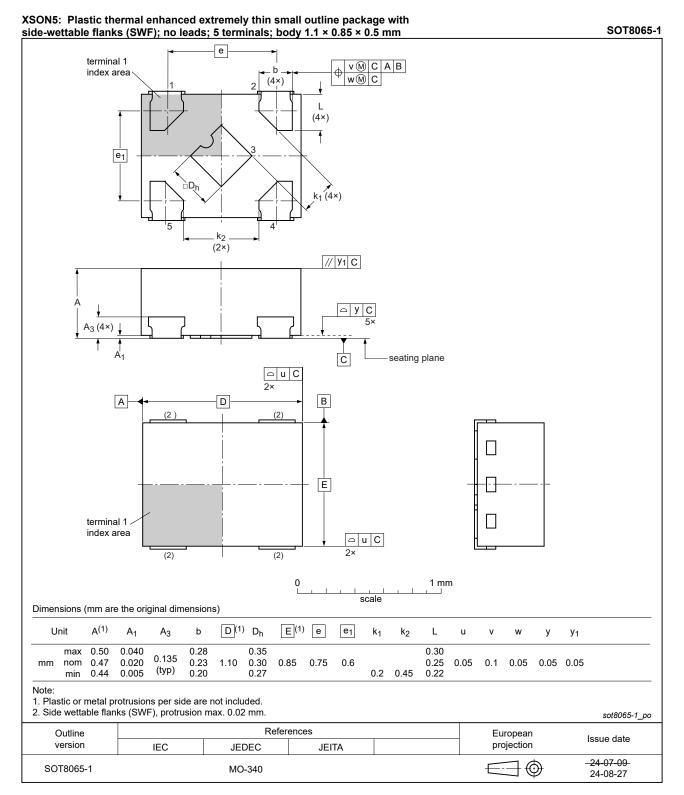


Fig. 11. Package outline SOT8065-1 (XSON5)

15 / 18

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
НВМ	Human Body Model
JEDEC	Joint Electron Device Engineering Council

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes					
74AUP1G06 v.12	20241113	Product data sheet	-	74AUP1G06 v.11.1					
Modifications:	Type numb	Type number 74AUP1G06GZ (SOT8065-1/XSON5) added.							
74AUP1G06 v.11.1	20230711	20230711 Product data sheet - 74AUP1G06 v.10							
Modifications:	Section 2: I	<u>Section 2</u> : ESD specification updated according to the latest JEDEC standard.							
74AUP1G06 v.10	20220113	Product data sheet	-	74AUP1G06 v.9					
Modifications:		 <u>Section 1</u> and <u>Section 2</u> updated. <u>Fig. 6</u>: Package outline drawing for SOT353-1 (TSSOP5) has changed. 							
74AUP1G06 v.9	20210706	Product data sheet	-	74AUP1G06 v.8					
Modifications:	 SOT1226 (Section 1 a 	occion i and occion z aparted.							
74AUP1G06 v.8	20180212	Product data sheet	-	74AUP1G06 v.7					
Modifications:	guidelines • Legal texts	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Pin configuration drawing of SOT1226 (X2SON5) updated. 							
74AUP1G06 v.7	20120628	Product data sheet	-	74AUP1G06 v.6					
Modifications:	7.	 Added type number 74AUP1G06GX (SOT1226) Package outline drawing of SOT886 (Fig. 7) modified. 							
74AUP1G06 v.6	20111115	Product data sheet	-	74AUP1G06 v.5					
Modifications:	Legal page	Legal pages updated.							
74AUP1G06 v.5	20101022	Product data sheet	-	74AUP1G06 v.4					
74AUP1G06 v.4	20090610	Product data sheet	-	74AUP1G06 v.3					
74AUP1G06 v.3	20070615	Product data sheet	-	74AUP1G06 v.2					
74AUP1G06 v.2	20060824	Product data sheet	-	74AUP1G06 v.1					
74AUP1G06 v.1	20050718	Product data sheet	-	-					

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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74AUP1G06

Low-power inverter with open-drain output

Contents

1. General description	1
2. Features and benefits	1
3. Ordering information	2
4. Marking	2
5. Functional diagram	2
6. Pinning information	3
6.1. Pinning	3
6.2. Pin description	3
7. Functional description	4
8. Limiting values	4
9. Recommended operating conditions	4
10. Static characteristics	5
11. Dynamic characteristics	7
11.1. Waveforms and test circuit	8
12. Package outline	10
13. Abbreviations	16
14. Revision history	16
15. Legal information	17

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