

74AUP1G08GM,115 Datasheet



DiGi Electronics Part Number	74AUP1G08GM,115-DG
Manufacturer	Nexperia USA Inc.
Manufacturer Product Number	74AUP1G08GM,115
Description	IC GATE AND 1CH 2-INP 6XSON
Detailed Description	AND Gate IC 1 Channel 6-XSON, SOT886 (1.45x1)



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Purchase and inquiry

Manufacturer Product Number:

74AUP1G08GM,115

Series:

74AUP

Logic Type:

AND Gate

Number of Inputs:

2

Voltage - Supply:

0.8V ~ 3.6V

Current - Output High, Low:

4mA, 4mA

Input Logic Level - High:

1.6V ~ 2V

Operating Temperature:

-40°C ~ 125°C

Supplier Device Package:

6-XSON, SOT886 (1.45x1)

Base Product Number:

74AUP1G08

Manufacturer:

Nexperia USA Inc.

Product Status:

Active

Number of Circuits:

1

Features:

-

Current - Quiescent (Max):

500 nA

Input Logic Level - Low:

0.7V ~ 0.9V

Max Propagation Delay @ V, Max CL:

6.2ns @ 3.3V, 30pF

Mounting Type:

Surface Mount

Package / Case:

6-XDFDN

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99



74AUP1G08

Low-power 2-input AND gate

Rev. 12.1 — 29 August 2024

Product data sheet

1. General description

The 74AUP1G08 is a single 2-input AND gate. Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times. This device ensures very low static and dynamic power consumption across the entire V_{CC} range from 0.8 V to 3.6 V. This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 0.8 V to 3.6 V
- CMOS low power dissipation
- High noise immunity
- Overvoltage tolerant inputs to 3.6 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Low static power consumption; $I_{CC} = 0.9 \mu\text{A}$ (maximum)
- Complies with JEDEC standards:
 - JESD8-12 (0.8 V to 1.3 V)
 - JESD8-11 (0.9 V to 1.65 V)
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8C (2.7 V to 3.6 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 3A exceeds 5000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AUP1G08GW	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74AUP1G08GM	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886
74AUP1G08GN	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 0.9 × 1.0 × 0.35 mm	SOT1115
74AUP1G08GS	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 1.0 × 1.0 × 0.35 mm	SOT1202
74AUP1G08GX	-40 °C to +125 °C	X2SON5	plastic thermal enhanced extremely thin small outline package; no leads; 5 terminals; body 0.8 × 0.8 × 0.32 mm	SOT1226-3
74AUP1G08GZ	-40 °C to +125 °C	XSON5	plastic thermal enhanced extremely thin small outline package with side-wettable flanks (SWF); no leads; 5 terminals; body 1.1 × 0.85 × 0.5 mm	SOT8065-1

4. Marking

Table 2. Marking

Type number	Marking code ^[1]
74AUP1G08GW	pE
74AUP1G08GM	pE
74AUP1G08GN	pE
74AUP1G08GS	pE
74AUP1G08GX	pE
74AUP1G08GZ	pE

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

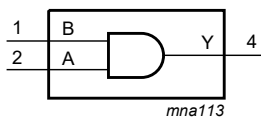


Fig. 1. Logic symbol

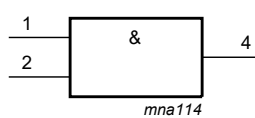


Fig. 2. IEC logic symbol

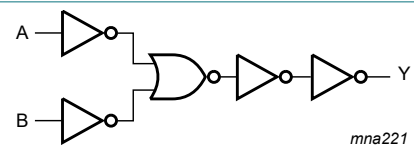
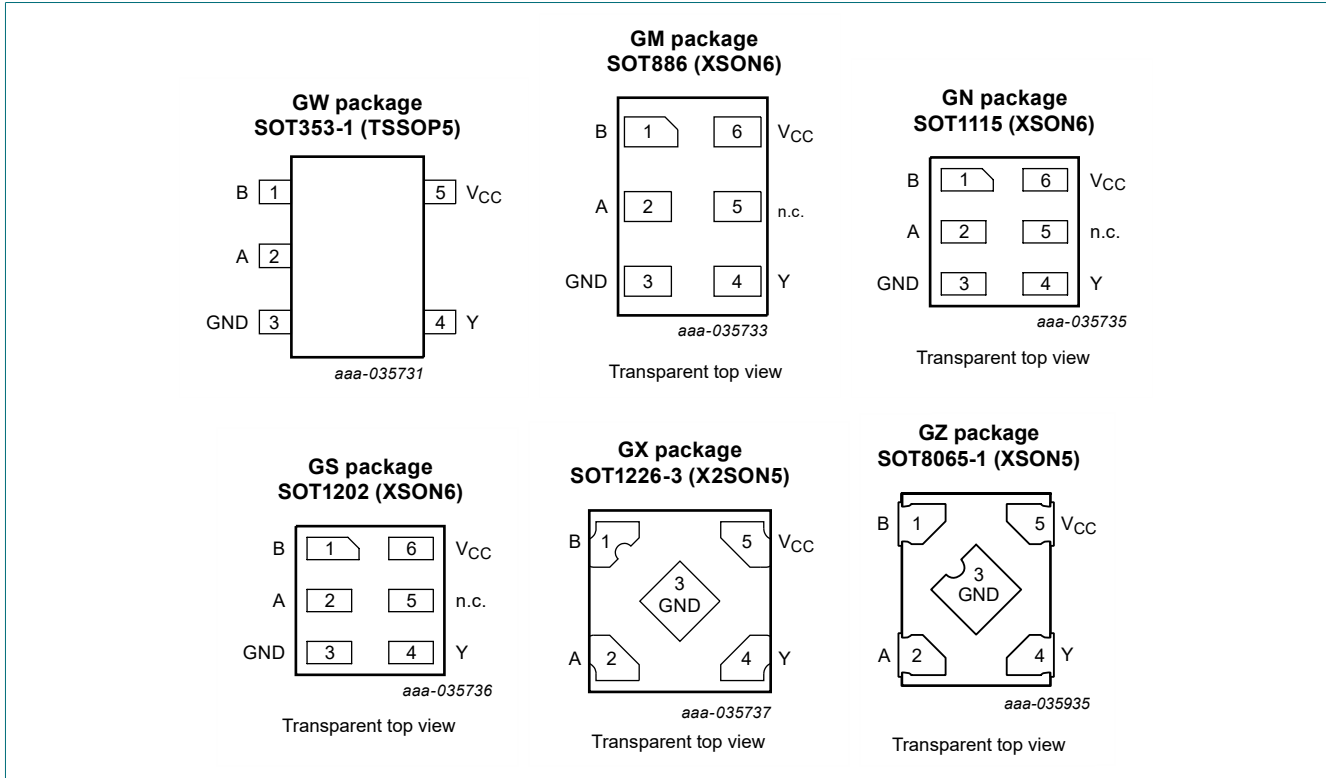


Fig. 3. Logic diagram

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 3. Pin description

Symbol	Pin		Description
	TSSOP5, XSON5 and X2SON5	XSON6	
B	1	1	data input
A	2	2	data input
GND	3	3	ground (0 V)
Y	4	4	data output
n.c.	-	5	not connected
V _{CC}	5	6	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
V_I	input voltage		[1] -0.5	+4.6	V
I_{OK}	output clamping current	$V_O < 0$ V	-50	-	mA
V_O	output voltage	Active mode and Power-down mode	[1] -0.5	+4.6	V
I_O	output current	$V_O = 0$ V to V_{CC}	-	± 20	mA
I_{CC}	supply current		-	+50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[2] -	250	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT353-1 (TSSOP5) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.

For SOT886 (XSON6) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.

For SOT1115 (XSON6) package: P_{tot} derates linearly with 3.2 mW/K above 71 °C.

For SOT1202 (XSON6) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.

For SOT1226-3 (X2SON5) package: P_{tot} derates linearly with 3.0 mW/K above 67 °C.

For SOT8065-1 (XSON5) package: P_{tot} derates linearly with 3.2 mW/K above 72 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		0.8	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	Active mode	0	V_{CC}	V
		Power-down mode; $V_{CC} = 0$ V	0	3.6	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 0.8$ V to 3.6 V	0	200	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 0.8 V	0.70 × V _{CC}	-	-	V
		V _{CC} = 0.9 V to 1.95 V	0.65 × V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V _{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 0.8 V	-	-	0.30 × V _{CC}	V
		V _{CC} = 0.9 V to 1.95 V	-	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 μA; V _{CC} = 0.8 V to 3.6 V	V _{CC} - 0.1	-	-	V
		I _O = -1.1 mA; V _{CC} = 1.1 V	0.75 × V _{CC}	-	-	V
		I _O = -1.7 mA; V _{CC} = 1.4 V	1.11	-	-	V
		I _O = -1.9 mA; V _{CC} = 1.65 V	1.32	-	-	V
		I _O = -2.3 mA; V _{CC} = 2.3 V	2.05	-	-	V
		I _O = -3.1 mA; V _{CC} = 2.3 V	1.9	-	-	V
		I _O = -2.7 mA; V _{CC} = 3.0 V	2.72	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 μA; V _{CC} = 0.8 V to 3.6 V	-	-	0.1	V
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	-	0.3 × V _{CC}	V
		I _O = 1.7 mA; V _{CC} = 1.4 V	-	-	0.31	V
		I _O = 1.9 mA; V _{CC} = 1.65 V	-	-	0.31	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.31	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.44	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.31	V
I _I	input leakage current	V _I = GND to 3.6 V; V _{CC} = 0 V to 3.6 V	-	-	±0.1	μA
		V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±0.2	μA
I _{OFF}	power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±0.2	μA
ΔI _{OFF}	additional power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V to 0.2 V	-	-	±0.2	μA
I _{CC}	supply current	V _I = GND or V _{CC} ; I _O = 0 A; V _{CC} = 0.8 V to 3.6 V	-	-	0.5	μA
ΔI _{CC}	additional supply current	V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 3.3 V [1]	-	-	40	μA
C _I	input capacitance	V _{CC} = 0 V to 3.6 V; V _I = GND or V _{CC}	-	0.8	-	pF
C _O	output capacitance	V _O = GND; V _{CC} = 0 V	-	1.7	-	pF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +85 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 0.8 V	0.70 × V _{CC}	-	-	V
		V _{CC} = 0.9 V to 1.95 V	0.65 × V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V _{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 0.8 V	-	-	0.30 × V _{CC}	V
		V _{CC} = 0.9 V to 1.95 V	-	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 μA; V _{CC} = 0.8 V to 3.6 V	V _{CC} - 0.1	-	-	V
		I _O = -1.1 mA; V _{CC} = 1.1 V	0.7 × V _{CC}	-	-	V
		I _O = -1.7 mA; V _{CC} = 1.4 V	1.03	-	-	V
		I _O = -1.9 mA; V _{CC} = 1.65 V	1.30	-	-	V
		I _O = -2.3 mA; V _{CC} = 2.3 V	1.97	-	-	V
		I _O = -3.1 mA; V _{CC} = 2.3 V	1.85	-	-	V
		I _O = -2.7 mA; V _{CC} = 3.0 V	2.67	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 μA; V _{CC} = 0.8 V to 3.6 V	-	-	0.1	V
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	-	0.3 × V _{CC}	V
		I _O = 1.7 mA; V _{CC} = 1.4 V	-	-	0.37	V
		I _O = 1.9 mA; V _{CC} = 1.65 V	-	-	0.35	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.33	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.45	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.33	V
I _I	input leakage current	V _I = GND to 3.6 V; V _{CC} = 0 V to 3.6 V	-	-	±0.5	μA
		V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±0.5	μA
ΔI _{OFF}	additional power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V to 0.2 V	-	-	±0.6	μA
I _{CC}	supply current	V _I = GND or V _{CC} ; I _O = 0 A; V _{CC} = 0.8 V to 3.6 V	-	-	0.9	μA
ΔI _{CC}	additional supply current	V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 3.3 V [1]	-	-	50	μA
T_{amb} = -40 °C to +125 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 0.8 V	0.75 × V _{CC}	-	-	V
		V _{CC} = 0.9 V to 1.95 V	0.70 × V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V _{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 0.8 V	-	-	0.25 × V _{CC}	V
		V _{CC} = 0.9 V to 1.95 V	-	-	0.30 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.9	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 μA; V _{CC} = 0.8 V to 3.6 V	V _{CC} - 0.11	-	-	V
		I _O = -1.1 mA; V _{CC} = 1.1 V	0.6 × V _{CC}	-	-	V
		I _O = -1.7 mA; V _{CC} = 1.4 V	0.93	-	-	V
		I _O = -1.9 mA; V _{CC} = 1.65 V	1.17	-	-	V
		I _O = -2.3 mA; V _{CC} = 2.3 V	1.77	-	-	V
		I _O = -3.1 mA; V _{CC} = 2.3 V	1.67	-	-	V
		I _O = -2.7 mA; V _{CC} = 3.0 V	2.40	-	-	V
		I _O = -4.0 mA; V _{CC} = 3.0 V	2.30	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 μA; V _{CC} = 0.8 V to 3.6 V	-	-	0.11	V
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	-	0.33 × V _{CC}	V
		I _O = 1.7 mA; V _{CC} = 1.4 V	-	-	0.41	V
		I _O = 1.9 mA; V _{CC} = 1.65 V	-	-	0.39	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.36	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.50	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.36	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.50	V
I _I	input leakage current	V _I = GND to 3.6 V; V _{CC} = 0 V to 3.6 V	-	-	±0.75	μA
I _{OFF}	power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±0.75	μA
ΔI _{OFF}	additional power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V to 0.2 V	-	-	±0.75	μA
I _{CC}	supply current	V _I = GND or V _{CC} ; I _O = 0 A; V _{CC} = 0.8 V to 3.6 V	-	-	1.4	μA
ΔI _{CC}	additional supply current	V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 3.3 V [1]	-	-	75	μA

[1] One input at V_{CC} - 0.6 V, other input at V_{CC} or GND.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
T_{amb} = 25 °C; C_L = 5 pF						
t _{pd}	propagation delay	A, B to Y; see Fig. 4 [2]				
		V _{CC} = 0.8 V	-	17.0	-	ns
		V _{CC} = 1.1 V to 1.3 V	2.6	5.1	10.8	ns
		V _{CC} = 1.4 V to 1.6 V	1.6	3.7	6.5	ns
		V _{CC} = 1.65 V to 1.95 V	1.3	3.0	5.2	ns
		V _{CC} = 2.3 V to 2.7 V	1.1	2.4	4.0	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.2	3.5	ns

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
T_{amb} = 25 °C; C_L = 10 pF						
t _{pd}	propagation delay	A, B to Y; see Fig. 4 [2]				
		V _{CC} = 0.8 V	-	20.6	-	ns
		V _{CC} = 1.1 V to 1.3 V	2.4	6.0	12.5	ns
		V _{CC} = 1.4 V to 1.6 V	2.0	4.3	7.6	ns
		V _{CC} = 1.65 V to 1.95 V	1.7	3.6	6.1	ns
		V _{CC} = 2.3 V to 2.7 V	1.4	2.9	4.8	ns
V _{CC} = 3.0 V to 3.6 V	1.3	2.7	4.2	ns		
T_{amb} = 25 °C; C_L = 15 pF						
t _{pd}	propagation delay	A, B to Y; see Fig. 4 [2]				
		V _{CC} = 0.8 V	-	24.1	-	ns
		V _{CC} = 1.1 V to 1.3 V	3.4	6.8	14.2	ns
		V _{CC} = 1.4 V to 1.6 V	2.3	4.9	8.6	ns
		V _{CC} = 1.65 V to 1.95 V	1.9	4.0	6.9	ns
		V _{CC} = 2.3 V to 2.7 V	1.7	3.4	5.5	ns
V _{CC} = 3.0 V to 3.6 V	1.5	3.1	4.8	ns		
T_{amb} = 25 °C; C_L = 30 pF						
t _{pd}	propagation delay	A, B to Y; see Fig. 4 [2]				
		V _{CC} = 0.8 V	-	34.4	-	ns
		V _{CC} = 1.1 V to 1.3 V	4.6	9.1	19.4	ns
		V _{CC} = 1.4 V to 1.6 V	3.4	6.4	11.5	ns
		V _{CC} = 1.65 V to 1.95 V	2.6	5.3	9.1	ns
		V _{CC} = 2.3 V to 2.7 V	2.3	4.5	7.2	ns
V _{CC} = 3.0 V to 3.6 V	2.2	4.2	6.2	ns		
T_{amb} = 25 °C						
C _{PD}	power dissipation capacitance	f = 1 MHz; V _I = GND to V _{CC} [3]				
		V _{CC} = 0.8 V	-	2.5	-	pF
		V _{CC} = 1.1 V to 1.3 V	-	2.7	-	pF
		V _{CC} = 1.4 V to 1.6 V	-	2.8	-	pF
		V _{CC} = 1.65 V to 1.95 V	-	2.9	-	pF
		V _{CC} = 2.3 V to 2.7 V	-	3.5	-	pF
V _{CC} = 3.0 V to 3.6 V	-	4.0	-	pF		

[1] All typical values are measured at nominal V_{CC}.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

Σ(C_L × V_{CC}² × f_o) = sum of the outputs.

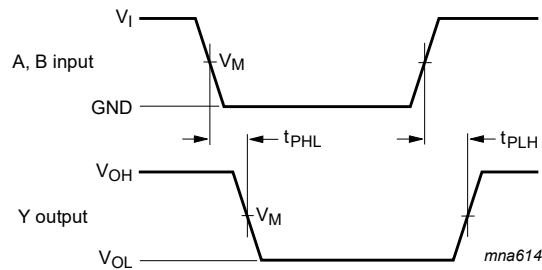
Table 9. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
C_L = 5 pF							
t _{pd}	propagation delay	A, B to Y; see Fig. 4 [1]					
		V _{CC} = 1.1 V to 1.3 V	2.1	11.7	2.1	12.9	ns
		V _{CC} = 1.4 V to 1.6 V	1.5	7.5	1.5	8.3	ns
		V _{CC} = 1.65 V to 1.95 V	1.3	6.1	1.3	6.7	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	4.8	1.0	5.3	ns
		V _{CC} = 3.0 V to 3.6 V	0.9	4.3	0.9	4.8	ns
C_L = 10 pF							
t _{pd}	propagation delay	A, B to Y; see Fig. 4 [1]					
		V _{CC} = 1.1 V to 1.3 V	2.2	13.6	2.2	15.0	ns
		V _{CC} = 1.4 V to 1.6 V	1.8	8.9	1.8	9.8	ns
		V _{CC} = 1.65 V to 1.95 V	1.6	7.2	1.6	7.9	ns
		V _{CC} = 2.3 V to 2.7 V	1.3	5.7	1.3	6.3	ns
		V _{CC} = 3.0 V to 3.6 V	1.2	4.7	1.2	5.2	ns
C_L = 15 pF							
t _{pd}	propagation delay	A, B to Y; see Fig. 4 [1]					
		V _{CC} = 1.1 V to 1.3 V	3.1	15.7	3.1	17.3	ns
		V _{CC} = 1.4 V to 1.6 V	2.1	10.1	2.1	11.2	ns
		V _{CC} = 1.65 V to 1.95 V	1.8	8.2	1.8	9.0	ns
		V _{CC} = 2.3 V to 2.7 V	1.6	6.5	1.6	7.2	ns
		V _{CC} = 3.0 V to 3.6 V	1.5	5.9	1.5	6.5	ns
C_L = 30 pF							
t _{pd}	propagation delay	A, B to Y; see Fig. 4 [1]					
		V _{CC} = 1.1 V to 1.3 V	4.1	21.8	4.1	24.0	ns
		V _{CC} = 1.4 V to 1.6 V	2.9	13.6	2.9	15.0	ns
		V _{CC} = 1.65 V to 1.95 V	2.4	10.9	2.4	12.1	ns
		V _{CC} = 2.3 V to 2.7 V	2.2	8.6	2.2	9.5	ns
		V _{CC} = 3.0 V to 3.6 V	2.1	7.5	2.1	8.3	ns

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

11.1. Waveforms and test circuit



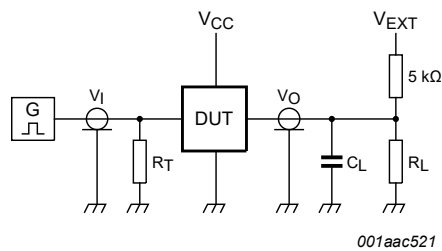
Measurement points are given in [Table 10](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 4. The data input (A or B) to output (Y) propagation delays

Table 10. Measurement points

Supply voltage	Output	Input		
V_{CC}	V_M	V_M	V_I	$t_r = t_f$
0.8 V to 3.6 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{CC}	≤ 3.0 ns



Test data is given in [Table 11](#).

Definitions for test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

Fig. 5. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	Load		V_{EXT}		
V_{CC}	C_L	R_L [1]	t_{PLH} , t_{PHL}	t_{PZH} , t_{PHZ}	t_{PZL} , t_{PLZ}
0.8 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 kΩ or 1 MΩ	open	GND	$2 \times V_{CC}$

[1] For measuring enable and disable times $R_L = 5$ kΩ.

For measuring propagation delays, setup and hold times and pulse width $R_L = 1$ MΩ.

12. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1

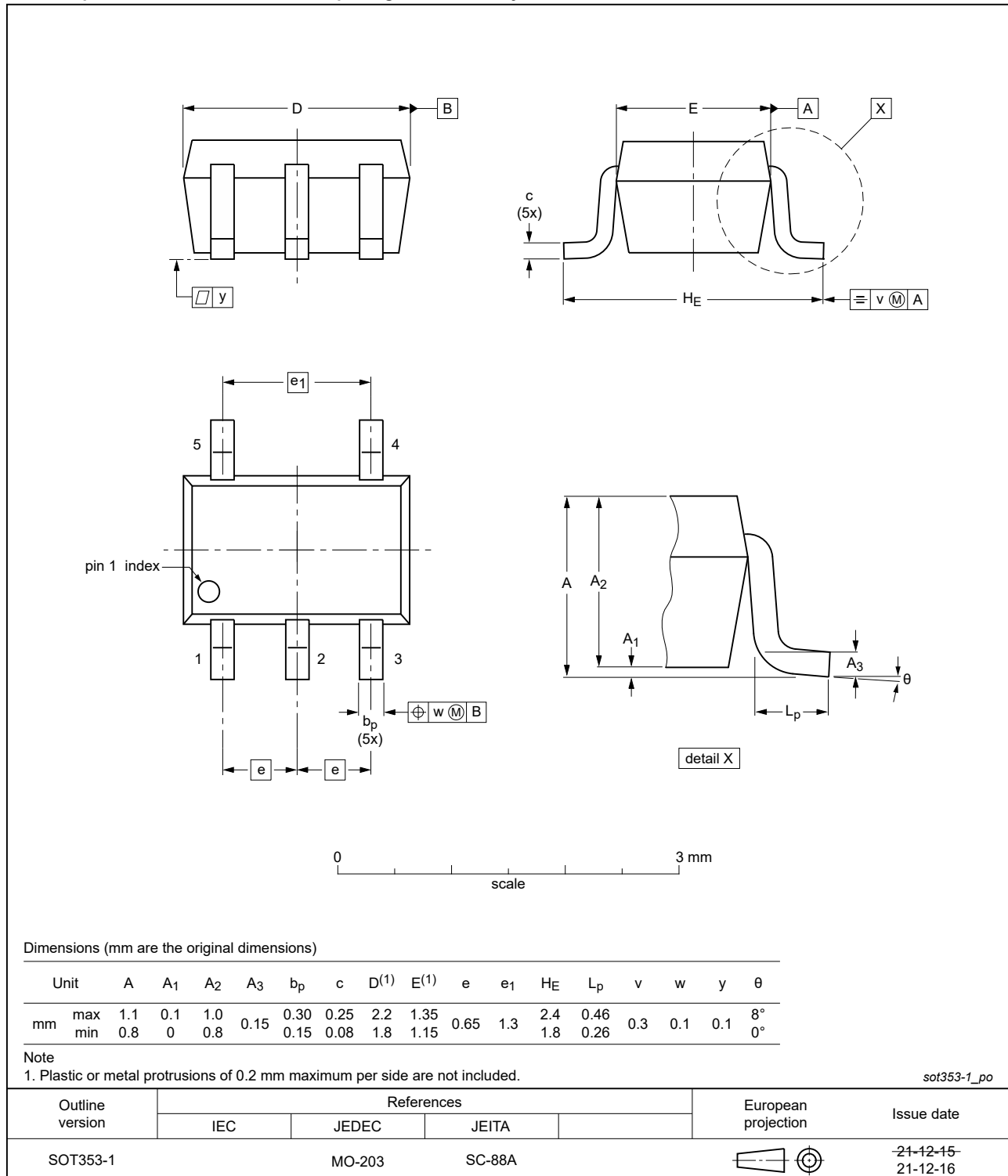


Fig. 6. Package outline SOT353-1 (TSSOP5)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm

SOT886

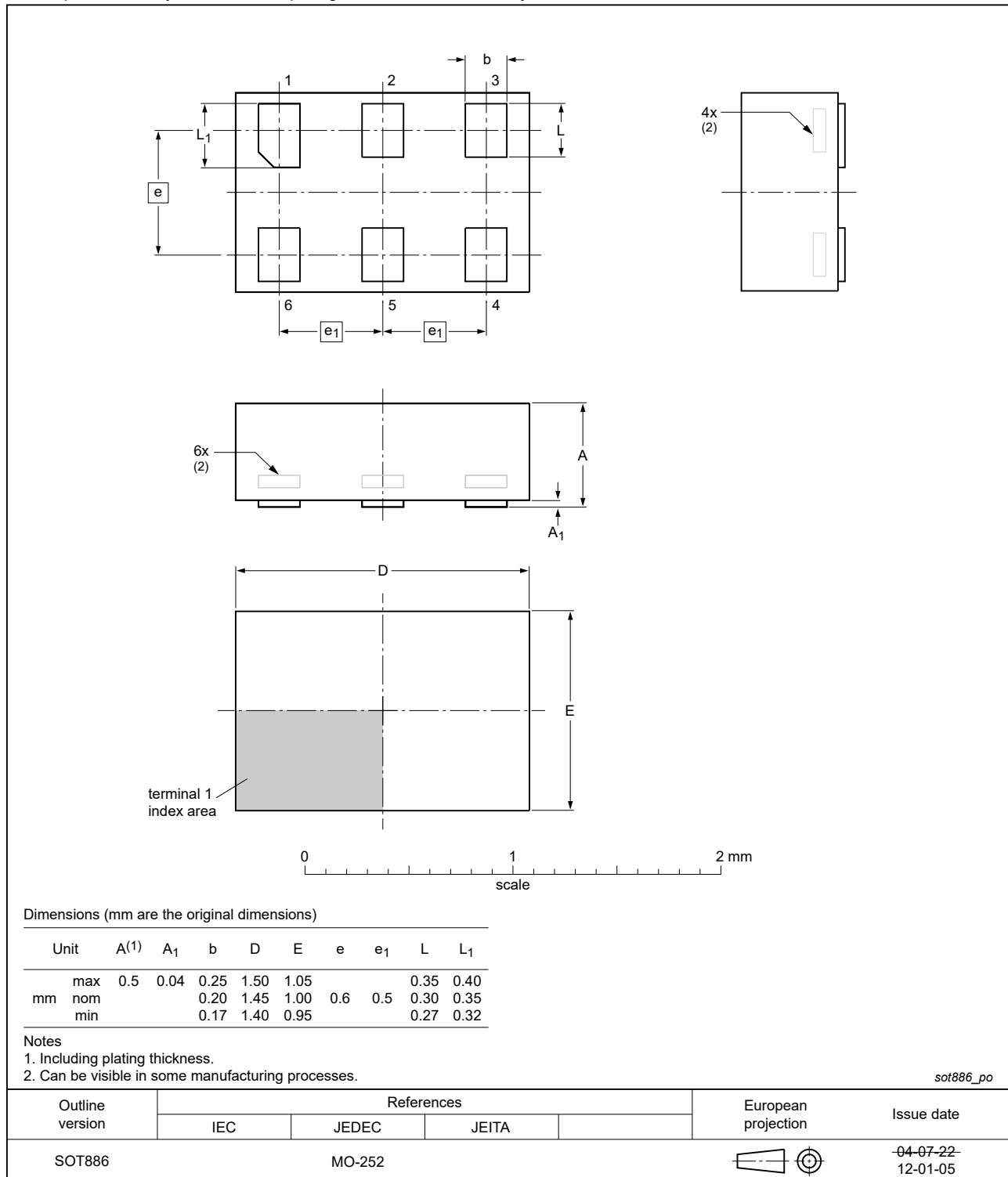
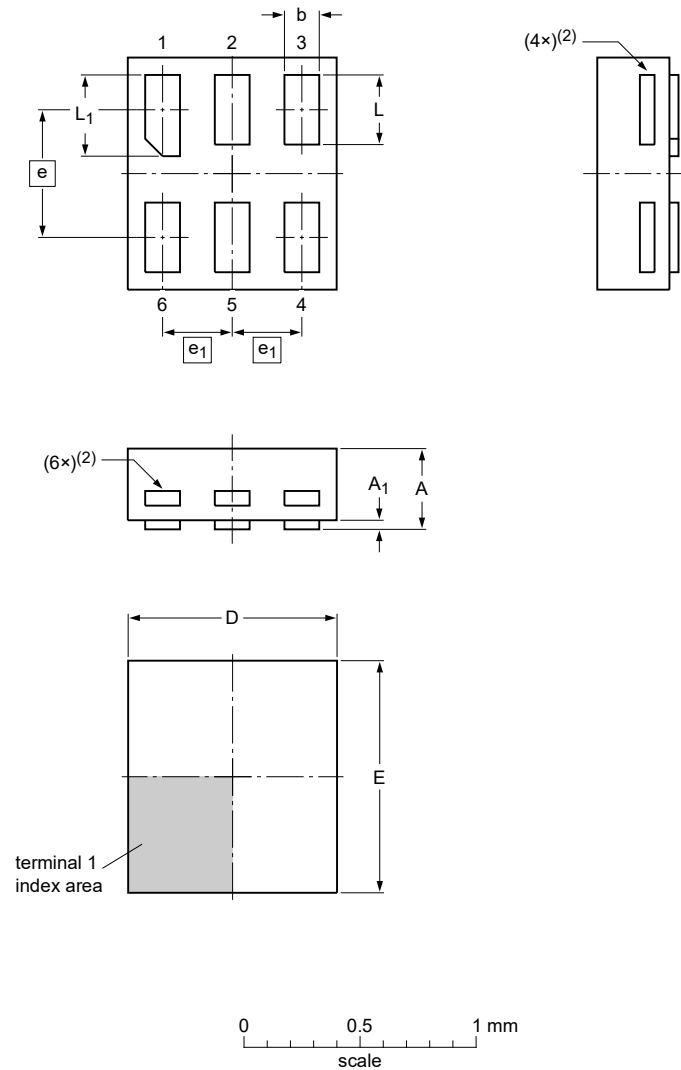


Fig. 7. Package outline SOT886 (XSON6)

**XSON6: extremely thin small outline package; no leads;
6 terminals; body 0.9 x 1.0 x 0.35 mm**

SOT1115



Dimensions

Unit	A ⁽¹⁾	A ₁	b	D	E	e	e ₁	L	L ₁
mm	max 0.35	0.04	0.20	0.95	1.05			0.35	0.40
	nom		0.15	0.90	1.00	0.55	0.3	0.30	0.35
	min		0.12	0.85	0.95			0.27	0.32

Note

- Including plating thickness.
- Visible depending upon used manufacturing technology.

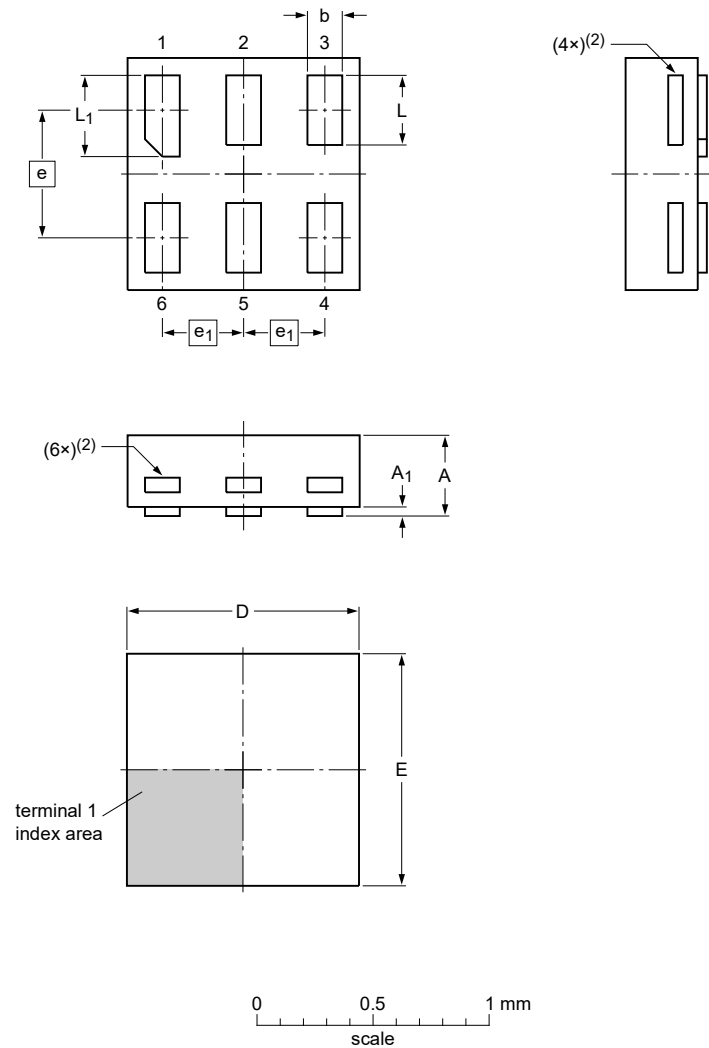
sot1115_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1115						10-04-02 10-04-07

Fig. 8. Package outline SOT1115 (XSON6)

**XSON6: extremely thin small outline package; no leads;
6 terminals; body 1.0 x 1.0 x 0.35 mm**

SOT1202



Dimensions

Unit	A ⁽¹⁾	A ₁	b	D	E	e	e ₁	L	L ₁
mm	max	0.35	0.04	0.20	1.05	1.05		0.35	0.40
	nom			0.15	1.00	1.00	0.55	0.30	0.35
	min			0.12	0.95	0.95		0.27	0.32

Note

- Including plating thickness.
- Visible depending upon used manufacturing technology.

sot1202_po

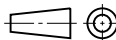
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1202						10-04-02 10-04-06

Fig. 9. Package outline SOT1202 (XSON6)

X2SON5: plastic thermal enhanced extremely thin small outline package; no leads; 5 terminals; body 0.8 x 0.8 x 0.32 mm

SOT1226-3

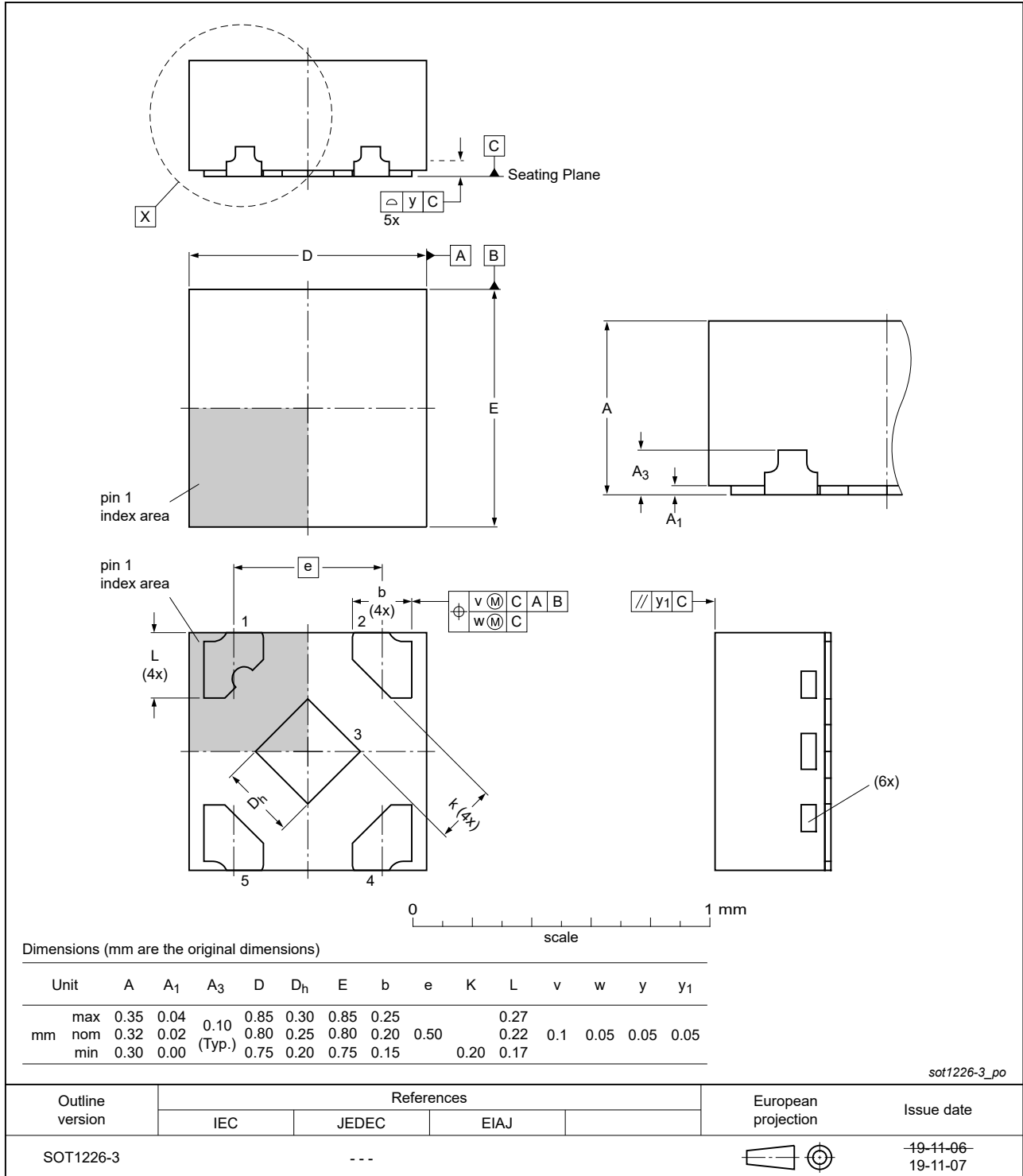


Fig. 10. Package outline SOT1226-3 (X2SON5)

XSON5: Plastic thermal enhanced extremely thin small outline package with side-wettable flanks (SWF); no leads; 5 terminals; body 1.1 × 0.85 × 0.5 mm

SOT8065-1

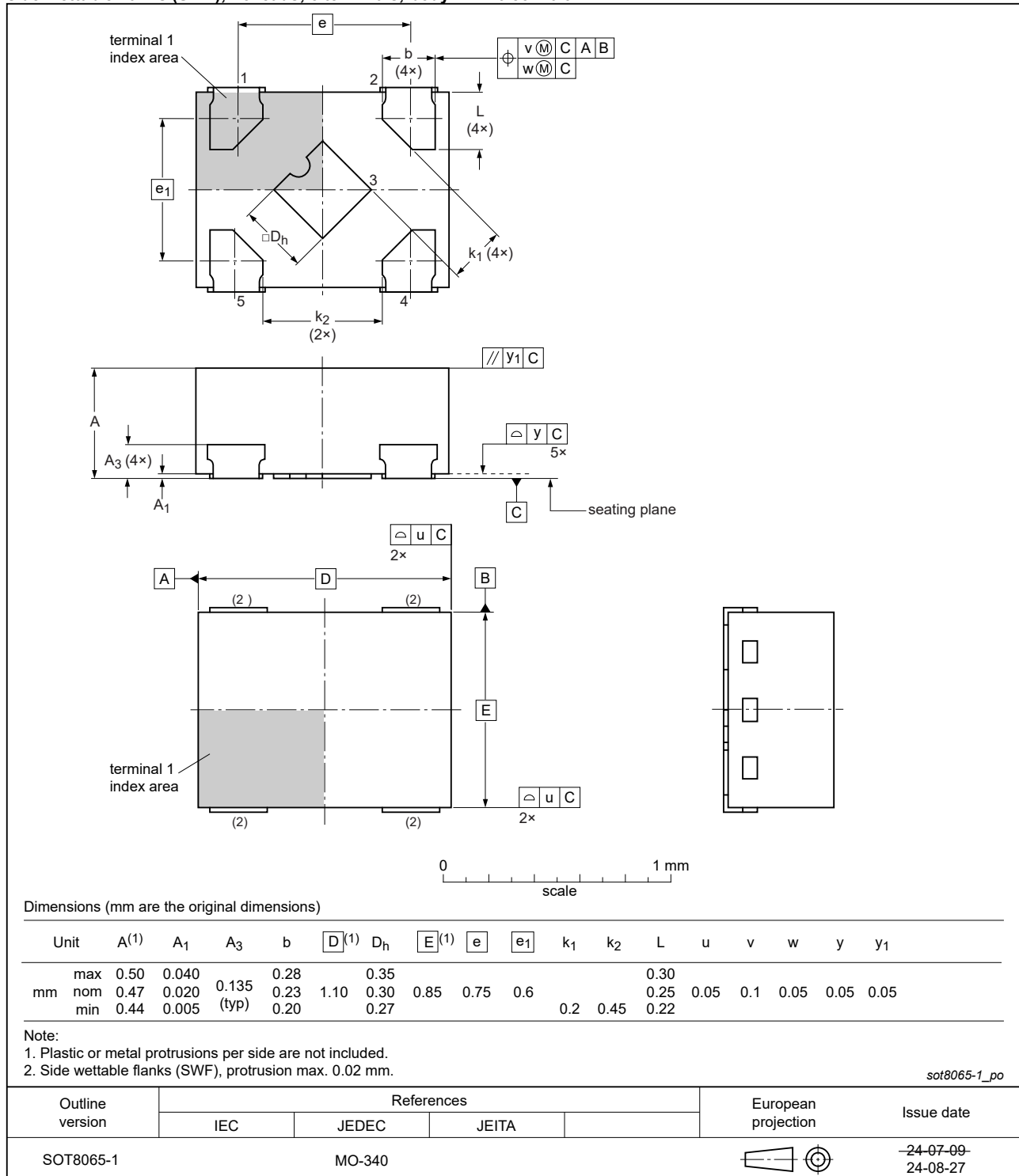


Fig. 11. Package outline SOT8065-1 (XSON5)

13. Abbreviations

Table 12. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council

14. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AUP1G08 v.12.1	20240829	Product data sheet	-	74AUP1G08 v.12
Modifications:	<ul style="list-style-type: none"> Fig. 11: Added JEDEC reference MO-340 to SOT8065-1 package outline drawing. 			
74AUP1G08 v.12	20240712	Product data sheet	-	74AUP1G08 v.11
Modifications:	<ul style="list-style-type: none"> Type number 74AUP1G08GZ (SOT8065-1/XSON5) added. 			
74AUP1G08 v.11	20230712	Product data sheet	-	74AUP1G08 v.10
Modifications:	<ul style="list-style-type: none"> Section 2: ESD specification updated according to the latest JEDEC standard. 			
74AUP1G08 v.10	20220113	Product data sheet	-	74AUP1G08 v.9
Modifications:	<ul style="list-style-type: none"> Section 1 and Section 2 updated. Fig. 6: Package outline drawing for SOT353-1(TSSOP5) has changed 			
74AUP1G08 v.9	20210805	Product data sheet	-	74AUP1G08 v.8
Modifications:	<ul style="list-style-type: none"> Section 1 and Section 2 updated. Type number 74AUP1G08GF (SOT891/XSON6) removed. 			
74AUP1G08 v.8	20210421	Product data sheet	-	74AUP1G08 v.7
Modifications:	<ul style="list-style-type: none"> SOT1226 (X2SON5) package changed to SOT1226-3 (X2SON5) package. Table 5: Derating values for P_{tot} total power dissipation updated. 			
74AUP1G08 v.7	20171130	Product data sheet	-	74AUP1G08 v.6
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 			
74AUP1G08 v.6	20120622	Product data sheet	-	74AUP1G08 v.5
Modifications:	<ul style="list-style-type: none"> Package outline drawing of SOT1226 modified. 			
74AUP1G08 v.5	20120412	Product data sheet	-	74AUP1G08 v.4
Modifications:	<ul style="list-style-type: none"> Added type number 74AUP1G08GX (SOT1226) Package outline drawing of SOT886 (Fig. 7) modified. 			
74AUP1G08 v.4	20111115	Product data sheet	-	74AUP1G08 v.3
Modifications:	<ul style="list-style-type: none"> Legal pages updated. 			
74AUP1G08 v.3	20101007	Product data sheet	-	74AUP1G08 v.2

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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