

74AUP1G58GXZ Datasheet

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DiGi Electronics Part Number	74AUP1G58GXZ-DG
Manufacturer	Nexperia USA Inc.
Manufacturer Product Number	74AUP1G58GXZ
Description	IC GATE CONFIG MULTI-FUNC X2SON6
Detailed Description	Configurable Multiple Function Configurable 1 Circuit 3 Input 6-X2SON (1.0x0.8)



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Purchase and inquiry

Manufacturer Product Number:

74AUP1G58GXZ

Series:

74AUP

Logic Type:

Configurable Multiple Function

Number of Inputs:

3

Output Type:

Single-Ended

Voltage - Supply:

0.8V ~ 3.6V

Mounting Type:

Surface Mount

Supplier Device Package:

6-X2SON (1.0x0.8)

Manufacturer:

Nexperia USA Inc.

Product Status:

Active

Number of Circuits:

1

Schmitt Trigger Input:

No

Current - Output High, Low:

4mA, 4mA

Operating Temperature:

-40°C ~ 125°C

Package / Case:

6-XFDN

Base Product Number:

74AUP1G58

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

74AUP1G58

Low-power configurable multiple function gate

Rev. 10 — 24 July 2023

Product data sheet

1. General description

The 74AUP1G58 is a configurable multiple function gate with Schmitt-trigger inputs. The device can be configured as any of the following logic functions AND, OR, NAND, NOR, XOR, inverter and buffer; using the 3-bit input. All inputs can be connected directly to V_{CC} or GND. This device ensures very low static and dynamic power consumption across the entire V_{CC} range from 0.8 V to 3.6 V. This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 0.8 V to 3.6 V
- CMOS low power dissipation
- High noise immunity
- Low static power consumption; $I_{CC} = 0.9 \mu\text{A}$ (maximum)
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Overvoltage tolerant inputs to 3.6 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- I_{OFF} circuitry provides partial power-down mode operation
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 3A exceeds 5000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AUP1G58GW	-40 °C to +125 °C	TSSOP6	plastic thin shrink small outline package; 6 leads; body width 1.25 mm	SOT363-2
74AUP1G58GM	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886
74AUP1G58GN	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 0.9 × 1.0 × 0.35 mm	SOT1115
74AUP1G58GS	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 1.0 × 1.0 × 0.35 mm	SOT1202
74AUP1G58GX	-40 °C to +125 °C	X2SON6	plastic thermal enhanced extremely thin small outline package; no leads; 6 terminals; body 1.0 × 0.8 × 0.32 mm	SOT1255-2

4. Marking

Table 2. Marking

Type number	Marking code [1]
74AUP1G58GW	aK
74AUP1G58GM	aK
74AUP1G58GN	aK
74AUP1G58GS	aK
74AUP1G58GX	aK

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

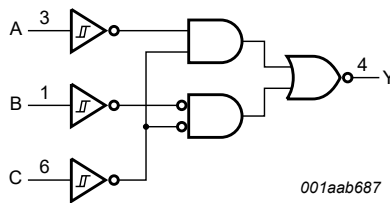


Fig. 1. Logic symbol

6. Pinning information

6.1. Pinning

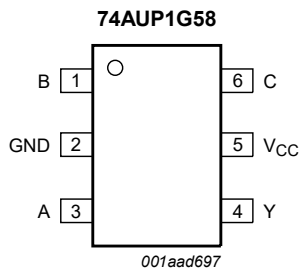


Fig. 2. Pin configuration SOT363-2 (TSSOP6)

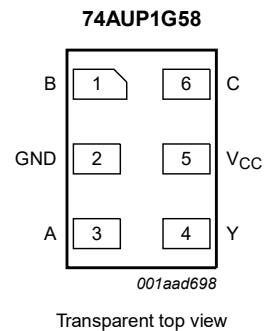


Fig. 3. Pin configuration SOT886 (XSON6)

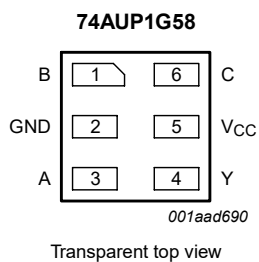


Fig. 4. Pin configuration SOT1115 and SOT1202 (XSON6)

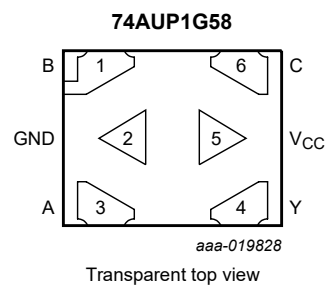


Fig. 5. Pin configuration SOT1255-2 (X2SON6)

6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
B	1	data input
GND	2	ground (0 V)
A	3	data input
Y	4	data output
V _{CC}	5	supply voltage
C	6	data input

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input			Output
C	B	A	Y
L	L	L	L
L	L	H	H
L	H	L	L
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	L
H	H	H	L

7.1. Logic configurations

Table 5. Function selection table

Logic function	Figure
2-input NAND	see Fig. 6
2-input NAND with both inputs inverted	see Fig. 9
2-input AND with inverted input	see Fig. 7 and Fig. 8
2-input NOR with inverted input	see Fig. 7 and Fig. 8
2-input OR	see Fig. 9
2-input OR with both inputs inverted	see Fig. 6
2-input XOR	see Fig. 10
Buffer	see Fig. 11
Inverter	see Fig. 12

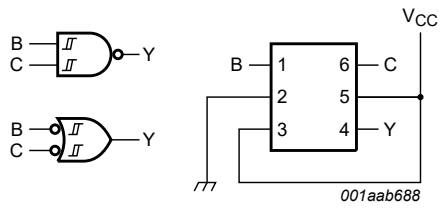


Fig. 6. 2-input NAND gate or 2-input OR with both inputs inverted

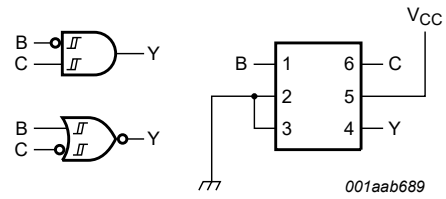


Fig. 7. 2-input AND gate with inverted B input or 2-input NOR gate with inverted C input

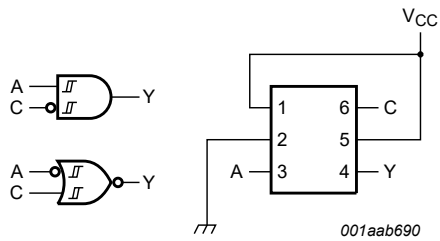


Fig. 8. 2-input AND gate with inverted C input or 2-input NOR gate with inverted A input

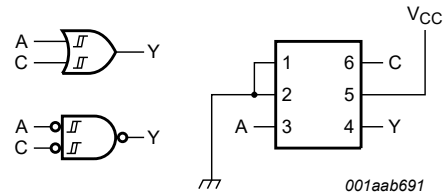


Fig. 9. 2-input OR gate or 2-input NAND gate with both inputs inverted

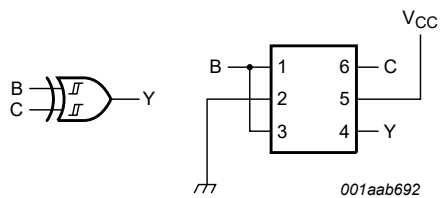


Fig. 10. 2-input XOR gate

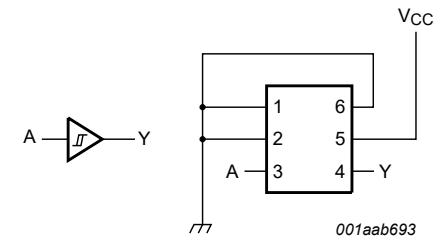


Fig. 11. Buffer

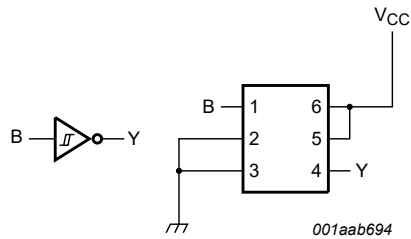


Fig. 12. Inverter

8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
V_I	input voltage		[1] -0.5	+4.6	V
I_{OK}	output clamping current	$V_O < 0$ V	-50	-	mA
V_O	output voltage	Active mode and Power-down mode	[1] -0.5	+4.6	V
I_O	output current	$V_O = 0$ V to V_{CC}	-	±20	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[2] -	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT363-2 (TSSOP6) package: P_{tot} derates linearly with 3.7 mW/K above 83 °C.

For SOT886 (XSON6) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.

For SOT1115 (XSON6) package: P_{tot} derates linearly with 3.2 mW/K above 71 °C.

For SOT1202 (XSON6) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.

For SOT1255-2 (X2SON6) package: P_{tot} derates linearly with 3.3 mW/K above 75 °C.

9. Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		0.8	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	Active mode	0	V_{CC}	V
		Power-down mode; $V_{CC} = 0$ V	0	3.6	V
T_{amb}	ambient temperature		-40	+125	°C

10. Static characteristics

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V _{OH}	HIGH-level output voltage	V _I = V _{T+} or V _{T-}				
		I _O = -20 μA; V _{CC} = 0.8 V to 3.6 V	V _{CC} - 0.1	-	-	V
		I _O = -1.1 mA; V _{CC} = 1.1 V	0.75 × V _{CC}	-	-	V
		I _O = -1.7 mA; V _{CC} = 1.4 V	1.11	-	-	V
		I _O = -1.9 mA; V _{CC} = 1.65 V	1.32	-	-	V
		I _O = -2.3 mA; V _{CC} = 2.3 V	2.05	-	-	V
		I _O = -3.1 mA; V _{CC} = 2.3 V	1.9	-	-	V
		I _O = -2.7 mA; V _{CC} = 3.0 V	2.72	-	-	V
	I _O = -4.0 mA; V _{CC} = 3.0 V	2.6	-	-	V	
V _{OL}	LOW-level output voltage	V _I = V _{T+} or V _{T-}				
		I _O = 20 μA; V _{CC} = 0.8 V to 3.6 V	-	-	0.1	V
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	-	0.3 × V _{CC}	V
		I _O = 1.7 mA; V _{CC} = 1.4 V	-	-	0.31	V
		I _O = 1.9 mA; V _{CC} = 1.65 V	-	-	0.31	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.31	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.44	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.31	V
	I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.44	V	
I _I	input leakage current	V _I = GND to 3.6 V; V _{CC} = 0 V to 3.6 V	-	-	±0.1	μA
I _{OFF}	power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±0.2	μA
ΔI _{OFF}	additional power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V to 0.2 V	-	-	±0.2	μA
I _{CC}	supply current	V _I = GND or V _{CC} ; I _O = 0 A; V _{CC} = 0.8 V to 3.6 V	-	-	0.5	μA
ΔI _{CC}	additional supply current	V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 3.3 V	-	-	40	μA
C _I	input capacitance	V _I = GND or V _{CC} ; V _{CC} = 0 V to 3.6 V	-	1.1	-	pF
C _O	output capacitance	V _O = GND; V _{CC} = 0 V	-	1.8	-	pF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +85 °C						
V _{OH}	HIGH-level output voltage	V _I = V _{T+} or V _{T-}				
		I _O = -20 μA; V _{CC} = 0.8 V to 3.6 V	V _{CC} - 0.1	-	-	V
		I _O = -1.1 mA; V _{CC} = 1.1 V	0.7 × V _{CC}	-	-	V
		I _O = -1.7 mA; V _{CC} = 1.4 V	1.03	-	-	V
		I _O = -1.9 mA; V _{CC} = 1.65 V	1.30	-	-	V
		I _O = -2.3 mA; V _{CC} = 2.3 V	1.97	-	-	V
		I _O = -3.1 mA; V _{CC} = 2.3 V	1.85	-	-	V
		I _O = -2.7 mA; V _{CC} = 3.0 V	2.67	-	-	V
I _O = -4.0 mA; V _{CC} = 3.0 V	2.55	-	-	V		
V _{OL}	LOW-level output voltage	V _I = V _{T+} or V _{T-}				
		I _O = 20 μA; V _{CC} = 0.8 V to 3.6 V	-	-	0.1	V
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	-	0.3 × V _{CC}	V
		I _O = 1.7 mA; V _{CC} = 1.4 V	-	-	0.37	V
		I _O = 1.9 mA; V _{CC} = 1.65 V	-	-	0.35	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.33	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.45	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.33	V
I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.45	V		
I _I	input leakage current	V _I = GND to 3.6 V; V _{CC} = 0 V to 3.6 V	-	-	±0.5	μA
I _{OFF}	power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±0.5	μA
ΔI _{OFF}	additional power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V to 0.2 V	-	-	±0.6	μA
I _{CC}	supply current	V _I = GND or V _{CC} ; I _O = 0 A; V _{CC} = 0.8 V to 3.6 V	-	-	0.9	μA
ΔI _{CC}	additional supply current	V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 3.3 V	-	-	50	μA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +125 °C						
V _{OH}	HIGH-level output voltage	V _I = V _{T+} or V _{T-}				
		I _O = -20 μA; V _{CC} = 0.8 V to 3.6 V	V _{CC} - 0.11	-	-	V
		I _O = -1.1 mA; V _{CC} = 1.1 V	0.6 × V _{CC}	-	-	V
		I _O = -1.7 mA; V _{CC} = 1.4 V	0.93	-	-	V
		I _O = -1.9 mA; V _{CC} = 1.65 V	1.17	-	-	V
		I _O = -2.3 mA; V _{CC} = 2.3 V	1.77	-	-	V
		I _O = -3.1 mA; V _{CC} = 2.3 V	1.67	-	-	V
		I _O = -2.7 mA; V _{CC} = 3.0 V	2.40	-	-	V
I _O = -4.0 mA; V _{CC} = 3.0 V	2.30	-	-	V		
V _{OL}	LOW-level output voltage	V _I = V _{T+} or V _{T-}				
		I _O = 20 μA; V _{CC} = 0.8 V to 3.6 V	-	-	0.11	V
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	-	0.33 × V _{CC}	V
		I _O = 1.7 mA; V _{CC} = 1.4 V	-	-	0.41	V
		I _O = 1.9 mA; V _{CC} = 1.65 V	-	-	0.39	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.36	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.50	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.36	V
I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.50	V		
I _I	input leakage current	V _I = GND to 3.6 V; V _{CC} = 0 V to 3.6 V	-	-	±0.75	μA
I _{OFF}	power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±0.75	μA
ΔI _{OFF}	additional power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V to 0.2 V	-	-	±0.75	μA
I _{CC}	supply current	V _I = GND or V _{CC} ; I _O = 0 A; V _{CC} = 0.8 V to 3.6 V	-	-	1.4	μA
ΔI _{CC}	additional supply current	V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 3.3 V	-	-	75	μA

11. Dynamic characteristics

Table 9. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 14.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
C_L = 5 pF										
t _{pd}	propagation delay	A, B and C to Y; see Fig. 13 [2]								
		V _{CC} = 0.8 V	-	22.8	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	2.8	6.6	12.9	2.6	13.1	2.6	13.3	ns
		V _{CC} = 1.4 V to 1.6 V	2.4	4.8	7.6	2.4	8.3	2.4	8.6	ns
		V _{CC} = 1.65 V to 1.95 V	2.1	4.0	6.3	2.0	6.9	2.0	7.3	ns
		V _{CC} = 2.3 V to 2.7 V	2.0	3.2	4.6	1.8	5.1	1.8	5.4	ns
		V _{CC} = 3.0 V to 3.6 V	1.9	2.9	3.9	1.6	4.2	1.6	4.4	ns

Low-power configurable multiple function gate

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
C_L = 10 pF										
t _{pd}	propagation delay	A, B and C to Y; see Fig. 13 [2]								
		V _{CC} = 0.8 V	-	26.4	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	3.2	7.4	14.5	3.0	14.9	3.0	15.2	ns
		V _{CC} = 1.4 V to 1.6 V	2.7	5.4	8.7	2.7	9.4	2.7	9.8	ns
		V _{CC} = 1.65 V to 1.95 V	2.5	4.5	7.1	2.3	7.9	2.3	8.3	ns
		V _{CC} = 2.3 V to 2.7 V	2.4	3.8	5.3	2.2	5.9	2.2	6.2	ns
V _{CC} = 3.0 V to 3.6 V	2.3	3.5	4.6	1.9	4.9	1.9	5.1	ns		
C_L = 15 pF										
t _{pd}	propagation delay	A, B and C to Y; see Fig. 13 [2]								
		V _{CC} = 0.8 V	-	29.9	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	3.6	8.3	16.1	3.3	16.7	3.3	17.0	ns
		V _{CC} = 1.4 V to 1.6 V	3.0	5.9	9.7	3.0	10.5	3.0	11.0	ns
		V _{CC} = 1.65 V to 1.95 V	2.8	5.0	7.9	2.5	8.7	2.5	9.2	ns
		V _{CC} = 2.3 V to 2.7 V	2.7	4.2	5.9	2.5	6.6	2.5	6.9	ns
V _{CC} = 3.0 V to 3.6 V	2.5	3.9	5.2	2.2	5.5	2.2	5.8	ns		
C_L = 30 pF										
t _{pd}	propagation delay	A, B and C to Y; see Fig. 13 [2]								
		V _{CC} = 0.8 V	-	38.0	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	4.5	10.5	20.8	4.1	21.9	4.1	24.1	ns
		V _{CC} = 1.4 V to 1.6 V	3.8	7.5	12.2	3.8	13.5	3.8	14.1	ns
		V _{CC} = 1.65 V to 1.95 V	3.4	6.3	10.0	3.1	11.2	3.1	11.9	ns
		V _{CC} = 2.3 V to 2.7 V	3.4	5.3	7.5	3.1	8.4	3.1	8.9	ns
V _{CC} = 3.0 V to 3.6 V	3.3	5.0	6.6	2.9	7.1	2.9	7.4	ns		
C_L = 5 pF, 10 pF, 15 pF and 30 pF										
C _{PD}	power dissipation capacitance	f _i = 1 MHz; V _I = GND to V _{CC} [3][4]								
		V _{CC} = 0.8 V	-	2.7	-	-	-	-	-	pF
		V _{CC} = 1.1 V to 1.3 V	-	2.8	-	-	-	-	-	pF
		V _{CC} = 1.4 V to 1.6 V	-	3.0	-	-	-	-	-	pF
		V _{CC} = 1.65 V to 1.95 V	-	3.2	-	-	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V	-	3.8	-	-	-	-	-	pF
V _{CC} = 3.0 V to 3.6 V	-	4.4	-	-	-	-	-	pF		

[1] All typical values are measured at nominal V_{CC}.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] All specified values are the average typical values over all stated loads.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

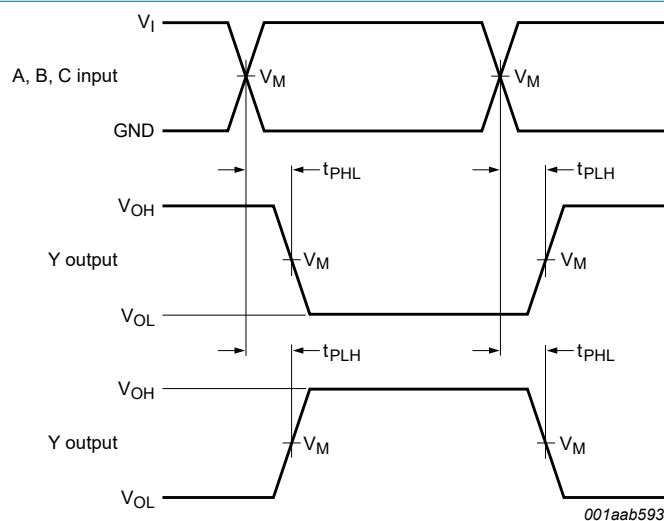
C_L = load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

Σ(C_L × V_{CC}² × f_o) = sum of the outputs.

11.1. Waveforms and test circuit



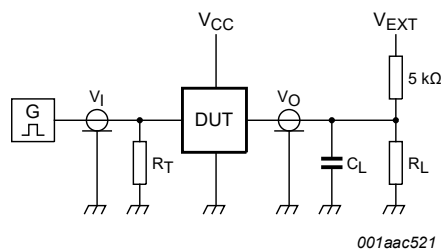
Measurement points are given in [Table 10](#).

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig. 13. Input A, B and C to output Y propagation delay times

Table 10. Measurement points

Supply voltage	Output	Input		
V_{CC}	V_M	V_M	V_I	$t_r = t_f$
0.8 V to 3.6 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{CC}	≤ 3.0 ns



Test data is given in [Table 11](#).

Definitions for test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

Fig. 14. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	Load		V_{EXT}			
V_{CC}	C_L	R_L [1]	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}	
0.8 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 kΩ or 1 MΩ	open	GND	$2 \times V_{CC}$	

[1] For measuring enable and disable times $R_L = 5$ kΩ.

For measuring propagation delays, setup and hold times and pulse width $R_L = 1$ MΩ.

12. Transfer characteristics

Table 12. Transfer characteristics

Voltages are referenced to GND (ground = 0 V; for test circuit see Fig. 14).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{T+}	positive-going threshold voltage	see Fig. 15 and Fig. 16								
		$V_{CC} = 0.8 \text{ V}$	0.30	-	0.60	0.30	0.60	0.30	0.62	V
		$V_{CC} = 1.1 \text{ V}$	0.53	-	0.90	0.53	0.90	0.53	0.92	V
		$V_{CC} = 1.4 \text{ V}$	0.74	-	1.11	0.74	1.11	0.74	1.13	V
		$V_{CC} = 1.65 \text{ V}$	0.91	-	1.29	0.91	1.29	0.91	1.31	V
		$V_{CC} = 2.3 \text{ V}$	1.37	-	1.77	1.37	1.77	1.37	1.80	V
		$V_{CC} = 3.0 \text{ V}$	1.88	-	2.29	1.88	2.29	1.88	2.32	V
V_{T-}	negative-going threshold voltage	see Fig. 15 and Fig. 16								
		$V_{CC} = 0.8 \text{ V}$	0.10	-	0.60	0.10	0.60	0.10	0.60	V
		$V_{CC} = 1.1 \text{ V}$	0.26	-	0.65	0.26	0.65	0.26	0.65	V
		$V_{CC} = 1.4 \text{ V}$	0.39	-	0.75	0.39	0.75	0.39	0.75	V
		$V_{CC} = 1.65 \text{ V}$	0.47	-	0.84	0.47	0.84	0.47	0.84	V
		$V_{CC} = 2.3 \text{ V}$	0.69	-	1.04	0.69	1.04	0.69	1.04	V
		$V_{CC} = 3.0 \text{ V}$	0.88	-	1.24	0.88	1.24	0.88	1.24	V
V_H	hysteresis voltage	$(V_{T+} - V_{T-})$; see Fig. 15, Fig. 16, Fig. 17 and Fig. 18								
		$V_{CC} = 0.8 \text{ V}$	0.07	-	0.50	0.07	0.50	0.07	0.50	V
		$V_{CC} = 1.1 \text{ V}$	0.08	-	0.46	0.08	0.46	0.08	0.46	V
		$V_{CC} = 1.4 \text{ V}$	0.18	-	0.56	0.18	0.56	0.18	0.56	V
		$V_{CC} = 1.65 \text{ V}$	0.27	-	0.66	0.27	0.66	0.27	0.66	V
		$V_{CC} = 2.3 \text{ V}$	0.53	-	0.92	0.53	0.92	0.53	0.92	V
		$V_{CC} = 3.0 \text{ V}$	0.79	-	1.31	0.79	1.31	0.79	1.31	V

12.1. Waveforms transfer characteristics

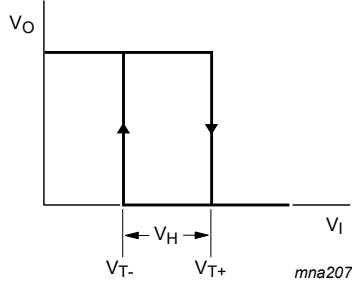


Fig. 15. Transfer characteristic

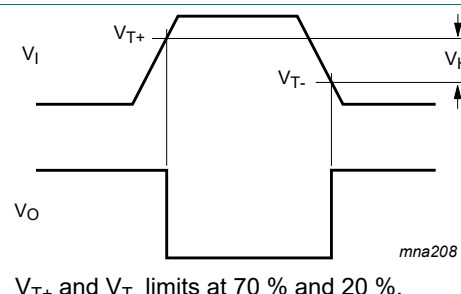
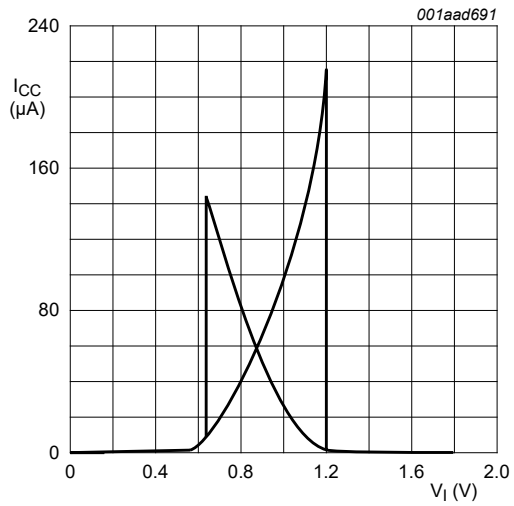
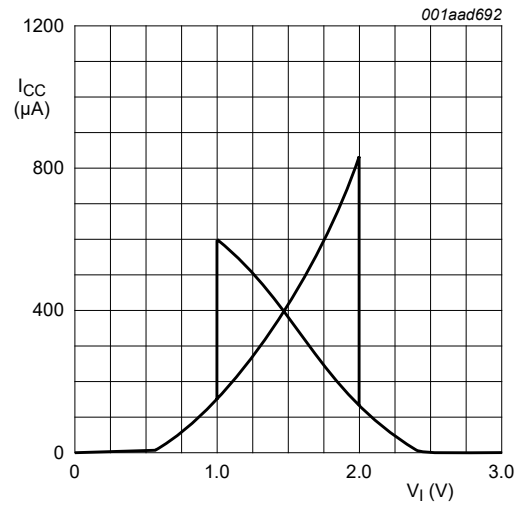


Fig. 16. Definition of V_{T+} , V_{T-} and V_H

Fig. 17. Typical transfer characteristics; $V_{CC} = 1.8\text{ V}$ Fig. 18. Typical transfer characteristics; $V_{CC} = 3.0\text{ V}$

13. Package outline

TSSOP6: plastic thin shrink small outline package; 6 leads; body width 1.25 mm

SOT363-2

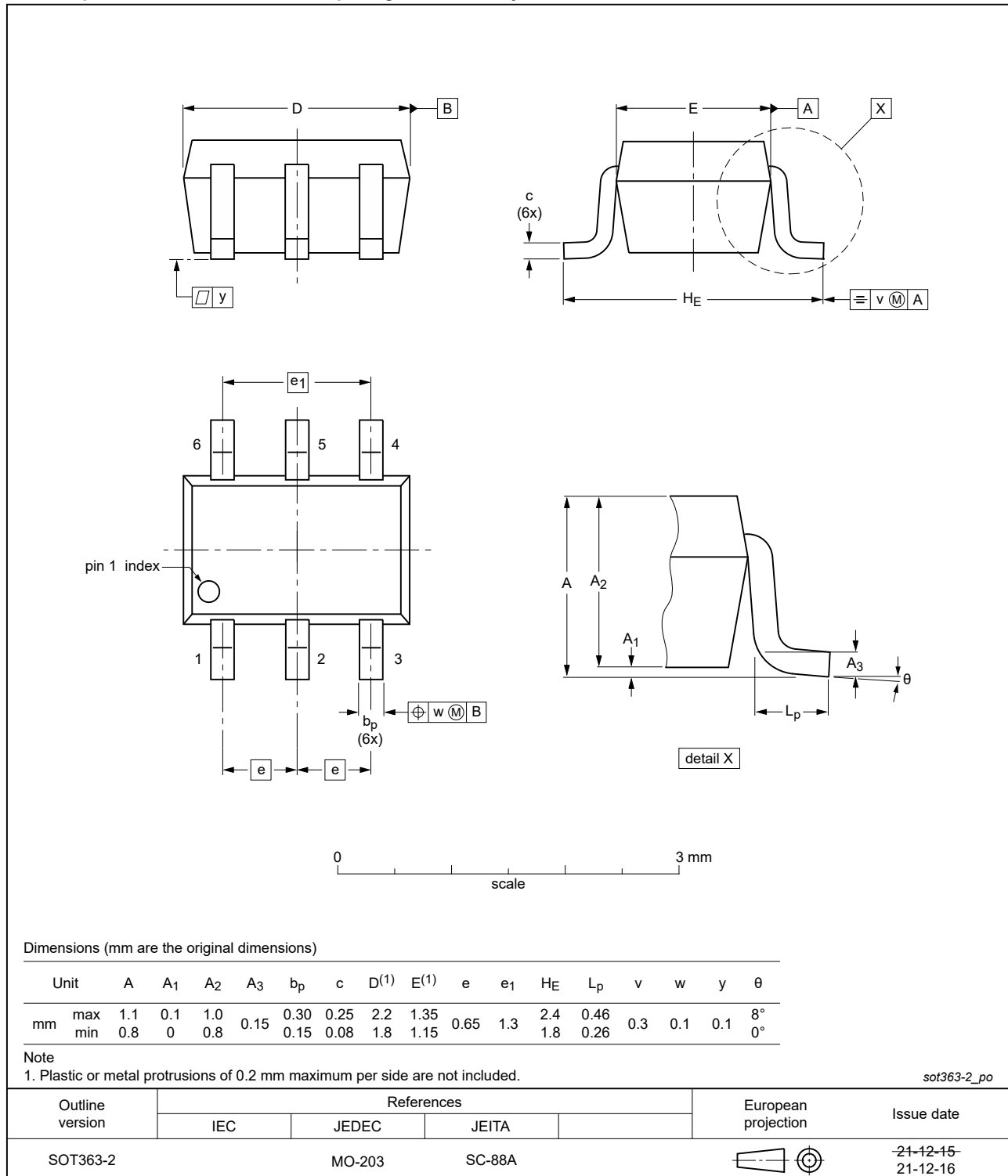


Fig. 19. Package outline SOT363-2 (TSSOP6)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm

SOT886

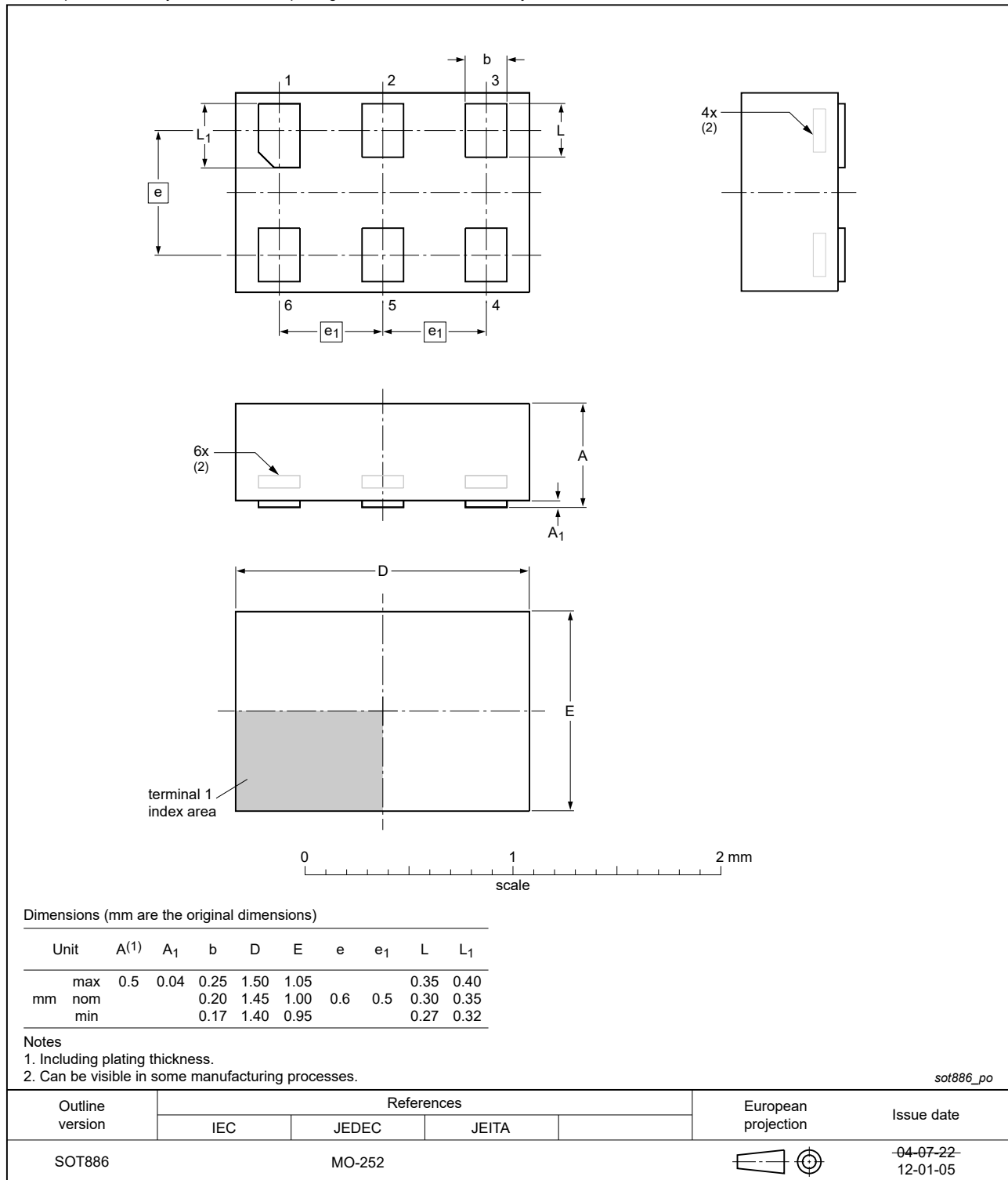
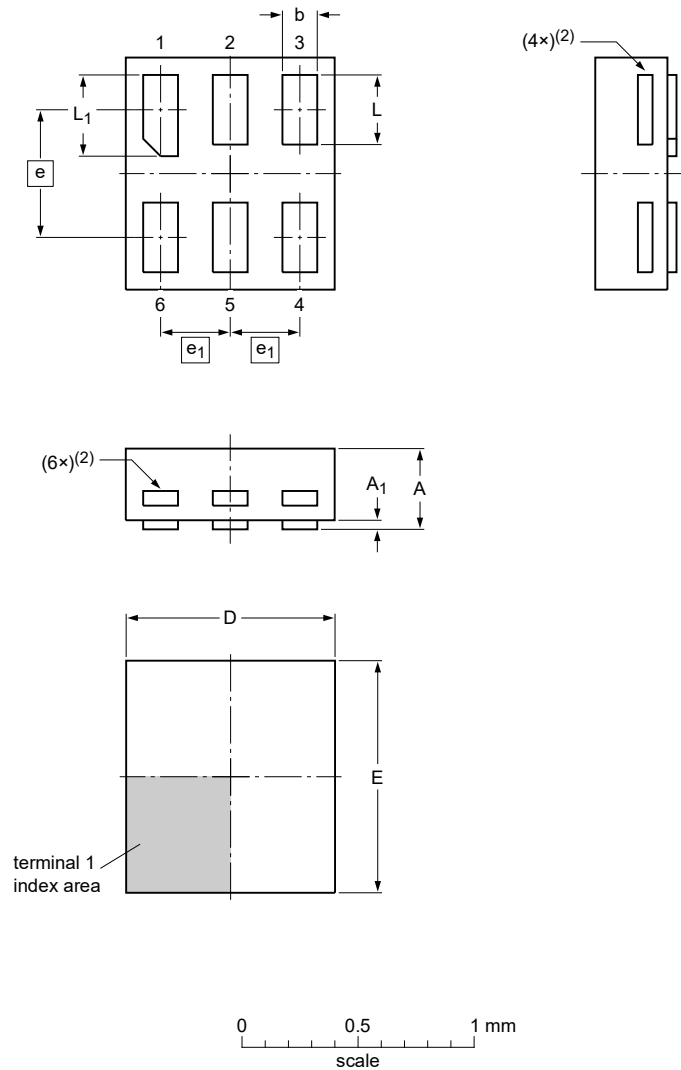


Fig. 20. Package outline SOT886 (XSON6)

**XSON6: extremely thin small outline package; no leads;
6 terminals; body 0.9 x 1.0 x 0.35 mm**

SOT1115



Dimensions

Unit	A ⁽¹⁾	A ₁	b	D	E	e	e ₁	L	L ₁
mm	max 0.35	0.04	0.20	0.95	1.05			0.35	0.40
	nom		0.15	0.90	1.00	0.55	0.3	0.30	0.35
	min		0.12	0.85	0.95			0.27	0.32

Note

- Including plating thickness.
- Visible depending upon used manufacturing technology.

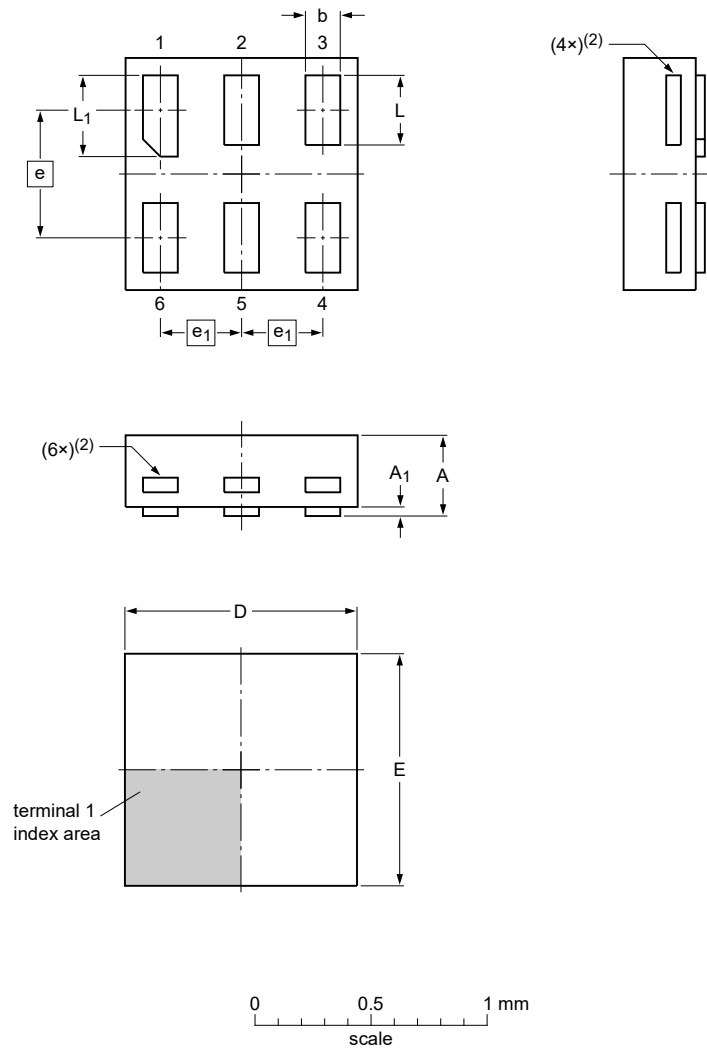
sot1115_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1115					10-04-02 10-04-07

Fig. 21. Package outline SOT1115 (XSON6)

**XSON6: extremely thin small outline package; no leads;
6 terminals; body 1.0 x 1.0 x 0.35 mm**

SOT1202



Dimensions

Unit	A ⁽¹⁾	A ₁	b	D	E	e	e ₁	L	L ₁
mm	max	0.35	0.04	0.20	1.05	1.05		0.35	0.40
	nom			0.15	1.00	1.00	0.55	0.30	0.35
	min			0.12	0.95	0.95		0.27	0.32

Note

- Including plating thickness.
- Visible depending upon used manufacturing technology.

sot1202_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1202						10-04-02 10-04-06

Fig. 22. Package outline SOT1202 (XSON6)

**X2SON6: plastic thermal enhanced extremely thin small outline package; no leads;
6 terminals; body 1.0 x 0.8 x 0.32 mm**

SOT1255-2

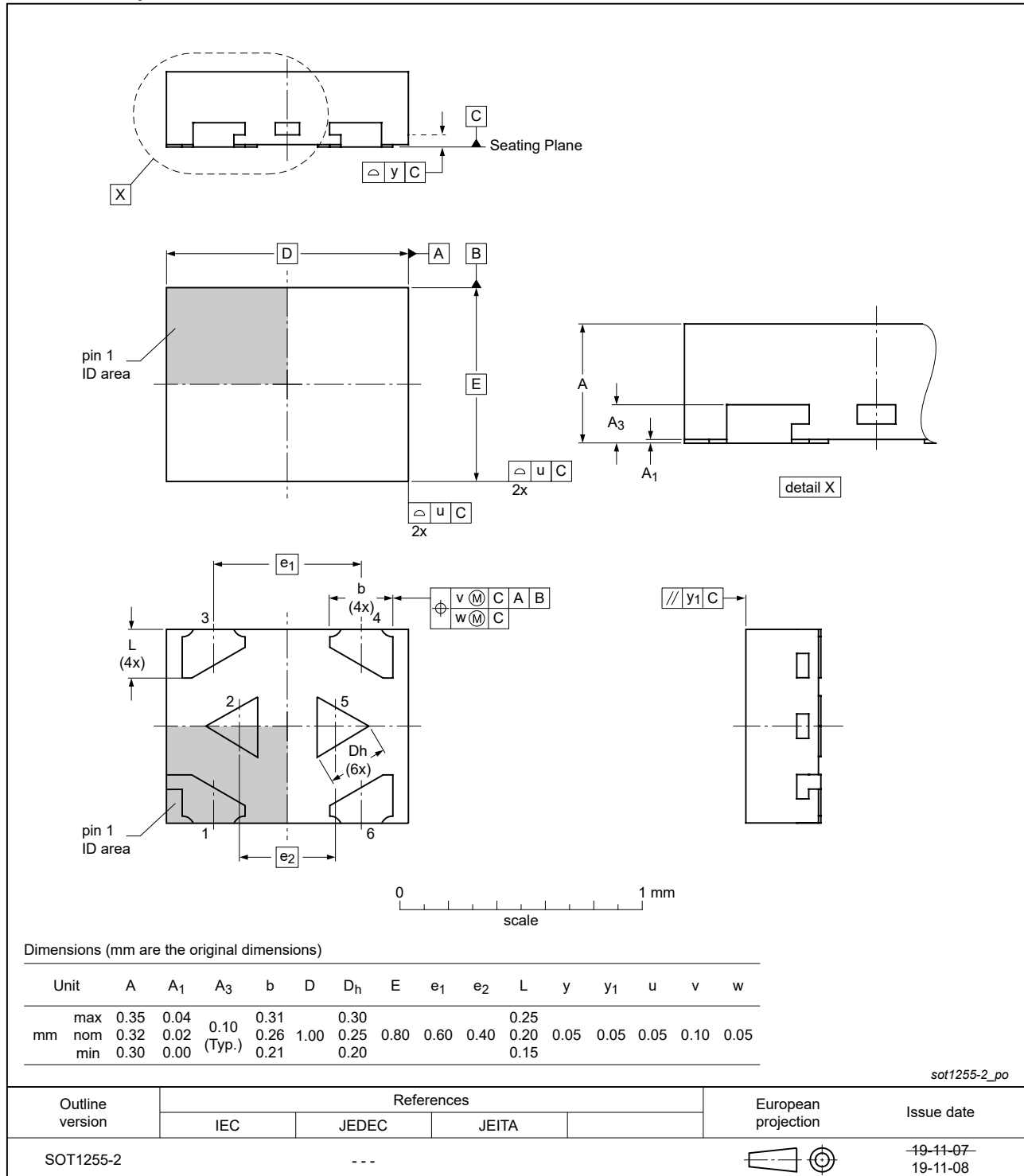


Fig. 23. Package outline SOT1255-2 (X2SON6)

14. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

15. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AUP1G58 v.10	20230724	Product data sheet	-	74AUP1G58 v.9
Modifications:	<ul style="list-style-type: none"> Section 2: ESD specification updated according to the latest JEDEC standard. 			
74AUP1G58 v.9	20220124	Product data sheet	-	74AUP1G58 v.8
Modifications:	<ul style="list-style-type: none"> SOT363 (SC-88) package changed to SOT363-2 (TSSOP6) package. 			
74AUP1G58 v.8	20210713	Product data sheet	-	74AUP1G58 v.7
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. SOT1255 (X2SON6) package changed to SOT1255-2 (X2SON6) package. Type number 74AUP1G58GF (SOT891/XSON6) removed. Section 1 and Section 2 updated. Table 6: Derating values for P_{tot} total power dissipation updated. 			
74AUP1G58 v.7	20150917	Product data sheet	-	74AUP1G58 v.6
Modifications:	<ul style="list-style-type: none"> Added type number 74AUP1G58GX (SOT1255/X2SON6). 			
74AUP1G58 v.6	20120815	Product data sheet	-	74AUP1G58 v.5
Modifications:	<ul style="list-style-type: none"> Package outline drawing of SOT886 (Fig. 20) modified. 			
74AUP1G58 v.5	20111129	Product data sheet	-	74AUP1G58 v.4
74AUP1G58 v.4	20101011	Product data sheet	-	74AUP1G58 v.3
74AUP1G58 v.3	20090622	Product data sheet	-	74AUP1G58 v.2
74AUP1G58 v.2	20090326	Product data sheet	-	74AUP1G58 v.1
74AUP1G58 v.1	20070131	Product data sheet	-	-

16. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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