74AUP2G86GM,125 Datasheet

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DiGi Electronics Part Number	74AUP2G86GM,125-DG
Manufacturer	Nexperia USA Inc.
Manufacturer Product Number	74AUP2G86GM,125
Description	IC GATE XOR 2CH 2-INP 8XQFN
Detailed Description	XOR (Exclusive OR) IC 2 Channel 8-XQFN (1.6x1.6)

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Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
74AUP2G86GM,125	Nexperia USA Inc.
Series:	Product Status:
74AUP	Obsolete
Logic Type:	Number of Circuits:
XOR (Exclusive OR)	2
Number of Inputs:	Features:
2	-
Voltage - Supply:	Current - Quiescent (Max):
0.8V ~ 3.6V	500 nA
Current - Output High, Low:	Input Logic Level - Low:
4mA, 4mA	0.7V ~ 0.9V
Input Logic Level - High:	Max Propagation Delay @ V, Max CL:
1.6V ~ 2V	7.1ns @ 3.3V, 30pF
Operating Temperature:	Mounting Type:
-40°C ~ 125°C	Surface Mount
Supplier Device Package:	Package / Case:
8-XQFN (1.6x1.6)	8-XFQFN Exposed Pad
Base Product Number:	
74AUP2G86	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8542.39.0001	

74AUP2G86

Low-power dual 2-input EXCLUSIVE-OR gate

Rev. 11 — 31 July 2023 Product data sheet

1. General description

The 74AUP2G86 provides the dual 2-input EXCLUSIVE-OR function.

Schmitt trigger action at all inputs makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range from 0.8 V to 3.6 V.

This device ensures a very low static and dynamic power consumption across the entire V_{CC} range from 0.8 V to 3.6 V.

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing a damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 0.8 V to 3.6 V
- High noise immunity
- Complies with JEDEC standards:
  - JESD8-12 (0.8 V to 1.3 V)
  - JESD8-11 (0.9 V to 1.65 V)
  - JESD8-7 (1.2 V to 1.95 V)
  - JESD8-5 (1.8 V to 2.7 V)
  - JESD8-B (2.7 V to 3.6 V)
- Low static power consumption; I_{CC} = 0.9 µA (maximum)
- Latch-up performance exceeds 100 mA per JESD78 Class II
- Inputs accept voltages up to 3.6 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- I_{OFF} circuitry provides partial Power-down mode operation
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 3A exceeds 5000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AUP2G86DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74AUP2G86GT	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1
74AUP2G86GN	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.2 × 1.0 × 0.35 mm	SOT1116
74AUP2G86GS	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1.0 × 0.35 mm	SOT1203

4. Marking

Table 2. Marking codes

Type number	Marking code[1]
74AUP2G86DC	p86
74AUP2G86GT	p86
74AUP2G86GN	pH
74AUP2G86GS	pH

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

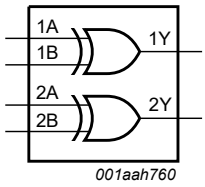


Fig. 1. Logic symbol

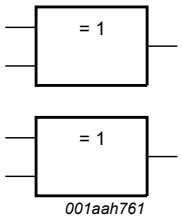


Fig. 2. IEC logic symbol

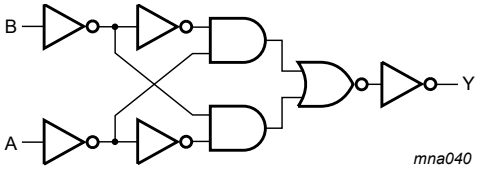


Fig. 3. Logic diagram (one gate)

6. Pinning information

6.1. Pinning

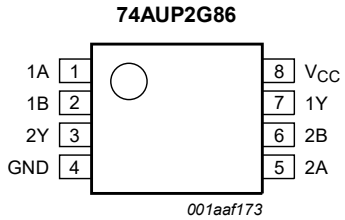
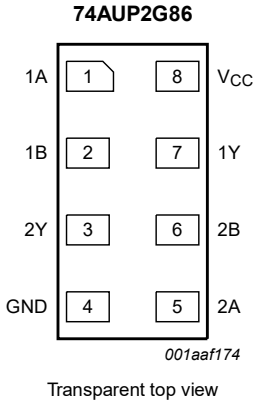


Fig. 4. Pin configuration SOT765-1 (VSSOP8)



Transparent top view

Fig. 5. Pin configuration SOT833-1, SOT1116 and SOT1203 (XSON8)

6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1A, 2A	1, 5	data input
1B, 2B	2, 6	data input
GND	4	ground (0 V)
1Y, 2Y	7, 3	data output
V_{CC}	8	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input		Output
nA	**nB**	**nY**
L	L	L
L	H	H
H	L	H
H	H	L

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
I_{IK}	input clamping current	V_I < 0 V	-50	-	mA
V_I	input voltage	[1]	-0.5	+4.6	V
I_{OK}	output clamping current	V_O < 0 V	-50	-	mA
V_O	output voltage	Active mode and Power-down mode [1]	-0.5	+4.6	V
I_O	output current	V_O = 0 V to V_{CC}	-	±20	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C [2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT765-1 (VSSOP8) package: P_{tot} derates linearly with 4.9 mW/K above 99 °C.
For SOT833-1 (XSON8) package: P_{tot} derates linearly with 3.1 mW/K above 68 °C.
For SOT1116 (XSON8) package: P_{tot} derates linearly with 4.2 mW/K above 90 °C.
For SOT1203 (XSON8) package: P_{tot} derates linearly with 3.6 mW/K above 81 °C.

9. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		0.8	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	Active mode	0	V_{CC}	V
		Power-down mode; V_{CC} = 0 V	0	3.6	V
T_{amb}	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 0.8 V to 3.6 V	0	200	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 0.8 V	0.70V_{CC}	-	-	V
		V_{CC} = 0.9 V to 1.95 V	0.65V_{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V_{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 0.8 V	-	-	0.30V_{CC}	V
		V_{CC} = 0.9 V to 1.95 V	-	-	0.35V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V_{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = -20 µA; V_{CC} = 0.8 V to 3.6 V	V_{CC} - 0.1	-	-	V
		I_O = -1.1 mA; V_{CC} = 1.1 V	0.75V_{CC}	-	-	V
		I_O = -1.7 mA; V_{CC} = 1.4 V	1.11	-	-	V
		I_O = -1.9 mA; V_{CC} = 1.65 V	1.32	-	-	V
		I_O = -2.3 mA; V_{CC} = 2.3 V	2.05	-	-	V
		I_O = -3.1 mA; V_{CC} = 2.3 V	1.9	-	-	V
		I_O = -2.7 mA; V_{CC} = 3.0 V	2.72	-	-	V
		I_O = -4.0 mA; V_{CC} = 3.0 V	2.6	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 20 µA; V_{CC} = 0.8 V to 3.6 V	-	-	0.1	V
		I_O = 1.1 mA; V_{CC} = 1.1 V	-	-	0.3V_{CC}	V
		I_O = 1.7 mA; V_{CC} = 1.4 V	-	-	0.31	V
		I_O = 1.9 mA; V_{CC} = 1.65 V	-	-	0.31	V
		I_O = 2.3 mA; V_{CC} = 2.3 V	-	-	0.31	V
		I_O = 3.1 mA; V_{CC} = 2.3 V	-	-	0.44	V
		I_O = 2.7 mA; V_{CC} = 3.0 V	-	-	0.31	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.44	V
I_I	input leakage current	V_I = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.1	µA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.2	µA
ΔI_{OFF}	additional power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V to 0.2 V	-	-	±0.2	µA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 0.8 V to 3.6 V	-	-	0.5	µA
ΔI_{CC}	additional supply current	V_I = V_{CC} - 0.6 V; I_O = 0 A; V_{CC} = 3.3 V [1]	-	-	40	µA
C_I	input capacitance	V_{CC} = 0 V to 3.6 V; V_I = GND or V_{CC}	-	0.6	-	pF
C_O	output capacitance	V_O = GND; V_{CC} = 0 V	-	1.3	-	pF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 0.8 V	0.70V_{CC}	-	-	V
		V_{CC} = 0.9 V to 1.95 V	0.65V_{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V_{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 0.8 V	-	-	0.30V_{CC}	V
		V_{CC} = 0.9 V to 1.95 V	-	-	0.35V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V_{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = -20 µA; V_{CC} = 0.8 V to 3.6 V	V_{CC} - 0.1	-	-	V
		I_O = -1.1 mA; V_{CC} = 1.1 V	0.7V_{CC}	-	-	V
		I_O = -1.7 mA; V_{CC} = 1.4 V	1.03	-	-	V
		I_O = -1.9 mA; V_{CC} = 1.65 V	1.30	-	-	V
		I_O = -2.3 mA; V_{CC} = 2.3 V	1.97	-	-	V
		I_O = -3.1 mA; V_{CC} = 2.3 V	1.85	-	-	V
		I_O = -2.7 mA; V_{CC} = 3.0 V	2.67	-	-	V
		I_O = -4.0 mA; V_{CC} = 3.0 V	2.55	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 20 µA; V_{CC} = 0.8 V to 3.6 V	-	-	0.1	V
		I_O = 1.1 mA; V_{CC} = 1.1 V	-	-	0.3V_{CC}	V
		I_O = 1.7 mA; V_{CC} = 1.4 V	-	-	0.37	V
		I_O = 1.9 mA; V_{CC} = 1.65 V	-	-	0.35	V
		I_O = 2.3 mA; V_{CC} = 2.3 V	-	-	0.33	V
		I_O = 3.1 mA; V_{CC} = 2.3 V	-	-	0.45	V
		I_O = 2.7 mA; V_{CC} = 3.0 V	-	-	0.33	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.45	V
I_I	input leakage current	V_I = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.5	µA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.5	µA
ΔI_{OFF}	additional power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V to 0.2 V	-	-	±0.6	µA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 0.8 V to 3.6 V	-	-	0.9	µA
ΔI_{CC}	additional supply current	V_I = V_{CC} - 0.6 V; I_O = 0 A; V_{CC} = 3.3 V [1]	-	-	50	µA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 0.8 V	0.75V_{CC}	-	-	V
		V_{CC} = 0.9 V to 1.95 V	0.70V_{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V_{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 0.8 V	-	-	0.25V_{CC}	V
		V_{CC} = 0.9 V to 1.95 V	-	-	0.30V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V_{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = -20 µA; V_{CC} = 0.8 V to 3.6 V	V_{CC} - 0.11	-	-	V
		I_O = -1.1 mA; V_{CC} = 1.1 V	0.6V_{CC}	-	-	V
		I_O = -1.7 mA; V_{CC} = 1.4 V	0.93	-	-	V
		I_O = -1.9 mA; V_{CC} = 1.65 V	1.17	-	-	V
		I_O = -2.3 mA; V_{CC} = 2.3 V	1.77	-	-	V
		I_O = -3.1 mA; V_{CC} = 2.3 V	1.67	-	-	V
		I_O = -2.7 mA; V_{CC} = 3.0 V	2.40	-	-	V
		I_O = -4.0 mA; V_{CC} = 3.0 V	2.30	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 20 µA; V_{CC} = 0.8 V to 3.6 V	-	-	0.11	V
		I_O = 1.1 mA; V_{CC} = 1.1 V	-	-	0.33V_{CC}	V
		I_O = 1.7 mA; V_{CC} = 1.4 V	-	-	0.41	V
		I_O = 1.9 mA; V_{CC} = 1.65 V	-	-	0.39	V
		I_O = 2.3 mA; V_{CC} = 2.3 V	-	-	0.36	V
		I_O = 3.1 mA; V_{CC} = 2.3 V	-	-	0.50	V
		I_O = 2.7 mA; V_{CC} = 3.0 V	-	-	0.36	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.50	V
I_I	input leakage current	V_I = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.75	µA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.75	µA
ΔI_{OFF}	additional power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V to 0.2 V	-	-	±0.75	µA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 0.8 V to 3.6 V	-	-	1.4	µA
ΔI_{CC}	additional supply current	V_I = V_{CC} - 0.6 V; I_O = 0 A; V_{CC} = 3.3 V [1]	-	-	75	µA

[1] One input at V_{CC} - 0.6 V, other input at V_{CC} or GND.

11. Dynamic characteristics

Table 8. Dynamic characteristics

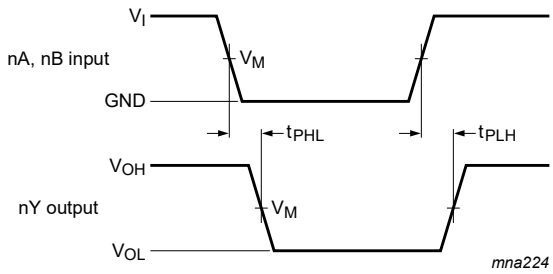
Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = -40 °C to +85 °C		T_{amb} = -40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
C_L = 5 pF										
t_{pd}	propagation delay	nA or nB to nY; see Fig. 6 [2]								
		V_{CC} = 0.8 V	-	21.2	-	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	2.3	5.9	13.1	2.1	14.3	2.1	15.8	ns
		V_{CC} = 1.4 V to 1.6 V	1.8	4.1	7.7	1.6	8.8	1.6	9.7	ns
		V_{CC} = 1.65 V to 1.95 V	1.5	3.3	5.9	1.4	6.9	1.4	7.6	ns
		V_{CC} = 2.3 V to 2.7 V	1.2	2.6	4.4	1.1	5.3	1.1	5.9	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.3	4.0	0.9	4.7	0.9	5.2	ns
C_L = 10 pF										
t_{pd}	propagation delay	nA or nB to nY; see Fig. 6 [2]								
		V_{CC} = 0.8 V	-	24.7	-	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	2.6	6.8	14.8	2.4	16.2	2.4	17.9	ns
		V_{CC} = 1.4 V to 1.6 V	2.2	4.8	8.7	1.9	10.0	1.9	11.0	ns
		V_{CC} = 1.65 V to 1.95 V	1.8	3.9	6.7	1.7	8.0	1.7	8.8	ns
		V_{CC} = 2.3 V to 2.7 V	1.5	3.1	5.2	1.4	6.2	1.4	6.9	ns
		V_{CC} = 3.0 V to 3.6 V	1.3	2.9	4.8	1.3	5.6	1.3	6.2	ns
C_L = 15 pF										
t_{pd}	propagation delay	nA or nB to nY; see Fig. 6 [2]								
		V_{CC} = 0.8 V	-	28.2	-	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	3.0	7.6	16.5	2.7	18.1	2.7	20.0	ns
		V_{CC} = 1.4 V to 1.6 V	2.4	5.3	9.6	2.2	11.3	2.2	12.5	ns
		V_{CC} = 1.65 V to 1.95 V	2.1	4.4	7.5	1.9	9.0	1.9	9.9	ns
		V_{CC} = 2.3 V to 2.7 V	1.8	3.6	5.9	1.6	7.0	1.6	7.7	ns
		V_{CC} = 3.0 V to 3.6 V	1.6	3.3	5.4	1.5	6.4	1.5	7.1	ns
C_L = 30 pF										
t_{pd}	propagation delay	nA or nB to nY; see Fig. 6 [2]								
		V_{CC} = 0.8 V	-	38.5	-	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	3.9	9.9	21.5	3.5	24.1	3.5	26.6	ns
		V_{CC} = 1.4 V to 1.6 V	3.2	6.9	12.5	2.8	14.8	2.8	16.3	ns
		V_{CC} = 1.65 V to 1.95 V	2.8	5.7	9.8	2.5	11.7	2.5	12.9	ns
		V_{CC} = 2.3 V to 2.7 V	2.4	4.7	7.6	2.2	9.1	2.2	10.1	ns
		V_{CC} = 3.0 V to 3.6 V	2.2	4.4	7.1	2.1	8.3	2.1	9.2	ns

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = -40 °C to +85 °C		T_{amb} = -40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
C_L = 5 pF, 10 pF, 15 pF and 30 pF										
C_{PD}	power dissipation capacitance	f = 1 MHz; V_I = GND to V_{CC} [3]								
		V_{CC} = 0.8 V	-	2.7	-	-	-	-	-	pF
		V_{CC} = 1.1 V to 1.3 V	-	2.9	-	-	-	-	-	pF
		V_{CC} = 1.4 V to 1.6 V	-	3.0	-	-	-	-	-	pF
		V_{CC} = 1.65 V to 1.95 V	-	3.1	-	-	-	-	-	pF
		V_{CC} = 2.3 V to 2.7 V	-	3.6	-	-	-	-	-	pF
		V_{CC} = 3.0 V to 3.6 V	-	4.2	-	-	-	-	-	pF

[1] All typical values are measured at nominal V_{CC}.
[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

11.1. Waveforms and test circuit

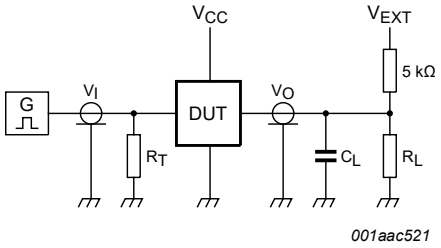


Measurement points are given in Table 9.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 6. The data input (nA or nB) to output (nY) propagation delays

Table 9. Measurement points

Supply voltage	Output	Input		
V_{CC}	V_M	V_M	V_I	$t_r = t_f$
0.8 V to 3.6 V	0.5 × V_{CC}	0.5 × V_{CC}	V_{CC}	≤ 3.0 ns



Test data is given in Table 10.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig. 7. Test circuit for measuring switching times

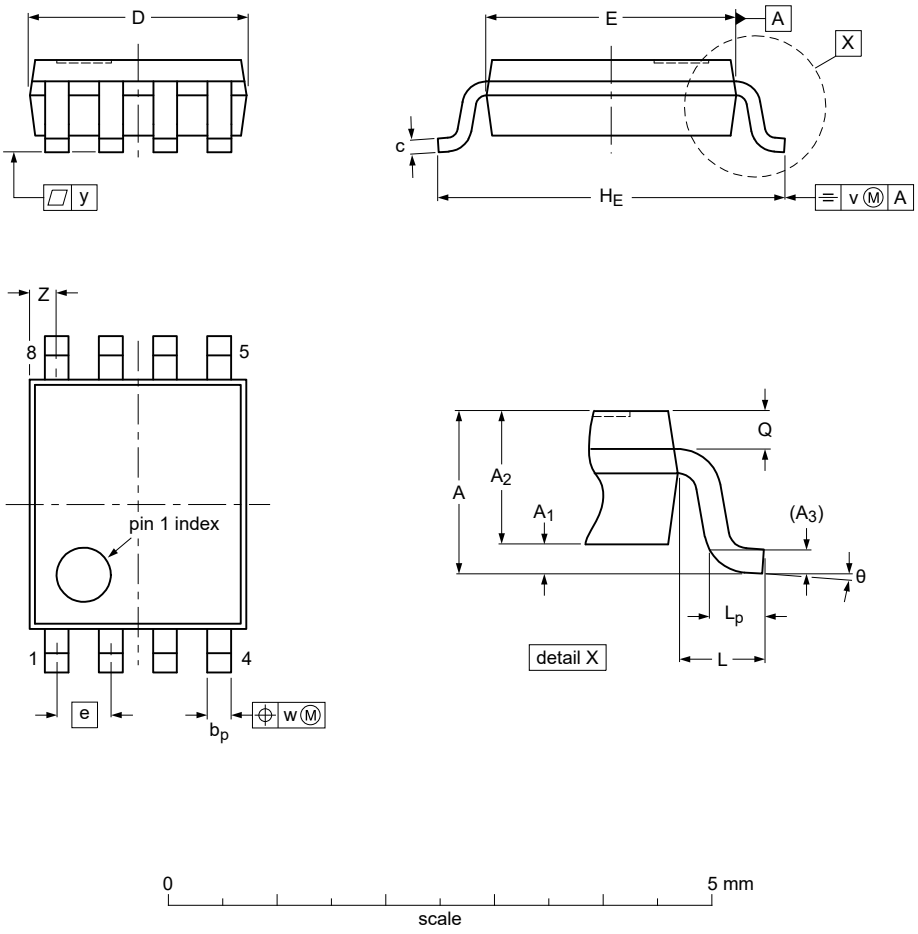
Table 10. Test data

Supply voltage	Load		V_{EXT}		
V_{CC}	C_L	R_L [1]	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
0.8 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 kΩ or 1 MΩ	open	GND	2 × V_{CC}

[1] For measuring enable and disable times R_L = 5 kΩ.
For measuring propagation delays, set-up and hold times and pulse width R_L = 1 MΩ.

12. Package outline

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm **SOT765-1**



Dimensions (mm are the original dimensions)

Unit		A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	max	1	0.15	0.85	0.12	0.27	0.23	2.1	2.4	0.5	3.2	0.4	0.40	0.21	0.2	0.08	0.1	0.4	8°
	nom																		
	min		0.00	0.60		0.17	0.08	1.9	2.2		3.0		0.15	0.19				0.1	0°

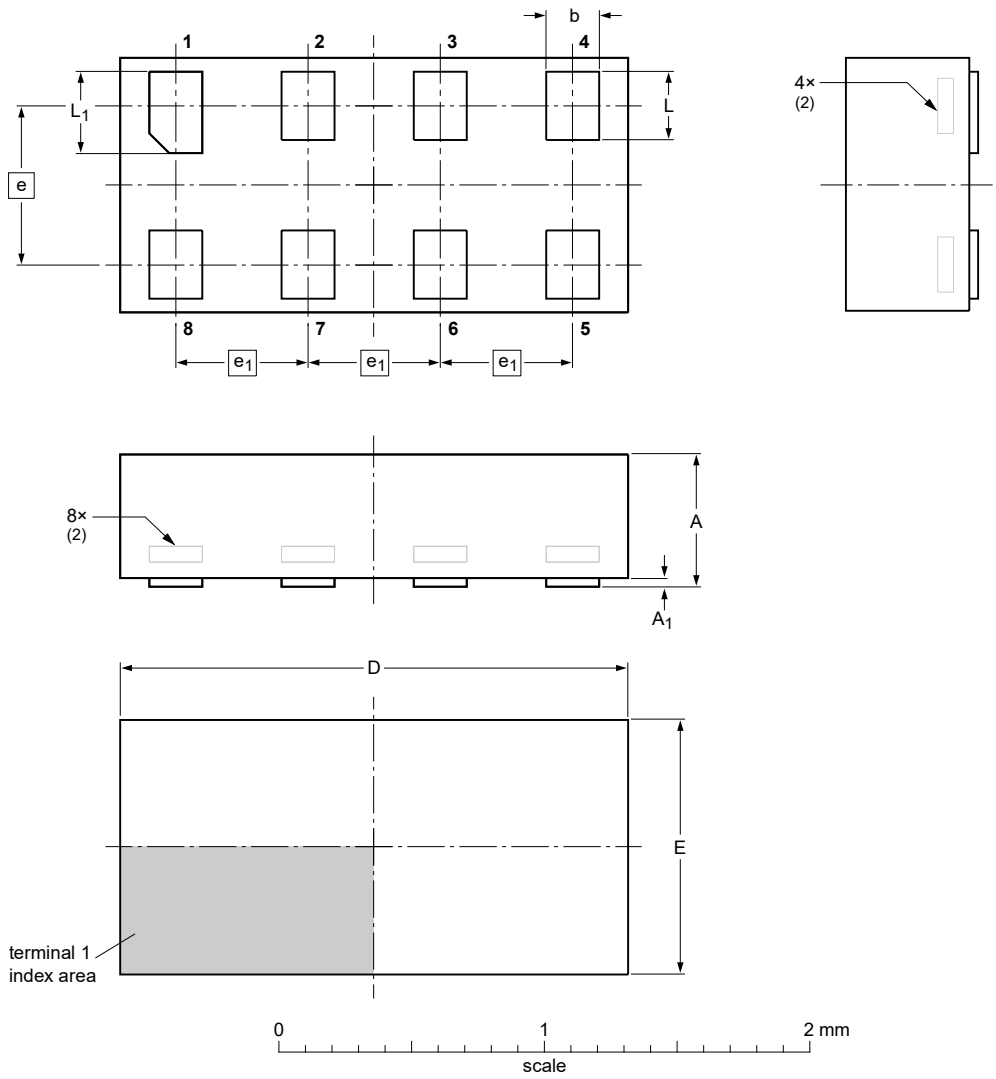
Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

sot765-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				~~07-06-02~~ 16-05-31

Fig. 8. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm **SOT833-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max	A_1 max	b	D	E	e	e_1	L	L_1
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

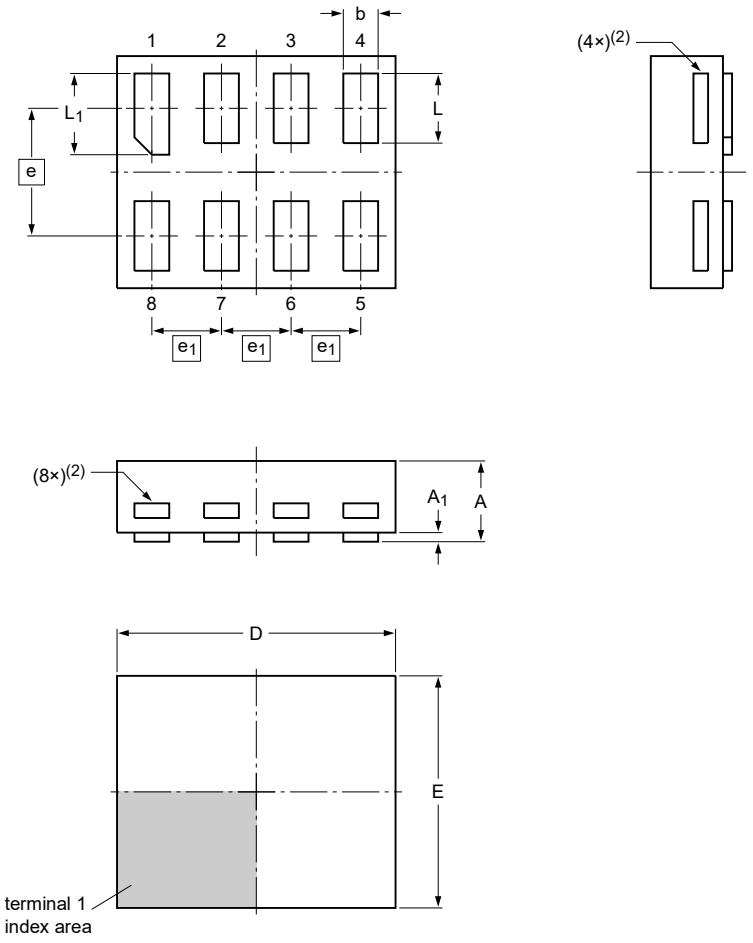
Notes

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT833-1	- - -	MO-252	- - -			~~07-11-14~~ 07-12-07

Fig. 9. Package outline SOT833-1 (XSON8)

XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.2 x 1.0 x 0.35 mm **SOT1116**



Dimensions

Unit		A(1)	A_1	b	D	E	e	e_1	L	L_1
mm	max	0.35	0.04	0.20	1.25	1.05			0.35	0.40
	nom			0.15	1.20	1.00	0.55	0.3	0.30	0.35
	min			0.12	1.15	0.95			0.27	0.32

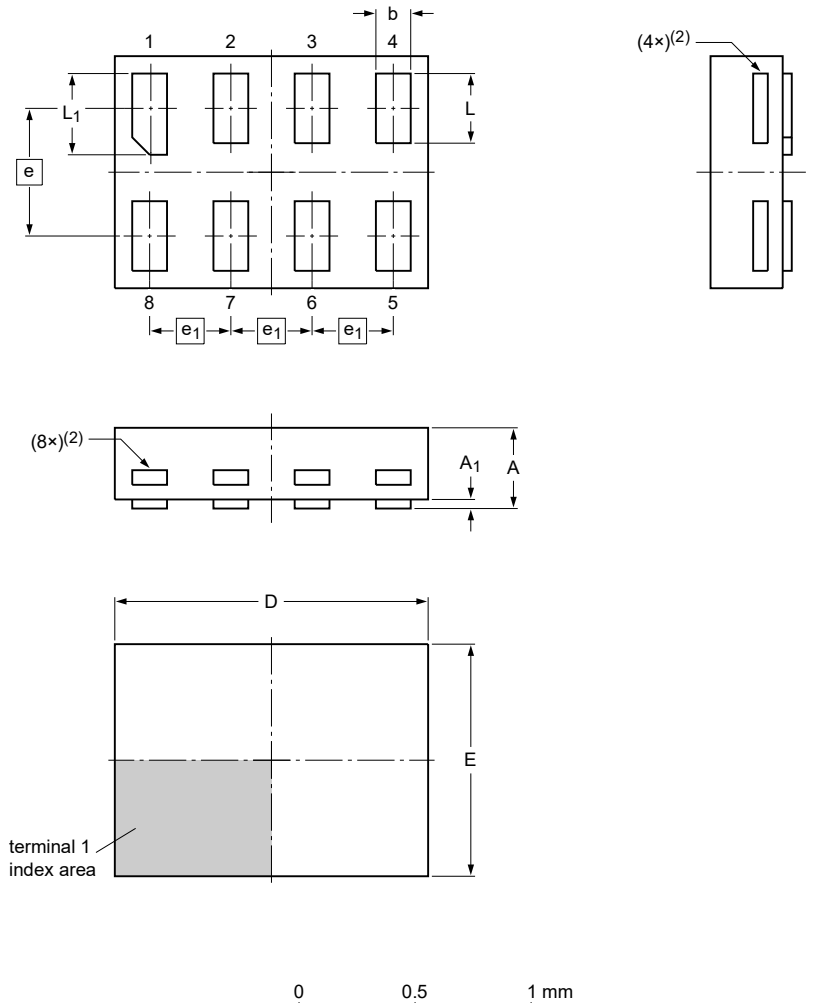
Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1116_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1116						~~10-04-02~~ 10-04-07

Fig. 10. Package outline SOT1116 (XSON8)

XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.35 x 1.0 x 0.35 mm **SOT1203**



Dimensions

Unit		A(1)	A_1	b	D	E	e	e_1	L	L_1
mm	max	0.35	0.04	0.20	1.40	1.05			0.35	0.40
	nom			0.15	1.35	1.00	0.55	0.35	0.30	0.35
	min			0.12	1.30	0.95			0.27	0.32

Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1203_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1203						~~10-04-02~~ 10-04-06

Fig. 11. Package outline SOT1203 (XSON8)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AUP2G86 v.11	20230731	Product data sheet	-	74AUP2G86 v.10
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard.			
74AUP2G86 v.10	20201207	Product data sheet	-	74AUP2G86 v.9
Modifications:	• Section 8: Derating values for P_{tot} total power dissipation have been updated. • Type numbers 74AUP2G86GF (SOT1089/XSON8) and 74AUP2G86GM (SOT902-1/ XQFN8) removed.			
74AUP2G86 v.9	20190328	Product data sheet	-	74AUP2G86 v.8
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type number 74AUP2G86GD (SOT996-2) removed. • Package outline drawing SOT765-1 (VSSOP8) updated. • Package outline drawing SOT902-2 (XQFN8) updated.			
74AUP2G86 v.8	20130124	Product data sheet	-	74AUP2G86 v.7
Modifications:	• For type number 74AUP2G86GD XSON8U has changed to XSON8.			
74AUP2G86 v.7	20120614	Product data sheet	-	74AUP2G86 v.6
74AUP2G86 v.6	20111208	Product data sheet	-	74AUP2G86 v.5
74AUP2G86 v.5	20100727	Product data sheet	-	74AUP2G86 v.4
74AUP2G86 v.4	20090629	Product data sheet	-	74AUP2G86 v.3
74AUP2G86 v.3	20090504	Product data sheet	-	74AUP2G86 v.2
74AUP2G86 v.2	20080319	Product data sheet	-	74AUP2G86 v.1
74AUP2G86 v.1	20061009	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Contents

1. General description....1
2. Features and benefits....1
3. Ordering information....2
4. Marking....2
5. Functional diagram....2
6. Pinning information....3
6.1. Pinning....3
6.2. Pin description....3
7. Functional description....3
8. Limiting values....4
9. Recommended operating conditions....4
10. Static characteristics....5
11. Dynamic characteristics....8
11.1. Waveforms and test circuit....9
12. Package outline....11
13. Abbreviations....15
14. Revision history....15
15. Legal information....16

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