74AUP2G97DPJ Datasheet

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DiGi Electronics Part Number	74AUP2G97DPJ-DG
Manufacturer	Nexperia USA Inc.
Manufacturer Product Number	74AUP2G97DPJ
Description	IC GATE DUAL PCB MULTI 10TSSOP
Detailed Description	Configurable Multiple Function Configurable 2 Circuit 3 Input 10-TSSOP

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RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
74AUP2G97DPJ	Nexperia USA Inc.
Series:	Product Status:
74AUP	Active
Logic Type:	Number of Circuits:
Configurable Multiple Function	2
Number of Inputs:	Schmitt Trigger Input:
3	Yes
Output Type:	Current - Output High, Low:
Single-Ended	4mA, 4mA
Voltage - Supply:	Operating Temperature:
0.8V ~ 3.6V	-40°C ~ 125°C
Mounting Type:	Package / Case:
Surface Mount	10-TFSOP, 10-MSOP (0.118", 3.00mm Width)
Supplier Device Package:	Base Product Number:
10-TSSOP	74AUP2G97

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8542.39.0001	

74AUP2G97

Low-power dual PCB configurable multiple function gate

Rev. 4 — 1 August 2023 Product data sheet

1. General description

The 74AUP2G97 is a dual configurable multiple function gate with Schmitt-trigger inputs. Each gate within the device can be configured as any of the following logic functions MUX, AND, OR, NAND, NOR, inverter and buffer; using the 3-bit input. All inputs can be connected directly to V_{CC} or GND.

This device ensures very low static and dynamic power consumption across the entire V_{CC} range from 0.8 V to 3.6 V.

This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 0.8 V to 3.6 V
- High noise immunity
- Low static power consumption; I_{CC} = 0.9 µA (maximum)
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- I_{OFF} circuitry provides partial power-down mode operation
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 3A exceeds 5000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AUP2G97DP	-40 °C to +125 °C	TSSOP10	plastic thin shrink small outline package; 10 leads; body width 3 mm	SOT552-1
74AUP2G97GU	-40 °C to +125 °C	XQFN10	plastic, extremely thin quad flat package; no leads; 10 terminals; body 1.40 × 1.80 × 0.50 mm	SOT1160-1

4. Marking

Table 2. Marking

Type number	Marking code [1]
74AUP2G97DP	aV
74AUP2G97GU	aV

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

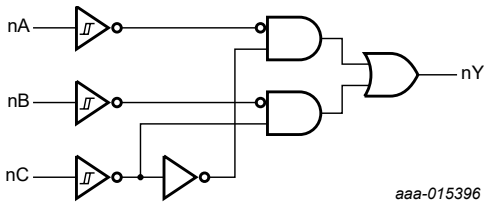
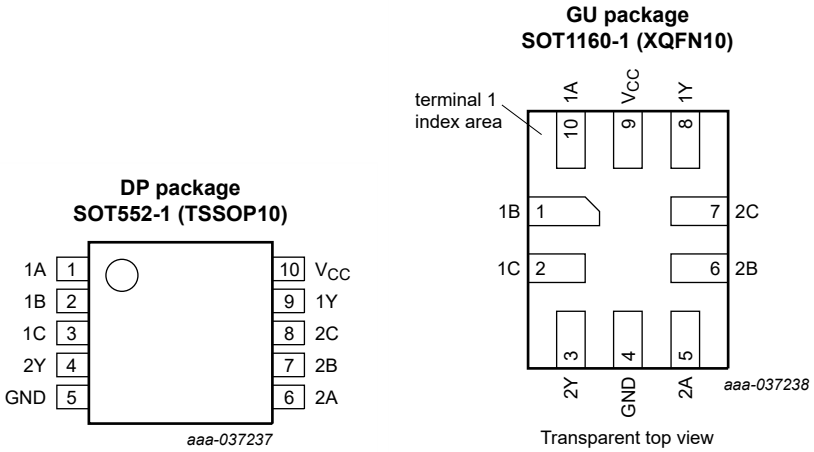


Fig. 1. Logic symbol (one gate)

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT552-1	SOT1160-1	
1A, 2A	1, 6	10, 5	data input
1B, 2B	2, 7	1, 6	data input
1C, 2C	3, 8	2, 7	data input
1Y, 2Y	9, 4	8, 3	data output
GND	5	4	ground (0 V)
V_{CC}	10	9	supply voltage

7. Functional description

Table 4. Function table

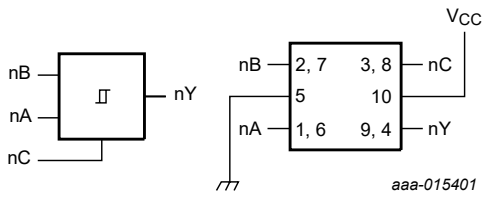
H = HIGH voltage level; L = LOW voltage level.

Input			Output
nC	**nB**	**nA**	**nY**
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	L
H	H	H	H

7.1. Logic configurations

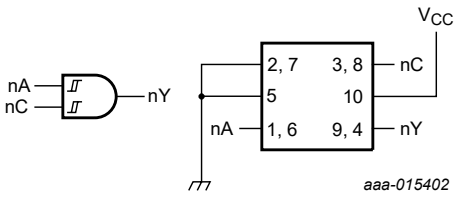
Table 5. Function selection table

Logic function	Figure
2-input MUX	see Fig. 2
2-input AND	see Fig. 3
2-input OR with one input inverted	see Fig. 4
2-input NAND with one input inverted	see Fig. 4
2-input AND with one input inverted	see Fig. 5
2-input NOR with one input inverted	see Fig. 5
2-input OR	see Fig. 6
Inverter	see Fig. 7
Buffer	see Fig. 8



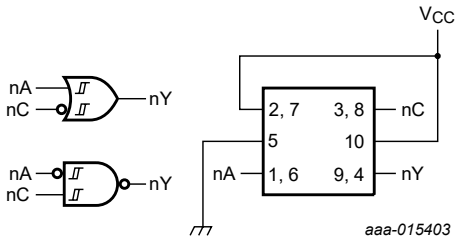
Pin numbers are not valid for SOT1160-1 package

Fig. 2. 2-input MUX



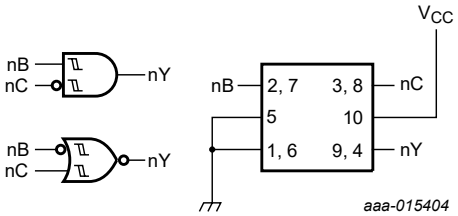
Pin numbers are not valid for SOT1160-1 package

Fig. 3. 2-input AND gate



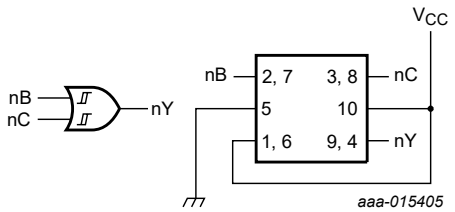
Pin numbers are not valid for SOT1160-1 package

Fig. 4. 2-input NAND gate with input A inverted or 2-input OR gate with input C inverted



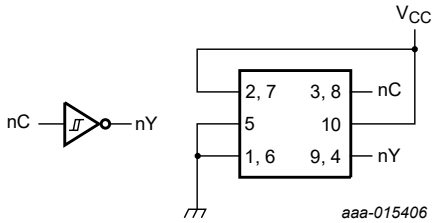
Pin numbers are not valid for SOT1160-1 package

Fig. 5. 2-input NOR gate with input B inverted or 2-input AND gate with input C inverted



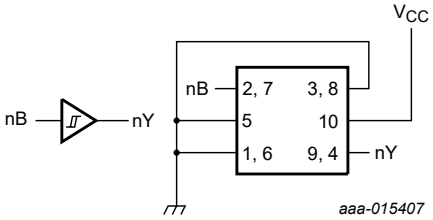
Pin numbers are not valid for SOT1160-1 package

Fig. 6. 2-input OR gate



Pin numbers are not valid for SOT1160-1 package

Fig. 7. Inverter



Pin numbers are not valid for SOT1160-1 package

Fig. 8. Buffer

8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V		-50	-	mA
V_I	input voltage		[1]	-0.5	+4.6	V
I_{OK}	output clamping current	$V_O < 0$ V		-50	-	mA
V_O	output voltage	Active mode and Power-down mode	[1]	-0.5	+4.6	V
I_O	output current	V_O = 0 V to V_{CC}		-	±20	mA
I_{CC}	supply current			-	50	mA
I_{GND}	ground current			-50	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	250	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT552-1 (TSSOP10) packages: P_{tot} derates linearly with 8.3 mW/K above 120 °C.
For SOT1160-1 (XQFN10) package: P_{tot} derates linearly with 7.1 mW/K above 115 °C.

9. Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		0.8	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	Active mode	0	V_{CC}	V
		Power-down mode; V_{CC} = 0 V	0	3.6	V
T_{amb}	ambient temperature		-40	+125	°C

10. Static characteristics

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{OH}	HIGH-level output voltage	V_I = V_{T+} or V_{T-}				
		I_O = -20 µA; V_{CC} = 0.8 V to 3.6 V	V_{CC} - 0.1	-	-	V
		I_O = -1.1 mA; V_{CC} = 1.1 V	0.75 × V_{CC}	-	-	V
		I_O = -1.7 mA; V_{CC} = 1.4 V	1.11	-	-	V
		I_O = -1.9 mA; V_{CC} = 1.65 V	1.32	-	-	V
		I_O = -2.3 mA; V_{CC} = 2.3 V	2.05	-	-	V
		I_O = -3.1 mA; V_{CC} = 2.3 V	1.9	-	-	V
		I_O = -2.7 mA; V_{CC} = 3.0 V	2.72	-	-	V
		I_O = -4.0 mA; V_{CC} = 3.0 V	2.6	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{T+} or V_{T-}				
		I_O = 20 µA; V_{CC} = 0.8 V to 3.6 V	-	-	0.1	V
		I_O = 1.1 mA; V_{CC} = 1.1 V	-	-	0.3 × V_{CC}	V
		I_O = 1.7 mA; V_{CC} = 1.4 V	-	-	0.31	V
		I_O = 1.9 mA; V_{CC} = 1.65 V	-	-	0.31	V
		I_O = 2.3 mA; V_{CC} = 2.3 V	-	-	0.31	V
		I_O = 3.1 mA; V_{CC} = 2.3 V	-	-	0.44	V
		I_O = 2.7 mA; V_{CC} = 3.0 V	-	-	0.31	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.44	V
I_I	input leakage current	V_I = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.1	µA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.2	µA
ΔI_{OFF}	additional power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V to 0.2 V	-	-	±0.2	µA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 0.8 V to 3.6 V	-	-	0.5	µA
ΔI_{CC}	additional supply current	V_I = V_{CC} - 0.6 V; I_O = 0 A; V_{CC} = 3.3 V [1]	-	-	40	µA
C_I	input capacitance	V_{CC} = 0 V to 3.6 V; V_I = GND or V_{CC}	-	1.1	-	pF
C_O	output capacitance	V_O = GND; V_{CC} = 0 V	-	1.7	-	pF
T_{amb} = -40 °C to +85 °C						
V_{OH}	HIGH-level output voltage	V_I = V_{T+} or V_{T-}				
		I_O = -20 µA; V_{CC} = 0.8 V to 3.6 V	V_{CC} - 0.1	-	-	V
		I_O = -1.1 mA; V_{CC} = 1.1 V	0.7 × V_{CC}	-	-	V
		I_O = -1.7 mA; V_{CC} = 1.4 V	1.03	-	-	V
		I_O = -1.9 mA; V_{CC} = 1.65 V	1.30	-	-	V
		I_O = -2.3 mA; V_{CC} = 2.3 V	1.97	-	-	V
		I_O = -3.1 mA; V_{CC} = 2.3 V	1.85	-	-	V
		I_O = -2.7 mA; V_{CC} = 3.0 V	2.67	-	-	V
		I_O = -4.0 mA; V_{CC} = 3.0 V	2.55	-	-	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage	$V_I = V_{T+}$ or V_{T-}				
		I_O = 20 µA; V_{CC} = 0.8 V to 3.6 V	-	-	0.1	V
		I_O = 1.1 mA; V_{CC} = 1.1 V	-	-	0.3 × V_{CC}	V
		I_O = 1.7 mA; V_{CC} = 1.4 V	-	-	0.37	V
		I_O = 1.9 mA; V_{CC} = 1.65 V	-	-	0.35	V
		I_O = 2.3 mA; V_{CC} = 2.3 V	-	-	0.33	V
		I_O = 3.1 mA; V_{CC} = 2.3 V	-	-	0.45	V
		I_O = 2.7 mA; V_{CC} = 3.0 V	-	-	0.33	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.45	V
I_I	input leakage current	V_I = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.5	µA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.5	µA
ΔI_{OFF}	additional power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V to 0.2 V	-	-	±0.6	µA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 0.8 V to 3.6 V	-	-	0.9	µA
ΔI_{CC}	additional supply current	$V_I = V_{CC}$ - 0.6 V; I_O = 0 A; V_{CC} = 3.3 V [1]	-	-	50	µA
T_{amb} = -40 °C to +125 °C						
V_{OH}	HIGH-level output voltage	$V_I = V_{T+}$ or V_{T-}				
		I_O = -20 µA; V_{CC} = 0.8 V to 3.6 V	V_{CC} - 0.11	-	-	V
		I_O = -1.1 mA; V_{CC} = 1.1 V	0.6 × V_{CC}	-	-	V
		I_O = -1.7 mA; V_{CC} = 1.4 V	0.93	-	-	V
		I_O = -1.9 mA; V_{CC} = 1.65 V	1.17	-	-	V
		I_O = -2.3 mA; V_{CC} = 2.3 V	1.77	-	-	V
		I_O = -3.1 mA; V_{CC} = 2.3 V	1.67	-	-	V
		I_O = -2.7 mA; V_{CC} = 3.0 V	2.40	-	-	V
		I_O = -4.0 mA; V_{CC} = 3.0 V	2.30	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{T+}$ or V_{T-}				
		I_O = 20 µA; V_{CC} = 0.8 V to 3.6 V	-	-	0.11	V
		I_O = 1.1 mA; V_{CC} = 1.1 V	-	-	0.33 × V_{CC}	V
		I_O = 1.7 mA; V_{CC} = 1.4 V	-	-	0.41	V
		I_O = 1.9 mA; V_{CC} = 1.65 V	-	-	0.39	V
		I_O = 2.3 mA; V_{CC} = 2.3 V	-	-	0.36	V
		I_O = 3.1 mA; V_{CC} = 2.3 V	-	-	0.50	V
		I_O = 2.7 mA; V_{CC} = 3.0 V	-	-	0.36	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.50	V
I_I	input leakage current	V_I = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.75	µA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.75	µA
ΔI_{OFF}	additional power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V to 0.2 V	-	-	±0.75	µA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 0.8 V to 3.6 V	-	-	1.4	µA
ΔI_{CC}	additional supply current	$V_I = V_{CC}$ - 0.6 V; I_O = 0 A; V_{CC} = 3.3 V [1]	-	-	75	µA

[1] One input at V_{CC} - 0.6 V, other input at V_{CC} or GND.

10.1. Transfer characteristics

Table 9. Transfer characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit, see Fig. 14.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{T+}	positive-going threshold voltage	see Fig. 9 and Fig. 10								
		V_{CC} = 0.8 V	0.30	-	0.60	0.30	0.60	0.30	0.62	V
		V_{CC} = 1.1 V	0.53	-	0.90	0.53	0.90	0.53	0.92	V
		V_{CC} = 1.4 V	0.74	-	1.11	0.74	1.11	0.74	1.13	V
		V_{CC} = 1.65 V	0.91	-	1.29	0.91	1.29	0.91	1.31	V
		V_{CC} = 2.3 V	1.37	-	1.77	1.37	1.77	1.37	1.80	V
		V_{CC} = 3.0 V	1.88	-	2.29	1.88	2.29	1.88	2.32	V
V_{T-}	negative-going threshold voltage	see Fig. 9 and Fig. 10								
		V_{CC} = 0.8 V	0.10	-	0.60	0.10	0.60	0.10	0.60	V
		V_{CC} = 1.1 V	0.26	-	0.65	0.26	0.65	0.26	0.65	V
		V_{CC} = 1.4 V	0.39	-	0.75	0.39	0.75	0.39	0.75	V
		V_{CC} = 1.65 V	0.47	-	0.84	0.47	0.84	0.47	0.84	V
		V_{CC} = 2.3 V	0.69	-	1.04	0.69	1.04	0.69	1.04	V
		V_{CC} = 3.0 V	0.88	-	1.24	0.88	1.24	0.88	1.24	V
V_H	hysteresis voltage	(V_{T+} - V_{T-}); see Fig. 9, Fig. 10, Fig. 11 and Fig. 12								
		V_{CC} = 0.8 V	0.07	-	0.50	0.07	0.50	0.07	0.50	V
		V_{CC} = 1.1 V	0.08	-	0.46	0.08	0.46	0.08	0.46	V
		V_{CC} = 1.4 V	0.18	-	0.56	0.18	0.56	0.18	0.56	V
		V_{CC} = 1.65 V	0.27	-	0.66	0.27	0.66	0.27	0.66	V
		V_{CC} = 2.3 V	0.53	-	0.92	0.53	0.92	0.53	0.92	V
		V_{CC} = 3.0 V	0.79	-	1.31	0.79	1.31	0.79	1.31	V

10.2. Waveforms transfer characteristics

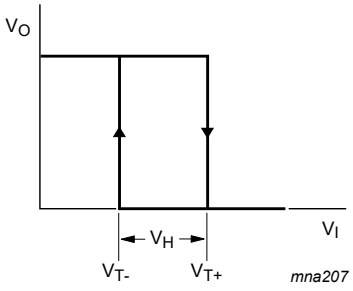
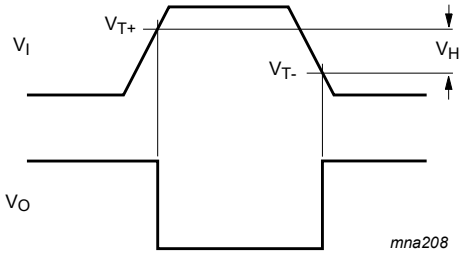


Fig. 9. Transfer characteristic



V_{T+} and V_{T-} limits at 70 % and 20 %.

Fig. 10. Definition of V_{T+}, V_{T-} and V_H

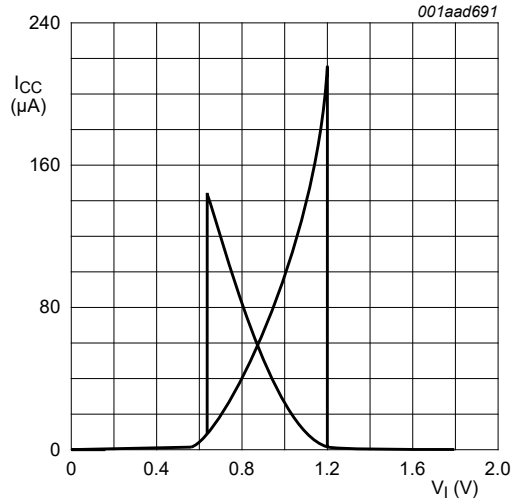


Fig. 11. Typical transfer characteristics; V_{CC} = 1.8 V

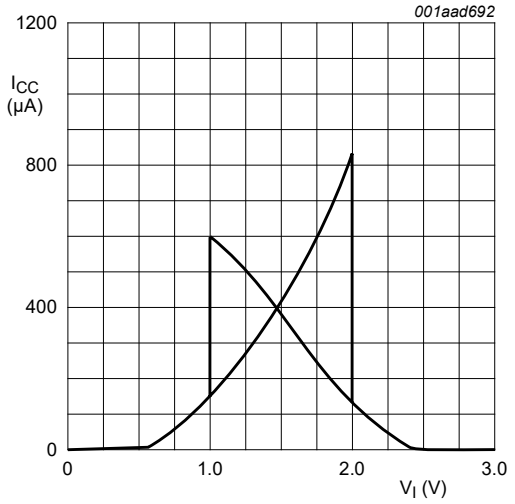


Fig. 12. Typical transfer characteristics; V_{CC} = 3.0 V

11. Dynamic characteristics

Table 10. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit, see Fig. 14.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
C_L = 5 pF										
t_{pd}	propagation delay	nA, nB, nC to nY; see Fig. 13 [2]								
		V_{CC} = 0.8 V	-	23.0	-	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	2.8	6.6	12.6	2.5	13.0	2.5	13.2	ns
		V_{CC} = 1.4 V to 1.6 V	2.3	4.7	7.6	2.5	8.2	2.5	8.6	ns
		V_{CC} = 1.65 V to 1.95 V	2.2	3.9	6.2	2.0	6.8	2.0	7.2	ns
		V_{CC} = 2.3 V to 2.7 V	2.0	3.2	4.5	1.7	5.1	1.7	5.3	ns
		V_{CC} = 3.0 V to 3.6 V	1.9	2.8	3.9	1.5	4.1	1.5	4.3	ns
C_L = 10 pF										
t_{pd}	propagation delay	nA, nB, nC to nY; see Fig. 13 [2]								
		V_{CC} = 0.8 V	-	26.6	-	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	3.2	7.4	14.3	2.9	14.9	2.9	15.2	ns
		V_{CC} = 1.4 V to 1.6 V	2.6	5.3	8.7	2.8	9.4	2.8	9.8	ns
		V_{CC} = 1.65 V to 1.95 V	2.5	4.5	7.0	2.3	7.8	2.3	8.2	ns
		V_{CC} = 2.3 V to 2.7 V	2.4	3.7	5.2	2.1	5.9	2.1	6.1	ns
		V_{CC} = 3.0 V to 3.6 V	2.3	3.4	4.6	1.9	4.9	1.9	5.1	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
C_L = 15 pF										
t_{pd}	propagation delay	nA, nB, nC to nY; see Fig. 13 [2]								
		V_{CC} = 0.8 V	-	30.1	-	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	3.6	8.2	16.0	3.2	16.7	3.2	17.0	ns
		V_{CC} = 1.4 V to 1.6 V	2.9	5.9	9.6	3.1	10.4	3.1	10.9	ns
		V_{CC} = 1.65 V to 1.95 V	2.8	5.0	7.8	2.5	8.7	2.5	9.1	ns
		V_{CC} = 2.3 V to 2.7 V	2.7	4.2	5.8	2.4	6.5	2.4	6.9	ns
		V_{CC} = 3.0 V to 3.6 V	2.5	3.8	5.1	2.2	5.5	2.2	5.7	ns
C_L = 30 pF										
t_{pd}	propagation delay	nA, nB, nC to nY; see Fig. 13 [2]								
		V_{CC} = 0.8 V	-	38.3	-	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	4.6	10.5	20.9	4.0	21.8	4.0	22.2	ns
		V_{CC} = 1.4 V to 1.6 V	3.7	7.4	12.2	3.8	13.3	3.8	14.0	ns
		V_{CC} = 1.65 V to 1.95 V	3.5	6.3	9.9	3.2	11.1	3.2	11.8	ns
		V_{CC} = 2.3 V to 2.7 V	3.4	5.3	7.4	3.1	8.3	3.1	8.8	ns
		V_{CC} = 3.0 V to 3.6 V	3.2	4.9	6.6	2.8	7.0	2.8	7.4	ns
C_L = 5 pF, 10 pF, 15 pF and 30 pF										
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = GND to V_{CC} [3]								
		V_{CC} = 0.8 V	-	2.6	-	-	-	-	-	pF
		V_{CC} = 1.1 V to 1.3 V	-	2.8	-	-	-	-	-	pF
		V_{CC} = 1.4 V to 1.6 V	-	2.9	-	-	-	-	-	pF
		V_{CC} = 1.65 V to 1.95 V	-	3.1	-	-	-	-	-	pF
		V_{CC} = 2.3 V to 2.7 V	-	3.7	-	-	-	-	-	pF
		V_{CC} = 3.0 V to 3.6 V	-	4.3	-	-	-	-	-	pF

[1] All typical values are measured at nominal V_{CC}.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

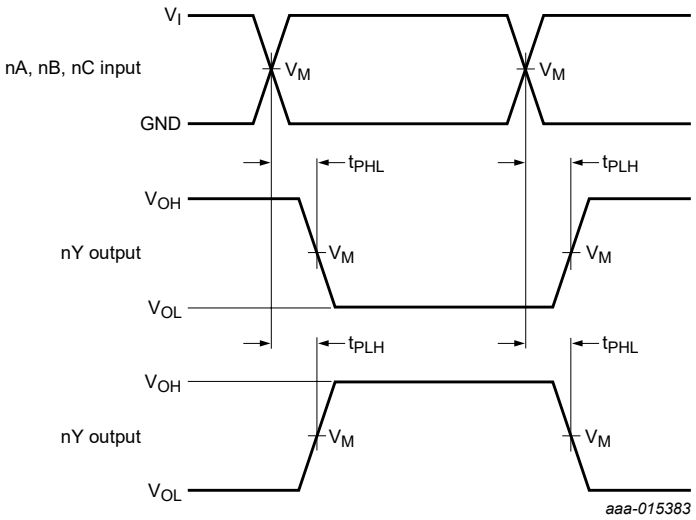
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

11.1. Waveforms and test circuit



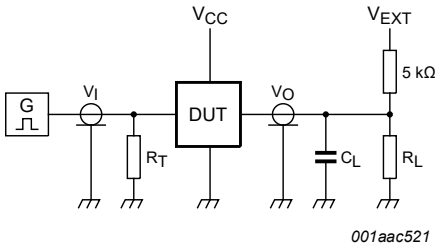
Measurement points are given in Table 11.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 13. Input nA, nB and nC to output nY propagation delay times

Table 11. Measurement points

Supply voltage	Output	Input		
V_{CC}	V_M	V_M	V_I	$t_r = t_f$
0.8 V to 3.6 V	0.5 × V_{CC}	0.5 × V_{CC}	V_{CC}	≤ 3.0 ns



Test data is given in Table 12.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig. 14. Test circuit for measuring switching times

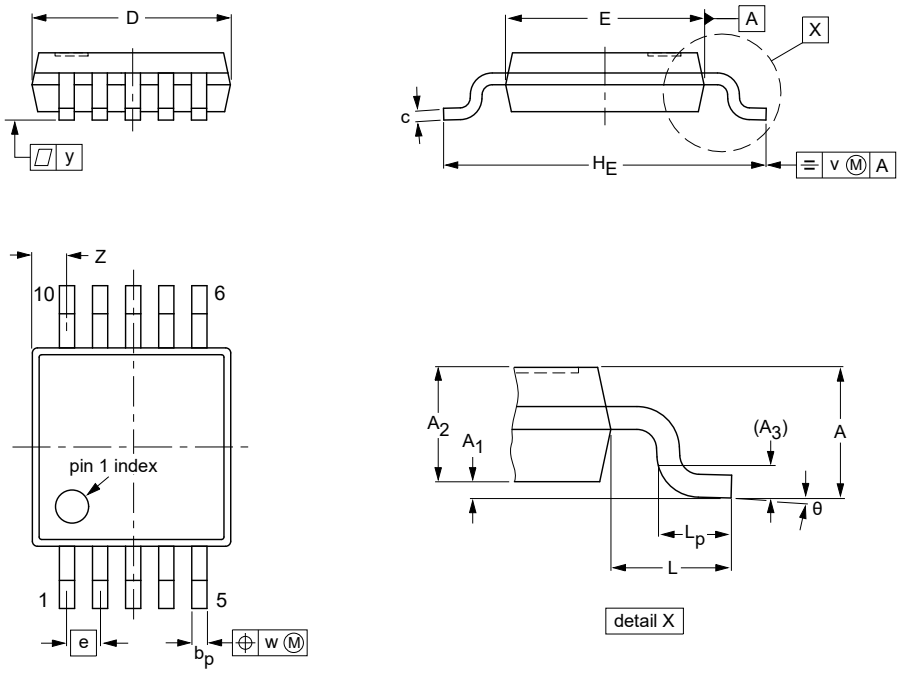
Table 12. Test data

Supply voltage	Load		V_{EXT}		
V_{CC}	C_L	R_L [1]	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
0.8 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 kΩ or 1 MΩ	open	GND	2V_{CC}

[1] For measuring enable and disable times, R_L = 5 kΩ.
For measuring propagation delays, setup and hold times and pulse width R_L = 1 MΩ.

12. Package outline

TSSOP10: plastic thin shrink small outline package; 10 leads; body width 3 mm **SOT552-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.15	0.23 0.15	3.1 2.9	3.1 2.9	0.5	5.0 4.8	0.95	0.7 0.4	0.1	0.1	0.1	0.67 0.34	6° 0°

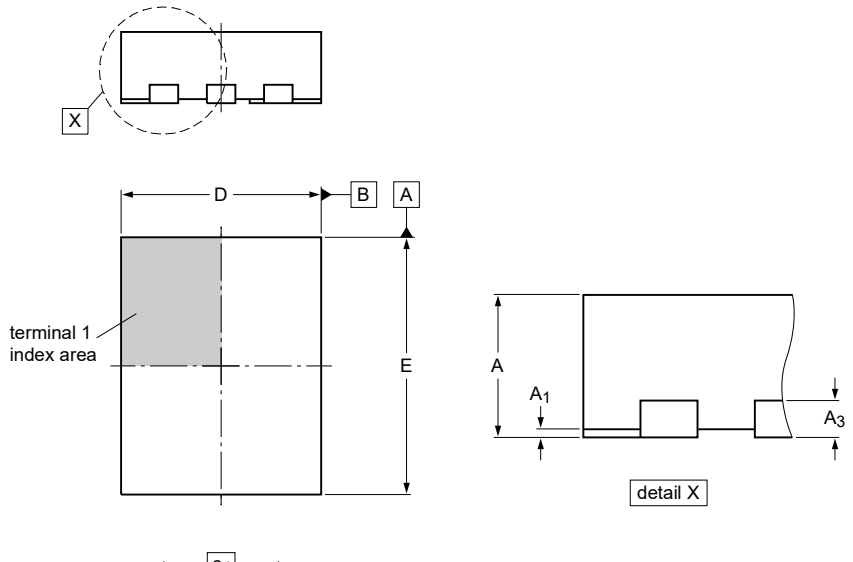
Notes

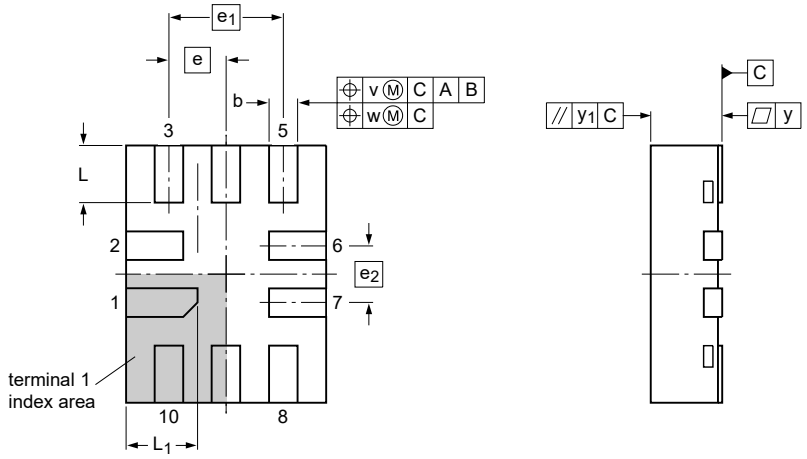
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

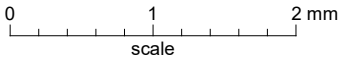
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT552-1						~~99-07-29~~ 03-02-18

Fig. 15. Package outline SOT552-1 (TSSOP10)

XQFN10: plastic, extremely thin quad flat package; no leads; 10 terminals; body 1.40 x 1.80 x 0.50 mm **SOT1160-1**







Dimensions

Unit[1]		A	A_1	A_3	b	D	E	e	e_1	e_2	L	L_1	v	w	y	y_1
mm	max	0.5	0.05		0.25	1.5	1.9				0.45	0.55				
	nom			0.127	0.20	1.4	1.8	0.4	0.8	0.4	0.40	0.50	0.1	0.05	0.05	0.05
	min		0.00		0.15	1.3	1.7				0.35	0.45				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1160-1_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1160-1	- - -	- - -	- - -		~~09-12-28~~ 09-12-29

Fig. 16. Package outline SOT1160-1 (XQFN10)

13. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
PCB	Printed-Circuit Board

14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AUP2G97 v.4	20230801	Product data sheet	-	74AUP2G97 v.3
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard.			
74AUP2G97 v.3	20190722	Product data sheet	-	74AUP2G97 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type number 74AUP2G97GF (SOT1081-2) removed.			
74AUP2G97 v.2	20151202	Product data sheet	-	74AUP2G97 v.1
Modifications:	• Maximum value temperature range TSSOP10 (74AUP2G97DP) changed from 85 °C to 125 °C. • Removed 74AUP2G97GM (SOT1049-3).			
74AUP2G97 v.1	20141104	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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