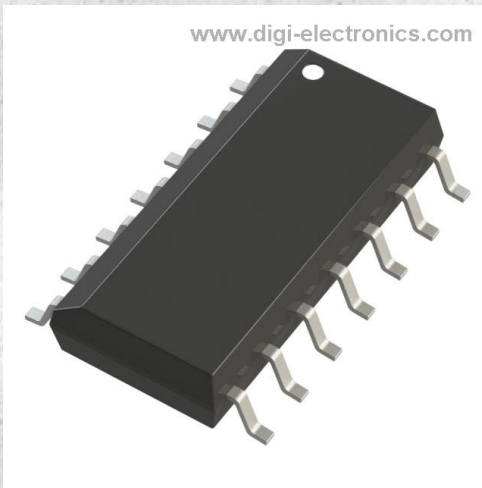


74HC05D-Q100,118 Datasheet



<https://www.DiGi-Electronics.com>

DiGi Electronics Part Number	74HC05D-Q100,118-DG
Manufacturer	Nexperia USA Inc.
Manufacturer Product Number	74HC05D-Q100,118
Description	IC INVERTER 6CH 1-INP 14SO
Detailed Description	Inverter IC 6 Channel Open Drain 14-SO



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RFQ Email: Info@DiGi-Electronics.com

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Purchase and inquiry

Manufacturer Product Number:

74HC05D-Q100,118

Series:

74HC

Logic Type:

Inverter

Number of Inputs:

1

Voltage - Supply:

2V ~ 6V

Current - Output High, Low:

-, 5.2mA

Input Logic Level - High:

1.5V ~ 4.2V

Operating Temperature:

-40°C ~ 125°C

Qualification:

AEC-Q100

Supplier Device Package:

14-SO

Base Product Number:

74HC05

Manufacturer:

Nexperia USA Inc.

Product Status:

Active

Number of Circuits:

6

Features:

Open Drain

Current - Quiescent (Max):2 μ A**Input Logic Level - Low:**

0.5V ~ 1.8V

Max Propagation Delay @ V, Max CL:

13ns @ 6V, 50pF

Grade:

Automotive

Mounting Type:

Surface Mount

Package / Case:

14-SOIC (0.154", 3.90mm Width)

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

74HC05-Q100

Hex inverter with open-drain outputs

Rev. 3 — 14 March 2024

Product data sheet

1. General description

The 74HC05-Q100 contains six inverters. The outputs of the 74HC05-Q100 are open-drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions. The open-drain outputs require pull-up resistors to perform correctly.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide operating voltage 2.0 V to 6.0 V
- CMOS input levels
- Latch-up performance exceeds 100 mA per JESD 78 Class II level A
- Complies with JEDEC standard no. 7A
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC05D-Q100	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HC05PW-Q100	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HC05BQ-Q100	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

4. Functional diagram

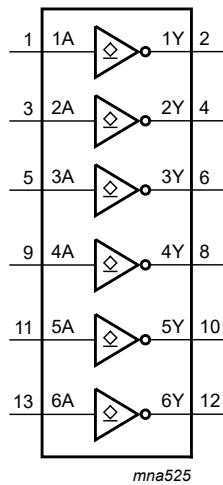


Fig. 1. Logic symbol

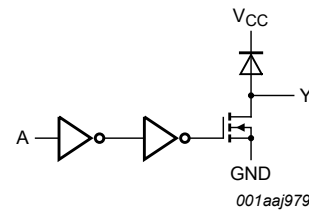


Fig. 2. Logic diagram (one gate)

5. Pinning information

5.1. Pinning

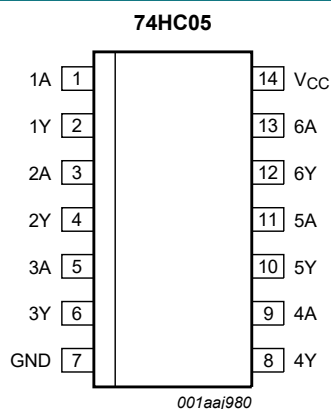


Fig. 3. Pin configuration SOT108-1 (SO14)

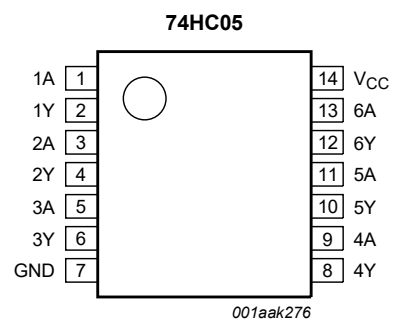
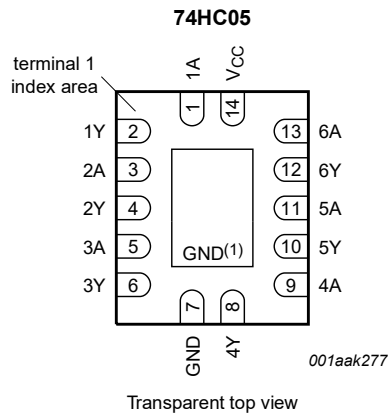


Fig. 4. Pin configuration SOT402-1 (TSSOP14)



(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

Fig. 5. Pin configuration SOT762-1 (DHVQFN14)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A to 6A	1, 3, 5, 9, 11, 13	data input
1Y to 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

Input	Output
nA	nY
L	Z
H	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ [1]	-	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ [1]	-	± 20	mA
V_O	output voltage	[1]	-0.5	$V_{CC} + 0.5\text{ V}$	V
I_O	output current	$V_O < V_{CC} + 0.5\text{ V}$	-	25	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.

For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1	-	±1	μA
I _{OZ}	OFF-state output current	V _I = V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.5	-	±5.0	-	±10	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	2.0	-	20	-	40	μA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics
GND = 0 V; for test circuit see Fig. 7.

Symbol	Parameter	Conditions	25 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Max (85 °C)	Max (125 °C)	
t _{PLZ}	LOW to OFF-state propagation delay	nA to nY; see Fig. 6						
		V _{CC} = 2.0 V	-	20	90	115	135	ns
		V _{CC} = 4.5 V	-	11	18	23	27	ns
t _{PZL}	OFF-state to LOW propagation delay	nA to nY; see Fig. 6						
		V _{CC} = 2.0 V	-	22	90	115	135	ns
		V _{CC} = 4.5 V	-	9	18	23	27	ns
t _{THL}	HIGH to LOW output transition time	see Fig. 6						
		V _{CC} = 2.0 V	-	18	75	95	110	ns
		V _{CC} = 4.5 V	-	6	15	19	22	ns
C _{PD}	power dissipation capacitance	per inverter; V _I = GND to V _{CC} ; V _{CC} = 5.0 V	[1]	4	-	-	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(0.5 \times C_L \times V_O^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

V_O = output voltage in V (output HIGH);

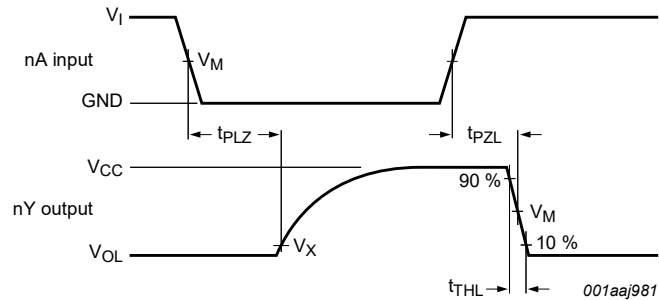
V_{CC} = supply voltage in V;

N = number of inputs switching;

R_L = load resistance in MΩ;

C_L = load capacitance in pF;

10.1. Waveforms and test circuit



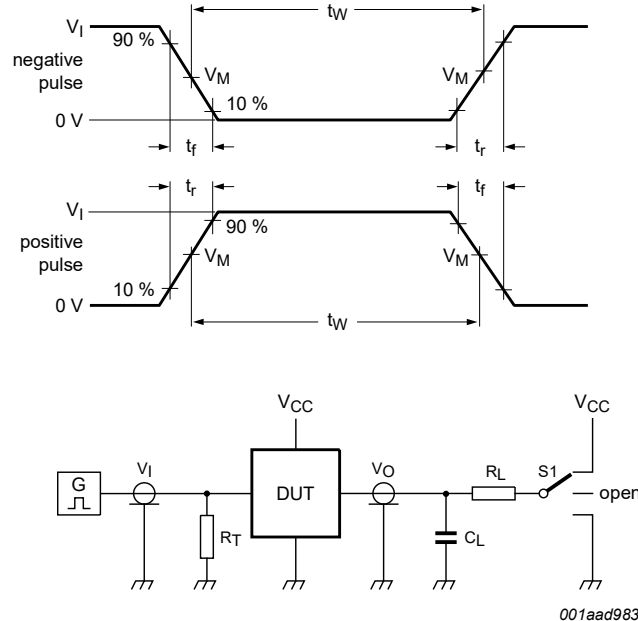
Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. The input nA to output nY propagation delays and output transition times

Table 8. Measurement points

Input	Output	
V_M	V_M	V_X
$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{CC}$



Test data is given in [Table 9](#).

Definitions test circuit:

R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

R_L = Load resistance.

Fig. 7. Test circuit for measuring switching times

Table 9. Test data

Input		Load		S1 position
V_I	t_r, t_f	C_L	R_L	t_{PZL}, t_{PLZ}
V_{CC}	6 ns	50 pF	1 kΩ	V_{CC}

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

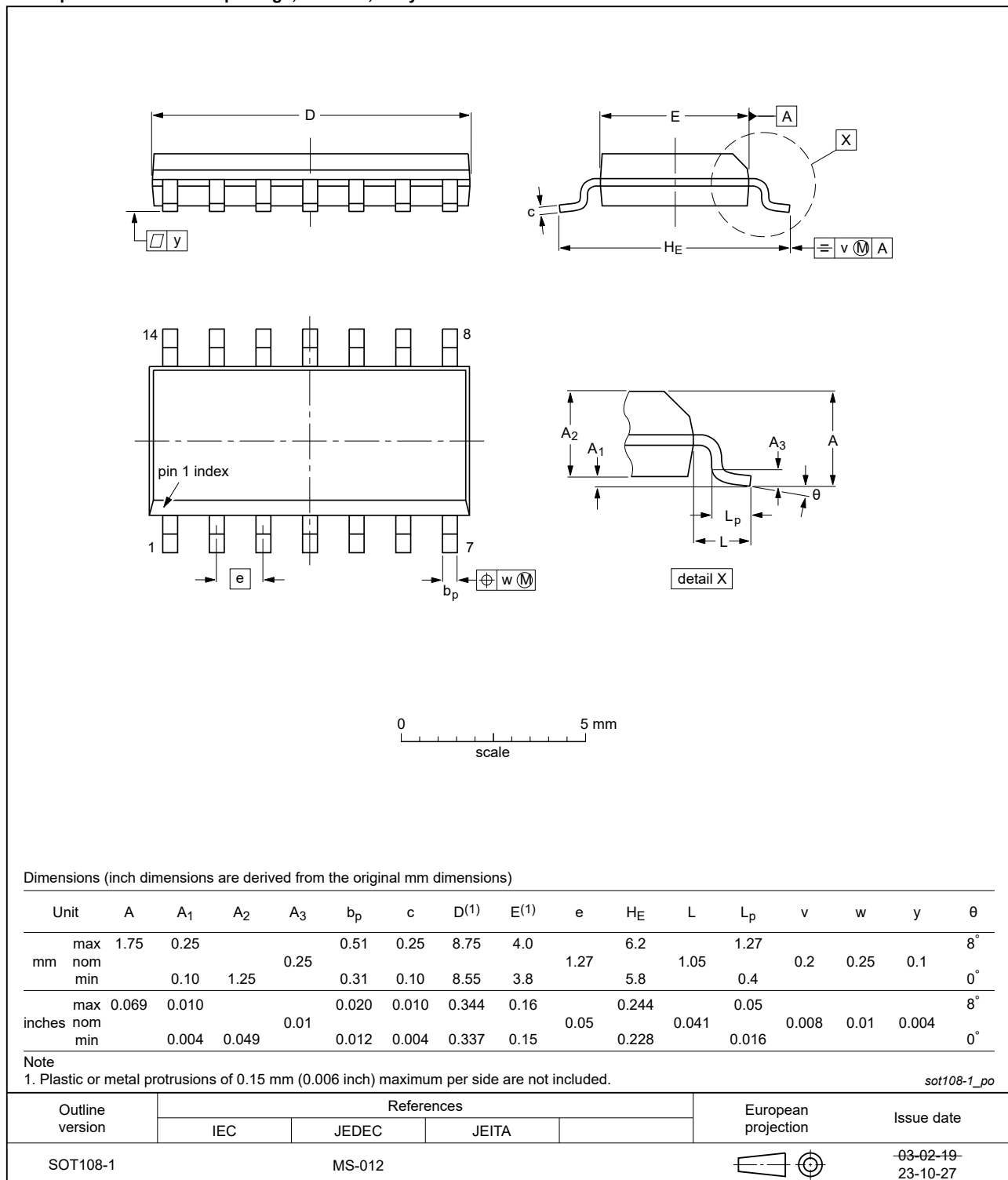


Fig. 8. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

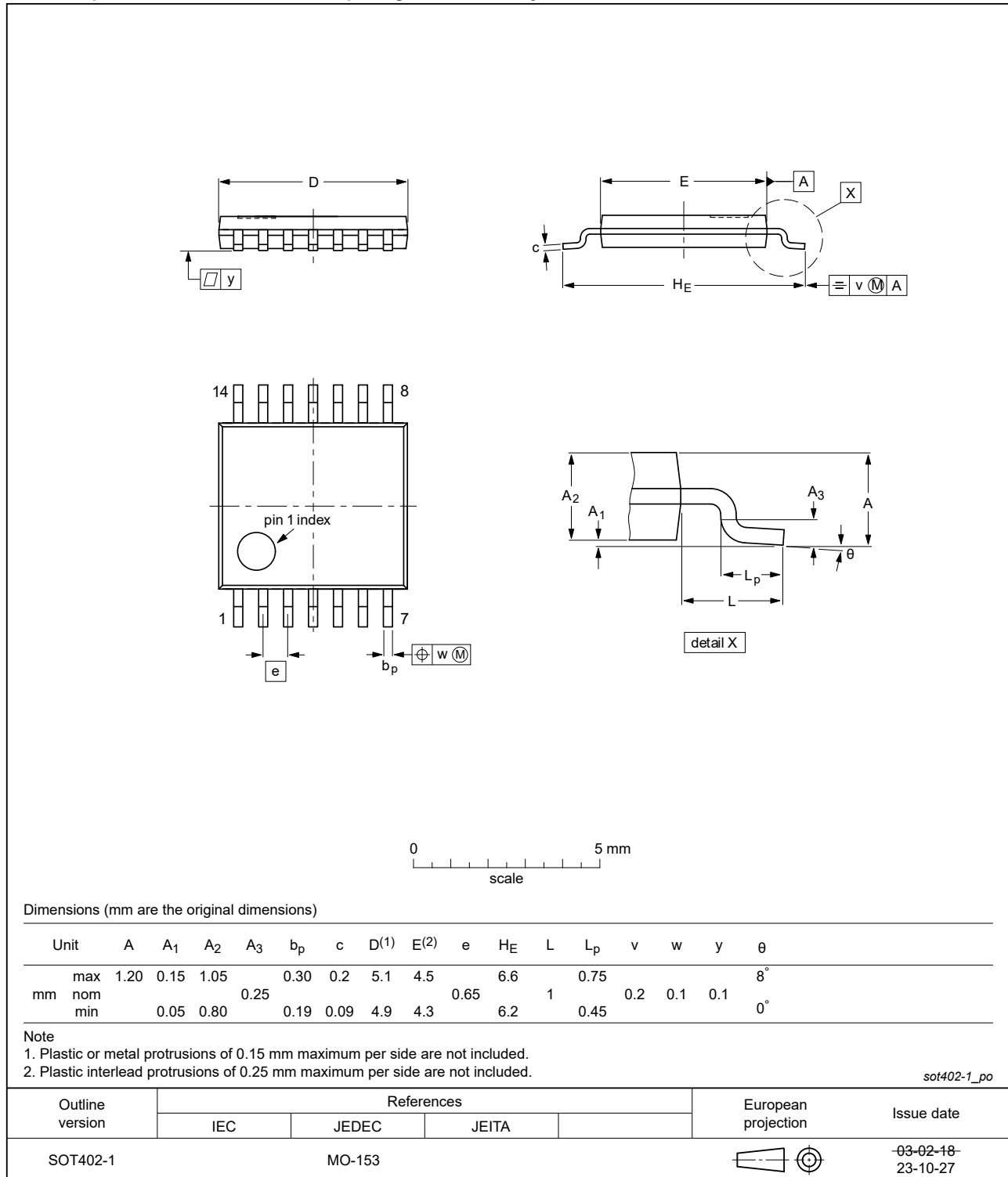


Fig. 9. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

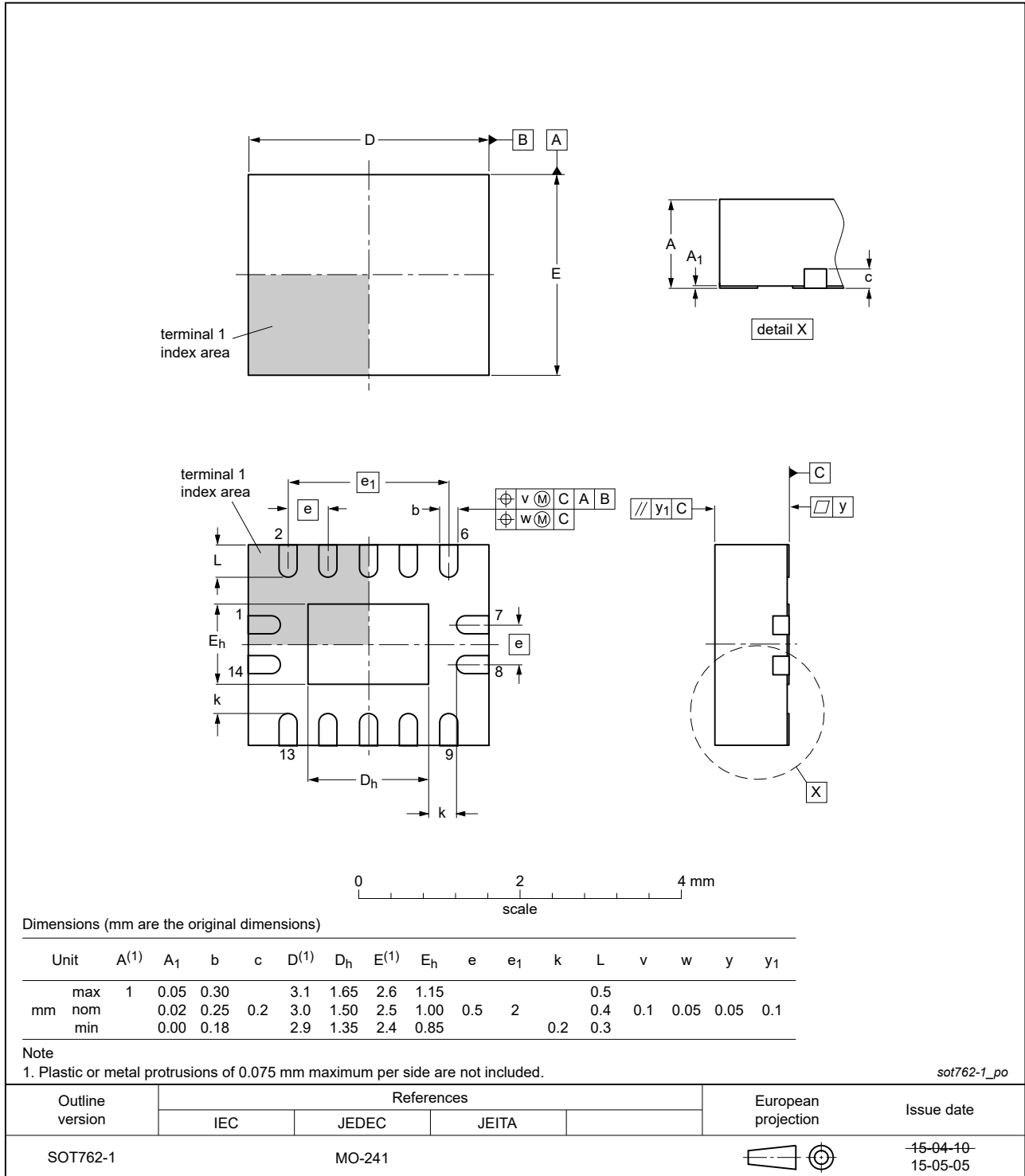


Fig. 10. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC05_Q100 v.3	20240314	Product data sheet	-	74HC05_Q100 v.2
Modifications:	<ul style="list-style-type: none"> • Fig. 8, Fig. 9: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153. • Section 2: ESD specification updated according to the latest JEDEC standard. 			
74HC05_Q100 v.2	20200708	Product data sheet	-	74HC05_Q100 v.1
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 1 and Section 2 updated. • Table 4: Derating values for P_{tot} total power dissipation have been updated. • Table 6: Conditions for I_{OZ} corrected. • Package outline drawing of SOT762-1 (Fig. 10) updated. 			
74HC05_Q100 v.1	20120709	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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Contents

1. General description	1
2. Features and benefits	1
3. Ordering information	1
4. Functional diagram	2
5. Pinning information	2
5.1. Pinning.....	2
5.2. Pin description.....	3
6. Functional description	3
7. Limiting values	4
8. Recommended operating conditions	4
9. Static characteristics	5
10. Dynamic characteristics	6
10.1. Waveforms and test circuit.....	7
11. Package outline	8
12. Abbreviations	11
13. Revision history	11
14. Legal information	12

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Date of release: 14 March 2024

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