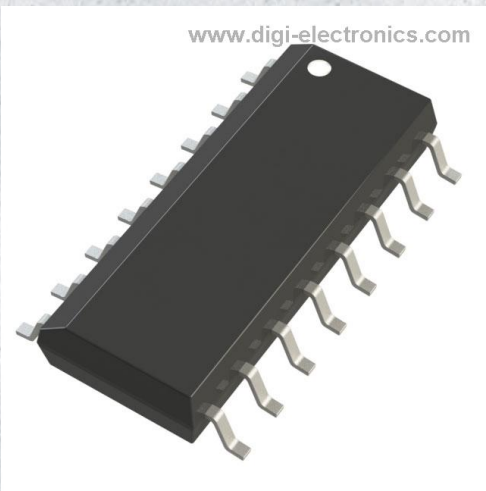
74HC175D,653 Datasheet



https://www.DiGi-Electronics.com

DiGi Electronics Part Number	74HC175D,653-DG
Manufacturer	Nexperia USA Inc.
Manufacturer Product Number	74HC175D,653
Description	IC FF D-TYPE SNGL 4BIT 16SO
Detailed Description	Flip Flop 1 Element D-Type 4 Bit Positive Edge 16-S OIC (0.154", 3.90mm Width)

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
74HC175D,653	Nexperia USA Inc.
Series:	Product Status:
74HC	Active
Function:	Type:
Master Reset	D-Type
Output Type:	Number of Elements:
Complementary	1
Number of Bits per Element:	Clock Frequency:
4	89 MHz
Max Propagation Delay @ V, Max CL:	Trigger Type:
30ns @ 6V, 50pF	Positive Edge
Current - Output High, Low:	Voltage - Supply:
5.2mA, 5.2mA	2V ~ 6V
Current - Quiescent (Iq):	Input Capacitance:
8 µA	3.5 pF
Operating Temperature:	Mounting Type:
-40°C ~ 125°C (TA)	Surface Mount
Supplier Device Package:	Package / Case:
16-SO	16-SOIC (0.154", 3.90mm Width)
Base Product Number:	
74HC175	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8542.39.0001	

74HC175; 74HCT175

Quad D-type flip-flop with reset; positive-edge trigger

Rev. 7 — 14 March 2024 Product data sheet

1. General description

The 74HC175; 74HCT175 is a quad positive-edge triggered D-type flip-flop with individual data inputs (Dn) and complementary outputs (Qn and $\overline{Qn}$). The common clock (CP) and master reset ($\overline{MR}$) inputs load and reset all flip-flops simultaneously. The D-input that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition will be stored in the flip-flop and appear at the Q output. A LOW on $\overline{MR}$ causes the flip-flops and outputs to be reset LOW. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Input levels:
  - For 74HC175: CMOS level
  - For 74HCT175: TTL level
- Four edge-triggered D-type flip-flops
- Asynchronous master reset
- Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C.

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC175D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT175D				
74HC175PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT175PW				

4. Functional diagram

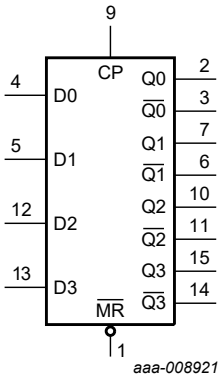


Fig. 1. Logic symbol

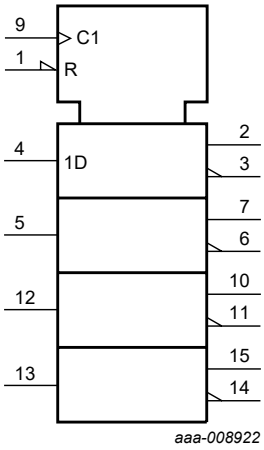


Fig. 2. IEC logic symbol

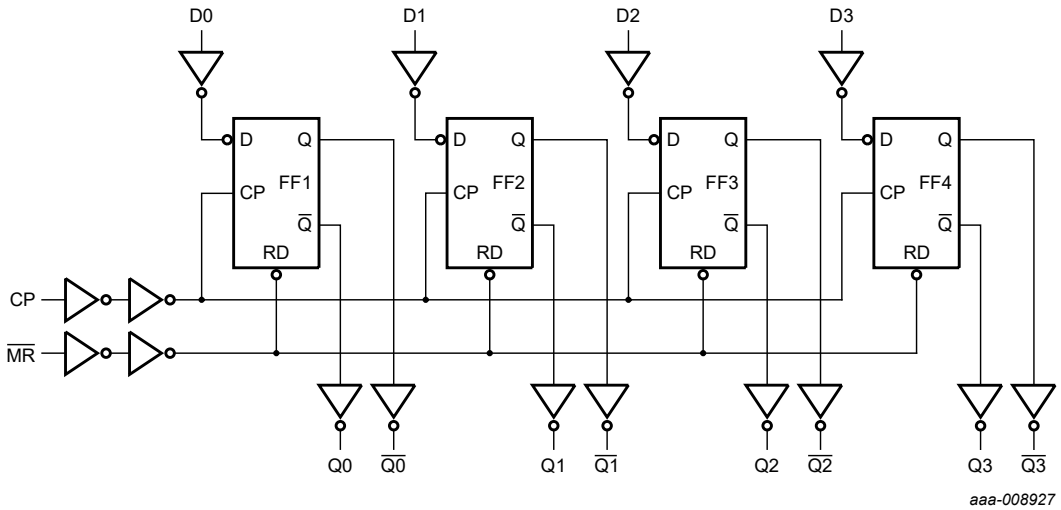


Fig. 3. Logic diagram

5. Pinning information

5.1. Pinning

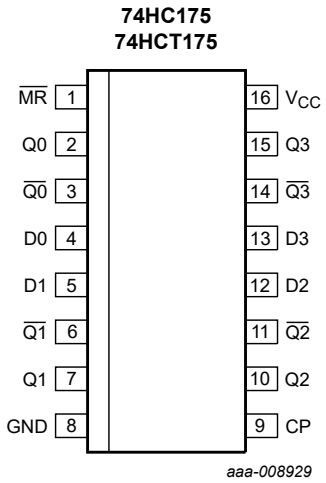


Fig. 4. Pin configuration SOT109-1 (SO16)

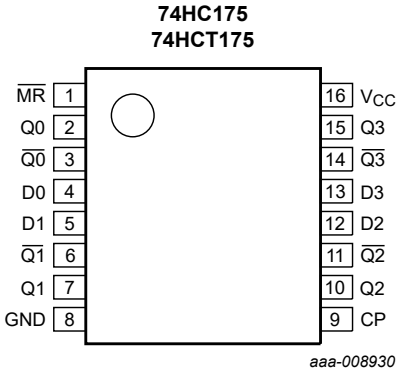


Fig. 5. Pin configuration SOT403-1 (TSSOP16)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{MR}$	1	asynchronous master reset input (active LOW)
Q0 to Q3	2, 7, 10, 15	flip-flop output
$\overline{Q0}$ to $\overline{Q3}$	3, 6, 11, 14	complementary flip-flop output
D0 to D3	4, 5, 12, 13	data input
GND	8	ground (0 V)
CP	9	clock input (LOW-to-HIGH edge-triggered)
V_{CC}	16	positive supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
X = don't care; ↑ = LOW-to-HIGH clock transition.

Operating modes	Inputs			Outputs	
	$\overline{MR}$	CP	Dn	Qn	$\overline{Qn}$
reset (clear)	L	X	X	L	H
load "1"	H	↑	h	H	L
load "0"	H	↑	l	L	H

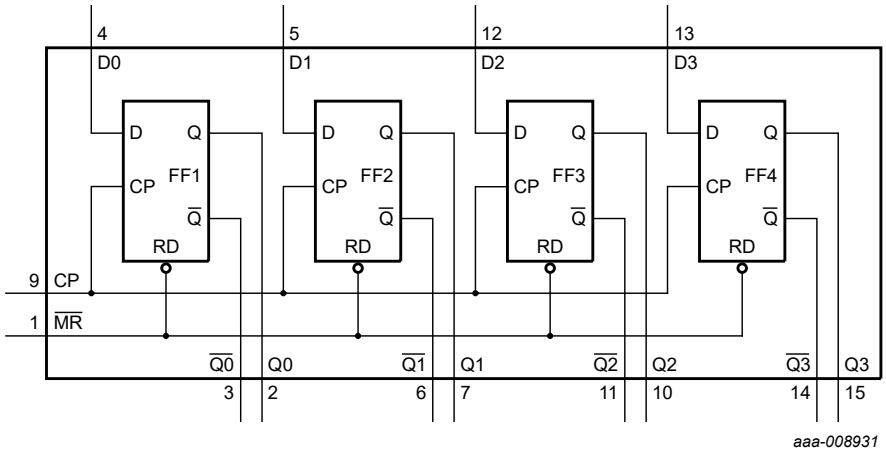


Fig. 6. Functional diagram

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V	-	±25	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C [1]	-	500	mW

[1] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC175			74HCT175			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	-	+125	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC175										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = -20 µA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = -20 µA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -20 µA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = -4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = -5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 20 µA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1	-	±1	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	-	80	-	160	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT175										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = 20 µA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 5.2 mA; V_{CC} = 5.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±0.1	-	±1	-	±1	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	8.0	-	80	-	160	µA
ΔI_{CC}	additional supply current	per input pin; V_I = V_{CC} - 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V								
		Dn input	-	40	144	-	180	-	196	µA
		CP input	-	60	216	-	270	-	294	µA
		$\overline{MR}$ input	-	100	360	-	450	-	490	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Fig. 10

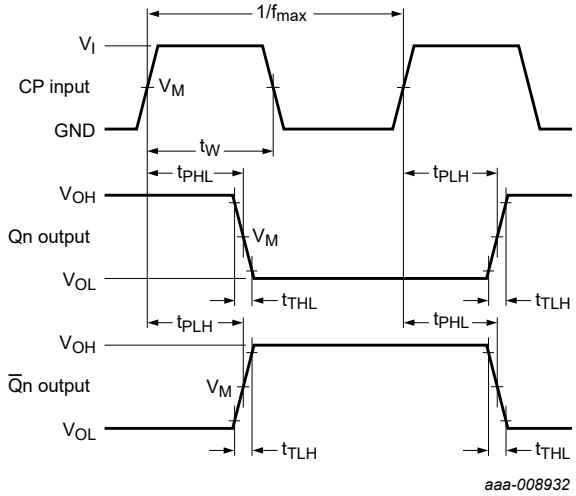
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC175										
t_{pd}	propagation delay	CP to Qn, $\overline{Q}$n; see Fig. 7 [1]								
		V_{CC} = 2.0 V	-	55	175	-	220	-	265	ns
		V_{CC} = 4.5 V	-	20	35	-	44	-	53	ns
		V_{CC} = 5 V; C_L = 15 pF	-	17	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	16	30	-	37	-	45	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Qn, $\overline{Q}$n; see Fig. 8								
		V_{CC} = 2.0 V	-	50	150	-	190	-	225	ns
		V_{CC} = 4.5 V	-	18	30	-	38	-	45	ns
		V_{CC} = 5 V; C_L = 15 pF	-	15	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	14	26	-	33	-	38	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_t	transition time	Qn output; see Fig. 7 [2]								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t_W	pulse width	CP input HIGH or LOW; see Fig. 7								
		V_{CC} = 2.0 V	80	22	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	8	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	6	-	17	-	20	-	ns
		$\overline{MR}$ input LOW; see Fig. 8								
		V_{CC} = 2.0 V	80	19	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	7	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	6	-	17	-	20	-	ns
t_{rec}	recovery time	$\overline{MR}$ to CP; see Fig. 8								
		V_{CC} = 2.0 V	5	-33	-	5	-	5	-	ns
		V_{CC} = 4.5 V	5	-12	-	5	-	5	-	ns
		V_{CC} = 6.0 V	5	-10	-	5	-	5	-	ns
t_{su}	set-up time	Dn to CP; see Fig. 9								
		V_{CC} = 2.0 V	80	3	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	1	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	1	-	17	-	20	-	ns
t_h	hold time	Dn to CP; see Fig. 9								
		V_{CC} = 2.0 V	25	2	-	30	-	40	-	ns
		V_{CC} = 4.5 V	5	0	-	6	-	8	-	ns
		V_{CC} = 6.0 V	4	0	-	5	-	7	-	ns
f_{max}	maximum frequency	CP input; see Fig. 7								
		V_{CC} = 2.0 V	6	25	-	4.8	-	4	-	MHz
		V_{CC} = 4.5 V	30	75	-	24	-	20	-	MHz
		V_{CC} = 5 V; C_L = 15 pF	-	83	-	-	-	-	-	MHz
		V_{CC} = 6.0 V	35	89	-	28	-	24	-	MHz
C_{PD}	power dissipation capacitance	per package; V_I = GND to V_{CC} [3]	-	32	-	-	-	-	-	pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT175										
t_{pd}	propagation delay	CP to Qn, $\overline{Q}$n; see Fig. 7 [1]								
		V_{CC} = 4.5 V	-	19	33	-	41	-	50	ns
		V_{CC} = 5 V; C_L = 15 pF	-	16	-	-	-	-	-	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to Qn; see Fig. 8								
		V_{CC} = 4.5 V	-	22	38	-	48	-	57	ns
		V_{CC} = 5 V; C_L = 15 pF	-	19	-	-	-	-	-	ns
		$\overline{MR}$ to $\overline{Q}$n; see Fig. 8								
		V_{CC} = 4.5 V	-	19	35	-	44	-	53	ns
		V_{CC} = 5 V; C_L = 15 pF	-	16	-	-	-	-	-	ns
t_t	transition time	Qn output; see Fig. 7 [2]								
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
t_W	pulse width	CP input HIGH or LOW; see Fig. 7								
		V_{CC} = 4.5 V	20	12	-	25	-	30	-	ns
		$\overline{MR}$ input LOW; see Fig. 8								
		V_{CC} = 4.5 V	20	11	-	25	-	30	-	ns
t_{rec}	recovery time	$\overline{MR}$ to CP; see Fig. 8								
		V_{CC} = 4.5 V	5	-10	-	5	-	5	-	ns
t_{su}	set-up time	Dn to CP; see Fig. 9								
		V_{CC} = 4.5 V	16	5	-	20	-	24	-	ns
t_h	hold time	Dn to CP; see Fig. 9								
		V_{CC} = 4.5 V	5	0	-	5	-	5	-	ns
f_{max}	maximum frequency	CP input; see Fig. 7								
		V_{CC} = 4.5 V	25	49	-	20	-	17	-	MHz
		V_{CC} = 5 V; C_L = 15 pF	-	54	-	-	-	-	-	MHz
C_{PD}	power dissipation capacitance	per package; V_I = GND to V_{CC} - 1.5 V [3]	-	34	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.
[2] t_t is the same as t_{THL} and t_{TLH}.
[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V.

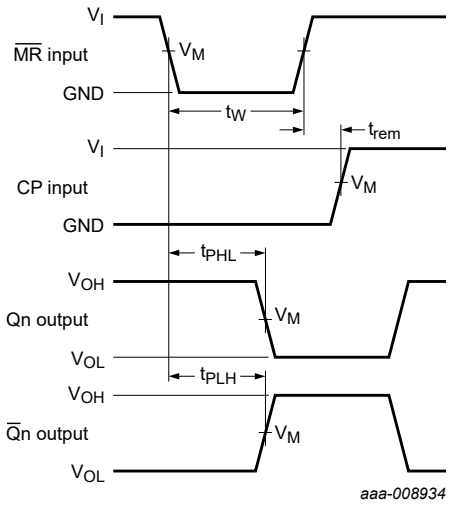
10.1. Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

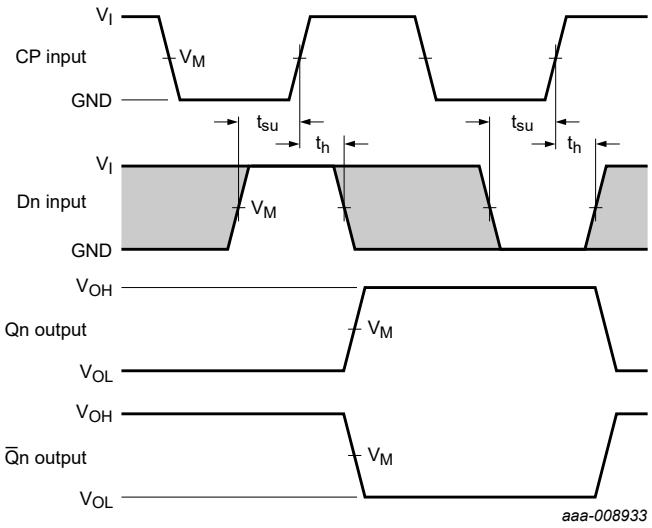
Fig. 7. Input to output propagation delay, output transition time, clock input pulse width and maximum frequency



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 8. Master reset to output propagation delays, master reset pulse width and master reset to clock recovery time



Measurement points are given in Table 8.

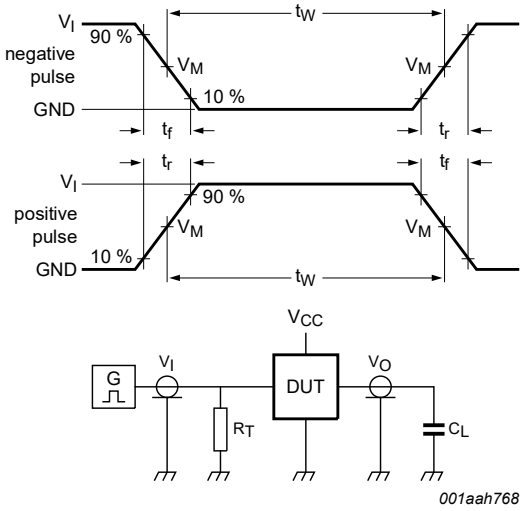
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 9. Data set-up and hold times for data input

Table 8. Measurement points

Type	Input		Output
	V_I	V_M	V_M
74HC175	V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$
74HCT175	3 V	1.3 V	1.3 V



Test data is given in Table 9.

Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

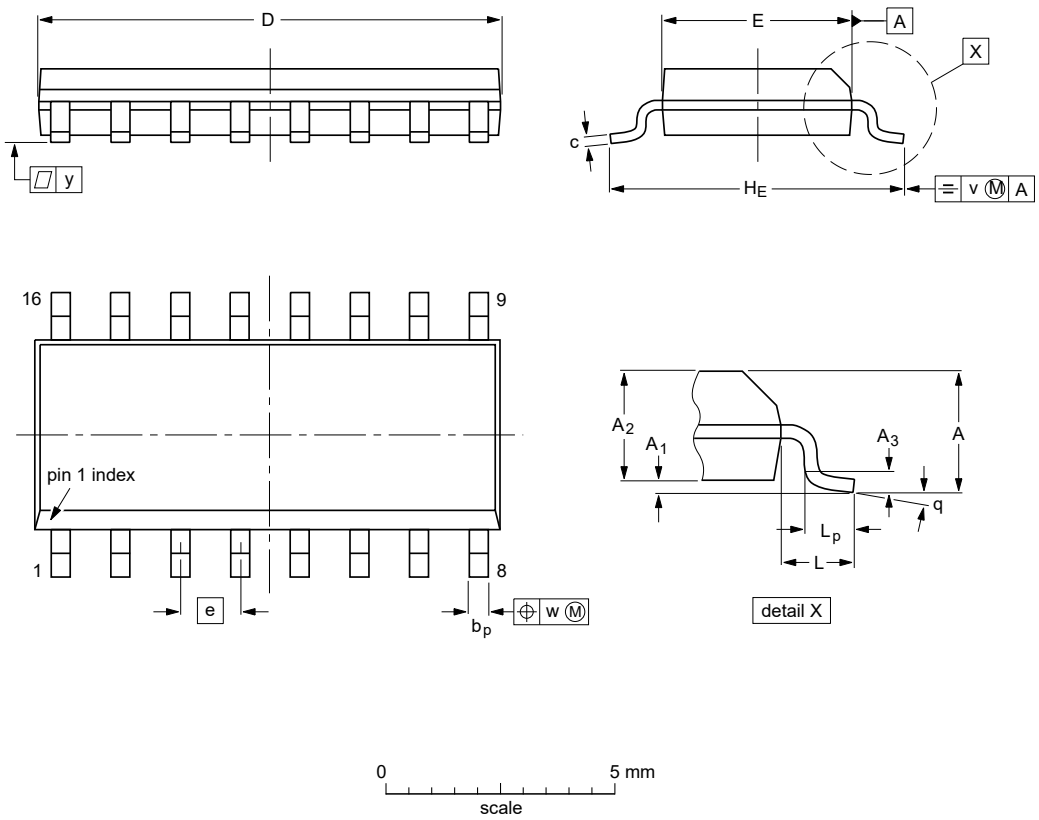
Fig. 10. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load		Test
	V_I	t_r, t_f	C_L	R_L	
74HC175	V_{CC}	6 ns	15 pF, 50 pF	1 kΩ	t_{PLH}, t_{PHL}
74HCT175	3 V	6 ns	15 pF, 50 pF	1 kΩ	t_{PLH}, t_{PHL}

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	10.0	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	9.8	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.394	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.386	0.15		0.228		0.016				0°

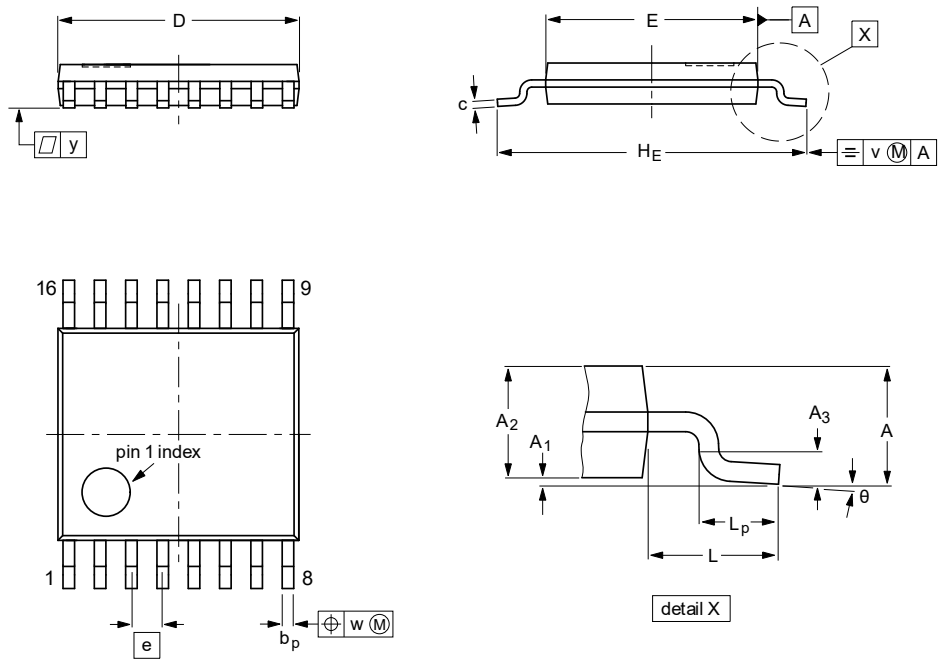
Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

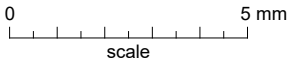
sot109-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT109-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 11. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**





Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
	nom				0.25					0.65		1		0.2	0.1	0.1	
	min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot403-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 12. Package outline SOT403-1 (TSSOP16)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT175 v.7	20240314	Product data sheet	-	74HC_HCT175 v.6
Modifications:	• Fig. 11, Fig. 12: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153. • Section 2: ESD specification updated according to the latest JEDEC standard.			
74HC_HCT175 v.6	20210204	Product data sheet	-	74HC_HCT175 v.5
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type numbers 74HC175DB and 74HCT175DB (SOT338-1 / SSOP16) removed. • Section 7: Derating values for P_{tot} total power dissipation updated.			
74HC_HCT175 v.5	20160129	Product data sheet	-	74HC_HCT175 v.4
Modifications:	• Type numbers 74HC175N and 74HCT175N (SOT38-4) removed.			
74HC_HCT175 v.4	20140408	Product data sheet	-	74HC_HCT175 v.3
Modifications:	• General description corrected (errata).			
74HC_HCT175 v.3	20140331	Product data sheet	-	74HC_HCT175_CNV_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
74HC_HCT175_CNV_2	19980708	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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Contents

1. General description....1
2. Features and benefits....1
3. Ordering information....1
4. Functional diagram....2
5. Pinning information....3
5.1. Pinning....3
5.2. Pin description....3
6. Functional description....3
7. Limiting values....4
8. Recommended operating conditions....4
9. Static characteristics....5
10. Dynamic characteristics....6
10.1. Waveforms and test circuit....9
11. Package outline....12
12. Abbreviations....14
13. Revision history....14
14. Legal information....15

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