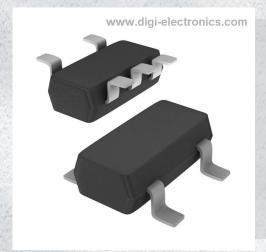


74HC1G86GV,125 Datasheet



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DiGi Electronics Part Number 74HC1G86GV,125-DG

Manufacturer Nexperia USA Inc.

Manufacturer Product Number 74HC1G86GV,125

Description IC GATE XOR 1CH 2-INP SC74A

Detailed Description XOR (Exclusive OR) IC 1 Channel SC-74A



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Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
74HC1G86GV,125	Nexperia USA Inc.
Series:	Product Status:
74HC	Active
Logic Type:	Number of Circuits:
XOR (Exclusive OR)	1
Number of Inputs:	Features:
2	
Voltage - Supply:	Current - Quiescent (Max):
2V ~ 6V	20 μΑ
Current - Output High, Low:	Input Logic Level - Low:
2.6mA, 2.6mA	0.5V ~ 1.8V
Input Logic Level - High:	Max Propagation Delay @ V, Max CL:
1.5V ~ 4.2V	23ns @ 6V, 50pF
Operating Temperature:	Mounting Type:
-40°C ~ 125°C	Surface Mount
Supplier Device Package:	Package / Case:
SC-74A	SC-74A, SOT-753
Base Product Number:	
74HC1G86	

Environmental & Export classification

8542.39.0001

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	

1. General description

The 74HC1G86; 74HCT1G86 is a single 2-input EXCLUSIVE-OR gate. Inputs also include clamp diodes, this enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- · Input levels:
 - For 74HC1G86: CMOS level
 - For 74HCT1G86: TTL level
- CMOS low power dissipation
- · High noise immunity
- · Symmetrical output impedance
- · Balanced propagation delays
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85° C and from -40° C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package					
	Temperature range	Name	Description	Version		
74HC1G86GW 74HCT1G86GW	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	<u>SOT353-1</u>		
74HC1G86GV 74HCT1G86GV	-40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	<u>SOT753</u>		



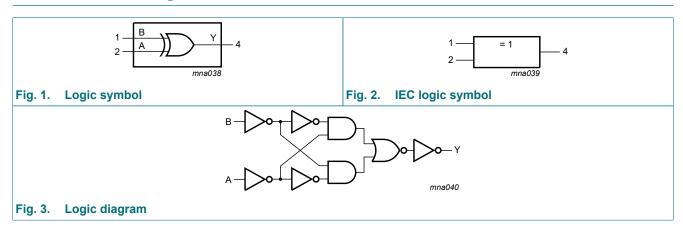
4. Marking

Table 2. Marking codes

Type number	Marking[1]
74HC1G86GW	НН
74HCT1G86GW	TH
74HC1G86GV	H86
74HCT1G86GV	Т86

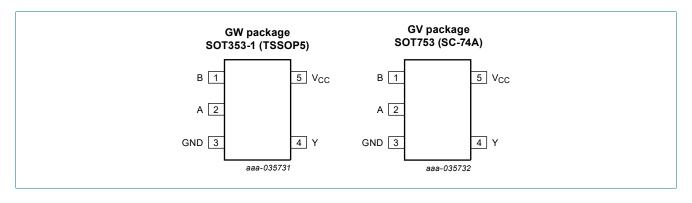
^[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram



6. Pinning information

6.1. Pinning



2/11

6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
В	1	data input
Α	2	data input
GND	3	ground (0 V)
Υ	4	data output
V _{CC}	5	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level

Inputs		Output
A	В	Υ
L	L	L
L	Н	Н
Н	L	Н
Н	Н	L

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			-0.5	+7.0	V
I _{IK}	input clamping current	$V_{I} < -0.5 \text{ V or } V_{I} > V_{CC} + 0.5 \text{ V}$		-	±20	mA
I _{OK}	output clamping current	$V_{O} < -0.5 \text{ V or } V_{O} > V_{CC} + 0.5 \text{ V}$		-	±20	mA
Io	output current	$-0.5 \text{ V} < \text{V}_{\text{O}} < \text{V}_{\text{CC}} + 0.5 \text{ V}$	[1]	-	±12.5	mA
I _{CC}	supply current			-	25	mA
I_{GND}	ground current			-25	-	mA
T _{stg}	storage temperature			-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	[2]	-	250	mW

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

^[2] For SOT353-1 (TSSOP5) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C. For SOT753 (SC-74A) package: P_{tot} derates linearly with 3.8 mW/K above 85 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74HC1G86		74HCT1G86			Unit	
			Min	Тур	Max	Min	Тур	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
VI	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
Vo	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
	fall rate	V _{CC} = 4.5 V	-	-	139	-	-	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V). All typical values are measured at T_{amb} = 25 °C.

Symbol	Parameter	Conditions	-40	°C to +8	5 °C	-40 °C to	+125 °C	Unit
			Min	Тур	Max	Min	Max	-
74HC1G	86		'					
V _{IH}	HIGH-level	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	V
	input voltage	V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	V
V _{IL}	LOW-level input	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	V
	voltage	V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL}						
	output voltage	I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	V
		I _O = -2.0 mA; V _{CC} = 4.5 V	4.13	4.32	-	3.7	-	V
		I _O = -2.6 mA; V _{CC} = 6.0 V	5.63	5.81	-	5.2	-	V
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL}						
	output voltage	I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	V
		I _O = 2.0 mA; V _{CC} = 4.5 V	-	0.15	0.33	-	0.4	V
		I _O = 2.6 mA; V _{CC} = 6.0 V	-	0.16	0.33	-	0.4	V
l _l	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	1.0	-	1.0	μA
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	-	10	-	20	μΑ
C _I	input capacitance		-	1.5	-	-	-	pF

2-input EXCLUSIVE-OR gate

Symbol	Parameter	Conditions	-40	°C to +8	5 °C	-40 °C to	+125 °C	Unit
			Min	Тур	Max	Min	Max	
74HCT1	G86				'		<u>'</u>	
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL}						
	output voltage	I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	V
		I _O = -2.0 mA; V _{CC} = 4.5 V	4.13	4.32	-	3.7	-	V
V_{OL}	LOW-level	V _I = V _{IH} or V _{IL}						
	output voltage	I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	V
		I _O = 2.0 mA; V _{CC} = 4.5 V	-	0.15	0.33	-	0.4	V
l _l	input leakage current	$V_1 = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	1.0	-	1.0	μA
I _{CC}	supply current	$V_{I} = V_{CC}$ or GND; $I_{O} = 0$ A; $V_{CC} = 5.5$ V	-	-	10	-	20	μA
ΔI _{CC}	additional supply current	per input; $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V};$ $V_1 = V_{CC} - 2.1 \text{ V}; I_O = 0 \text{ A}$	-	-	500	-	850	μΑ
Cı	input capacitance		-	1.5	-	-	-	pF

11. Dynamic characteristics

Table 8. Dynamic characteristics

GND = 0 V; $t_r = t_f \le 6.0$ ns; All typical values are measured at $T_{amb} = 25$ °C. For test circuit see Fig. 5

Symbol	abol Parameter Conditions		-40	°C to +8	5 °C	-40 °C to	-40 °C to +125 °C		
				Min	Тур	Max	Min	Max	
74HC1G	86								
t _{pd}	propagation delay	A and B to Y; see Fig. 4	[1]						
		V _{CC} = 2.0 V; C _L = 50 pF		-	22	115	-	135	ns
		V _{CC} = 4.5 V; C _L = 50 pF		-	11	23	-	27	ns
		V _{CC} = 5.0 V; C _L = 15 pF		-	9	-	-	-	ns
		V _{CC} = 6.0 V; C _L = 50 pF		-	9	20	-	23	ns
C_{PD}	power dissipation capacitance	$V_I = GND \text{ to } V_{CC}$	[2]	-	23	-	-	-	pF
74HCT1	G86		·						
t _{pd}	propagation delay	A and B to Y; see Fig. 4	[1]						
		V _{CC} = 4.5 V; C _L = 50 pF		-	13	23	-	27	ns
		V _{CC} = 5.0 V; C _L = 15 pF		-	10	-	-	-	ns
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} - 1.5 V	[2]	-	23	-	-	-	pF

 t_{pd} is the same as t_{PLH} and t_{PHL} . C_{PD} is used to determine the dynamic power dissipation P_D (µW). $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where: $f_i = \text{input frequency in MHz}$

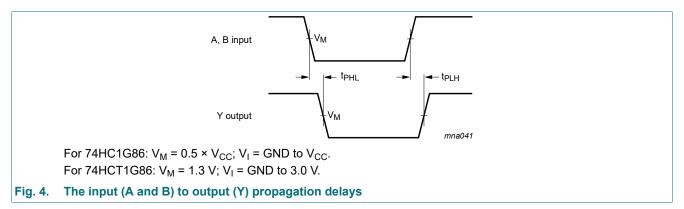
f_o = output frequency in MHz

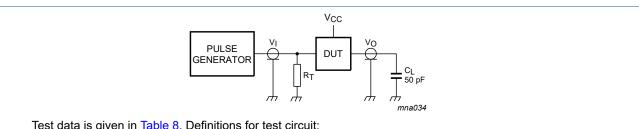
C_L = output load capacitance in pF

 V_{CC} = supply voltage in V $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

2-input EXCLUSIVE-OR gate

11.1. Waveforms and test circuit





Test data is given in <u>Table 8</u>. Definitions for test circuit:

C_L = Load capacitance including jig and probe capacitance;

 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Test circuit for measuring switching times Fig. 5.

12. Package outline

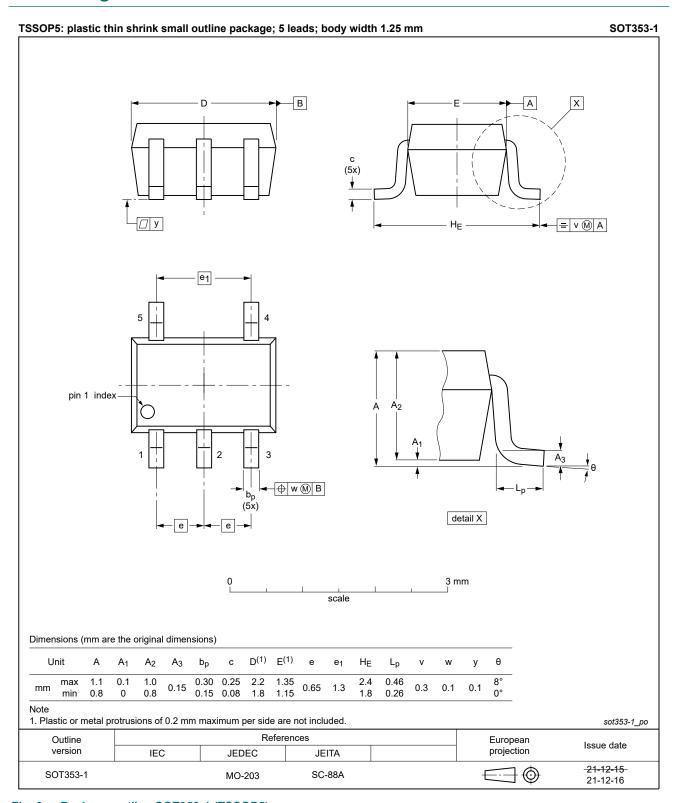


Fig. 6. Package outline SOT353-1 (TSSOP5)

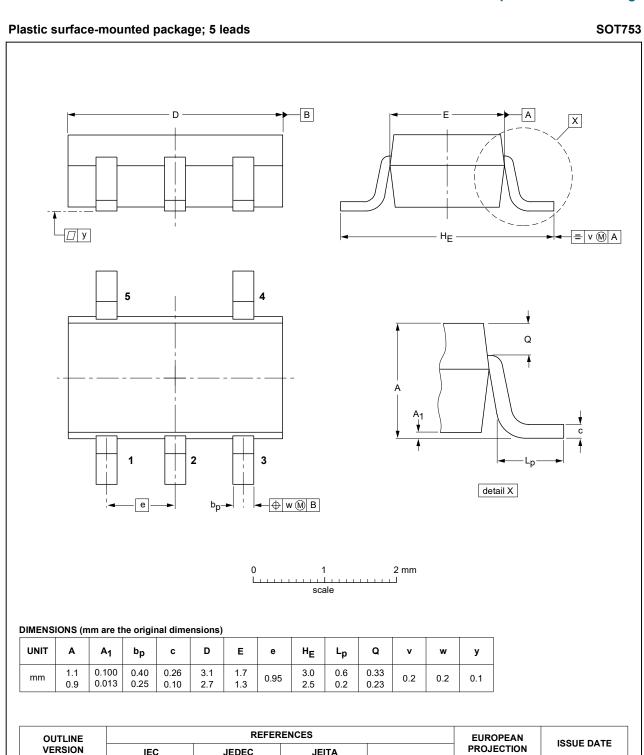


Fig. 7. Package outline SOT753 (SC-74A)

SOT753

IEC

JEDEC

JEITA

SC-74A

02-04-16

06-03-16

2-input EXCLUSIVE-OR gate

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
НВМ	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
74HC_HCT1G86 v.6	20240625	Product data sheet	-	74HC_HCT1G86 v.5	
Modifications:	<u>Section 2</u> : ESD specification updated according to the latest JEDEC standard.				
74HC_HCT1G86 v.5	20220127	Product data sheet	-	74HC_HCT1G86 v.4	
Modifications:	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Section 1 and Section 2 updated. Table 5: Derating values for P_{tot} total power dissipation updated. Fig. 6: Package outline drawing for SOT353-1 (TSSOP5) has changed. 				
74HC_HCT1G86 v.4	20070720	Product data sheet	-	74HC_HCT1G86 v.3	
Modifications:	 The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Package SOT353 changed to SOT353-1 in <u>Table 1</u> and <u>Fig. 6</u>. Quick Reference Data and Soldering sections removed. <u>Section 2</u> updated. 				
74HC_HCT1G86 v.3	20020515	Product specification	-	74HC_HCT1G86 v.2	
74HC_HCT1G86 v.2	20010406	Product specification	-	74HC_HCT1G86 v.1	
74HC_HCT1G86 v.1	19980805	Product specification	-	-	

2-input EXCLUSIVE-OR gate

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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2-input EXCLUSIVE-OR gate

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