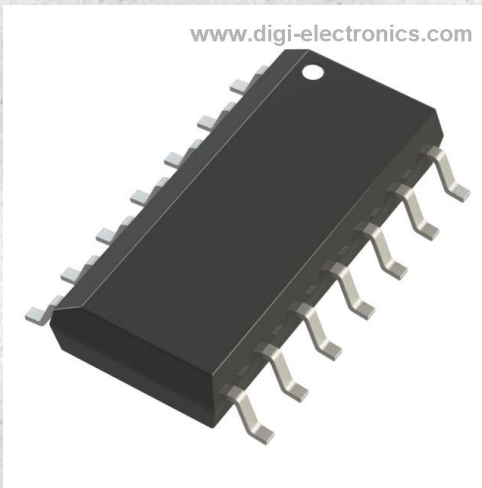


74HC86D,653 Datasheet



<https://www.DiGi-Electronics.com>

| | |
|------------------------------|---------------------------------------|
| DiGi Electronics Part Number | 74HC86D,653-DG |
| Manufacturer | Nexperia USA Inc. |
| Manufacturer Product Number | 74HC86D,653 |
| Description | IC GATE XOR 4CH 2-INP 14SO |
| Detailed Description | XOR (Exclusive OR) IC 4 Channel 14-SO |



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RFQ Email: Info@DiGi-Electronics.com

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Purchase and inquiry

Manufacturer Product Number:

74HC86D,653

Series:

74HC

Logic Type:

XOR (Exclusive OR)

Number of Inputs:

2

Voltage - Supply:

2V ~ 6V

Current - Output High, Low:

5.2mA, 5.2mA

Input Logic Level - High:

1.5V ~ 4.2V

Operating Temperature:

-40°C ~ 125°C

Supplier Device Package:

14-SO

Base Product Number:

74HC86

Manufacturer:

Nexperia USA Inc.

Product Status:

Active

Number of Circuits:

4

Features:

-

Current - Quiescent (Max):2 μ A**Input Logic Level - Low:**

0.5V ~ 1.8V

Max Propagation Delay @ V, Max CL:

20ns @ 6V, 50pF

Mounting Type:

Surface Mount

Package / Case:

14-SOIC (0.154", 3.90mm Width)

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

74HC86; 74HCT86

Quad 2-input EXCLUSIVE-OR gate

Rev. 7 — 2 April 2024

Product data sheet

1. General description

The 74HC86; 74HCT86 is a quad 2-input EXCLUSIVE-OR gate. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- Input levels:
 - For 74HC86: CMOS level
 - For 74HCT86: TTL level
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | |
|---|-------------------|---------|---|--------------------------|
| | Temperature range | Name | Description | Version |
| 74HC86D 74HCT86D | -40 °C to +125 °C | SO14 | plastic small outline package; 14 leads; body width 3.9 mm | SOT108-1 |
| 74HC86PW 74HCT86PW | -40 °C to +125 °C | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |

4. Functional diagram

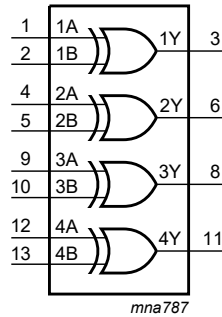


Fig. 1. Logic symbol

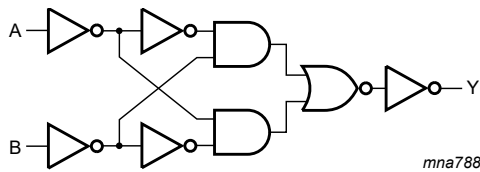


Fig. 2. Logic diagram (one gate)

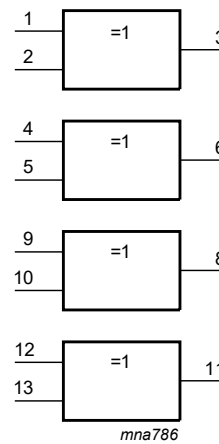
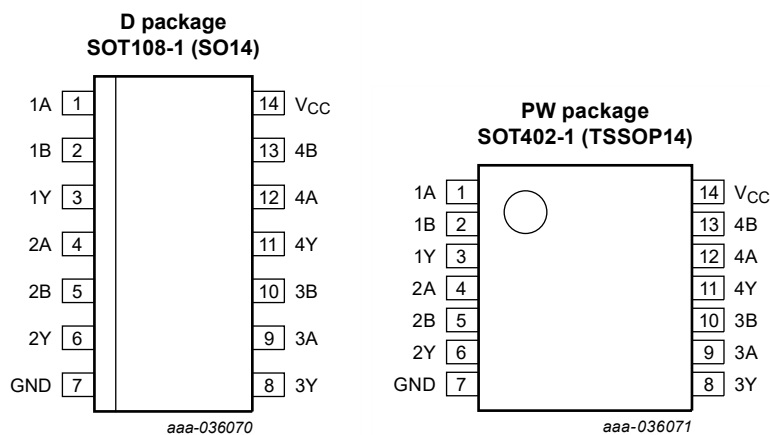


Fig. 3. IEC logic symbol

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|-----------------|--------------|----------------|
| 1A to 4A | 1, 4, 9, 12 | data input |
| 1B to 4B | 2, 5, 10, 13 | data input |
| 1Y to 4Y | 3, 6, 8, 11 | data output |
| GND | 7 | ground (0 V) |
| V _{CC} | 14 | supply voltage |

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level.

| Input nA | Input nB | Output nY |
|----------|----------|-----------|
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------|---|------|------|------|
| V _{CC} | supply voltage | | -0.5 | +7 | V |
| I _{IK} | input clamping current | V _I < -0.5 V or V _I > V _{CC} + 0.5 V [1] | - | ±20 | mA |
| I _{OK} | output clamping current | V _O < -0.5 V or V _O > V _{CC} + 0.5 V [1] | - | ±20 | mA |
| I _O | output current | -0.5 V < V _O < V _{CC} + 0.5 V | - | ±25 | mA |
| I _{CC} | supply current | | - | 50 | mA |
| I _{GND} | ground current | | -50 | - | mA |
| T _{stg} | storage temperature | | -65 | +150 | °C |
| P _{tot} | total power dissipation | [2] | - | 500 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.
For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

| Symbol | Parameter | Conditions | 74HC86 | | | 74HCT86 | | | Unit |
|---------------------|-------------------------------------|-------------------------|--------|------|----------|---------|------|----------|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V_{CC} | supply voltage | | 2.0 | 5.0 | 6.0 | 4.5 | 5.0 | 5.5 | V |
| V_I | input voltage | | 0 | - | V_{CC} | 0 | - | V_{CC} | V |
| V_O | output voltage | | 0 | - | V_{CC} | 0 | - | V_{CC} | V |
| T_{amb} | ambient temperature | | -40 | +25 | +125 | -40 | +25 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 2.0\text{ V}$ | - | - | 625 | - | - | - | ns/V |
| | | $V_{CC} = 4.5\text{ V}$ | - | 1.67 | 139 | - | 1.67 | 139 | ns/V |
| | | $V_{CC} = 6.0\text{ V}$ | - | - | 83 | - | - | - | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|---------------|---------------------------|---|-------|------|-----------|------------------|---------|-------------------|---------|---------------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74HC86 | | | | | | | | | | |
| V_{IH} | HIGH-level input voltage | $V_{CC} = 2.0\text{ V}$ | 1.5 | 1.2 | - | 1.5 | - | 1.5 | - | V |
| | | $V_{CC} = 4.5\text{ V}$ | 3.15 | 2.4 | - | 3.15 | - | 3.15 | - | V |
| | | $V_{CC} = 6.0\text{ V}$ | 4.2 | 3.2 | - | 4.2 | - | 4.2 | - | V |
| V_{IL} | LOW-level input voltage | $V_{CC} = 2.0\text{ V}$ | - | 0.8 | 0.5 | - | 0.5 | - | 0.5 | V |
| | | $V_{CC} = 4.5\text{ V}$ | - | 2.1 | 1.35 | - | 1.35 | - | 1.35 | V |
| | | $V_{CC} = 6.0\text{ V}$ | - | 2.8 | 1.8 | - | 1.8 | - | 1.8 | V |
| V_{OH} | HIGH-level output voltage | $V_I = V_{IH}$ or V_{IL} | | | | | | | | |
| | | $I_O = -20\text{ }\mu\text{A}$; $V_{CC} = 2.0\text{ V}$ | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | $I_O = -20\text{ }\mu\text{A}$; $V_{CC} = 4.5\text{ V}$ | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | $I_O = -20\text{ }\mu\text{A}$; $V_{CC} = 6.0\text{ V}$ | 5.9 | 6.0 | - | 5.9 | - | 5.9 | - | V |
| | | $I_O = -4.0\text{ mA}$; $V_{CC} = 4.5\text{ V}$ | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| V_{OL} | LOW-level output voltage | $I_O = -5.2\text{ mA}$; $V_{CC} = 6.0\text{ V}$ | 5.48 | 5.81 | - | 5.34 | - | 5.2 | - | V |
| | | $V_I = V_{IH}$ or V_{IL} | | | | | | | | |
| | | $I_O = 20\text{ }\mu\text{A}$; $V_{CC} = 2.0\text{ V}$ | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O = 20\text{ }\mu\text{A}$; $V_{CC} = 4.5\text{ V}$ | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | $I_O = 20\text{ }\mu\text{A}$; $V_{CC} = 6.0\text{ V}$ | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| I_I | input leakage current | $I_O = 4.0\text{ mA}$; $V_{CC} = 4.5\text{ V}$ | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| | | $I_O = 5.2\text{ mA}$; $V_{CC} = 6.0\text{ V}$ | - | 0.16 | 0.26 | - | 0.33 | - | 0.4 | V |
| | | $V_I = V_{CC}$ or GND; $V_{CC} = 6.0\text{ V}$ | - | - | ± 0.1 | - | ± 1 | - | ± 1 | μA |
| I_{CC} | supply current | $V_I = V_{CC}$ or GND; $I_O = 0\text{ A}$; $V_{CC} = 6.0\text{ V}$ | - | - | 2.0 | - | 20 | - | 40 | μA |
| C_I | input capacitance | | - | 3.5 | - | - | - | - | - | pF |

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|------------------|---------------------------|---|-------|------|------|------------------|------|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74HCT86 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 4.5 V to 5.5 V | 2.0 | 1.6 | - | 2.0 | - | 2.0 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 4.5 V to 5.5 V | - | 1.2 | 0.8 | - | 0.8 | - | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = -20 µA | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -4.0 mA | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = 20 µA | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 5.2 mA | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 5.5 V | - | - | ±0.1 | - | ±1 | - | ±1 | µA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 2.0 | - | 20 | - | 40 | µA |
| ΔI _{CC} | additional supply current | per input pin; V _I = V _{CC} - 2.1 V; I _O = 0 A; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V | - | 100 | 360 | - | 450 | - | 490 | µA |
| C _I | input capacitance | | - | 3.5 | - | - | - | - | - | pF |

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; C_L = 50 pF; for test circuit see Fig. 5.

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|-----------------|-------------------------------|--|-------|-----|-----|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74HC86 | | | | | | | | | | |
| t _{pd} | propagation delay | nA, nB to nY; see Fig. 4 [1] | | | | | | | | |
| | | V _{CC} = 2.0 V | - | 39 | 120 | - | 150 | - | 180 | ns |
| | | V _{CC} = 4.5 V | - | 14 | 24 | - | 30 | - | 36 | ns |
| | | V _{CC} = 5.0 V; C _L = 15 pF | - | 11 | - | - | - | - | - | ns |
| | | V _{CC} = 6.0 V | - | 11 | 20 | - | 26 | - | 31 | ns |
| t _t | transition time | nY; see Fig. 4 [2] | | | | | | | | |
| | | V _{CC} = 2.0 V | - | 19 | 75 | - | 95 | - | 110 | ns |
| | | V _{CC} = 4.5 V | - | 7 | 15 | - | 19 | - | 22 | ns |
| | | V _{CC} = 6.0 V | - | 6 | 13 | - | 16 | - | 19 | ns |
| C _{PD} | power dissipation capacitance | per package; V _I = GND to V _{CC} [3] | - | 30 | - | - | - | - | - | pF |

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|----------------|-------------------------------|---|-------|-----|-----|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74HCT86 | | | | | | | | | | |
| t_{pd} | propagation delay | nA, nB to nY; see Fig. 4 [1] | | | | | | | | |
| | | $V_{CC} = 4.5\text{ V}$ | - | 17 | 32 | - | 40 | - | 48 | ns |
| | | $V_{CC} = 5.0\text{ V}; C_L = 15\text{ pF}$ | - | 14 | - | - | - | - | - | ns |
| t_t | transition time | nY; $V_{CC} = 4.5\text{ V}$; see Fig. 4 [2] | - | 7 | 15 | - | 19 | - | 22 | ns |
| C_{PD} | power dissipation capacitance | per package; $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$ [3] | - | 30 | - | - | - | - | - | pF |

[1] t_{pd} is the same as t_{PHL} and t_{PLH} .

[2] t_t is the same as t_{THL} and t_{TLH} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit

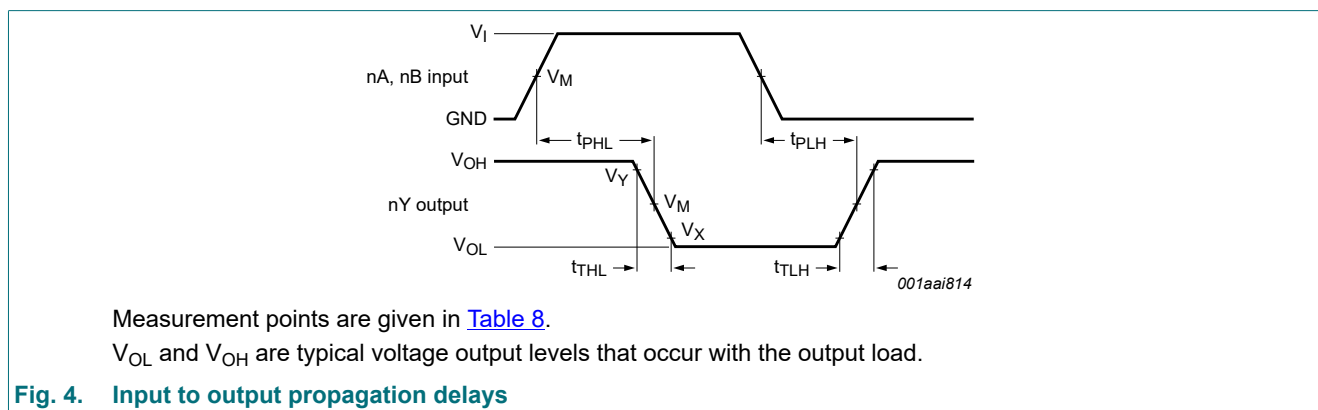
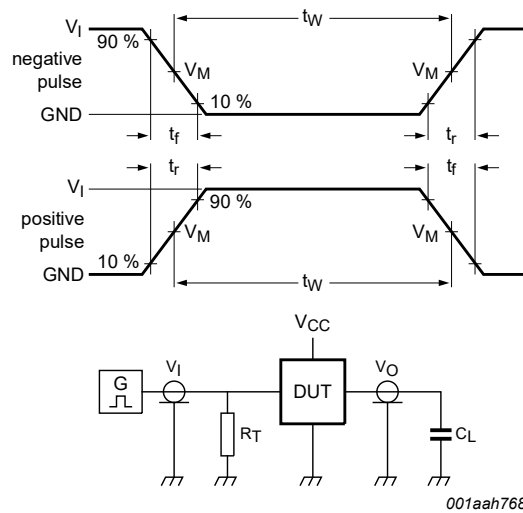


Table 8. Measurement points

| Type | Input | Output | | |
|---------|-------------|-------------|-------------|-------------|
| | V_M | V_M | V_X | V_Y |
| 74HC86 | $0.5V_{CC}$ | $0.5V_{CC}$ | $0.1V_{CC}$ | $0.9V_{CC}$ |
| 74HCT86 | 1.3 V | 1.3 V | $0.1V_{CC}$ | $0.9V_{CC}$ |



Test data is given in [Table 9](#).

Definitions test circuit:

R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = load capacitance including jig and probe capacitance.

Fig. 5. Test circuit for measuring switching times

Table 9. Test data

| Type | Input | | Load | Test |
|---------|----------|------------|--------------|--------------------|
| | V_I | t_r, t_f | C_L | |
| 74HC86 | V_{CC} | 6.0 ns | 15 pF, 50 pF | t_{PLH}, t_{PHL} |
| 74HCT86 | 3.0 V | 6.0 ns | 15 pF, 50 pF | t_{PLH}, t_{PHL} |

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

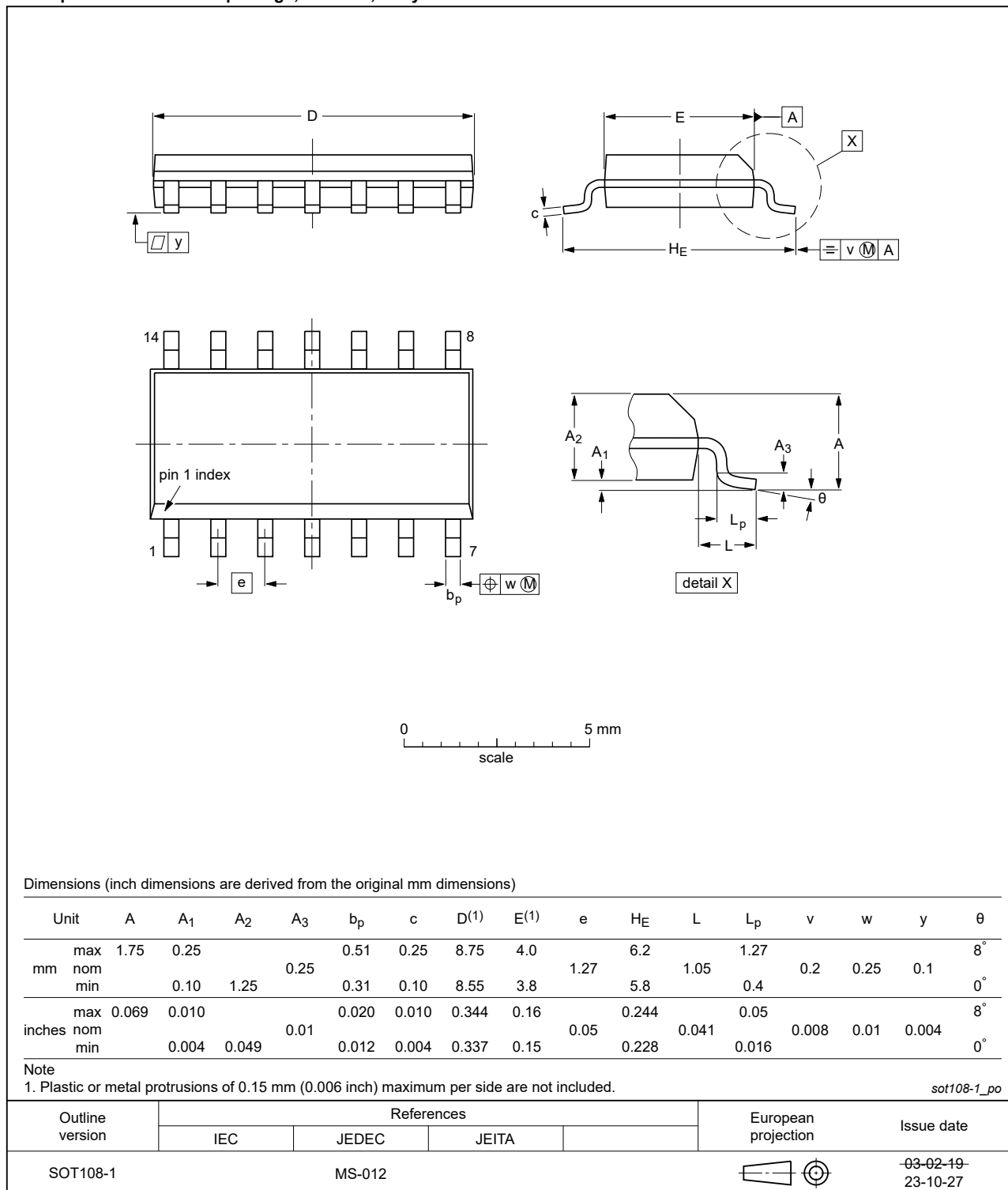


Fig. 6. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

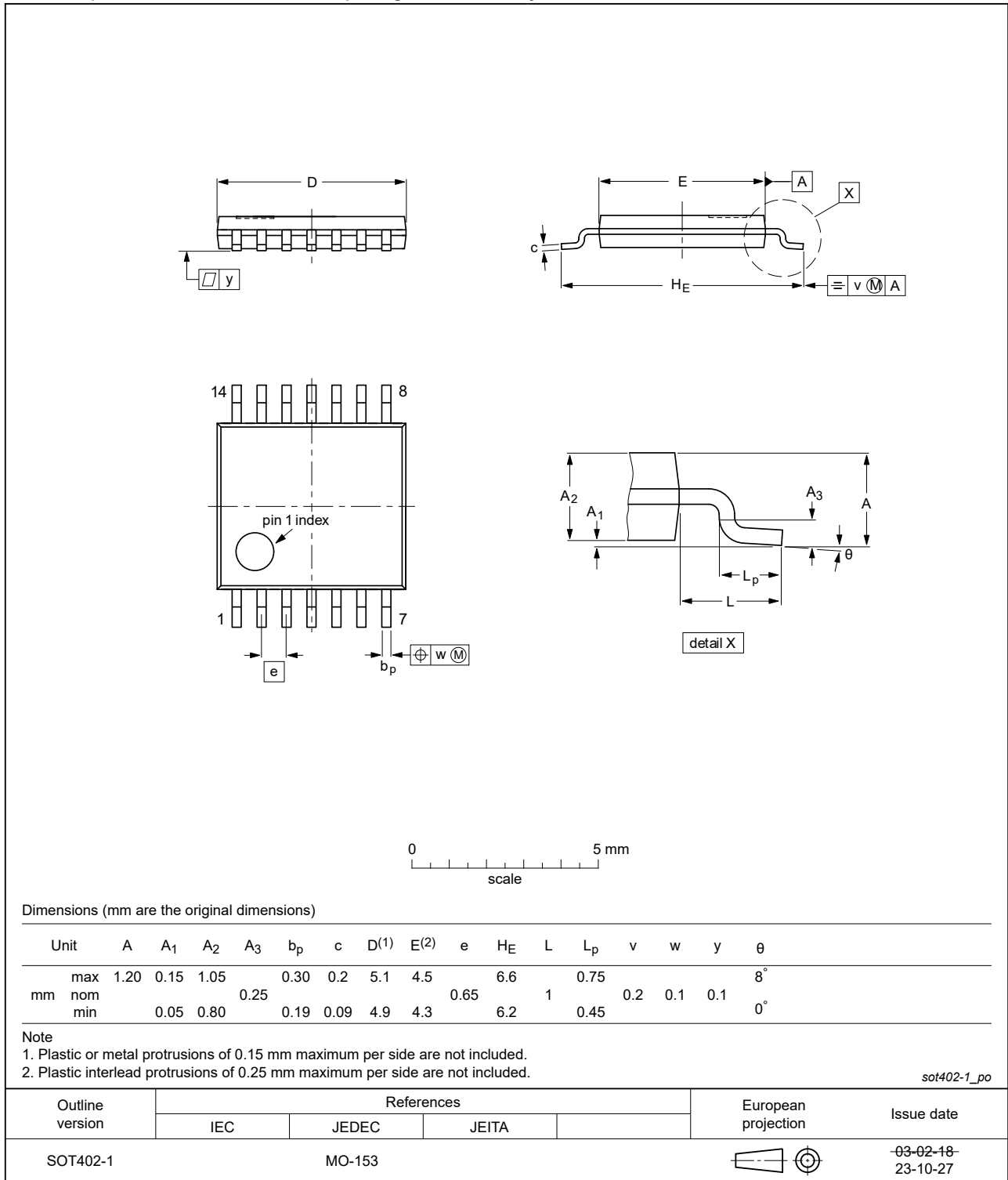


Fig. 7. Package outline SOT402-1 (TSSOP14)

12. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|---|
| CDM | Charged Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| TTL | Transistor-Transistor Logic |

13. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|--------------------|--|-----------------------|---------------|--------------------|
| 74HC_HCT86 v.7 | 20240402 | Product data sheet | - | 74HC_HCT86 v.6 |
| Modifications: | <ul style="list-style-type: none"> • Fig. 6, Fig. 7: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153. • Section 2: ESD specification updated according to the latest JEDEC standard. | | | |
| 74HC_HCT86 v.6 | 20210913 | Product data sheet | - | 74HC_HCT86 v.5 |
| Modifications: | <ul style="list-style-type: none"> • Type number 74HC86DB (SOT337-1/SSOP14) removed. | | | |
| 74HC_HCT86 v.5 | 20210310 | Product data sheet | - | 74HC_HCT86 v.4 |
| Modifications: | <ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 2 updated. • Section 7: Derating values for P_{tot} total power dissipation have changed. • Type number 74HCT86DB (SOT337-1/SSOP14) removed. | | | |
| 74HC_HCT86 v.4 | 20151204 | Product data sheet | - | 74HC_HCT86 v.3 |
| Modifications: | <ul style="list-style-type: none"> • Type numbers 74HC86N and 74HCT86N (SOT27-1) removed. | | | |
| 74HC_HCT86 v.3 | 20120827 | Product data sheet | - | 74HC_HCT86_CNV v.2 |
| Modifications: | <ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. | | | |
| 74HC_HCT86_CNV v.2 | 19970918 | Product specification | - | - |

14. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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