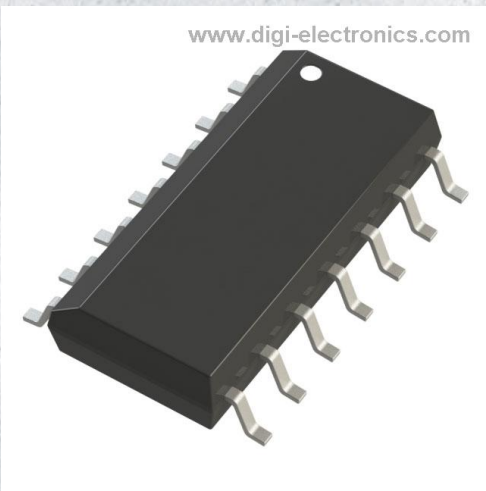
74HCT107D-Q100J Datasheet



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DiGi Electronics Part Number	74HCT107D-Q100J-DG
Manufacturer	Nexperia USA Inc.
Manufacturer Product Number	74HCT107D-Q100J
Description	IC FF JK TYPE DUAL 1BIT 14SO
Detailed Description	Flip Flop 2 Element JK Type 1 Bit Negative Edge 14-SOIC (0.154", 3.90mm Width)

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
74HCT107D-Q100J	Nexperia USA Inc.
Series:	Product Status:
74HCT	Active
Function:	Type:
Reset	JK Type
Output Type:	Number of Elements:
Complementary	2
Number of Bits per Element:	Clock Frequency:
1	66 MHz
Max Propagation Delay @ V, Max CL:	Trigger Type:
17ns @ 5V, 15pF	Negative Edge
Current - Output High, Low:	Voltage - Supply:
4mA, 4mA	4.5V ~ 5.5V
Current - Quiescent (Iq):	Input Capacitance:
4 µA	3.5 pF
Operating Temperature:	Grade:
-40°C ~ 125°C (TA)	Automotive
Qualification:	Mounting Type:
AEC-Q100	Surface Mount
Supplier Device Package:	Package / Case:
14-SO	14-SOIC (0.154", 3.90mm Width)
Base Product Number:	
74HCT107	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8542.39.0001	

74HC107-Q100; 74HCT107-Q100

Dual JK flip-flop with reset; negative-edge trigger

Rev. 4 — 20 February 2024 Product data sheet

1. General description

The 74HC107-Q100; 74HCT107-Q100 is a dual negative edge triggered JK flip-flop featuring individual J and K inputs, clock ($\overline{CP}$) and reset ($\overline{R}$) inputs and complementary Q and $\overline{Q}$ outputs. The reset is an asynchronous active LOW input and operates independently of the clock input. The J and K inputs control the state changes of the flip-flops as described in the mode select function table. The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- Input levels:
  - For 74HC107-Q100: CMOS level
  - For 74HCT107-Q100: TTL level
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC107D-Q100 74HCT107D-Q100	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HC107PW-Q100	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

4. Functional diagram

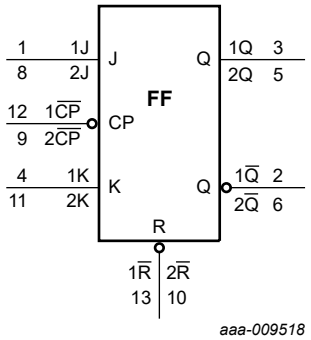


Fig. 1. Logic symbol

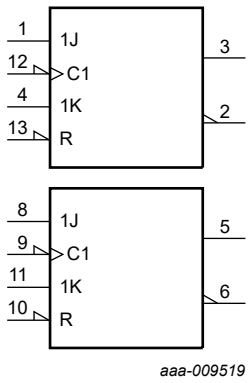


Fig. 2. IEC logic symbol

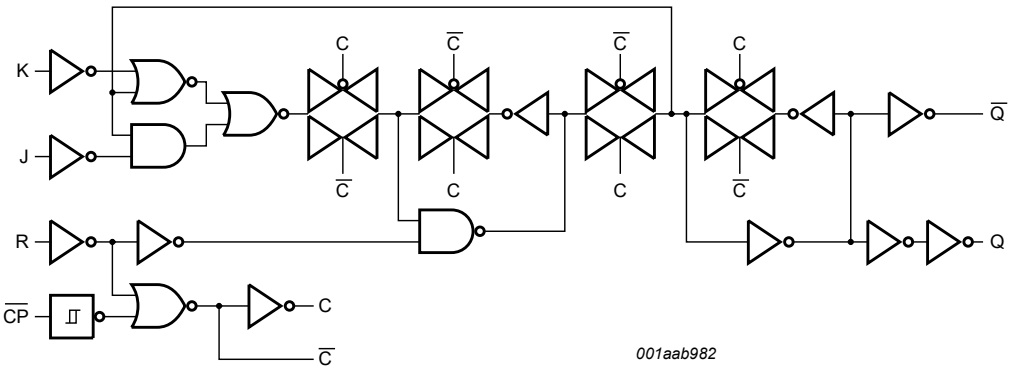
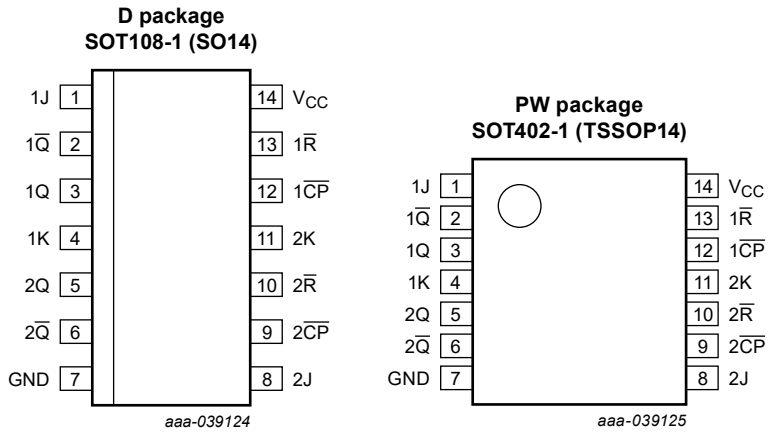


Fig. 3. Logic diagram (one flip-flop)

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1J, 2J	1, 8	synchronous J input
$1\overline{Q}$, $2\overline{Q}$	2, 6	complement output
1Q, 2Q	3, 5	true output
1K, 2K	4, 11	synchronous K input
$1\overline{CP}$, $2\overline{CP}$	12, 9	clock input (HIGH-to-LOW edge-triggered)
$1\overline{R}$, $2\overline{R}$	13, 10	asynchronous reset input (active LOW)
GND	7	ground (0 V)
V_{CC}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the HIGH-to-LOW clock transition;
L = LOW voltage level; l = LOW voltage level one set-up time prior to the HIGH-to-LOW clock transition;
q = state of referenced output one set-up time prior to the HIGH-to-LOW clock transition; X = don't care;
↓ = HIGH-to-LOW clock transition.

Input				Output		Operating mode
$\overline{R}$	$\overline{CP}$	J	K	Q	$\overline{Q}$	
L	X	X	X	L	H	asynchronous reset
H	↓	h	h	$\overline{q}$	q	toggle
H	↓	l	h	L	H	load 0 (reset)
H	↓	h	l	H	L	load 1 (set)
H	↓	l	l	q	$\overline{q}$	hold (no change)

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_O	output current	$V_O = -0.5$ V to $V_{CC} + 0.5$ V		-	±25	mA
I_{CC}	supply current			-	50	mA
I_{GND}	ground current			-50	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.
For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC107-Q100			74HCT107-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC107-Q100										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = -20 µA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = -20 µA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -20 µA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = -4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = -5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 20 µA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	4.0	-	40	-	80	µA
C_I	input capacitance		-	3.5	-					pF
74HCT107-Q100										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -4 mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = 20 µA	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	4.0	-	40	-	80	µA

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC}$ - 2.1 V; I_O = 0 A; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V								
		pin $n\overline{CP}$, nJ	-	100	360	-	450	-	490	µA
		pin $n\overline{R}$	-	65	234	-	293	-	319	µA
		pin nK	-	60	216	-	270	-	294	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Fig. 6

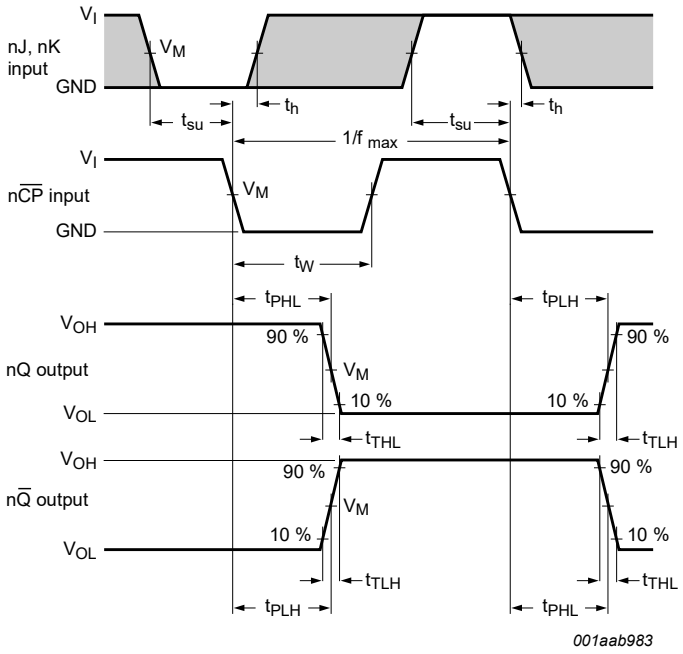
Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC107-Q100										
t_{pd}	propagation delay	$n\overline{CP}$ to nQ; see Fig. 4 [1]								
		V_{CC} = 2.0 V	-	52	160	-	200	-	240	ns
		V_{CC} = 4.5 V	-	19	32	-	40	-	48	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	16	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	15	27	-	34	-	41	ns
		$n\overline{CP}$ to $n\overline{Q}$; see Fig. 4								
		V_{CC} = 2.0 V	-	52	160	-	200	-	240	ns
		V_{CC} = 4.5 V	-	19	32	-	40	-	48	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	16	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	15	27	-	34	-	41	ns
		$n\overline{R}$ to nQ, $n\overline{Q}$; see Fig. 5								
		V_{CC} = 2.0 V	-	52	155	-	195	-	235	ns
		V_{CC} = 4.5 V	-	19	31	-	39	-	47	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	16	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	15	26	-	33	-	40	ns
t_t	transition time	nQ, $n\overline{Q}$; see Fig. 4 [2]								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_W	pulse width	$n\overline{CP}$ input, HIGH or LOW; see Fig. 4								
		V_{CC} = 2.0 V	80	22	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	8	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	6	-	17	-	20	-	ns
		$n\overline{R}$ input, HIGH or LOW; see Fig. 5								
		V_{CC} = 2.0 V	80	22	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	8	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	6	-	17	-	20	-	ns
t_{rec}	recovery time	$n\overline{R}$ to $n\overline{CP}$; see Fig. 5								
		V_{CC} = 2.0 V	60	19	-	75	-	90	-	ns
		V_{CC} = 4.5 V	12	7	-	15	-	18	-	ns
		V_{CC} = 6.0 V	20	6	-	13	-	15	-	ns
t_{su}	set-up time	nJ, nK to $n\overline{CP}$; see Fig. 4								
		V_{CC} = 2.0 V	100	22	-	125	-	150	-	ns
		V_{CC} = 4.5 V	20	8	-	25	-	30	-	ns
		V_{CC} = 6.0 V	17	6	-	21	-	26	-	ns
t_h	hold time	nJ, nK to $n\overline{CP}$; see Fig. 4								
		V_{CC} = 2.0 V	3	-6	-	3	-	3	-	ns
		V_{CC} = 4.5 V	3	-2	-	3	-	3	-	ns
		V_{CC} = 6.0 V	3	-2	-	3	-	3	-	ns
f_{max}	maximum frequency	$n\overline{CP}$ input; see Fig. 4								
		V_{CC} = 2.0 V	6	23	-	4.8	-	4.0	-	MHz
		V_{CC} = 4.5 V	30	70	-	24	-	20	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF	-	78	-	-	-	-	-	MHz
		V_{CC} = 6.0 V	35	85	-	28	-	24	-	MHz
C_{PD}	power dissipation capacitance	per flip-flop; V_I = GND to V_{CC} [3]	-	30	-	-	-	-	-	pF
74HCT107-Q100										
t_{pd}	propagation delay	$n\overline{CP}$ to nQ; see Fig. 4 [1]								
		V_{CC} = 4.5 V	-	19	36	-	45	-	54	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	16	-	-	-	-	-	ns
		$n\overline{CP}$ to $n\overline{Q}$; see Fig. 4								
		V_{CC} = 4.5 V	-	21	36	-	45	-	54	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	18	-	-	-	-	-	ns
		$n\overline{R}$ to nQ, $n\overline{Q}$; see Fig. 5								
		V_{CC} = 4.5 V	-	20	38	-	48	-	57	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	17	-	-	-	-	-	ns
t_t	transition time	nQ, $n\overline{Q}$; see Fig. 4 [2]								
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_W	pulse width	$n\overline{CP}$ input, HIGH or LOW; see Fig. 4								
		V_{CC} = 4.5 V	16	9	-	20	-	24	-	ns
		$n\overline{R}$ input, HIGH or LOW; see Fig. 5								
		V_{CC} = 4.5 V	20	11	-	25	-	30	-	ns
t_{rec}	recovery time	$n\overline{R}$ to $n\overline{CP}$; see Fig. 5								
		V_{CC} = 4.5 V	14	8	-	18	-	21	-	ns
t_{su}	set-up time	nJ, nK to $n\overline{CP}$; see Fig. 4								
		V_{CC} = 4.5 V	20	7	-	25	-	30	-	ns
t_h	hold time	nJ, nK to $n\overline{CP}$; see Fig. 4								
		V_{CC} = 4.5 V	5	-2	-	5	-	5	-	ns
f_{max}	maximum frequency	$n\overline{CP}$ input; see Fig. 4								
		V_{CC} = 4.5 V	30	66	-	24	-	20	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF	-	73	-	-	-	-	-	MHz
C_{PD}	power dissipation capacitance	per flip-flop; [3] V_I = GND to V_{CC} - 1.5 V	-	30	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL}, t_{PLH}.
[2] t_t is the same as t_{THL}, t_{TLH}.
[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

10.1. Waveforms and test circuit

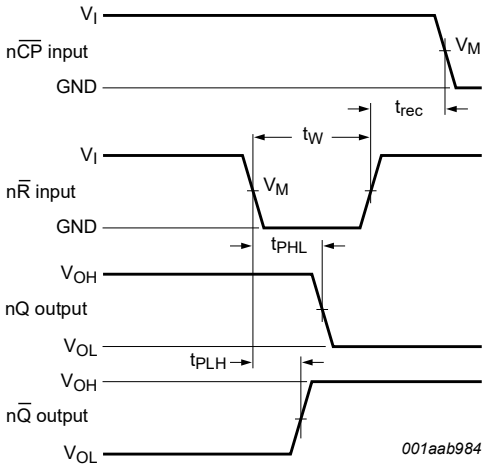


The shaded areas indicate when the input is permitted to change for predictable output performance.

Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 4. Clock propagation delays, pulse width, set-up and hold times, output transition times and the maximum frequency



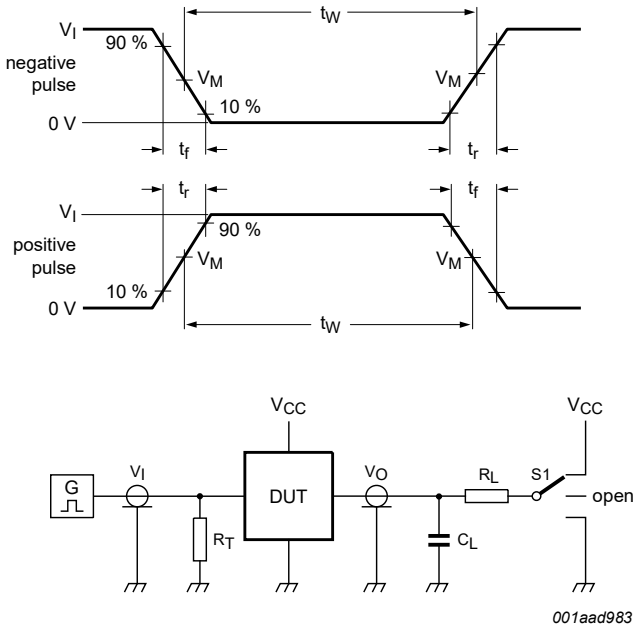
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 5. Reset propagation delays, pulse width and recovery time

Table 8. Measurement points

Type	Input		Output
	V_I	V_M	V_M
74HC107-Q100	V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$
74HCT107-Q100	3 V	1.3 V	1.3 V



Test data is given in Table 9.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

C_L = Load capacitance including jig and probe capacitance;

R_L = Load resistance;

S1 = Test selection switch.

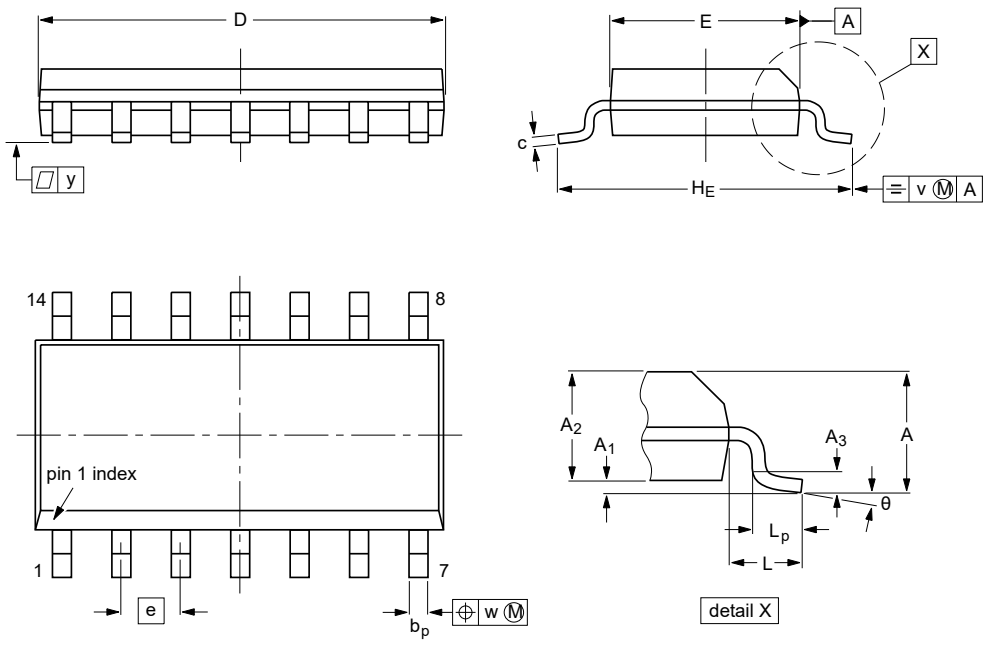
Fig. 6. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC107-Q100	V_{CC}	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}
74HCT107-Q100	3 V	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	8.75	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	8.55	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.344	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.337	0.15		0.228		0.016				0°

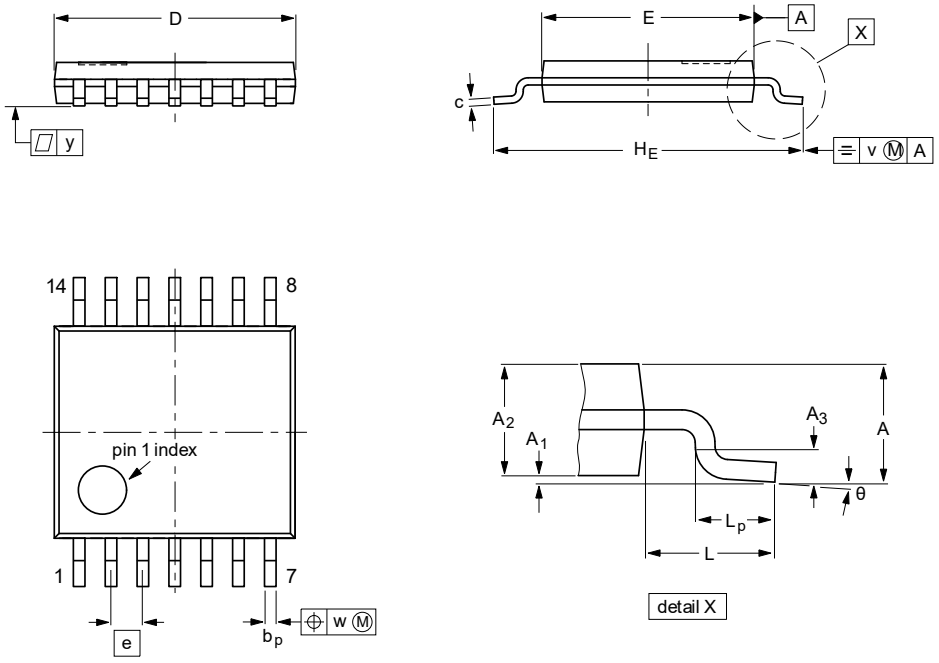
Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

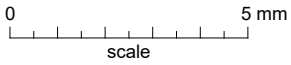
sot108-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT108-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 7. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**





Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
	nom				0.25					0.65		1		0.2	0.1	0.1	
	min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot402-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 8. Package outline SOT402-1 (TSSOP14)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT107_Q100 v.4	20240220	Product data sheet	-	74HC_HCT107_Q100 v.3
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard. • Fig. 7, Fig. 8: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153			
74HC_HCT107_Q100 v.3	20210707	Product data sheet	-	74HC_HCT107_Q100 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 2 updated. • Section 7: Derating values for P_{tot} total power dissipation have changed.			
74HC_HCT107_Q100 v.2	20150126	Product data sheet	-	74HC_HCT107_Q100 v.1
Modifications:	• Table 7: Power dissipation capacitance condition for 74HCT107-Q100 is corrected.			
74HC_HCT107_Q100 v.1	20131118	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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