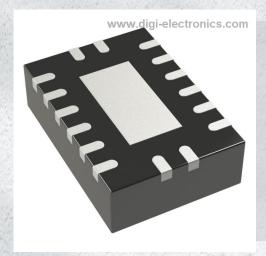


# 74HCT157BQ-Q100,11 Datasheet



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DiGi Electronics Part Number 74HCT157BQ-Q100,11-DG

Manufacturer Nexperia USA Inc.

Manufacturer Product Number 74HCT157BQ-Q100,11

Description IC MULTIPLEXER 4 X 2:1 16DHVQFN

Detailed Description Multiplexer 4 x 2:1 16-DHVQFN (2.5x3.5)



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# **Purchase and inquiry**

Manufacturer Product Number:	Manufacturer:						
74HCT157BQ-Q100,11	Nexperia USA Inc.						
Series:	Product Status:						
74HCT	Active						
Type:	Circuit:						
Multiplexer	4 x 2:1						
Independent Circuits:	Current - Output High, Low:						
1	4mA, 4mA						
Voltage Supply Source:	Voltage - Supply:						
Single Supply	4.5V ~ 5.5V						
Operating Temperature:	Grade:						
-40°C ~ 125°C	Automotive						
Qualification:	Mounting Type:						
AEC-Q100	Surface Mount						
Package / Case:	Supplier Device Package:						
16-VFQFN Exposed Pad	16-DHVQFN (2.5x3.5)						
Base Product Number:							
74HCT157							

# **Environmental & Export classification**

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8542.39.0001	



# Quad 2-input multiplexer Rev. 4 — 28 May 2024

Product data sheet

## 1. General description

The 74HC157-Q100; 74HCT157-Q100 is a quad 2-input multiplexer. The device features select (S) and enable E inputs. A HIGH on S selects data source 1, a LOW data source 0. A HIGH on E forces all the outputs (1Y to 4Y) LOW. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V<sub>CC</sub>.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

#### 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 2.0 V to 6.0 V
- · CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- Input levels:
  - For 74HC157-Q100: CMOS level
  - For 74HCT157-Q100: TTL level
- Non-inverting data path
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

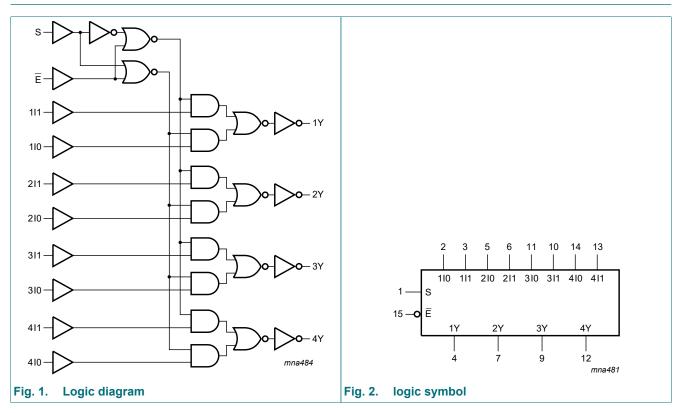
# 3. Ordering information

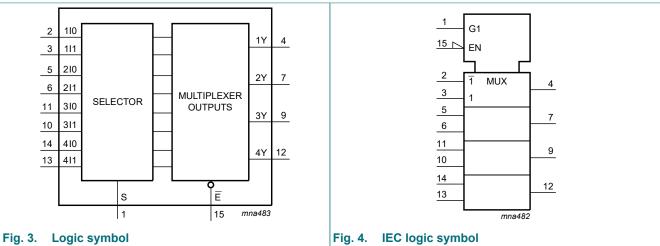
**Table 1. Ordering information** 

Type number	Package										
	Temperature range	Name	Description	Version							
74HC157D-Q100 74HCT157D-Q100	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1							
74HC157PW-Q100 74HCT157PW-Q100	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1							
74HC157BQ-Q100 74HCT157BQ-Q100	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1							



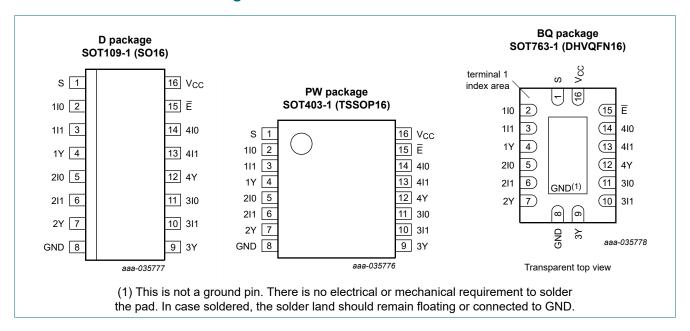
# 4. Functional diagram





## 5. Pinning information

#### 5.1. Pinning



### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
S	1	common data select input
1I0 to 4I0	2, 5, 11, 14	data inputs from source 0
1I1 to 4I1	3, 6, 10, 13	data inputs from source 1
1Y to 4Y	4, 7, 9, 12	multiplexer outputs
GND	8	ground (0 V)
Ē	15	enable input (active LOW)
V <sub>CC</sub>	16	supply voltage

# 6. Functional description

#### **Table 3. Function table**

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input	Output			
E	S	nI0	nl1	nY
Н	X	Х	Х	L
L	L	L	X	L
L	L	Н	Х	Н
L	Н	X	L	L
L	Н	X	Н	Н

# 7. Limiting values

#### **Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>CC</sub>	supply voltage			-0.5	+7	V
I <sub>IK</sub>	input clamping current	$V_{I} < -0.5 \text{ V or } V_{I} > V_{CC} + 0.5 \text{ V}$		-	±20	mA
I <sub>OK</sub>	output clamping current	$V_{O} < -0.5 \text{ V or } V_{O} > V_{CC} + 0.5 \text{ V}$		-	±20	mA
Io	output current	$V_{O} = -0.5 \text{ V to } V_{CC} + 0.5 \text{ V}$		-	±25	mA
I <sub>CC</sub>	supply current			-	+50	mA
I <sub>GND</sub>	ground current			-50	-	mA
T <sub>stg</sub>	storage temperature			-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C	[1]	-	500	mW

<sup>[1]</sup> For SOT109-1 (SO16) package: P<sub>tot</sub> derates linearly with 12.4 mW/K above 110 °C. For SOT403-1 (TSSOP16) package: P<sub>tot</sub> derates linearly with 8.5 mW/K above 91 °C. For SOT763-1 (DHVQFN16) package: P<sub>tot</sub> derates linearly with 11.2 mW/K above 106 °C.

# 8. Recommended operating conditions

#### Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC157-Q100		74HCT157-Q100			Unit	
			Min	Тур	Max	Min	Тур	Max	
V <sub>CC</sub>	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
VI	input voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
Vo	output voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 2.0 V	-	-	625	-	-	-	ns/V
		V <sub>CC</sub> = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V <sub>CC</sub> = 6.0 V	-	-	83	-	-	-	ns/V

# 9. Static characteristics

#### **Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Tar	<sub>nb</sub> = 25	°C		-40 °C 35 °C	T <sub>amb</sub> = -40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HC15	7-Q100									
V <sub>IH</sub>	HIGH-level	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
	input voltage	V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V <sub>IL</sub>	LOW-level	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
	input voltage	V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V <sub>OH</sub>	HIGH-level	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
	output voltage	I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		$I_{O}$ = -20 $\mu$ A; $V_{CC}$ = 6.0 $V$	5.9	6.0	-	5.9	-	5.9	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I <sub>O</sub> = -5.2 mA; V <sub>CC</sub> = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V <sub>OL</sub>	LOW-level	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
	output voltage	I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
l <sub>l</sub>	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±0.1	-	±1.0	-	±1.0	μΑ
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0 \text{ V}$	-	-	8.0	-	80	-	160	μΑ
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF

## Quad 2-input multiplexer

Symbol	Parameter	Conditions	T <sub>amb</sub> = 25 °C		°C		-40 °C 35 °C	T <sub>amb</sub> = -40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HCT1	57-Q100									
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 V$								
	output voltage	I <sub>O</sub> = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -4 mA	3.98	4.32	-	3.84	-	3.7	-	V
V <sub>OL</sub>	LOW-level	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 V$								
	output voltage	I <sub>O</sub> = 20 μA	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±0.1	-	±1.0	-	±1.0	μA
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	8.0	-	80	-	160	μA
Δl <sub>CC</sub>	additional supply current	$V_I = V_{CC} - 2.1 \text{ V}; I_O = 0 \text{ A};$ other inputs at $V_{CC}$ or GND; $V_{CC} = 4.5 \text{ V}$ to 5.5 V								
		per input pin; nI0, nI1 inputs	-	100	360	-	450	-	490	μA
		per input pin; E input	-	60	216	-	270	-	294	μA
		per input pin; S input	-	100	360	-	450	-	490	μΑ
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF

**Quad 2-input multiplexer** 

# 10. Dynamic characteristics

#### **Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V);  $C_L$  = 50 pF unless otherwise specified; for test circuit see Fig. 7.

Symbol	Parameter	Conditions		T <sub>amb</sub> = 25 °C			= -40 °C 85 °C	T <sub>amb</sub> = -40 °C to +125 °C		Unit	
				Min	Тур	Max	Min	Max	Min	Max	
74HC15	7-Q100		'								
t <sub>pd</sub>	propagation	nl0, nl1 to nY; see Fig. 5	[1]								
	delay	V <sub>CC</sub> = 2.0 V		-	36	125	-	155	-	190	ns
		V <sub>CC</sub> = 4.5 V		-	13	25	-	31	-	38	ns
		V <sub>CC</sub> = 5 V; C <sub>L</sub> = 15 pF		-	11	-	-	-	-	-	ns
		V <sub>CC</sub> = 6.0 V		-	10	21	-	26	-	32	ns
		S to nY; see Fig. 5	[1]								
		V <sub>CC</sub> = 2.0 V		-	41	125	-	155	-	190	ns
		V <sub>CC</sub> = 4.5 V		-	15	25	-	31	-	38	ns
		V <sub>CC</sub> = 5 V; C <sub>L</sub> = 15 pF		-	12	-	-	-	-	-	ns
		V <sub>CC</sub> = 6.0 V		-	12	21	-	26	-	32	ns
		E to nY; see Fig. 6	[1]								
		V <sub>CC</sub> = 2.0 V		-	39	115	-	145	-	175	ns
		V <sub>CC</sub> = 4.5 V		-	14	23	-	29	-	35	ns
		V <sub>CC</sub> = 5 V; C <sub>L</sub> = 15 pF		-	11	-	-	-	-	-	ns
		V <sub>CC</sub> = 6.0 V		-	11	20	-	25	-	30	ns
t <sub>t</sub>	transition	nY; see Fig. 5	[2]								
	time	V <sub>CC</sub> = 2.0 V		-	19	75	-	95	-	110	ns
		V <sub>CC</sub> = 4.5 V		-	7	15	-	19	-	22	ns
		V <sub>CC</sub> = 6.0 V		-	6	13	-	16	-	19	ns
C <sub>PD</sub>	power dissipation capacitance	$C_L$ = 50 pF; f = 1 MHz; $V_I$ = GND to $V_{CC}$	[3]	-	70	-	-	-	-	-	pF

## **Quad 2-input multiplexer**

Symbol	Parameter	Conditions		T <sub>ar</sub>	<sub>nb</sub> = 25	°C		= -40 °C ·85 °C		= -40 °C 125 °C	Unit
				Min	Тур	Max	Min	Max	Min	Max	
74HCT1	57-Q100				•						
t <sub>pd</sub>	propagation	nI0, nI1 to nY; see Fig. 5	[1]								
	delay	V <sub>CC</sub> = 4.5 V		-	16	27	-	34	-	41	ns
		V <sub>CC</sub> = 5 V; C <sub>L</sub> = 15 pF		-	13	-	-	-	-	-	ns
		S to nY; see Fig. 5	[1]								
		V <sub>CC</sub> = 4.5 V		-	22	37	-	46	-	56	ns
		V <sub>CC</sub> = 5 V; C <sub>L</sub> = 15 pF		-	19	-	-	-	-	-	ns
		E to nY; see Fig. 6	[1]								
		V <sub>CC</sub> = 4.5 V		-	15	26	-	33	-	39	ns
		V <sub>CC</sub> = 5 V; C <sub>L</sub> = 15 pF		-	12	-	-	-	-	-	ns
t <sub>t</sub>	transition	nY; see Fig. 5	[2]								
time	V <sub>CC</sub> = 4.5 V		-	7	15	-	19	-	22	ns	
C <sub>PD</sub>	power dissipation capacitance	$C_L$ = 50 pF; f = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> - 1.5 V	[3]	-	70	-	-	-	-	-	pF

- $t_{\text{pd}}$  is the same as  $t_{\text{PLH}}$  and  $t_{\text{PHL}}.$
- [2]
- $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$  where:

 $f_i$  = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

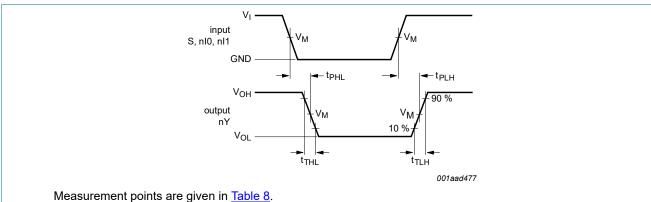
C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs.}$ 

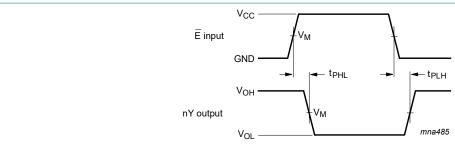
## 10.1. Waveforms and test circuit



 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

Propagation delay input (nI0, nI1, S) to output (nYn) Fig. 5.

## **Quad 2-input multiplexer**



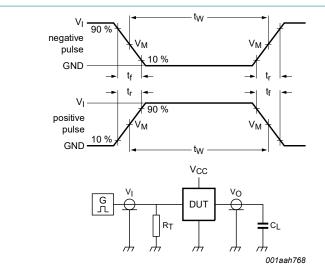
Measurement points are given in Table 8.

V<sub>OL</sub> and V<sub>OH</sub> are typical voltage output levels that occur with the output load.

#### Fig. 6. Propagation delay input (E) to output (nY)

**Table 8. Measurement points** 

Туре	Input	Output
	V <sub>M</sub>	V <sub>M</sub>
74HC157-Q100	0.5V <sub>CC</sub>	0.5V <sub>CC</sub>
74HCT157-Q100	1.3 V	1.3 V



Test data is given in Table 9.

Definitions test circuit:

 $R_T$  = Termination resistance should be equal to output impedance  $Z_0$  of the pulse generator;

C<sub>L</sub> = Load capacitance including jig and probe capacitance;

R<sub>L</sub> = Load resistance;

S1 = Test selection switch

#### Fig. 7. Test circuit for measuring switching times

#### Table 9. Test data

Туре	Input		Load	Test
	V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	C <sub>L</sub>	
74HC157-Q100	V <sub>CC</sub>	6.0 ns	15 pF, 50 pF	t <sub>PLH</sub> , t <sub>PHL</sub>
74HCT157-Q100	3.0 V	6.0 ns	15 pF, 50 pF	t <sub>PLH</sub> , t <sub>PHL</sub>

# 11. Package outline

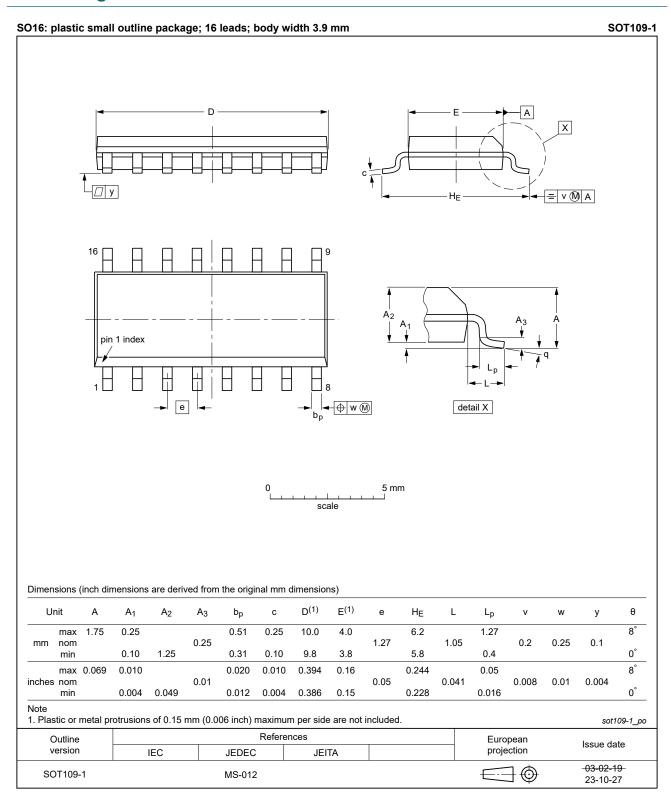


Fig. 8. Package outline SOT109-1 (SO16)

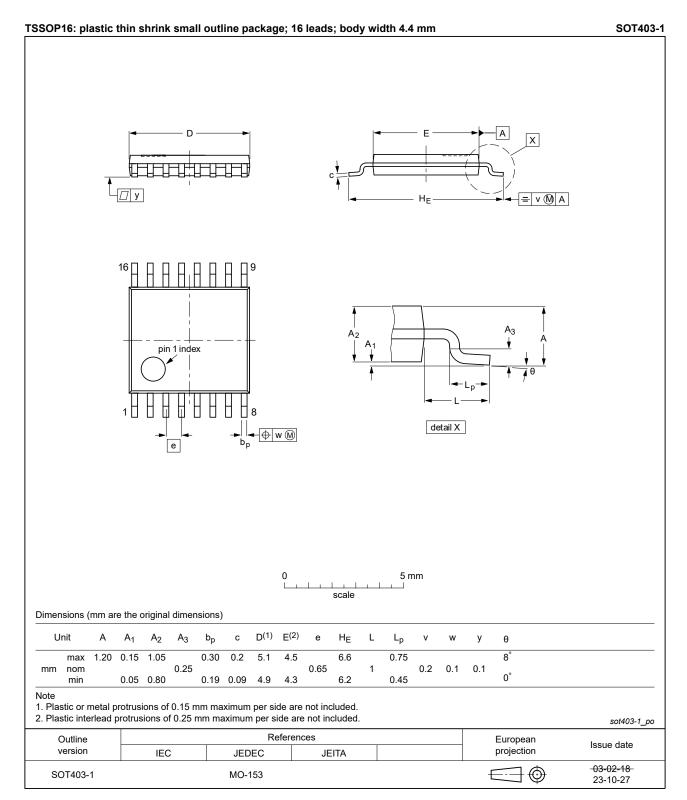


Fig. 9. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm SOT763-1

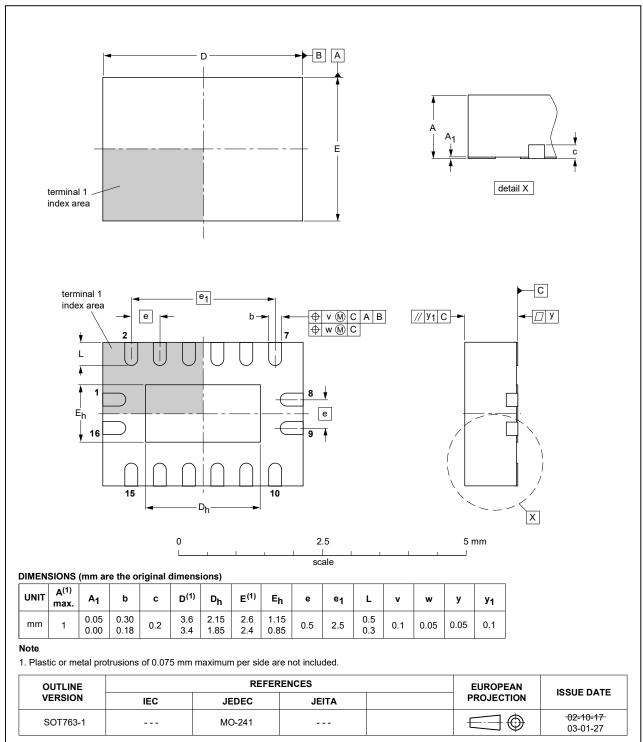


Fig. 10. Package outline SOT763-1 (DHVQFN16)

## 12. Abbreviations

#### **Table 10. Abbreviations**

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
НВМ	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

# 13. Revision history

#### Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT157_Q100 v.4	20240528	Product data sheet	-	74HC_HCT157_Q100 v.3
Modifications:	<ul> <li>Fig. 8, Fig. 9: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.</li> <li>Section 2: ESD specification updated according to the latest JEDEC standard.</li> </ul>			
74HC_HCT157_Q100 v.3	20200724	Product data sheet	-	74HC_HCT157_Q100 v.2
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Section 1 and Section 2 updated.</li> <li>Table 4: Derating values for Ptot total power dissipation have been updated.</li> </ul>			
74HC_HCT157_Q100 v.2	20150121	Product data sheet	-	74HC_HCT157_Q100 v.1
Modifications:	<u>Table 7</u> : Power dissipation capacitance condition for 74HCT157 is corrected.			
74HC_HCT157_Q100 v.1	20120802	Product data sheet	-	-

## 14. Legal information

#### **Data sheet status**

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <a href="https://www.nexperia.com">https://www.nexperia.com</a>.

#### **Definitions**

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## **Nexperia**

# 74HC157-Q100; 74HCT157-Q100

**Quad 2-input multiplexer** 

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