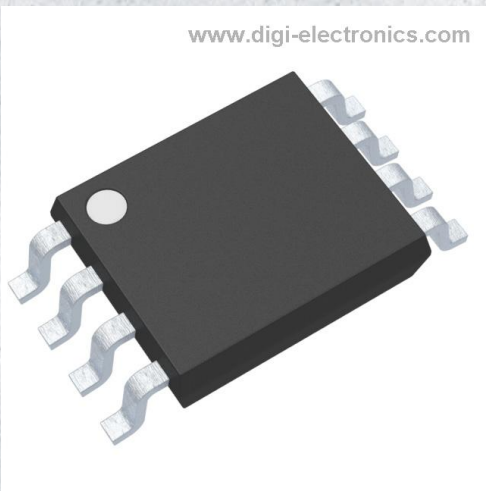
74HCT2G86DC,125 Datasheet



https://www.DiGi-Electronics.com

DiGi Electronics Part Number	74HCT2G86DC,125-DG
Manufacturer	Nexperia USA Inc.
Manufacturer Product Number	74HCT2G86DC,125
Description	IC GATE XOR 2CH 2-INP 8VSSOP
Detailed Description	XOR (Exclusive OR) IC 2 Channel 8-VSSOP

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
74HCT2G86DC,125	Nexperia USA Inc.
Series:	Product Status:
74HCT	Active
Logic Type:	Number of Circuits:
XOR (Exclusive OR)	2
Number of Inputs:	Features:
2	-
Voltage - Supply:	Current - Quiescent (Max):
4.5V ~ 5.5V	1 µA
Current - Output High, Low:	Input Logic Level - Low:
4mA, 4mA	0.8V
Input Logic Level - High:	Max Propagation Delay @ V, Max CL:
2V	19ns @ 4.5V, 50pF
Operating Temperature:	Mounting Type:
-40°C ~ 125°C	Surface Mount
Supplier Device Package:	Package / Case:
8-VSSOP	8-VFSOP (0.091", 2.30mm Width)
Base Product Number:	
74HCT2G86	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8542.39.0001	

74HC2G86; 74HCT2G86

Dual 2-input EXCLUSIVE-OR gate

Rev. 6 — 28 November 2023 Product data sheet

1. General description

The 74HC2G86; 74HCT2G86 is a dual 2-input EXCLUSIVE-OR gate. Inputs also include clamp diodes, this enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Input levels:
  - For 74HC2G86: CMOS level
  - For 74HCT2G86: TTL level
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC2G86DP	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74HC2G86DC 74HCT2G86DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1

4. Marking

Table 2. Marking code

Type number	Marking code[1]
74HC2G86DP	H86
74HC2G86DC	H86
74HCT2G86DC	T86

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

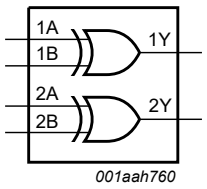


Fig. 1. Logic symbol

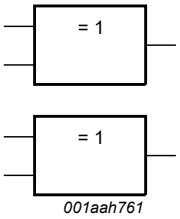


Fig. 2. IEC logic symbol

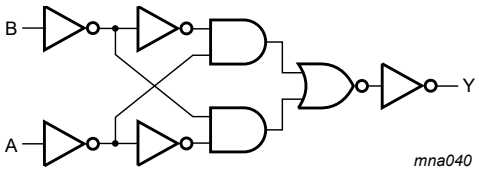
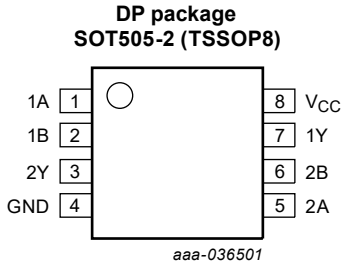
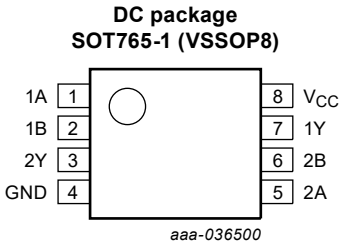


Fig. 3. Logic diagram (one gate)

6. Pinning information

6.1. Pinning





6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1A, 2A	1, 5	data input
1B, 2B	2, 6	data input
GND	4	ground (0 V)
1Y, 2Y	7, 3	data output
V_{CC}	8	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input		Output
nA	**nB**	**nY**
L	L	L
L	H	H
H	L	H
H	H	L

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_O	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5$ V)	[1]	-	25	mA
I_{CC}	supply current		[1]	-	50	mA
I_{GND}	ground current		[1]	-50	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_D	dynamic power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT505-2 (TSSOP8) package: P_{tot} derates linearly with 4.6 mW/K above 96 °C.
For SOT765-1 (VSSOP8) package: P_{tot} derates linearly with 4.9 mW/K above 99 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74HC2G86			74HCT2G86			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC2G86										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = -20 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = -20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -20 μA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = -4.0 mA; V_{CC} = 4.5 V	4.18	4.32	-	4.13	-	3.7	-	V
		I_O = -5.2 mA; V_{CC} = 6.0 V	5.68	5.81	-	5.63	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	1.0	-	10	-	20	μA
C_I	input capacitance		-	1.5	-	-	-	-	-	pF
74HCT2G86										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -4.0 mA	4.18	4.32	-	4.13	-	3.7	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = 20 μA	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	1.0	-	10	-	20	μA
ΔI_{CC}	additional supply current	per input; V_{CC} = 4.5 V to 5.5 V; V_I = V_{CC} - 2.1 V; I_O = 0 A	-	-	300	-	375	-	410	μA
C_I	input capacitance		-	1.5	-	-	-	-	-	pF

11. Dynamic characteristics

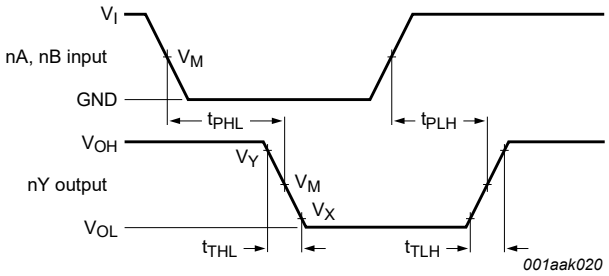
Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit, see Fig. 5.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC2G86										
t_{pd}	propagation delay	nA, nB to nY; see Fig. 4 [1]								
		V_{CC} = 2.0 V	-	34	120	-	150	-	180	ns
		V_{CC} = 4.5 V	-	11	20	-	25	-	36	ns
		V_{CC} = 6.0 V	-	9.0	17	-	21	-	30	ns
t_t	transition time	nY; see Fig. 4 [2]								
		V_{CC} = 2.0 V	-	18	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	6	15	-	19	-	22	ns
		V_{CC} = 6.0 V		5	13	-	16	-	20	ns
C_{PD}	power dissipation capacitance	per buffer; C_L = 50 pF; f_i = 1 MHz; V_I = GND to V_{CC} [3]	-	10	-	-	-	-	-	pF
74HCT2G86										
t_{pd}	propagation delay	nA, nB to nY; see Fig. 4 [1]								
		V_{CC} = 4.5 V	-	11	19	-	23	-	48	ns
t_t	transition time	nY; see Fig. 4 [2]								
		V_{CC} = 4.5 V	-	6	15	-	19	-	22	ns
C_{PD}	power dissipation capacitance	per buffer; C_L = 50 pF; f_i = 1 MHz; V_I = GND to V_{CC} [3]	-	9	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.
[2] t_t is the same as t_{TLH} and t_{THL}.
[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

11.1. Waveforms and test circuit



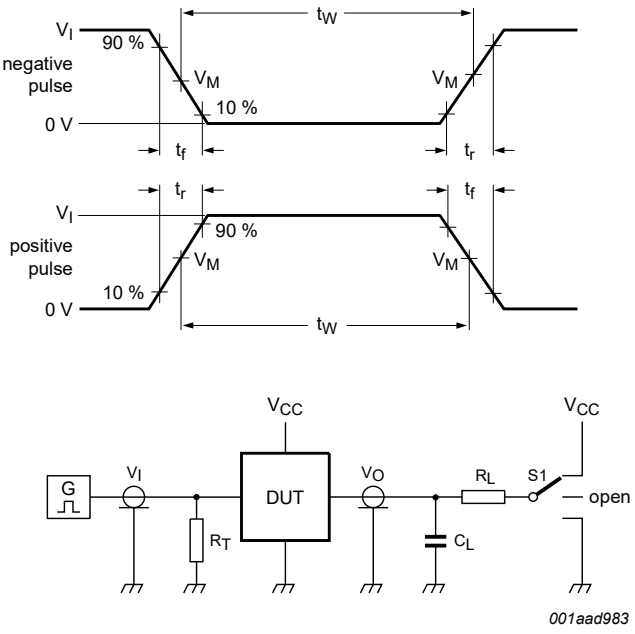
Measurement points are given in Table 9.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 4. Propagation delay data input (nA, nB) to data output (nY) and transition time output (nY)

Table 9. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74HC2G86	0.5 × V_{CC}	0.5 × V_{CC}	0.1 × V_{CC}	0.9 × V_{CC}
74HCT2G86	1.3 V	1.3 V	0.1 × V_{CC}	0.9 × V_{CC}



Test data is given in Table 10.

Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

C_L = Load capacitance including jig and probe capacitance; R_L = Load resistance and S1 = Test selection switch.

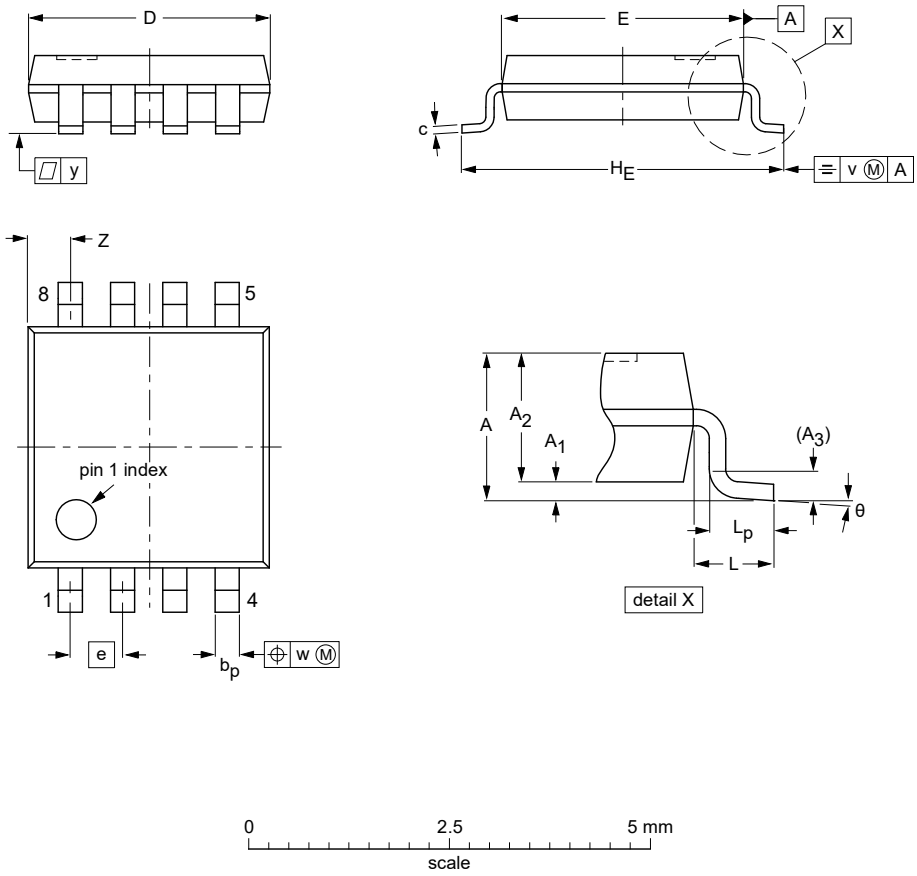
Fig. 5. Test circuit for measuring switching times

Table 10. Test data

Type	Input		Load		S1 position
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
74HC2G86	GND to V_{CC}	≤ 6 ns	50 pF	1 kΩ	open
74HCT2G86	GND to 3 V	≤ 6 ns	50 pF	1 kΩ	open

12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

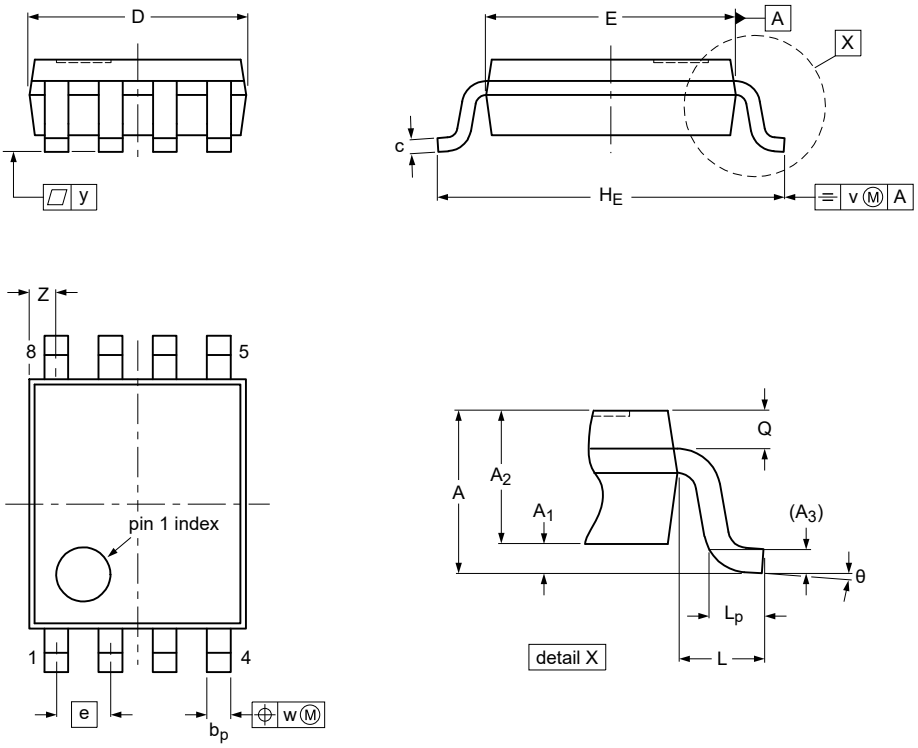
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		- - -				02-01-16

Fig. 6. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm **SOT765-1**



Dimensions (mm are the original dimensions)

Unit	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm max	1	0.15	0.85	0.12	0.27	0.23	2.1	2.4	0.5	3.2	0.4	0.40	0.21	0.2	0.08	0.1	0.4	8°
nom																		
min		0.00	0.60		0.17	0.08	1.9	2.2		3.0		0.15	0.19				0.1	0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

sot765-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				~~07-06-02~~ 16-05-31

Fig. 7. Package outline SOT765-1 (VSSOP8)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT2G86 v.6	20231128	Product data sheet	-	74HC_HCT2G86 v.5
Modifications:	• Section 2 updated. • Section 2: ESD specification updated according to the latest JEDEC standard. • Section 8: P_{tot} and derating values for P_{tot} total power dissipation updated. • Section 11: C_{PD} conditions for 74HCT2G86 aligned with 74HC2G86 (errata).			
74HC_HCT2G86 v.5	20181218	Product data sheet	-	74HC_HCT2G86 v.4
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type numbers 74HCT2G86DP, 74HC2G86GD and 74HCT2G86GD removed.			
74HC_HCT2G86 v.4	20140314	Product data sheet	-	74HC_HCT2G86 v.3
Modifications:	• For type numbers 74HC2G86GD and 74HCT2G86GD XSON8U has changed to XSON8.			
74HC_HCT2G86 v.3	20090507	Product data sheet	-	74HC_HCT2G86 v.2
74HC_HCT2G86 v.2	20030728	Product specification	-	74HC_HCT2G86 v.1
74HC_HCT2G86 v.1	20020717	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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