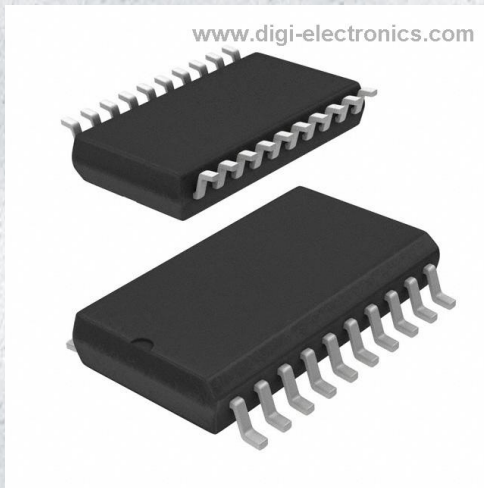


74LV245D,112 Datasheet



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DiGi Electronics Part Number	74LV245D,112-DG
Manufacturer	Nexperia USA Inc.
Manufacturer Product Number	74LV245D,112
Description	IC TXRX NON-INVERT 5.5V 20SO
Detailed Description	Transceiver, Non-Inverting 1 Element 8 Bit per Element 3-State Output 20-SO



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.

Purchase and inquiry

Manufacturer Product Number:

74LV245D,112

Series:

74LV

Logic Type:

Transceiver, Non-Inverting

Number of Bits per Element:

8

Output Type:

3-State

Voltage - Supply:

1V ~ 5.5V

Mounting Type:

Surface Mount

Supplier Device Package:

20-SO

Manufacturer:

Nexperia USA Inc.

Product Status:

Obsolete

Number of Elements:

1

Input Type:

-

Current - Output High, Low:

16mA, 16mA

Operating Temperature:

-40°C ~ 125°C (TA)

Package / Case:

20-SOIC (0.295", 7.50mm Width)

Base Product Number:

74LV245

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

74LV245

Octal bus transceiver; 3-state

Rev. 6 — 4 July 2024

Product data sheet

1. General description

The 74LV245 is an 8-bit transceiver with 3-state outputs. The device features an output enable (\overline{OE}) and send/receive (DIR) for direction control. A HIGH on \overline{OE} causes the outputs to assume a high-impedance OFF-state. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess V_{CC} .

2. Features and benefits

- Wide supply voltage range from 1.0 V to 5.5 V
- CMOS low power dissipation
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Optimized for low voltage applications: 1.0 V to 3.6 V
- Accepts TTL input levels between $V_{CC} = 2.7$ V and $V_{CC} = 3.6$ V
- Typical output ground bounce < 0.8 V at $V_{CC} = 3.3$ V and $T_{amb} = 25$ °C
- Typical HIGH-level output voltage (V_{OH}) undershoot: > 2 V at $V_{CC} = 3.3$ V and $T_{amb} = 25$ °C
- Complies with JEDEC standards:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8C (2.7 V to 3.6 V)
 - JESD36 (4.5 V to 5.5 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to $+85$ °C and from -40 °C to $+125$ °C

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LV245D	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LV245PW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

4. Functional diagram

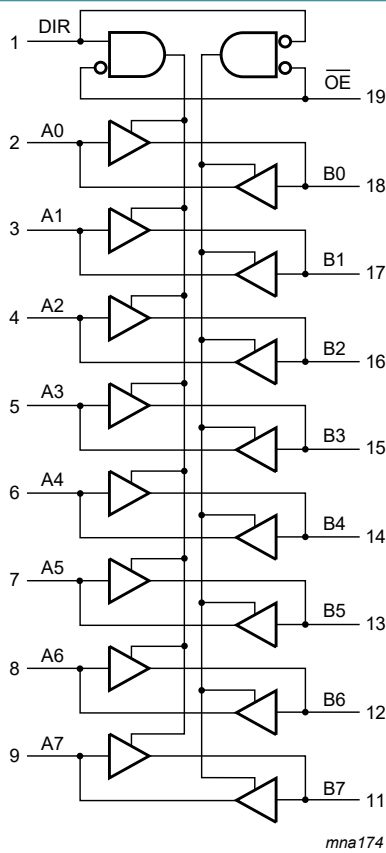


Fig. 1. Logic symbol

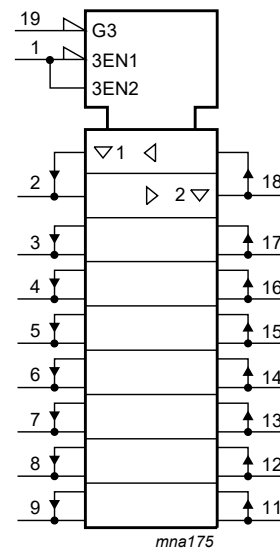
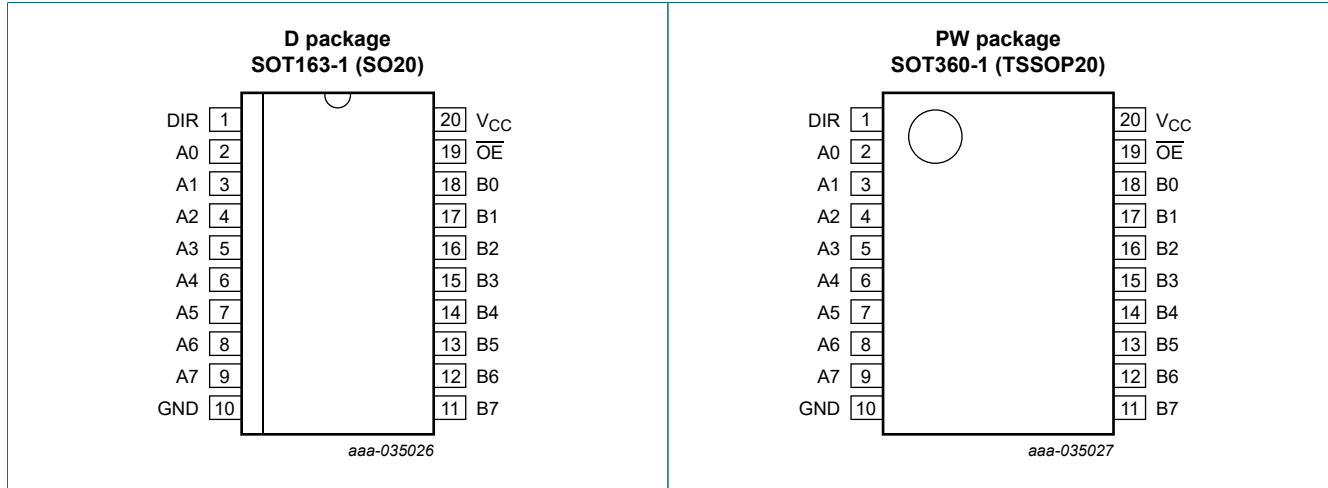


Fig. 2. IEC logic symbol

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
DIR	1	direction control
A0, A1, A2, A3, A4, A5, A6, A7	2, 3, 4, 5, 6, 7, 8, 9	data input/output
GND	10	ground (0 V)
B0, B1, B2, B3, B4, B5, B6, B7	18, 17, 16, 15, 14, 13, 12, 11	data input/output
\overline{OE}	19	output enable input (active LOW)
V _{CC}	20	supply voltage

6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Input		Output/input	
\overline{OE}	DIR	A _n	B _n
L	L	A = B	input
L	H	input	B = A
H	X	Z	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ [1]	-	± 20	mA
I_{OK}	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ [1]	-	± 50	mA
I_O	output current	$V_O = -0.5\text{ V}$ to $(V_{CC} + 0.5\text{ V})$	-	± 35	mA
I_{CC}	supply current		-	70	mA
I_{GND}	ground current		-70	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT163-1 (SO20) package: P_{tot} derates linearly with 12.3 mW/K above 109 °C.
For SOT360-1 (TSSOP20) package: P_{tot} derates linearly with 10.0 mW/K above 100 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	[1]	1.0	3.3	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.0\text{ V}$ to 2.0 V	-	-	500	ns/V
		$V_{CC} = 2.0\text{ V}$ to 2.7 V	-	-	200	ns/V
		$V_{CC} = 2.7\text{ V}$ to 3.6 V	-	-	100	ns/V
		$V_{CC} = 3.6\text{ V}$ to 5.5 V	-	-	50	ns/V

[1] The static characteristics are guaranteed from $V_{CC} = 1.2\text{ V}$ to $V_{CC} = 5.5\text{ V}$, but LV devices are guaranteed to function down to $V_{CC} = 1.0\text{ V}$ (with input levels GND or V_{CC}).

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	0.9	-	-	0.9	-	V
		V _{CC} = 2.0 V	1.4	-	-	1.4	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}	-	-	0.7 × V _{CC}	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.3	-	0.3	V
		V _{CC} = 2.0 V	-	-	0.6	-	0.6	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3 × V _{CC}	-	0.3 × V _{CC}	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -100 μA; V _{CC} = 1.2 V	-	1.2	-	-	-	V
		I _O = -100 μA; V _{CC} = 2.0 V	1.8	2.0	-	1.8	-	V
		I _O = -100 μA; V _{CC} = 2.7 V	2.5	2.7	-	2.5	-	V
		I _O = -100 μA; V _{CC} = 3.0 V	2.8	3.0	-	2.8	-	V
		I _O = -100 μA; V _{CC} = 4.5 V	4.3	4.5	-	4.3	-	V
		I _O = -8 mA; V _{CC} = 3.0 V	2.4	2.82	-	2.2	-	V
I _O = -16 mA; V _{CC} = 4.5 V	3.6	4.2	-	3.5	-	V		
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 100 μA; V _{CC} = 1.2 V	-	0	-	-	-	V
		I _O = 100 μA; V _{CC} = 2.0 V	-	0	0.2	-	0.2	V
		I _O = 100 μA; V _{CC} = 2.7 V	-	0	0.2	-	0.2	V
		I _O = 100 μA; V _{CC} = 3.0 V	-	0	0.2	-	0.2	V
		I _O = 100 μA; V _{CC} = 4.5 V	-	0	0.2	-	0.2	V
		I _O = 8 mA; V _{CC} = 3.0 V	-	0.25	0.40	-	0.50	V
I _O = 16 mA; V _{CC} = 4.5 V	-	0.35	0.55	-	0.65	V		
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	1.0	-	1.0	μA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 5.5 V	-	-	5	-	10	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	20	-	160	μA
ΔI _{CC}	additional supply current	per input; V _I = V _{CC} - 0.6 V; V _{CC} = 2.7 V to 3.6 V	-	-	500	-	850	μA
C _I	input capacitance		-	3.5	-	-	-	pF
C _{I/O}	input/output capacitance		-	10	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 5.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t _{pd}	propagation delay	An, Bn to Bn, An; see Fig. 3 [2]						
		V _{CC} = 1.2 V	-	45	28	-	-	ns
		V _{CC} = 2.0 V	-	15	28	-	34	ns
		V _{CC} = 2.7 V	-	11	19	-	24	ns
		V _{CC} = 3.0 V to 3.6 V; C _L = 15 pF [3]	-	7	-	-	-	ns
		V _{CC} = 3.0 V to 3.6 V [3]	-	9	16	-	20	ns
		V _{CC} = 4.5 V to 5.5 V [3]	-	8	11	-	14	ns
t _{en}	enable time	\overline{OE} to An, Bn; see Fig. 4 [2]						
		V _{CC} = 1.2 V	-	55	-	-	-	ns
		V _{CC} = 2.0 V	-	19	31	-	39	ns
		V _{CC} = 2.7 V	-	14	23	-	29	ns
		V _{CC} = 3.0 V to 3.6 V [3]	-	10	18	-	23	ns
		V _{CC} = 4.5 V to 5.5 V [3]	-	8.5	14	-	18	ns
t _{dis}	disable time	\overline{OE} to An, Bn; see Fig. 4 [2]						
		V _{CC} = 1.2 V	-	65	-	-	-	ns
		V _{CC} = 2.0 V	-	24	32	-	39	ns
		V _{CC} = 2.7 V	-	18	24	-	29	ns
		V _{CC} = 3.0 V to 3.6 V [3]	-	14	20	-	24	ns
		V _{CC} = 4.5 V to 5.5 V [3]	-	11.5	16	-	19	ns
C _{PD}	power dissipation capacitance	C _L = 50 pF; f _i = 1 MHz; V _I = GND to V _{CC} ; V _{CC} = 3.3 V [4]	-	40	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

t_{en} is the same as t_{PZL} and t_{PZH}.

t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

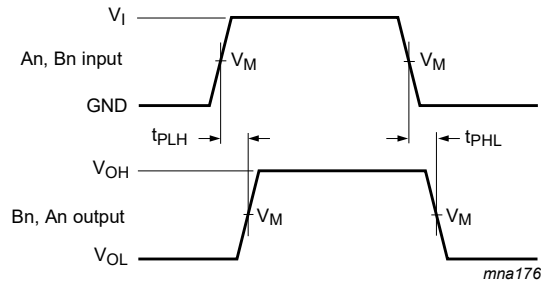
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

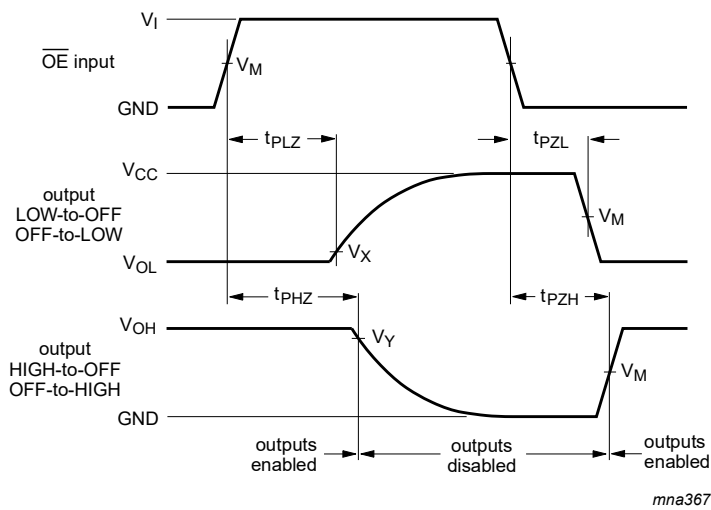
10.1. Waveforms and test circuit



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 3. The input (An, Bn) to output (Bn, An) propagation delays



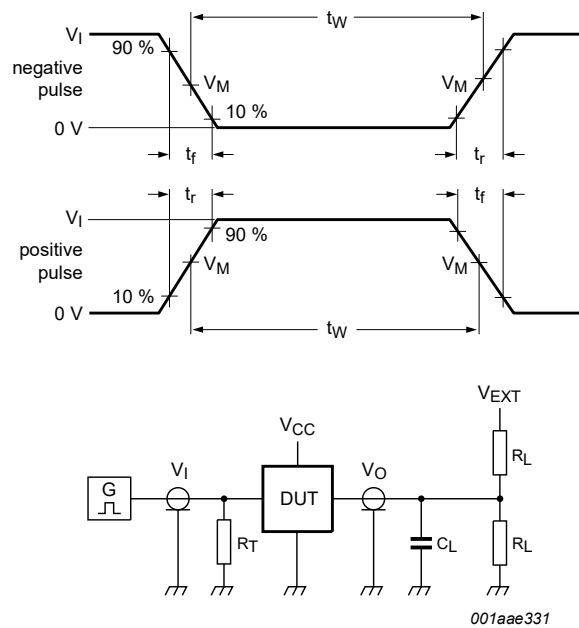
Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 4. Enable and disable times

Table 8. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
< 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.1V_{CC}$	$V_{OH} - 0.1V_{CC}$
2.7 V to 3.6 V	1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$
$\geq 4.5 V$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.1V_{CC}$	$V_{OH} - 0.1V_{CC}$



Test data is given in [Table 9](#).

Definitions for test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

Fig. 5. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
< 2.7 V	V_{CC}	≤ 2.5 ns	50 pF	1 k Ω	open	GND	$2 \times V_{CC}$
2.7 V to 3.6 V	2.7 V	≤ 2.5 ns	15 pF, 50 pF	1 k Ω	open	GND	$2 \times V_{CC}$
≥ 4.5 V	V_{CC}	≤ 2.5 ns	50 pF	1 k Ω	open	GND	$2 \times V_{CC}$

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

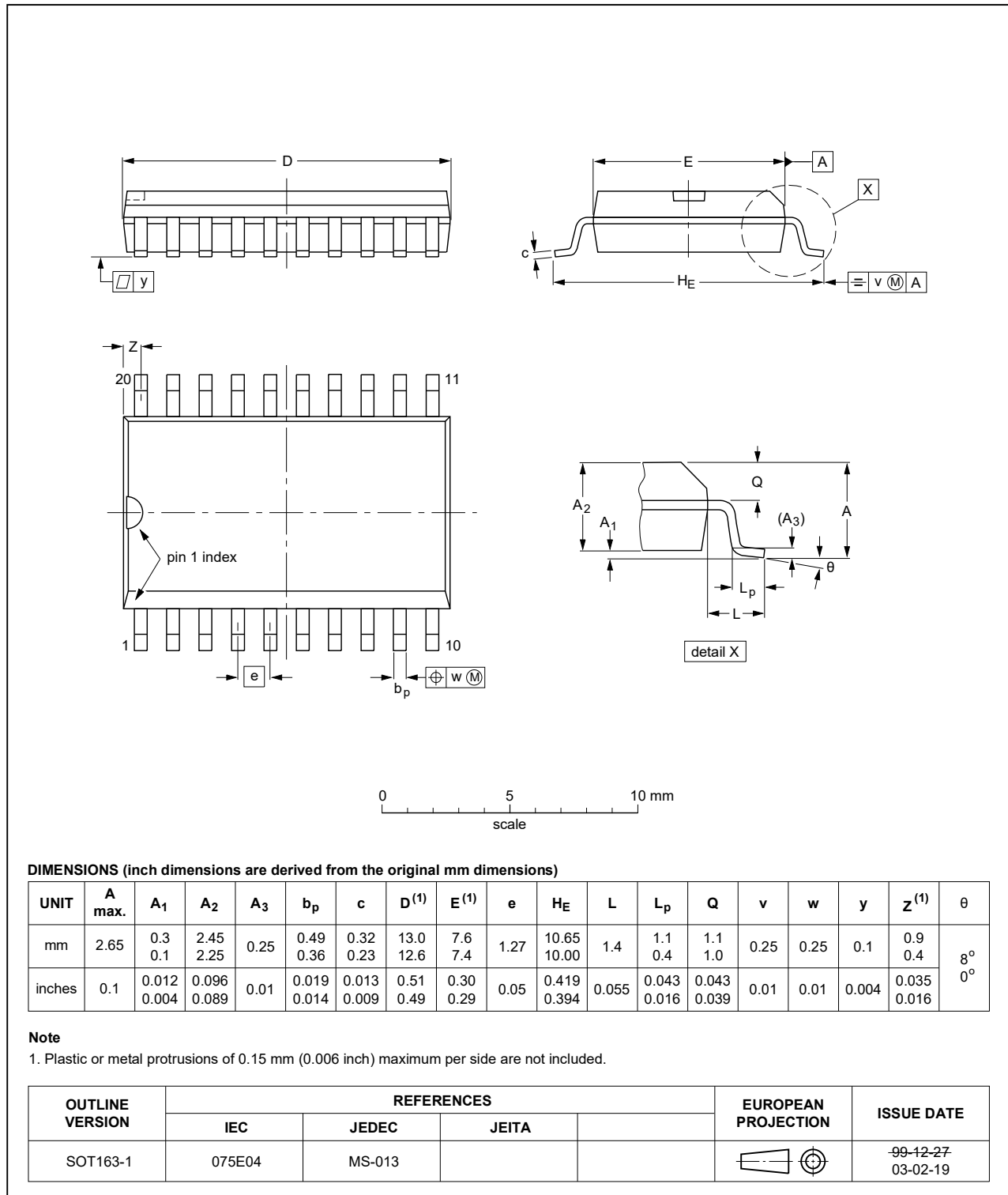


Fig. 6. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

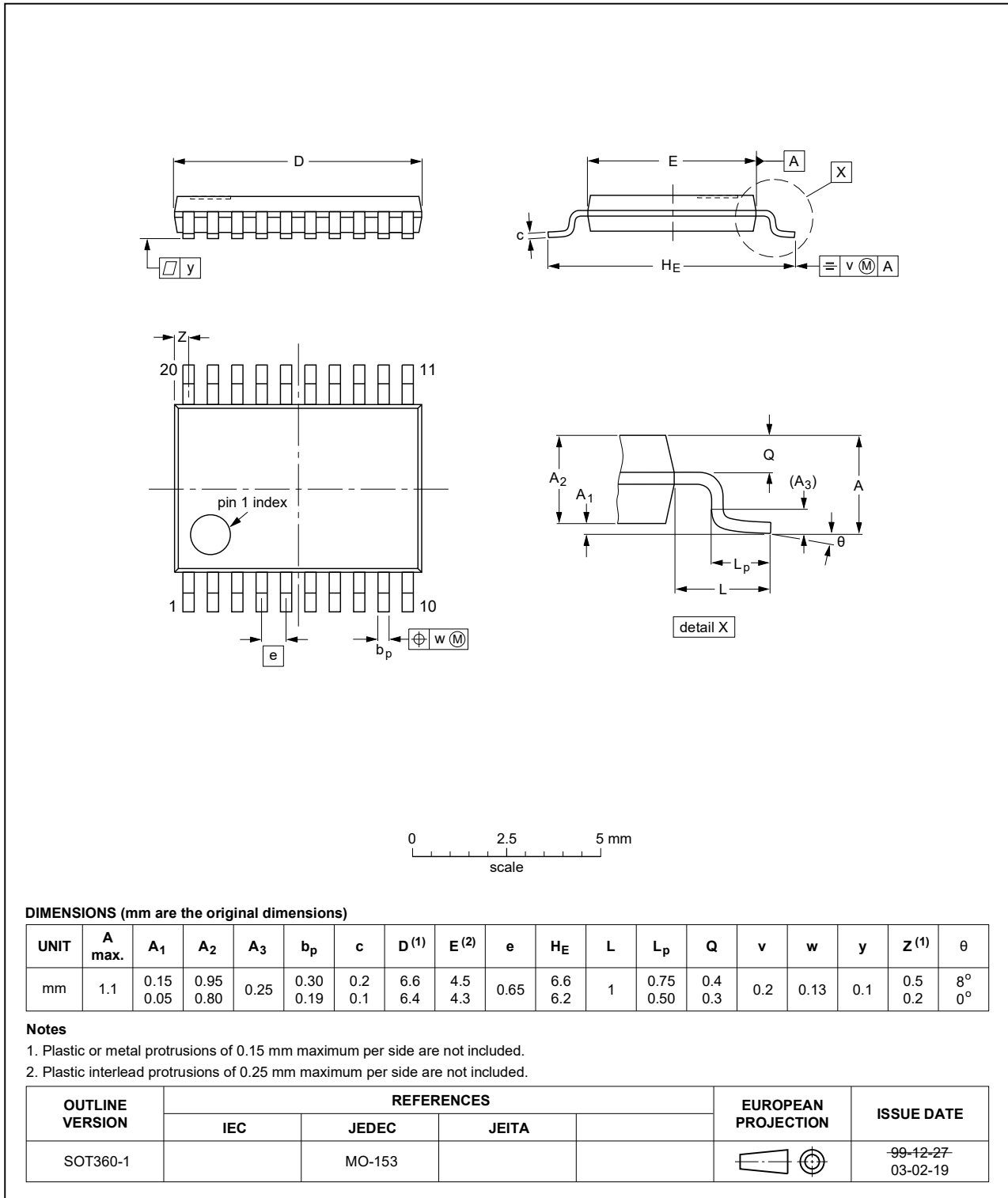


Fig. 7. Package outline SOT360-1 (TSSOP20)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV245 v.6	20240704	Product data sheet	-	74LV245 v.5
Modifications:	<ul style="list-style-type: none"> • Section 2: ESD specification updated according to the latest JEDEC standard. 			
74LV245 v.5	20210928	Product data sheet	-	74LV245 v.4
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 1 and Section 2 updated. • Section 7: Derating values for P_{tot} total power dissipation updated. • Type number 74LV245DB (SOT339-1/SSOP20) removed. 			
74LV245 v.4	20160309	Product data sheet	-	74LV245 v.3
Modifications:	<ul style="list-style-type: none"> • Type number 74LV245N (SOT146-1) removed. 			
74LV245 v.3	20090415	Product data sheet	-	74LV245 v.2
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name when appropriate. 			
74LV245 v.2	19980420	Product specification	-	74LV245 v.1
74LV245 v.1	19970303	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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